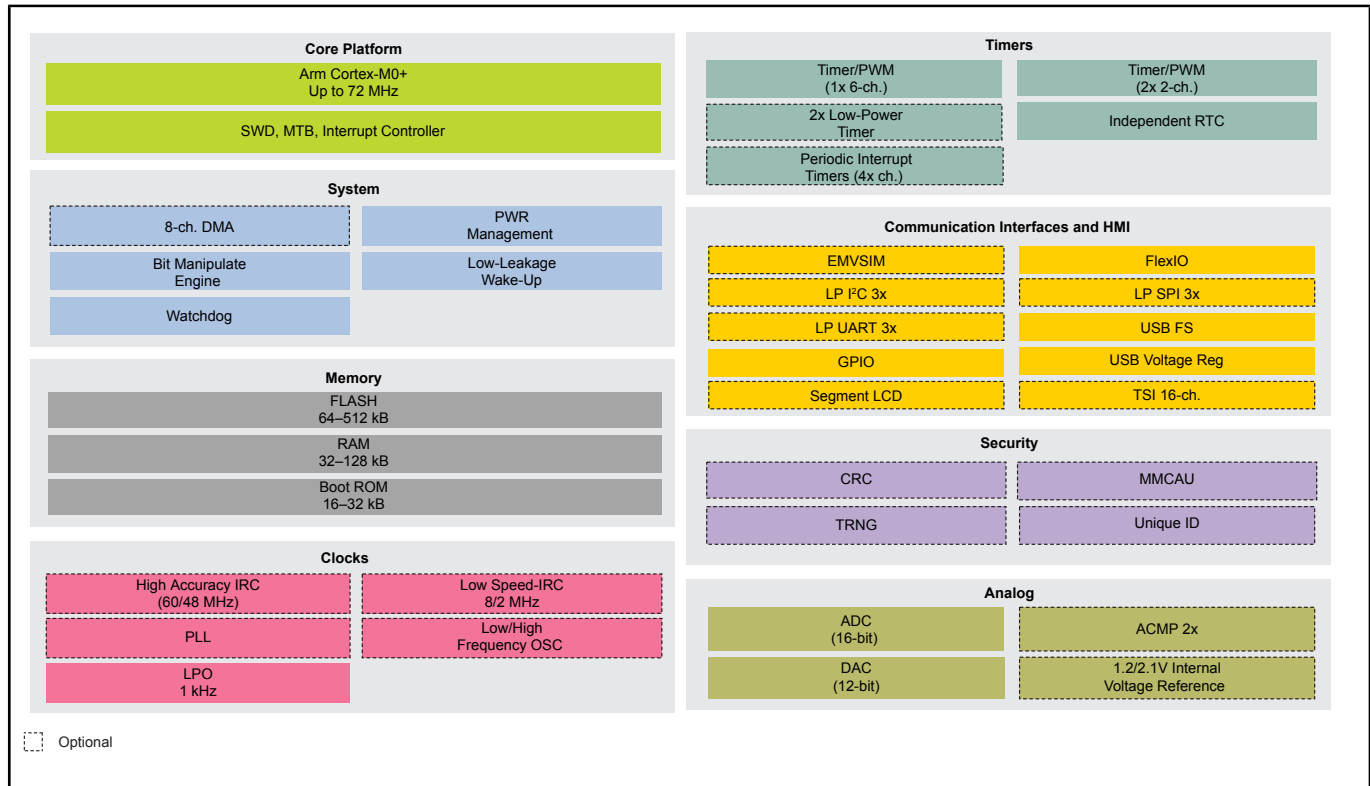# Ultra-Low-Power, Highly Integrated MCU

K32-L2

Last Updated: Apr 10, 2024

The K32 L2 MCU family's low-leakage architecture, combined with its power-optimized peripherals and security features (such as cryptographic acceleration technology, cyclic redundancy check and a true random number generator), make it ideal for consumer, industrial and IoT applications requiring a low-priced, power efficient option with longer battery life.

This family includes a low power Arm® Cortex®-M0+ core and with options scaling from 64 KB to 512 KB Flash and from 32 kB to 128 kB SRAM, the K32 L2 family offers a wide range of memory resources to fit different application tasks within a small-form factor, low power, and highly integrated design.

K32 L2 MCU Block Diagram

Core Platform

Arm Cortex-M0+
Up to 72 MHz

SWD, MTB, Interrupt Controller

System

8-ch. DMA	PWR Management
Bit Manipulate Engine	Low-Leakage Wake-Up
Watchdog	

Memory

FLASH
64–512 kB

RAM
32–128 kB

Boot ROM
16–32 kB

Clocks

High Accuracy IRC (60/48 MHz)	Low Speed-IRC 8/2 MHz
PLL	Low/High Frequency OSC
LPO 1 kHz	

Timers

Timer/PWM (1x 6-ch.)	Timer/PWM (2x 2-ch.)
2x Low-Power Timer	Independent RTC
Periodic Interrupt Timers (4x ch.)	

Communication Interfaces and HMI

EMVSIM	FlexIO
LP I²C 3x	LP SPI 3x
LP UART 3x	USB FS
GPIO	USB Voltage Reg
Segment LCD	TSI 16-ch.

Security

| CRC | MMCAU |
| TRNG | Unique ID |

Analog

| ADC (16-bit) | ACMP 2x |
| DAC (12-bit) | 1.2/2.1V Internal Voltage Reference |

Optional

View additional information for Ultra-Low-Power, Highly Integrated MCU.

Note: The information on this document is subject to change without notice.