



# SPI to I<sup>2</sup>C-Bus Interface

## SC18IS600\_601

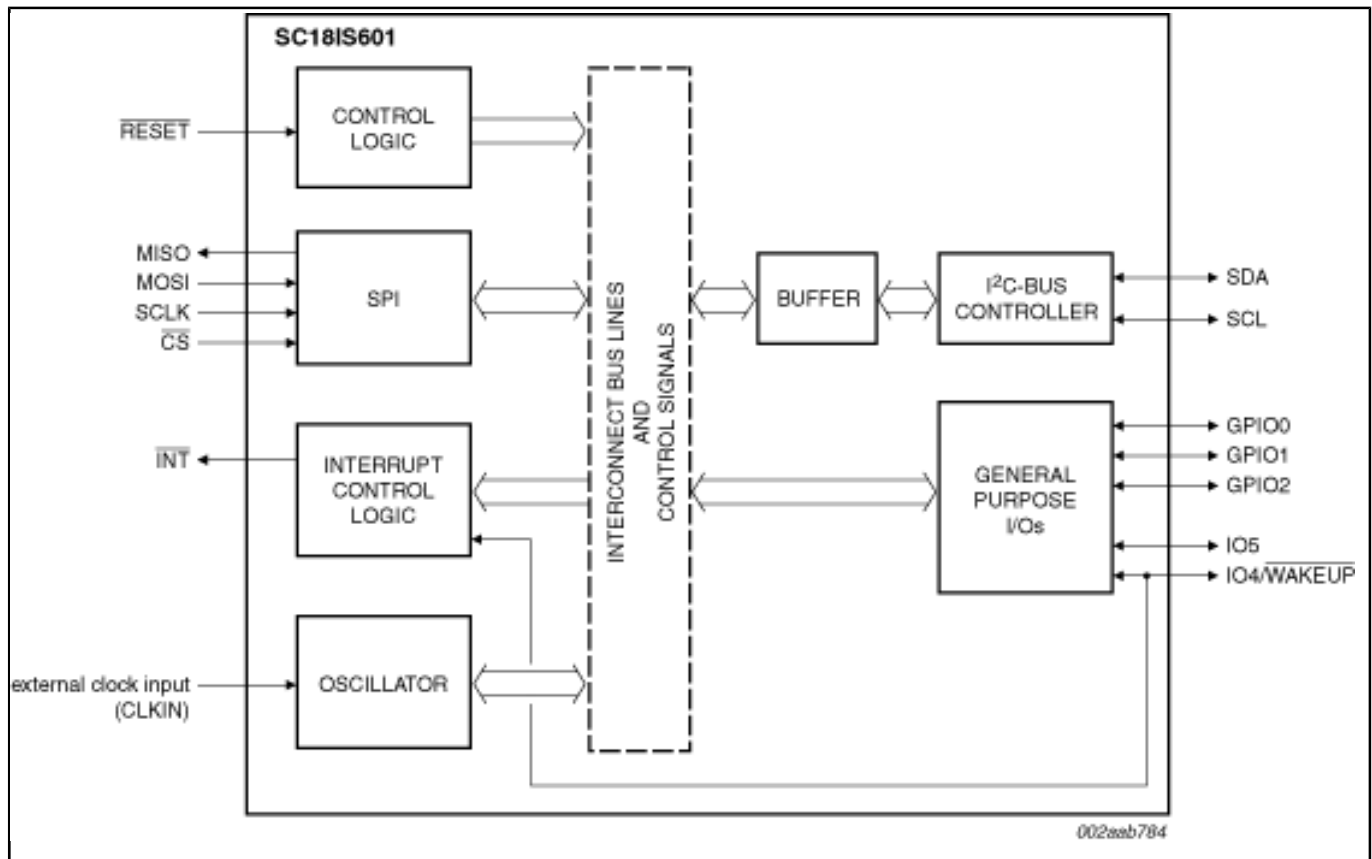
新規採用非推奨

このページでは、新規設計を推奨しない製品に関する情報を掲載しています。

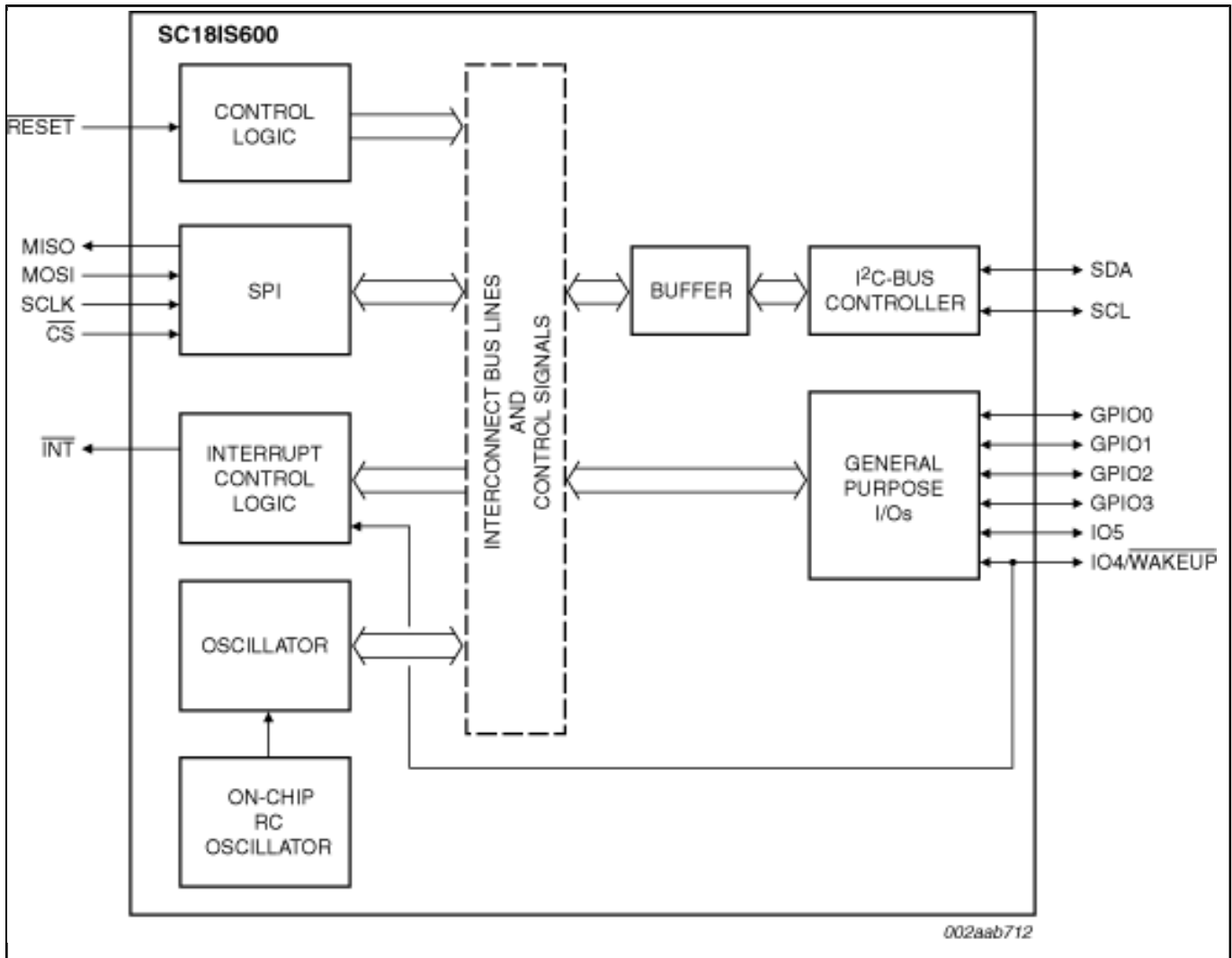
Last Updated: Oct 13, 2023

The SC18IS600 is designed to serve as an interface between the standard SPI of a host (microcontroller, microprocessor, chip set, etc.) and the serial I<sup>2</sup>C-bus. This allows the host to communicate directly with other I<sup>2</sup>C-bus devices. The SC18IS600 can operate as an I<sup>2</sup>C-bus controller-transmitter or controller-receiver. The SC18IS600 controls all the I<sup>2</sup>C-bus specific sequences, protocol, arbitration and timing.

### SC18IS600IPW, SC18IS601IPW Block Diagram



### SC18IS600IPW, SC18IS601IPW Block Diagram



View additional information for [SPI to I<sup>2</sup>C-Bus Interface](#).

Note: The information on this document is subject to change without notice.

[www.nxp.com](http://www.nxp.com)

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2024 NXP B.V.