APPLICATION NOTE

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MF RC500
Active Antenna Concept

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Philips
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Active Antenna Concept

MF RC500

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1 INTRODUCTION

1.1 Scope

This document describes the implementation of an active antenna concept by using the contactless reader ICs MF RC500. It includes the functional description of the active antenna configuration, and give details on how to apply this concept from a system and software viewpoint.

By default, the MF RC500 is configured to drive a passive antenna directly. In fact, with the active antenna concept, it is possible to run up to two antennas quasi parallel. Details on the configuration and software example will be shown here.

In some applications there may be a need for tiding over a longer distance between the MF RC500 and the active antenna. In this case we would need a line driver to provide a relatively noise immune path with a communication distance of up to approximately 100m. An example of using line drivers to extend the length will be covered in this document.

In order to be backwards compatible to the well established reader components as the MF CM200, MF RC 150, MF RC 170 or MF RC 171 an example is given showing an active antenna concept using the MF RC 171 as a master and the MF RC 500 as a slave.

1.2 General description

Because of physical limitation and for optimum operating condition, the length of the antenna cable between the reader IC and the antenna coil is limited to 50cm. On the other hand the reader IC itself has to be located within 20cm of the controlling microprocessor because of physical restrictions of the parallel interface. In this case, we need to have a solution for the link between the antenna and the host device.

The contactless reader IC MF RC500 comprises of two main blocks. A digital circuitry, comprising state machines, coder and decoder logic, and an analogue circuitry with the modulator and antenna drivers, receiver and amplification circuitry. The interface between these two blocks can be configured in the way, that the interfacing signals may be routed to the pins MFIN and MFOUT.

This topology support that the analogue part of the reader IC may be connected to the digital part of another MF RC500 or other device, allowing the analogue circuitry to be driven by an externally connected device.

The active antenna concept is driven from this fundamental topology of the reader IC. The following description will go into details on the configuration of the various blocks.

The active antenna concept is applicable on all Philips contactless reader IC (MF RC530, MF RC531 & CL RC632). All the descriptions of MF RC500's application in this document are applicable to the other reader IC.

Note: The active antenna concept is limited to ISO14443A at 106kb baud rate.
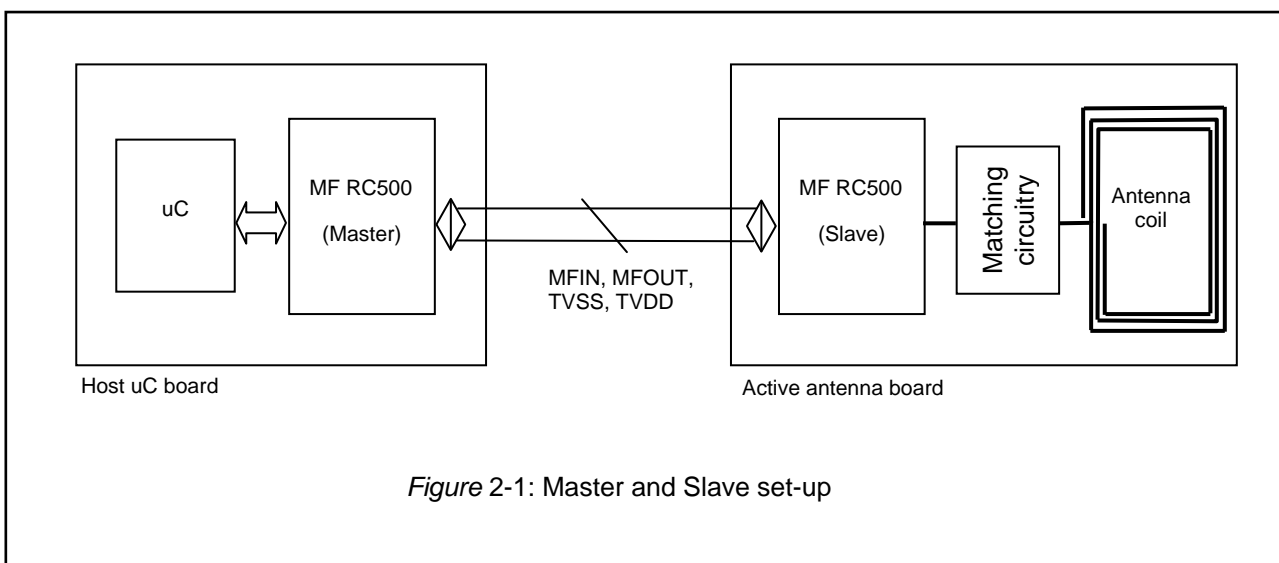
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2 MF RC500 MASTER AND SLAVE CONFIGURATION

2.1 Introduction

For implementation of an active antenna concept, the digital circuitry of one device is used to link to the analogue circuitry of another device. This is a form of master and slave configuration, where the master is the host device that encompassed the digital circuitry, and the slave is the active antenna that encompassed the analogue circuitry.

The reader IC MF RC500 can be used in both the master and slave configuration through proper setting of the serial signal switches within the reader ICs. In this case, the links between the master and slave are the pins MFIN and MFOUT. MFIN of one MF RC500 should be connected to MFOUT of another MF RC500.

Figure 2-1 shows a typical master and slave set-up using two MF RC500.

Figure 2-1: Master and Slave set-up

Any communication between the host and the active antenna is initialised by the host µC. The master MF RC500 performs any data control necessary and route the encoded digital signal onto the MFOUT pin. The slave MF RC500 receives the encoded digital signal on its MFIN pin, and routes this signal to its analogue circuitry for transmission via the antenna coil. Similarly, signal received on the antenna is de-modulated by the slave and the encoded digital signal is sent out on it MFOUT pin. The master receives this encoded signal on its MFIN pin and performs the decoding, and error checking before sending the result to the host µC.

Master and slave MF RC500 must be connected with a common ground base – use TVSS. The supply voltage (TVDD) is normally transmitted together with the data signals, but it is also allowed to use a local supply voltage at the active antenna. In case of cable length more than 10m, it is strongly recommended to use a local supply voltage.

Two main issues in the design requirements:

- One is the proper design of the serial transportation of the two signals: MFIN and MFOUT. Depending on the environment and the length of the cable, signal may be reduced and noise will be coupled onto the signal and cause error communication. It is highly recommended to use symmetrical interface driver like RS422 between the signal path.

- Secondly is the proper selection of the BitPhase register values of the MF RC500 in both the master and slave. The BitPhase value will affect the proper linking between the master and slave.

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2.2 Master configuration

The MF RC500 can be configured as a master by using it digital circuitry via the pins MFIN and MFOUT. To do so, the following register settings have to be made:

Register	Value	Signal	At MF RC500 Pin
ModulatorSource (0x11)	X	-	-
MFOUTSelect (0x26)	2	Miller Pulse Coded	MFOUT
DecoderSource (0x1E)	2	Manchester Coded with sub-carrier	MFIN
BitPhase Register (0x1B)	0x11	-	-

Table 2-1: Register setting to use the MF RC500 digital circuitry only

Note: TX1 and TX2 (bit0 and bit1, TXControl Register 0x11) should be disabled when the MF RC500 is in master mode.

Figure 2-2 shows the master configured signal switches and the routed signal flow from the digital circuitry to the pin MFOUT, and from the pin MFIN to the digital circuitry.
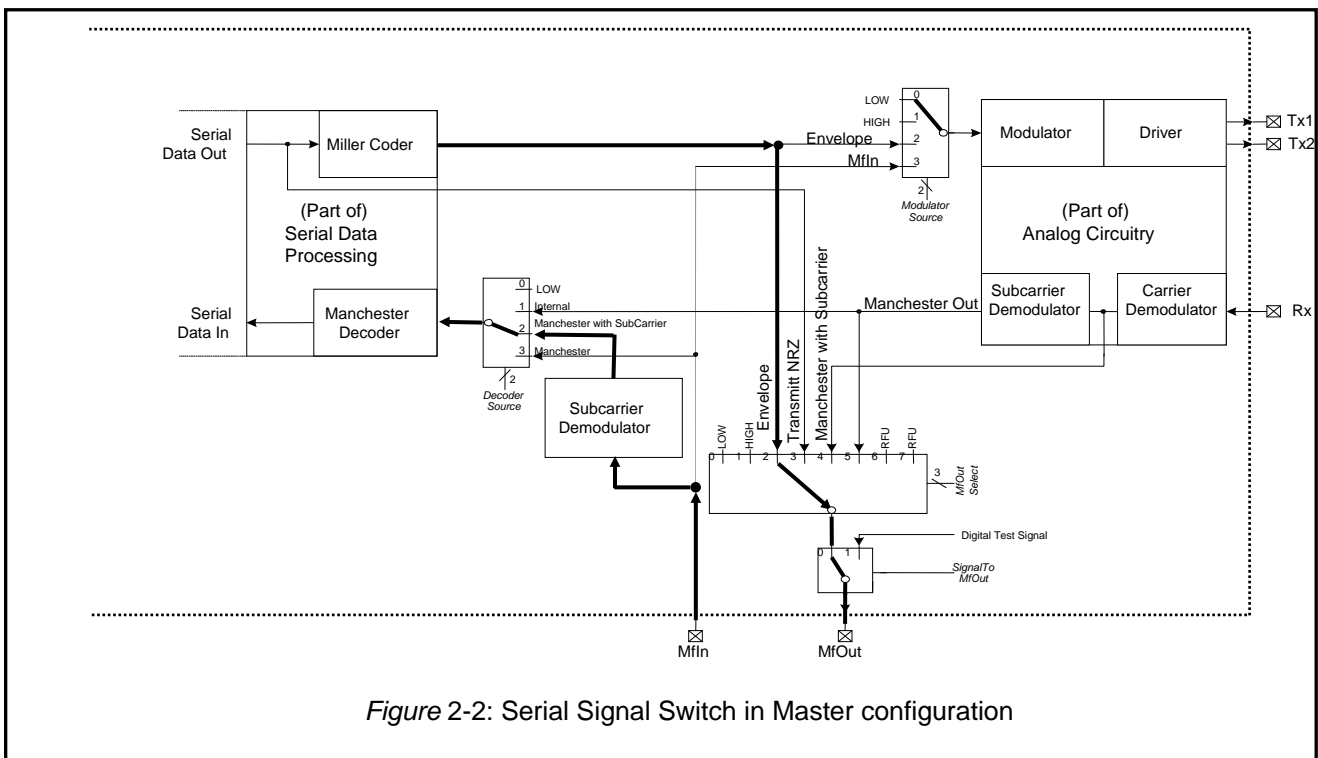

Figure 2-2: Serial Signal Switch in Master configuration

BitPhase Register setting:

For the MF RC500 to receive digital signal on the MFIN pin, the BitPhase value must be set to 0x11. When used with the normal antenna circuit, the BitPhase must be set to the default value of 0xAD.

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2.3 Slave configuration

The MF RC500 can be configured as a slave by using the analogue circuitry via the pins MFIN and MFOUT. To do so, the following register settings have to be made:

Register	Value	Signal	At MF RC500 Pin
ModulatorSource (0x11)	3	Miller Pulse Coded	MFIN
MFOUTSelect (0x26)	4	Manchester Coded with sub-carrier	MFOUT
DecoderSource (0x1E)	X	-	-
BitPhase Register (0x1B)	0x6D	-	-

Table 2-2: Register setting to use the MF RC500 analogue circuitry only

Figure 2-3 shows the slave configured signal switches and the routed signal flow from the analogue circuitry to the pin MFOUT, and from the pin MFIN to the analogue circuitry.
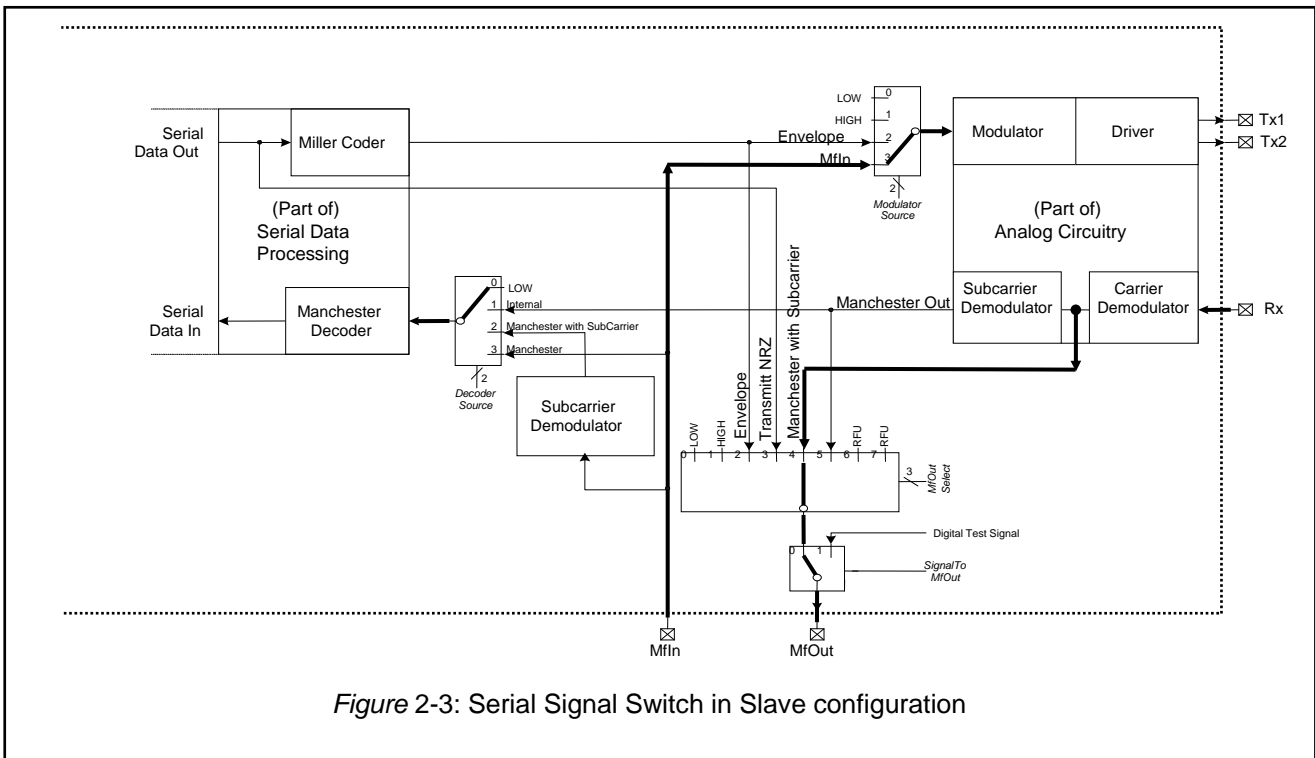

Figure 2-3: Serial Signal Switch in Slave configuration

BitPhase Register setting:

The BitPhase register defines the phase offset between the transmitter and receiver clock of the analogue circuit. It is used to adjust the bit phase of the received data related to the receiver circuitry. The value of the BitPhase register in the slave configuration is always taken to be 0x40 less then the value set in the normal antenna circuit. For proper operation with MIFARE[®] card, 0xAD is used in the normal antenna circuit. Therefore, 0x6D should be used here for the active antenna setting.

Pre-configuration of slave MF RC500

Usually, the active antenna does not contain any controlling microprocessor. Therefore, in order to make the MF RC500 to be powered up as a slave, the "Start Up Register Initialisation Files" within the MF RC500's E²PROM have to be pre-configured with the slave's settings. An example of initialising the slave MF RC500 will be shown in the later session.
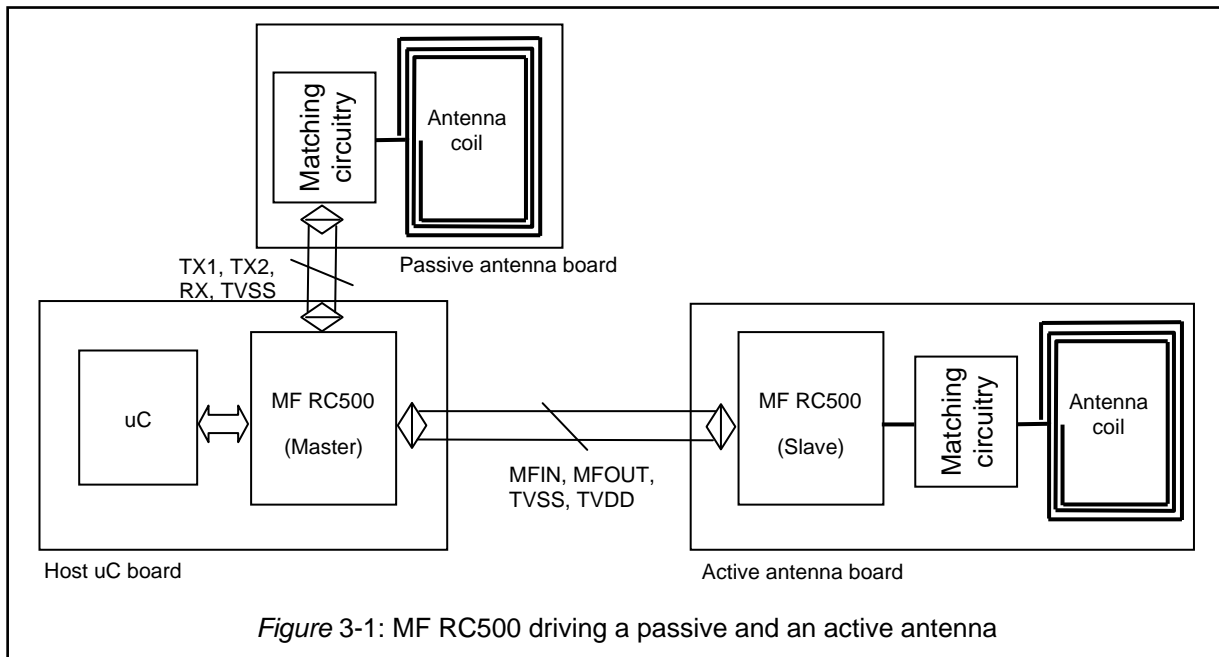
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3 DRIVING TWO ANTENNAS

It is possible to connect a passive antenna to pins TX1, TX2 and RX (via the appropriate filter and matching circuit) and at the same time an active antenna to pins MFOUT and MFIN.
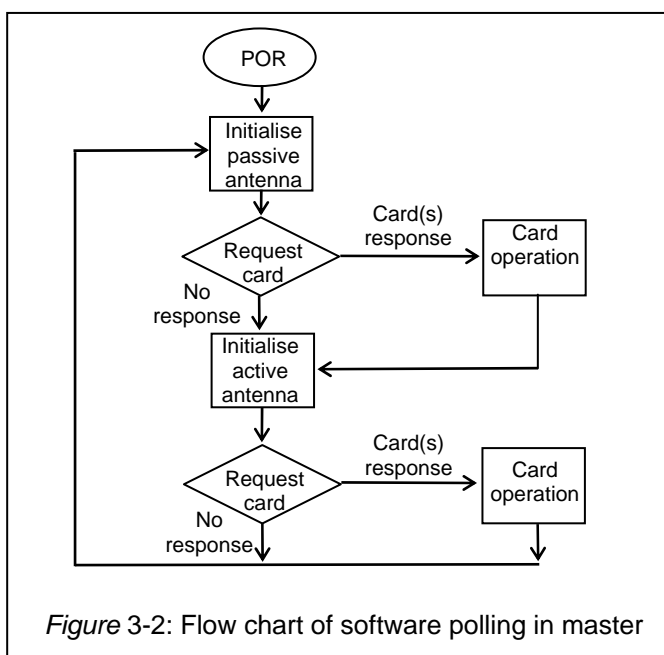
In this configuration, two RF-parts may be driven (one after another) by one microprocessor.

Figure 3-1 shows the set-up for this configuration.

Figure 3-1: MF RC500 driving a passive and an active antenna

Sample software flow for polling between passive and active antenna:

Figure 3-2 shows a possible software flow for polling of a card response.

Figure 3-2: Flow chart of software polling in master

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Explanation:

After the power-on reset, the MF RC500 is initialised in default condition to use the passive antenna. The main loop is a sequence of polling of the card's response to the Request command. When the µC get no response, it will then turn off the passive antenna and poll the active antenna. This polling sequence is repeated until there is a card response in either of the antennas. The µC will then go into the card selection sequence to activate one card for operation. When the card operation is done, the polling sequence will be continued. The activation of each of the antennas can be done easily with the proper setting of the registers. This is shown in the following software example.

Software routine example for switching between passive and active antenna

Figure 3-3 shows a programming example of switching between the two antennas.

```
void        M500PcdMfInOutMasterConfig (char SW)

{

   if (SW == ON){   // Select and initialised active antenna

          WriteRC(RegRxControl2,0x42);        // decorder source at pin MFIN

          WriteRC(RegTxControl,0x10);         // disable TX1 & TX2

          WriteRC(RegBitPhase,0x11);          // Bitphase value for driving a slave MF RC500

          WriteRC(RegMfOutSelect,0x02);       // route digital coded signal to pin MFOUT

   }

   else {           // Select and initialised passive antenna

          WriteRC(RegRxControl2,0x41);        // decorder source from internal

          WriteRC(RegTxControl,0x5B);         // enable TX1 & TX2, modulator source from internal

          WriteRC(RegBitPhase,0xAD);          // Bitphase value for passive antenna

          WriteRC(RegMfOutSelect,0x00);       // set MFOUT to low

   }

}
```

Figure 3-3: Software routine for antenna switching

Note: It is recommended to set MFOUT to low when the active antenna is not in used. By doing so, the RF output of the active antenna will always be low, thus save on power consumption.

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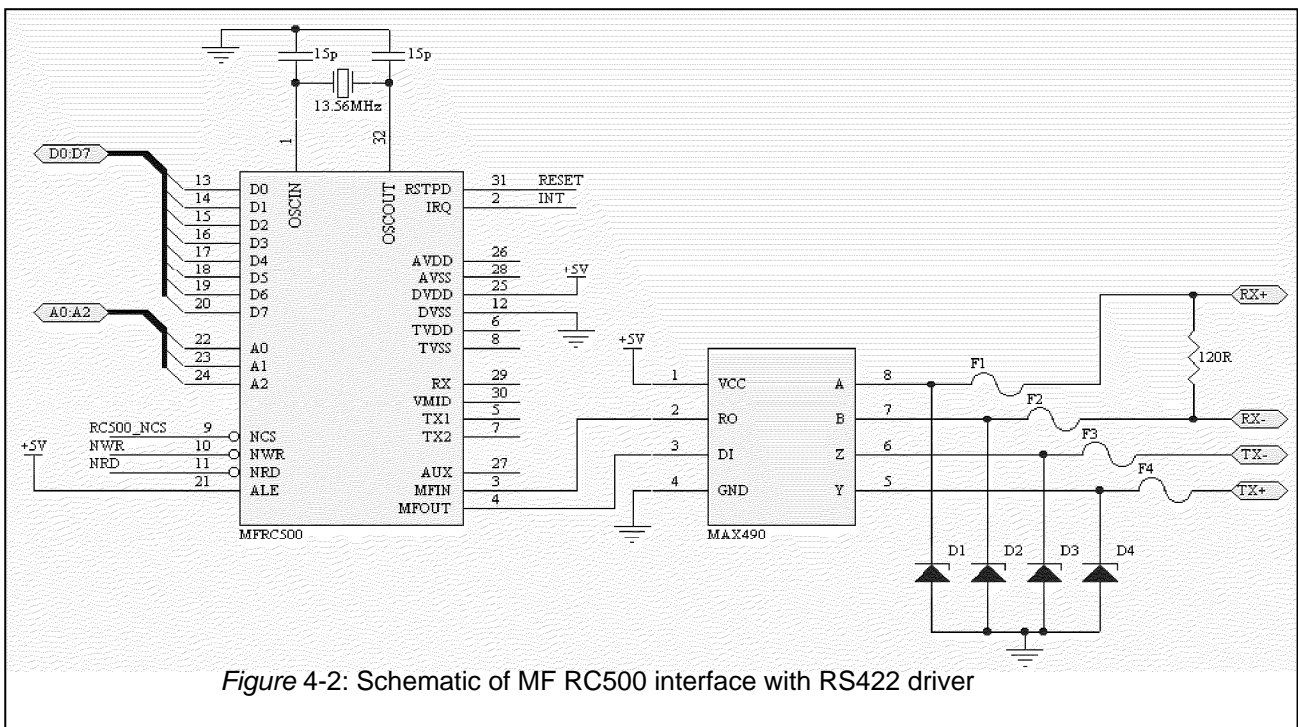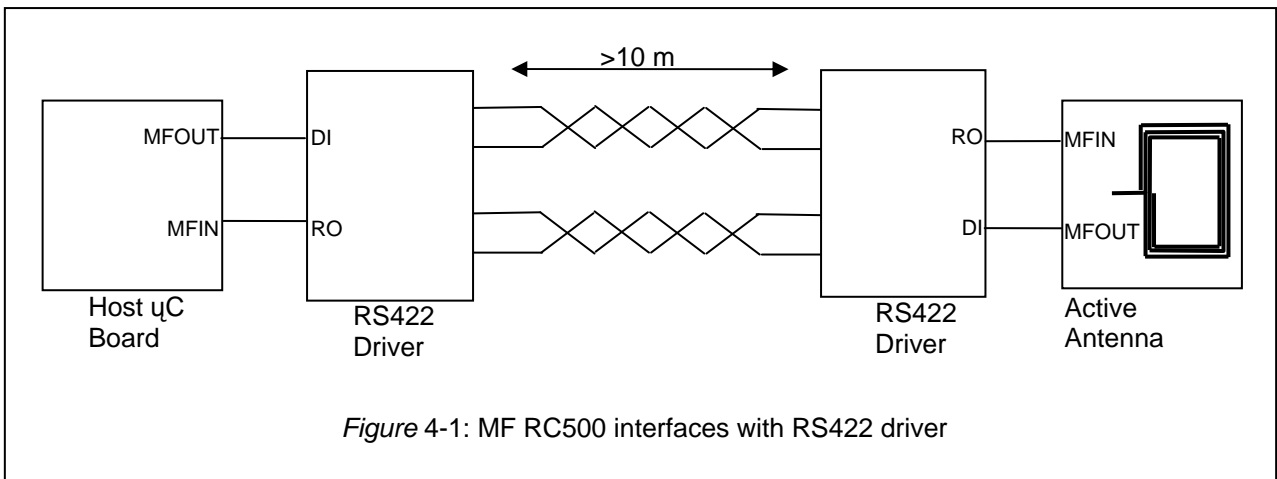
4 ACTIVE ANTENNA WITH SYMMETRICAL INTERFACE DRIVER

In some applications, the antenna may be located far apart from the host unit. By using a common ground transmission of the digital signals MFIN and MFOUT, signal loss and noise coupling will be higher as the distance get further. It normally limits the distance to less then 10 meters.

For remote antenna located at more then 10 meters away, a serial driver is needed to link between the host unit and the active antenna. It allows distances of approximately 100 meters between the host and the active antenna. In fact the maximum allowed distance is mainly dependent on the specification of the serial driver components.

Figure 4-1 shows an example of using two RS422 symmetrical interface drivers ICs. The settings for the MF RC500 are exactly the same as for the master and slave configurations.

Figure 4-2 shows the schematic drawing of a MF RC500 and a MAX490 RS422 driver IC

Figure 4-1: MF RC500 interfaces with RS422 driver

Figure 4-2: Schematic of MF RC500 interface with RS422 driver

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5 MF RC171 DRIVING A MF RC500 ACTIVE ANTENNA

In order to be backwards compatible to the well established reader components as the MF CM200, MF RC 150, MF RC 170 or MF RC 171 an example is given showing an active antenna concept using the MF RC 171 as a master and the MF RC 500 as a slave.

The MF RC171 is an ISO 14443A compatible digital reader IC. Unlike the MF RC500, the MF RC171 will drive an external analogue RF module.

Instead of a discreet RF part, the MF RC500 can be used to replace it. The MF RC500 is configured as a slave (refer to section 2.3), only the analogue part of the IC is used. The MF RC171 can be treated like a master as in section 2.2. The pins KOMP0 and NPAUSE0, are connected to the pins MFIN and MFOUT of the slave. The link between MF RC171 and MF RC500 is similar to the master and slave configuration as in section 2.1.

The combination of the MF RC171 and MF RC500 give the advantage of the advanced security features in the MF RC171. At the same time, it also reduce the components count and board size with the use of the MF RC500, without any compromising to the optimum operating distance. The use of MF RC500 also simplifies of designing the RF analogue stage.

Figure 5-1 shows the connection between the MF RC171 and MF RC500. The MF RC171 is driven directly by a microprocessor. There is no connection between the microprocessor and the MF RC500.
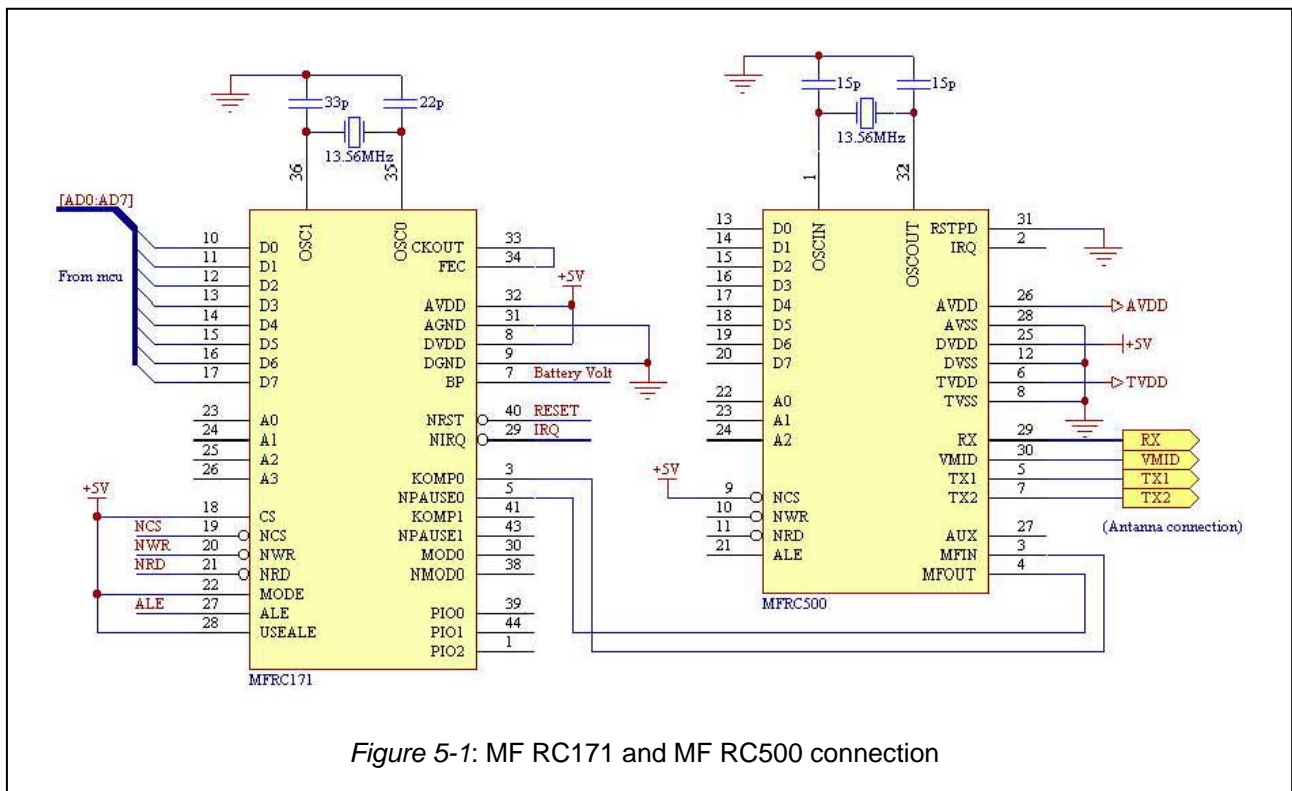

Figure 5-1: MF RC171 and MF RC500 connection

Note: the MF RC500 has to be pre-configured as a slave device.

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6 EXAMPLE: ACTIVE ANTENNA LAYOUT AND SCHEMATIC

A schematic example of the MF RC500 active antenna is given in Figure 6-1.
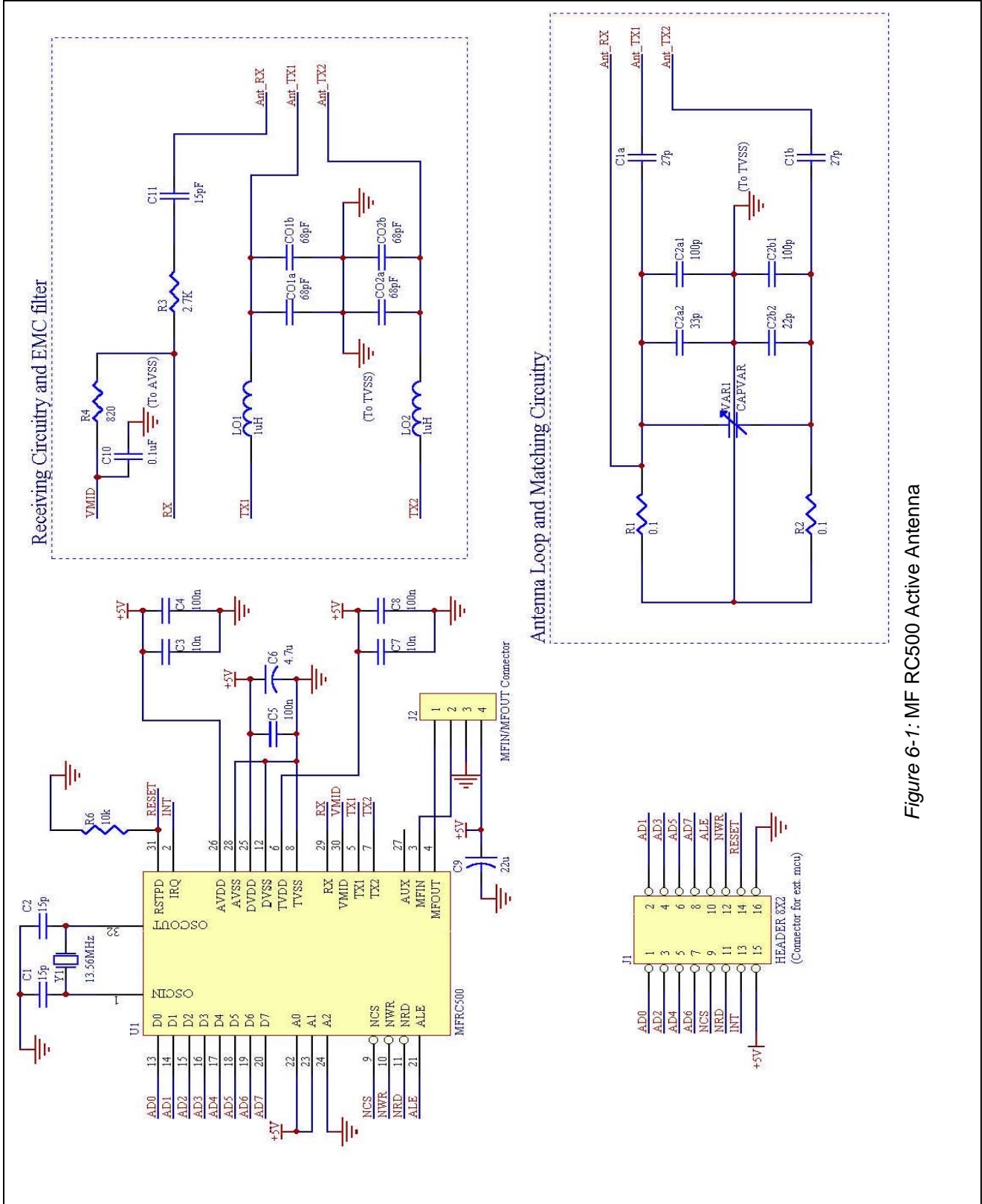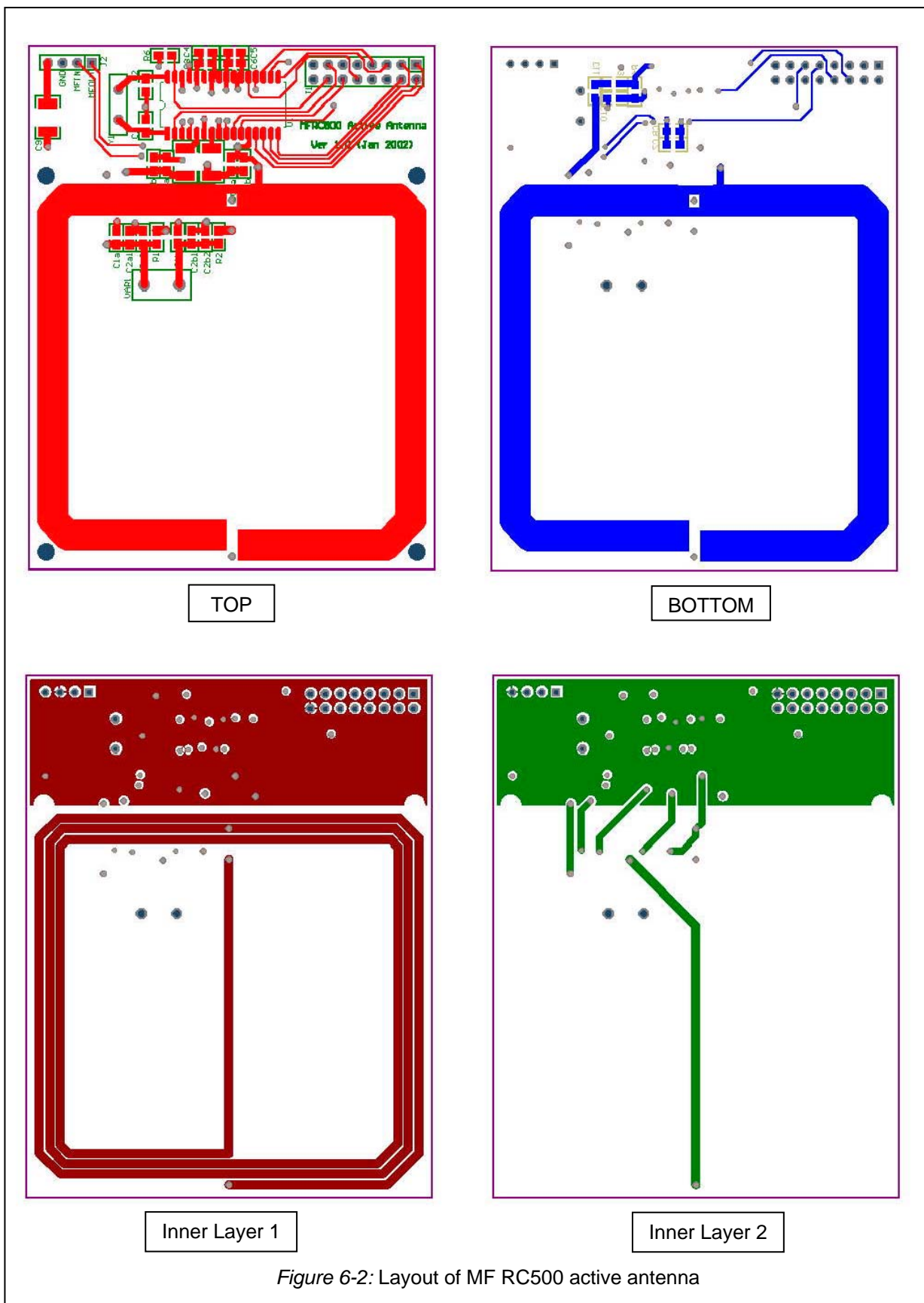

Figure 6-1: MF RC500 Active Antenna

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A layout example of the MF RC500 active antenna is given in Figure 6-2.

Figure 6-2: Layout of MF RC500 active antenna

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7 EXAMPLE: INITIALISE OF SLAVE MF RC500

In the active antenna concept, the slave antenna is usually designed without any microprocessor with it. In order for the MF RC500 to power up in the "slave" mode, the "Start Up Register Initialisation File" (0x10 to 0x2F of MF RC500) should be pre-configured with the "slave" mode settings as describe in session 2.3.

Since the factory default configuration for the IC is not set to "slave" mode, it has to be done at the user's site. It will be demonstrated here, a simple way of configuring the MF RC500 as a "slave" on the final hardware.

To achieve this, we need to have a final hardware that allows external access to the MF RC500's data bus and access control pins. This is shown in session 6, an example of the active antenna with connector for external microprocessor access. For the programmer, a microprocessor board with data and control bus for external connection is required. The microprocessor board can be the same board as the "master" MF RC500, but with a modified firmware and "master" MF RC500 removed when serve as a "slave" programmer.

To initialise the "slave" MF RC500, the Slave antenna is connected to the microprocessor board via the external connection. The microprocessor will access the MF RC500 registers and perform the initialisation.

Figure 7-1 shows the blocks diagram for the above configuration. The slave antenna illustrated here is described in session 6. The microprocessor board is assumed to be the "master" board that drive the slave antenna.
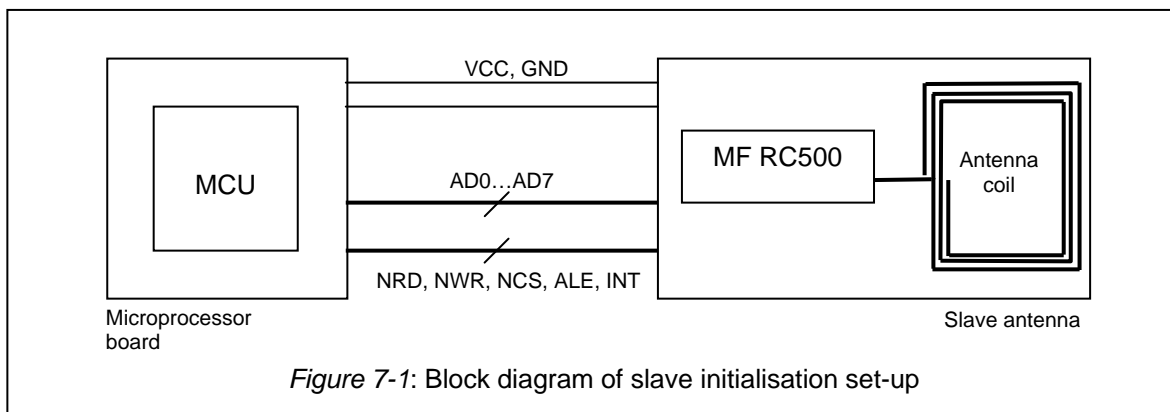

Figure 7-1: Block diagram of slave initialisation set-up

The firmware within the microprocessor is a simple program that handled detection, initialisation and verification of the "slave" MF RC500 on the Slave antenna. The firmware routine "*MF500ActivateAntennaSlaveConfig (void)*" as describe in the document "*MF RC500, Basic Function Library*" is used to configure the ic.

Figure 7-2 shows the flow chart of the microprocessor' firmware.
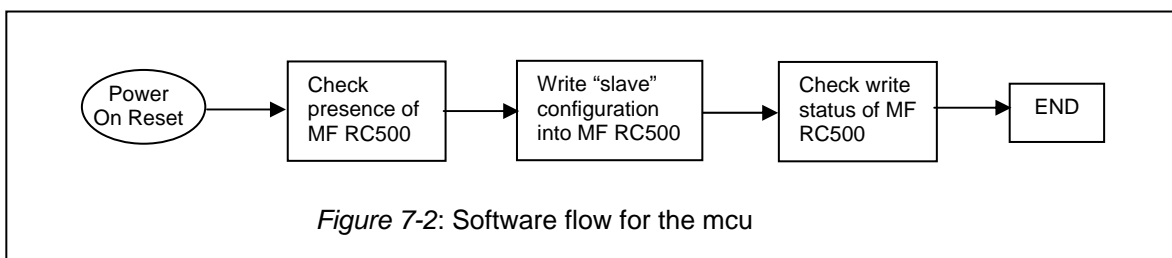

Figure 7-2: Software flow for the mcu

One of the advantages of initialising the MF RC500 in the final board is the reduction in handling the ic manually. Thus it reduces the chance of damaging the ic, and at the same time production flow is not interrupted. On the other hand, it has the flexibility to modify the configuration for optimum performance on the field.

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8 EXAMPLE: DRIVING MULTIPLE ACTIVE ANTENNAS

In some applications, the use of more then two antennas may be required. This example demonstrates a possible solution of driving four active antennas, one at a time.

Theoretically, it is possible to drive as many active antennas as desired, but the speed of polling through all the antennas have to be considered. The worst case situation happens when every antenna is scanned by a card. This resulted in slowness in the response time.

Figure 8-1 shows the schematic of a MF RC500 connection with a 74HC4052 (multiplexer/demultiplexer) to drive four MF RC500 active antennas.
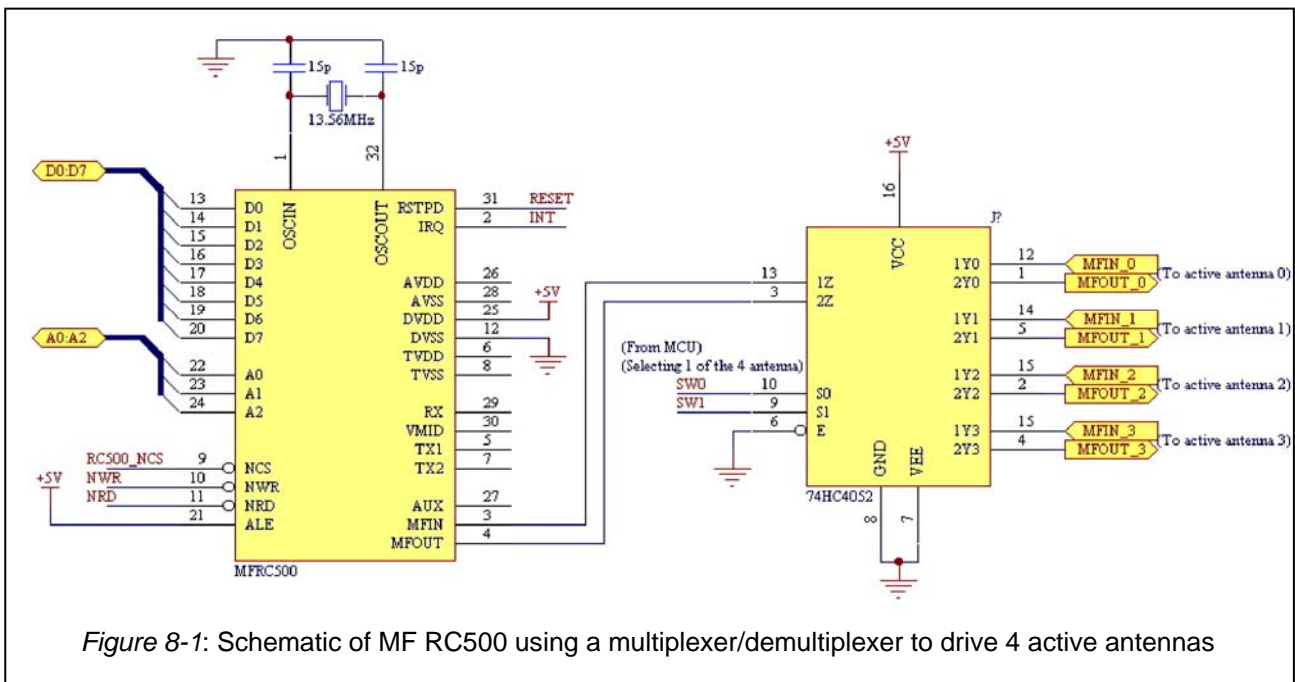

Figure 8-1: Schematic of MF RC500 using a multiplexer/demultiplexer to drive 4 active antennas

The MF RC500 active antenna can be connected directly or through line drivers as described in the previous section.

The microprocessor switches between the four antennas via the pins SW0 and SW1. When an antenna is selected, its pins MFIN and MFOUT will be connected to that of the master MF RC500. The communication between the selected active antenna and the master MF RC500 can be established as before. The microprocessor polls sequentially each antenna and operates with the card if it is present.

Figure 8-2 shows the flow diagram of the software polling through the antennas.
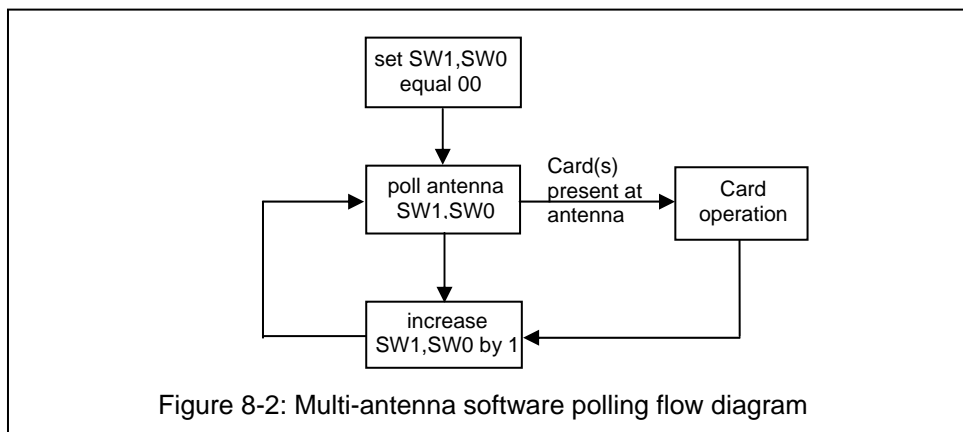

Figure 8-2: Multi-antenna software polling flow diagram

Definitions

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics section of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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