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AN10333

SC16CXXXB baud rate deviation tolerance

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Document information

Info	Content
Keywords	UART, baud rate
Abstract	This application note details the baud rate deviation tolerated by a SC16CXXXB device and a communicating remote UART.

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Revision history

Rev	Date	Description
02	20041206	Application note (9397 750 14411). Second version. Modifications: • Section 1 “Introduction” re-written. • Section 2 “Baud rate deviation”: – added title Section 2.1 “Background” – changed baud rate tolerance from 4.5 % to –4.4 %, and from 5.3 % to +5.6 %. – added new section Section 2.2 “Change” • Section 3 “Conclusion” modified to include date code of devices.
01	20040908	Application note (9397 750 14043). Initial version.

Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

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1. Introduction

This application note is used to replace the errata for 'SC16C550B, SC16C650B, SC16C2550B, SC16C2552B, SC16C652B, SC16C750B, SC16C752B with top mark date code (third line) of 'bxYYWW Z' where YY indicates the year, WW indicates the week and Z indicates the device revision. Due to space constraint the letter Z is found on the fourth line on the LQFP48 package. The new device revision is changed from the letter B to the letter D.

2. Baud rate deviation

2.1 Background

A UART's baud rates can be set by programming the internal divisor DLL and DLM registers of the UART. The exact baud rates can be calculated by applying the following formula:

$$\text{Baud rate} = \frac{\text{X1 clock}}{(16 \times \text{divisor})} \quad (1)$$

Normally an X1 clock is chosen so that standard baud rates of 50, 300, 600, 2400, 4800, 9600, 19.2 k, 38.4 k, 57.6 k and 115.2 k bits are supported by the UART. In most UART applications these standard baud rates can be derived from the standard 1.8432 MHz crystal or oscillator. And because the baud rates are very much depending on the frequency used, any deviation of the X1 clock will also cause the baud rates to deviate from their desired values.

For example, if a UART is programmed to a desired baud rate of 9600 based on a 1.8432 MHz clock (DLL = 0x0C and DLM = 0x00), and now assume that this 1.8432 MHz clock changes to 1.8063 MHz (–2 %), the baud rate now instead of 9600 will be 9408 (using the formula in Equation 1), which corresponds to –2 % of the 9600.

Because UARTs communicate with each other based on asynchronous methodology, they use start and stop bits to indicate the beginning and the end of a byte, rather than a clock signal. Therefore, both UARTs must be programmed to the same baud rate. A large deviation of baud rate from either UART will cause the receive UART to sample the wrong bit, and hence, the wrong byte.

One method most UARTs now employ to allow larger frequency deviation of the baud rates is to over-sample the incoming data at 16 times the baud rate to determine the near center of the start bit. Once this is done, the next bit is sampled 16 clocks later. At 16× over-sampling of the incoming data, the UART typically allows about ±5 % of deviation (assume a byte consists of one start bit, 8 data bits, and one stop bit) from its programmed baud rate value without causing any receiving error due to the baud rate differentiation between the two UARTs.

Devices with date code prior to 0443 (Revision B die) allow frequency deviation up to –0.5 % if the incoming baud rate is less than their programmed baud rate, and up to 5.6 % if the incoming baud rate is more than their programmed baud rate.

Therefore, if the UART is programmed to 9600 baud, and if the baud rate of the incoming signal is slightly off, for example 9550 baud, then the allowable deviation from 9600 is only –0.5 %. If the baud rate of the incoming signal is slightly faster, for example 9690 baud, then the allowable deviation from 9600 is around 5.6 %.

2.2 Change

The baud rate tolerance is now increased from –0.5 % to –4.4 % and the +5.6 % tolerance remains the same.

3. Conclusion

Any device with date code of 0443 or later should have the –4.4 % and +5.6 % baud rate tolerance (one start bit, 8 data bits, no parity, and one stop bit), and therefore, is immune to the variation between the transmitter and the receiver clocks up to the specified tolerances. If you have further technical questions, e-mail us at datacom.tech-support@philips.com.

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5. Contents

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