AN10576

Migrating to the LPC2300/2400 family

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Document information

Info	Content
Keywords	LPC2000, LPC23xx, LPC24xx, Migration
Abstract	This application note covers the important features that were added to the LPC23xx/24xx family of devices. These features should be considered if one is currently migrating from an LPC210x/LPC22xx/LPC21xx device.

Revision history

Rev	Date	Description
01	20070201	First revision

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1. Introduction

LPC2364/2366/2368/2378 are ARM-based microcontrollers for applications that require serial communication for a variety of purposes. These microcontrollers incorporate a 10/100 Ethernet MAC, USB 2.0 Full Speed interface, four UARTs, two CAN channels, an SPI interface, two Synchronous Serial Ports (SSP), three I^2C interfaces, an I^2S interface, and a MiniBus (LPC2378 only: 8-bit data/16-bit address parallel bus).

LPC2468 is similar to the LPC2300 family. The LPC2468 also adds an USB Host/OTG, an external bus, and higher I/O count, making this simply the most powerful series of ARM7-based microcontrollers in the marketplace.

Significant improvements were made to these devices, and an application previously designed for an LPC2000 device (except LPC28xx devices) may have to consider them during the porting process.

The following sections are covered in this document:

1. Clock structure
2. APB divider
3. Dual AHB bus architecture
4. DMA engines
5. Enhanced peripherals
6. Miscellaneous notes

2. Clock structure

The clock structure in the LPC2300/2400 follows the following block diagram:

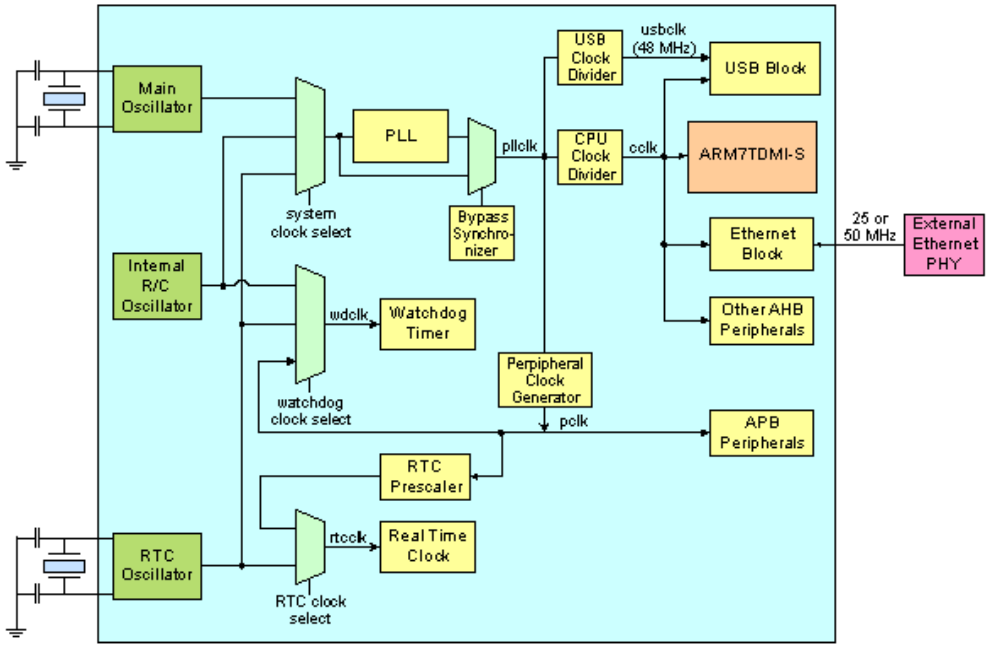

Fig 1. LPC2300/2400 clock structure

Points to be considered:

1. The internal RC oscillator can be considered as an important addition to this device. Chip operations (on reset or power-on) always begin with the internal RC oscillator. The IRC also gives an option of fast wakeup from the power saving “sleep” mode.
2. For USB and CAN applications, it is required that one uses the external oscillator. The USB block does not have a dedicated PLL and its clock is derived from the “pllclk” or “cclk” (please see above diagram). This further implies that crystal selection is limited (if USB is used).
3. The PLL accepts the RTC oscillator output as one of the clock sources. Hence, the chip can also just run out of the RTC oscillator. CAN and USB peripherals can also function from the RTC oscillator.
4. The internal watchdog timer can now select its clock source from three clock sources including the RTC oscillator.
5. The output of the PLL is termed as “pllclk”. A new CPU Clock Configuration Register (CCLKCFG- 0XE01F C104) takes “pllclk” as an input and generates “cclk”, which enables the CPU to run at a much slower frequency as compared to the PLL output. For instance, setting this register to 1 would enable the CPU to run at half the speed of the PLL output.
6. The main oscillator can accept an input frequency from a 1-24 MHz crystal.
7. PLL accepts an input frequency from 32 kHz to 50 MHz.

3. APB divider

In LPC2000, there used to be the APB divider register (also called VPB Divider register), which took the system clock (cclk) as the input frequency and generated the peripheral clock (pclk). “pclk” was then provided to all the peripherals. The APB divider register had three divider values- 00 (1/4th of cclk), 01 (pclk= cclk) or 02(1/2 of cclk). This implementation may cause some limitations on peripheral speeds.

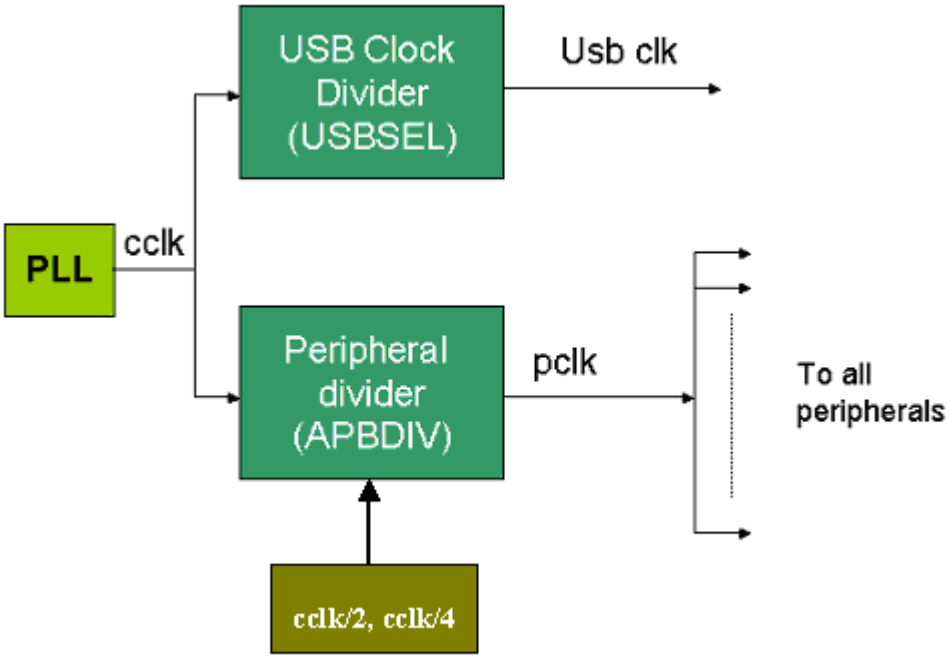

Fig 2. LPC2000 APB divider register

This approach of deriving pclk is improved in this family. ”cclk” is fed to a new register called Peripheral Clock Selection register (PCLKSELx- There is no APB Divider register). Using the PCLKSELx register the application can program individual clock dividers for the different peripherals according to the application’s needs. An additional divider of 1/8th is also added (which would be 1/6th in case of CAN).

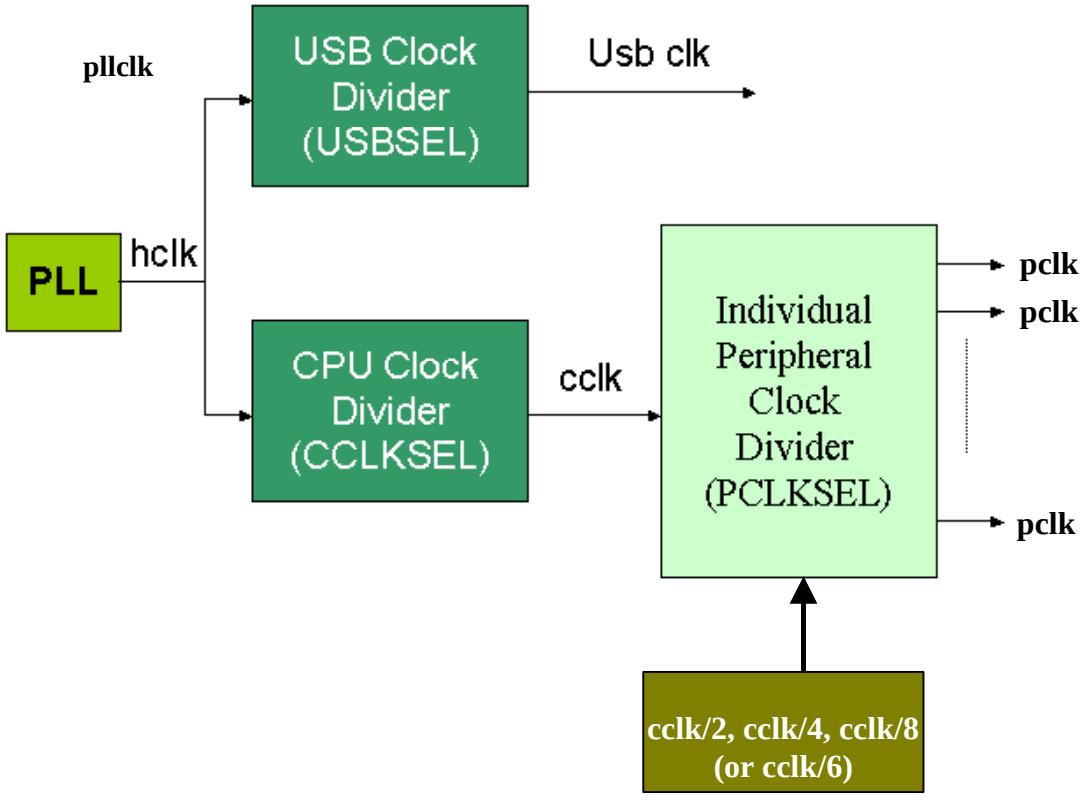

Fig 3. LPC2300/2400 clock selection registers

4. Dual AHB architecture

The dual AHB bus architecture allows simultaneous operations from the following modules:

1. CPU operation from internal memory
2. USB operation
3. Ethernet operation
4. General purpose DMA operation from peripherals that can support DMA

No manual configuration is needed to use the Dual AHB bus feature.

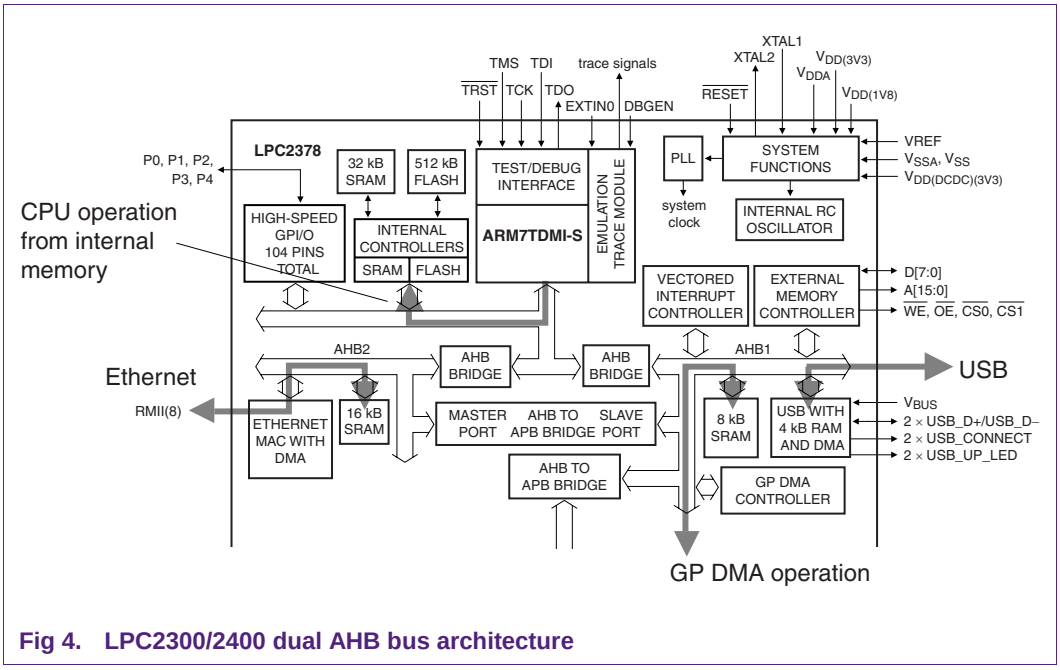

Fig 4. LPC2300/2400 dual AHB bus architecture

5. DMA engines

There are three main DMA engines in this family:

1. Dedicated DMA for Ethernet
2. Dedicated DMA for USB
3. General Purpose DMA for the following peripherals:
   a. SSP
   b. SD/MMC
   c. I^2S

5.1 Memory restrictions

Each DMA has restricted access to certain memories in the microcontroller.

5.1.1 Ethernet DMA

The Ethernet DMA has direct access to the 16kB of Ethernet SRAM. In addition to this memory, it can also access the 8kB of general purpose SRAM and the memory on the external memory bus (applies only for the LPC2378 and LPC24xx family). Both these memories are on the AHB2 bus.

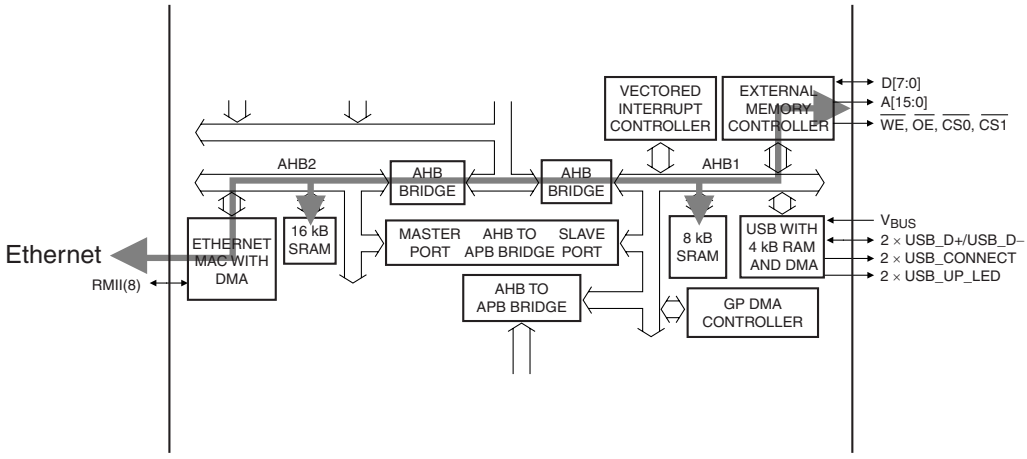

Fig 5. Ethernet memory access

5.1.2 USB DMA

The USB DMA has direct access to all the memories on the AHB2 bus including 4 kB of dedicated SRAM, 8 kB of general purpose SRAM, and the memory on the external memory bus (applies only to LPC2378 and the LPC24xx family).

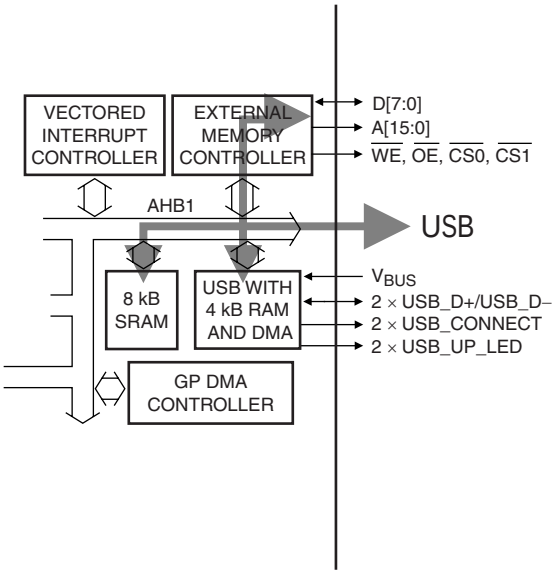

Fig 6. USB DMA memory access

5.1.3 General Purpose DMA

Similar to the USB DMA, it can access all the memories on the AHB2 bus except the 4 kB of dedicated USB SRAM.

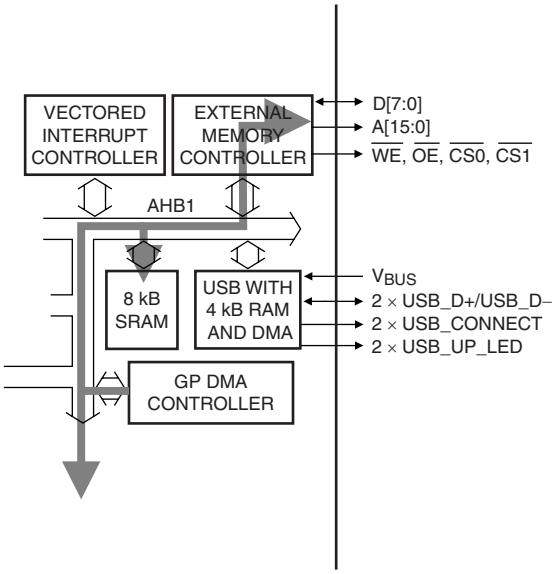

Fig 7. GPDMA memory access

Please note that none of the above DMA engines can access the memory on the ARM7 local bus. The memory on the local bus is only accessible by the ARM7 CPU. Below is a snapshot of the memory on the ARM7 local bus on the LPC2378:

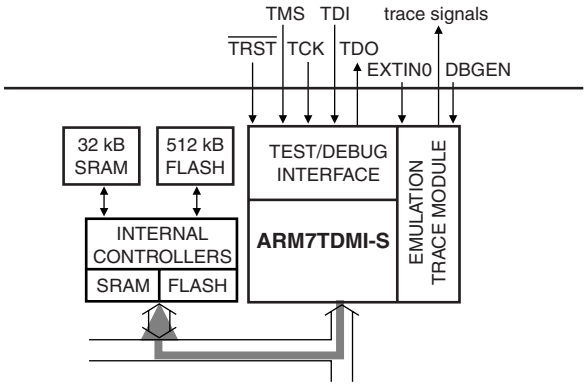

Fig 8. Memory access on the ARM local bus

6. Enhanced peripherals

6.1 GPIO

6.1.1 Pull-up resistors

In previous implementations of LPC2000, the pull-up resistors were always active. In LPC2300/2468, application has control over the activation/de-activation of pull-up resistors. Pin Mode Select Registers (PINMODEx) are now integrated into the LPC2000 family to provide this feature.

Table 1. Pin Mode Select register

PINMODE0 to PINMODE9 values	Function	Value after reset
00	Pin has an on-chip pull-up resistor enabled.	00
01	Reserved. This value should not be used.	
10	Pin has neither pull-up nor pull-down resistor enabled.	
11	Pin has an on-chip pull-down register enabled.	

On reset, the pull-resistors are always enabled.

6.1.2 External interrupts

All pins on ports 0 and 2 can now be used as external interrupts for rising and falling edges. The following registers in the GPIO chapter handle this feature:

- GPIO Interrupt Enable for Rising edge register (IO0IntEnR - 0xE002 8090 and IO2IntEnR - 0xE002 80B0)
- GPIO Interrupt Enable for Falling edge register (IO0IntEnF - 0xE002 8094 and IO2IntEnF - 0xE002 80B4)
- GPIO Interrupt Status for Rising edge register (IO0IntStatR - 0xE002 8084 and IO2IntStatR - 0xE002 80A4)
- GPIO Interrupt Status for Falling edge register (IO0IntStatF - 0xE002 8088 and IO2IntStatF - 0xE002 80A8)
- GPIO Interrupt Clear register (IO0IntClr - 0xE002 808C and IO2IntClr - 0xE002 80AC)

The traditional implementation of four external interrupt pins (EINT0-EINT3) is still intact which also have the optional wake up from Power-down mode feature.

6.2 Vectored Interrupt Controller (VIC)

Previous register map (LPC2000):

- Software Interrupt register (VICSoftInt - 0xFFFF F018)
- Software Interrupt Clear register (VICSoftIntClear - 0xFFFF F01C)
- Raw Interrupt status register (VICRawIntr - 0xFFFF F008)
- Interrupt Enable register (VICIntEnable - 0xFFFF F010)
- Interrupt Enable Clear register (VICIntEnClear - 0xFFFF F014)
- Interrupt Select register (VICIntSelect - 0xFFFF F00C)

- IRQ Status register (VICIRQStatus - 0xFFFF F000)
- FIQ Status register (VICFIQStatus - 0xFFFF F004)
  - Vector Control registers 0-15 (VICVectCntl0-15 - 0xFFFF F200-23C)
  - Vector Address registers 0-15 (VICVectAddr0-15 - 0xFFFF F100-13C)
  - Default Vector Address register (VICDefVectAddr - 0xFFFF F034)
  - Vector Address register **(VICVectAddr - 0xFFFF F030)**
  - Protection Enable register (VICProtection - 0xFFFF F020)

Current register map (LPC2300/LPC2400):

- Software Interrupt Register (VICSoftInt - 0xFFFF F018)
- Software Interrupt Clear Register (VICSoftIntClear - 0xFFFF F01C)
- Raw Interrupt Status Register (VICRawIntr - 0xFFFF F008)
- Interrupt Enable Register (VICIntEnable - 0xFFFF F010)
- Interrupt Enable Clear Register (VICIntEnClear - 0xFFFF F014)
- Interrupt Select Register (VICIntSelect - 0xFFFF F00C)
- IRQ Status Register (VICIRQStatus - 0xFFFF F000)
- FIQ Status Register (VICFIQStatus - 0xFFFF F004)
  - Vector Address Registers 0-31 (VICVectAddr0-31 - 0xFFFF F100 to 17C)
  - Vector Priority Registers 0-31 (VICVectPriority0-31 - 0xFFFF F200 to 27C)
  - Vector Address Register **(VICAddress - 0xFFFF FF00)**
  - Software Priority Mask Register (VICSWPriorityMask - 0xFFFF F024)
  - Protection Enable Register (VICProtection - 0xFFFF F020)

The following key improvements have been done to the VIC:

1. VIC register accesses are now controlled by software using the Protection Enable register (VICProtection-0xFFFF F020). This register is accessible only in an ARM privileged mode.
2. The VICAddress register resides in a new location in memory, i.e. 0xFFFF FF00. Hence the IRQ interrupt vector (residing at 0x18) should now be modified as:

   LDR PC, [PC, # -0x0120]

   Previously, the instruction would be:

   LDR PC, [PC, # -0x0FF0]
3. Spurious interrupts can no longer occur in the LPC23xx/LPC24xx. Hence the Default Address Register is no longer available in this family.

6.3 I^2C

There are 3 interfaces for the I^2C bus- I^2C0, I^2C1 and I^2C2. The three I^2C interfaces are identical except for the pin I/O characteristics. I^2C0 complies with entire I^2C specification, supporting the ability to turn power off to the LPC2300 without causing a problem with other devices on the same I^2C0 bus (which means that they are true open-drain pins). This is sometimes a useful capability, but intrinsically limits alternate uses for the same

pins if the I^2C interface is not used. Seldom is this capability needed on multiple I^2C interfaces within the same microcontroller.

Therefore, I^2C1 and I^2C2 are implemented using standard port pins and do not support the ability to turn power off to the LPC2300 while leaving the I^2C bus functioning between other devices. This difference should be considered during system design while assigning uses for the I^2C interfaces.

6.4 Watchdog

The watchdog now has three clock sources: RTC Oscillator, IRC Oscillator and peripheral clock (pclk). In the previous implementation of the LPC2000, the watchdog only accepted pclk as the clock source.

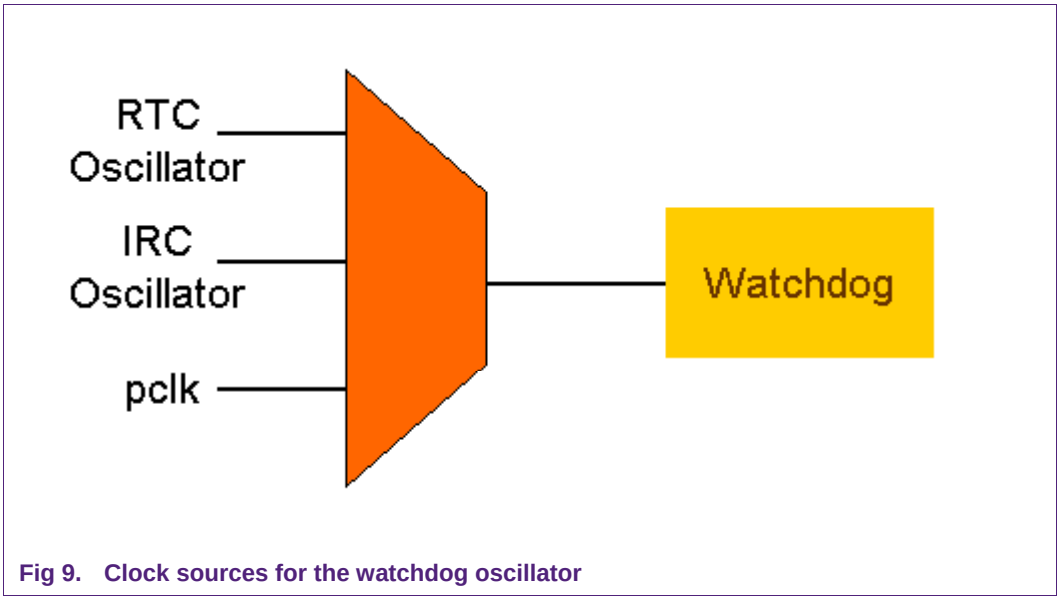

Fig 9. Clock sources for the watchdog oscillator

6.5 PWM

PWM capture inputs are provided along with the regular PWM outputs.

Table 2. PWM capture inputs

Pin name	Function	Description
PCAP1[1:0]	Input	Capture inputs. A transition on a capture pin can be configured to load the corresponding Capture register with the value of the Timer Counter and optionally generate an interrupt. PWM1 brings out 2 capture inputs.

6.6 RTC

The following improvements have been done to the RTC.

6.6.1 Battery SRAM:

2 kB of battery SRAM is provided in the RTC domain. In Deep Power-down mode (explained later in Section 6.7), the chip power can be removed and only the RTC

domain can be kept active using the VBAT and RTC X1/X2. VBAT also keeps the battery RAM alive.

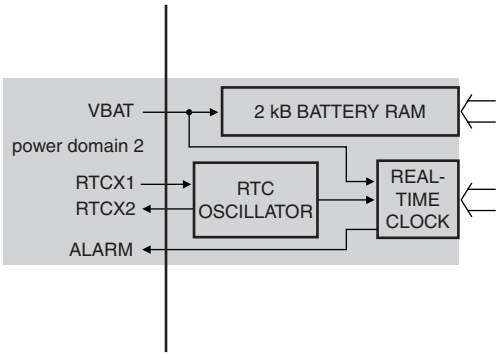

Fig 10. Battery SRAM

6.6.2 RTC interrupts

Sub-second interrupts are now available in the LPC2300/2400 devices. Interrupt granularity can now be as low as 488 microseconds. Please refer to the Counter Increment Select Mask (CISS- 0XE002 4040) for further details.

6.7 Power saving modes

Two additional power saving modes have been added to LPC2300/2400.

6.7.1 Sleep mode

When the chip enters the Sleep mode, the main oscillator is powered down and all clocks are stopped. The output of the IRC is disabled, but the IRC is not powered down for a fast wakeup later. The 32 kHz RTC oscillator is not stopped because the RTC interrupts may be used as the wakeup source. The flash is left in the standby mode allowing a very quick wakeup. The PLL is automatically turned off and disconnected. The CCLK and USBCLK clock dividers automatically get reset to zero.

6.7.2 Deep Power-down mode

Deep Power-down mode is like Power-down mode, but the on-chip regulator that supplies power to internal logic is also shut off. This produces the lowest possible power consumption without actually removing power from the entire chip. Since Deep Power-down mode shuts down the on-chip logic power supply, there is no register or memory retention, and resumption of operation involves the same activities as a full-chip reset. If power is supplied to the LPC2300 during Deep Power-down mode, wakeup can be caused by the RTC Alarm or external Reset. While in Deep Power-down mode, external device power may be removed. In this case, the LPC2300 will start up when external power is restored.

7. Miscellaneous notes

7.1 Note 1- ISP entry

It’s no longer P0_14 that controls the entry into ISP mode. ISP mode entry is now transferred to P2_10.

7.2 Note 2- bootloader

The boot code for the LPC2300 is a little different from those for the previous NXP’s ARM7 LPC2000 chips. When there is no valid code (determined by the checksum word) in the user flash, or the ISP enable pin (P2_10) is pulled low on startup, the ISP mode will be entered, and the boot code will setup the PLL with the IRC. Therefore it cannot be assumed that the PLL is disabled when the user opens a debug session to debug the application code. The user startup code must follow the steps described in the “Clocking and power control” chapter to disconnect the PLL. The boot code may also change the values for some registers when the chip enters ISP mode. For example, the GPIOM bit in the SCS register is set in ISP mode. If the user doesn't notice it and clears the GPIOM bit in the application code, the application code will not be able to operate with the traditional GPIO function on PORT0 and PORT1.

7.3 Flash programming

The Philips ISP Utility will not be supporting this family of devices. Instead, NXP has partnered with Embedded Systems Academy to provide the Flash Magic software for the LPC2000 family. Flash Magic has been a very successful tool for our 8-bit family, and currently they have integrated support for the entire LPC2000 family. This software is free for download at http://www.nxp.com/esacademy/.

7.4 Boundary scan

The JTAG port may be used either for debug or for boundary scan. The state of the DBGEN pin determines which function is available. When DBGEN = 0, the JTAG port may be used for boundary scan. When DBGEN = 1, the JTAG port may be used for debug. BSDL files are now available for some devices of this family, which can be found at http://www.nxp.com/standardics/support/documents/.

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