AN11404

Pin FMEA for NX5P/NX18P3001 bidirectional high-side power switches for chargers and USB-OTG combined applications

Rev. 1 — 23 January 2014 **Application note**

Document information

Info	Content
Keywords	FMEA
Abstract	This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of NXP Semiconductors bidirectional high-side power switches

Revision history

Rev	Date	Description
v.1	20140123	initial version

Contact information

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1. Introduction

The NX5P/NX18P3001 is an advanced bidirectional power switch and ESD-protection device for combined USB-OTG and charger port applications. It includes under voltage lockout, over voltage lockout and over temperature protection circuits designed to automatically isolate the power switch terminals when a fault condition occurs.

The device features two power switch input/output terminals (VBUSI and VBUSO), an open-drain acknowledge output (ACK), an enable input which includes logic level translation ($\overline{EN}$) and low capacitance transient voltage suppression (TVS) type ESD clamps for USB data and ID pins.

When $\overline{EN}$ is set HIGH the device enters a low-power mode, disabling all protection circuits. When used in combined charger and USB-OTG applications, the 30 V tolerant VBUSI switch terminal is used as the supply and switch input when charging. For USB-OTG the VBUSO switch terminal is used as the supply and switch input.

Designed for operation from 3.2 V to 6.35 V (17.5 V for NX18P3001), it is used in battery charging and power domain isolation applications to reduce power dissipation and extend battery life.

2. Pin FMEA

This chapter provides an FMEA (Failure Mode and Effect Analysis) for typical failure situations, when the pins of bidirectional high-side power switch for charger and USB-OTG combined applications family are short circuited to supply IO, GND or neighbor pins or simply left open.

The individual failures are classified, according to their corresponding effects on a device and the functionality; see Table 1.

Table 1. Classification of failure effects

Class	Failure effect
A	damage to this device
	functionality of application affected
B	no damage to this device
	functionality of application may be affected
C	no damage to this device
	functionality of application not affected

Table 2. FMEA matrix for pin short-circuit to supply IO

Pin	Class	Remarks
Input	A	When Supply IO is higher than 6.35 V, it causes device damage.
	B	When Supply IO is lower than 6.35 V, no damage to this device. Functionality is affected.

Table 2. FMEA matrix for pin short-circuit to supply IO *…continued*

Pin	Class	Remarks
Output	C	If output defined HIGH and supply IO is lower than 6.35 V, the device has no damage, no leakages.
	A	If output defined HIGH and supply IO is higher than 6.35 V, it causes device damage.
	A	If output defined LOW, short circuited and high currents can damage device. Output level changed.
ESD IO	B	No damage to this device if supply IO is lower than 6.35 V, increased leakages. Functionality of application is affected. Functionality of the device is not affected.
	A	If supply IO is higher than 6.35 V, it causes device damage. Functionality of application is affected.
GND	A	Short circuited and high currents can damage device. Functionality is affected.

Table 3. FMEA matrix for pin short-circuit to GND

Pin	Class	Remarks
Input	B	No damage to this device, no leakages, functionality may be affected
Output	C	If output defined LOW, no damage, no leakages, same output level
	A	If output defined HIGH, short circuited and high currents can damage device. Output level changed.
ESD IO	B	No damage to this device. Functionality of application is affected. Functionality of the device is not affected.
Supply IO	-	see Table 2

Table 4. FMEA matrix for pin left open

Pin	Class	Remarks
Input	B	undefined operating condition, no damage, increased leakage, functionality may be affected
Output	C	normal operating condition, no damage, no leakages.
GND	B	undefined operating condition, no damage, increased leakages. functionality is affected.
ESD IO	C	normal operating condition, increased leakages. Functionality of application not affected
Supply IO	B	If all supply IO's are left open, undefined operating conditions, no damage, increased leakages. functionality is affected
	A	If part of supply IO's are left open and part of supply IO is connected to source, it causes device damage in case of large continuous current.

Table 5. FMEA matrix for pin short-circuits between neighbor pins

Pin	Class	Remarks
Input to ESD IO	B	no damage to this device, increased leakages. functionality may be affected.
Input to supply IO	-	see Table 2

Table 5. FMEA matrix for pin short-circuits between neighbor pins *...continued*

Pin	Class	Remarks
Input to output	A	Different input and output voltage levels, causes circuit high-currents and device damage. functionality is affected.
	C	When input has same voltage level as output, no damage, no leakages.
Output to ESD IO	B	no damage to this device, increased leakages. functionality may be affected
Output to input	-	see “Input to output”
Output to GND	-	see Table 3
Output to supply IO	-	see Table 2
GND to supply IO	-	see Table 2
GND to ESD IO	-	see Table 3
Supply input to supply output	B	no damage to this device. functionality is affected.

2.1 Pin name mapping

Supply IO: VBUSI, VBUSO

ESD IO: D+, D–, ID

Input: $\overline{\text{EN}}$

Output: ACK

3. Abbreviations

Table 6. Abbreviations

Acronym	Description
FMEA	Failure Mode and Effect Analysis

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