AN11590

PTN3356 PCB Layout Guideline, Reference Schematics and BOM

Rev. 1 — 29 January 2015 Application note

Document information

Info	Content
Keywords	DisplayPort, PTN3356
Abstract	This document provides a practical guideline to PTN3356 application design and layout.

Revision history

Rev	Date	Description
1	20150129	Initial version

Contact information

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1. Introduction

This document provides a guideline for PTN3356 application and layout guide line in ULT notebook, docking station and dongle designs.

PTN3356 is a small packaged low power DisplayPort to VGA adapter IC designed to connect a DisplayPort source to a VGA sink. PTN3356 is in HVQFN32 package, which is 5mmx5mm, with 0.5 mm pitch. PTN3356 consumes approximately 200 mW of power for video streaming in WUXGA resolution and 410 uW of power in low-power mode.

The VGA output is powered down when there is no valid DisplayPort source data being transmitted. PTN3356 is suitable for Ultra Low Power Notebook and other low power devices.

PTN3356 is powered from a 3.3 V power supply, and generated 1.5 V through an internal step-down switch regulator and buck converter for internal core usage and DAC usage.

The PTN3356 also aids in monitor detection by performing load sensing and reporting sink connection status to the source.

2. Reference designs

2.1 ULT notebook design

PTN3356 can be connected directly to the DP lanes on mother board, or on docking station.

Connect PTN3356 to one of the DP port on PCH/GPU with 0.1 uF AC caps in series for DP data lanes and AUX lanes. PTN3356 probably will be used as primary display, make sure BIOS is set accordingly.

Below is a reference design for one VGA application.

Note:

1. ESD protection is optional circuitry.
2. U3 is required to support 5 V H/V for legacy projectors and CRTs.
3. PI filter design is customer specific.

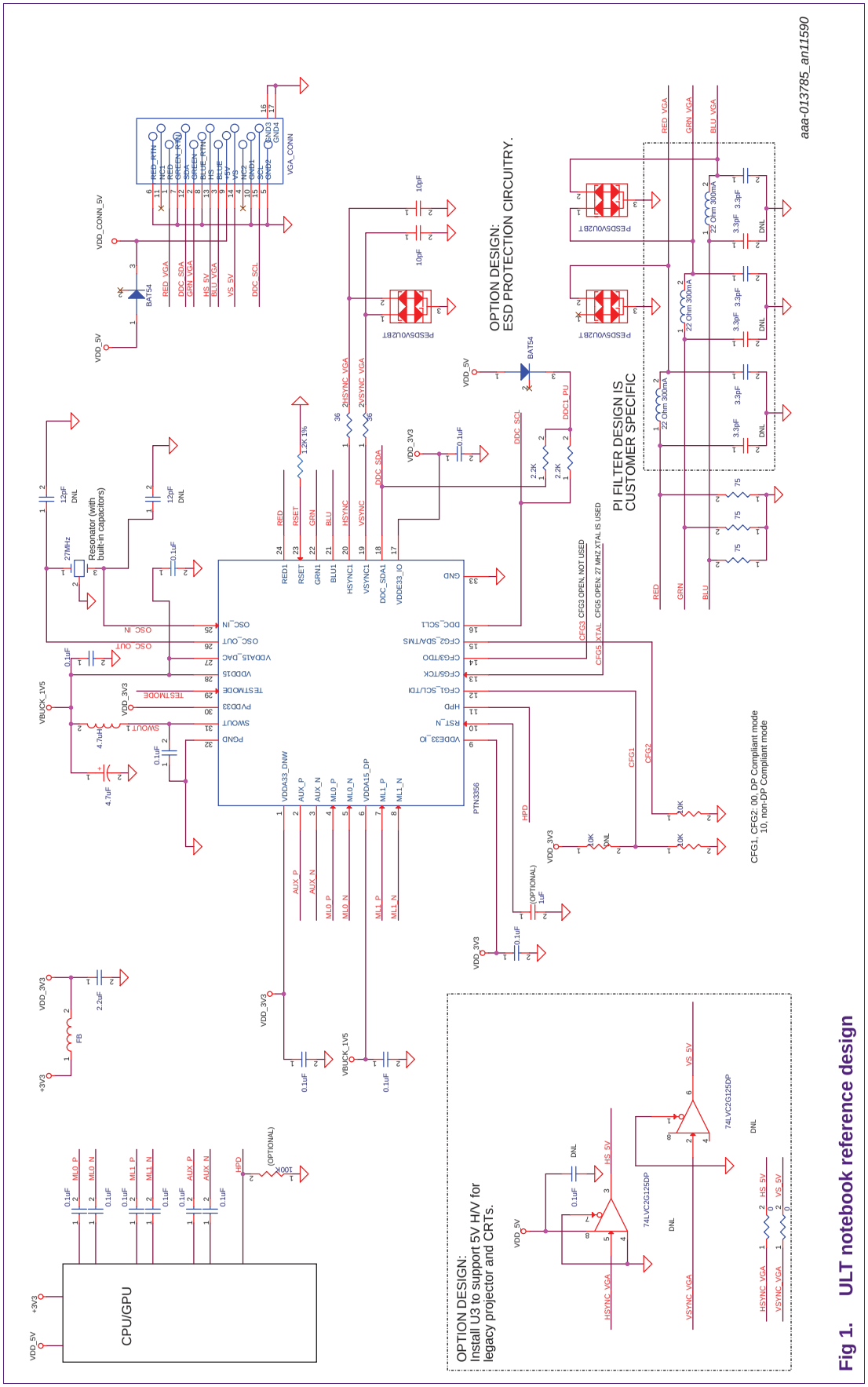

Fig 1. ULT notebook reference design

2.2 Dongle design

PTN3356 can also be used on DP-VGA dongles.

Connect PTN3356 DPVGA to one of the DP port on the system board.

DPVGA dongle gets 3V3 power from DP connector for PTN3356 IC operation, then boost up to 5V for VGA connector.

Note:

1. ESD protection is optional circuitry.
2. U3 is required to support 5 V H/V for legacy projectors and CRTs.
3. PI filter design is customer specific.

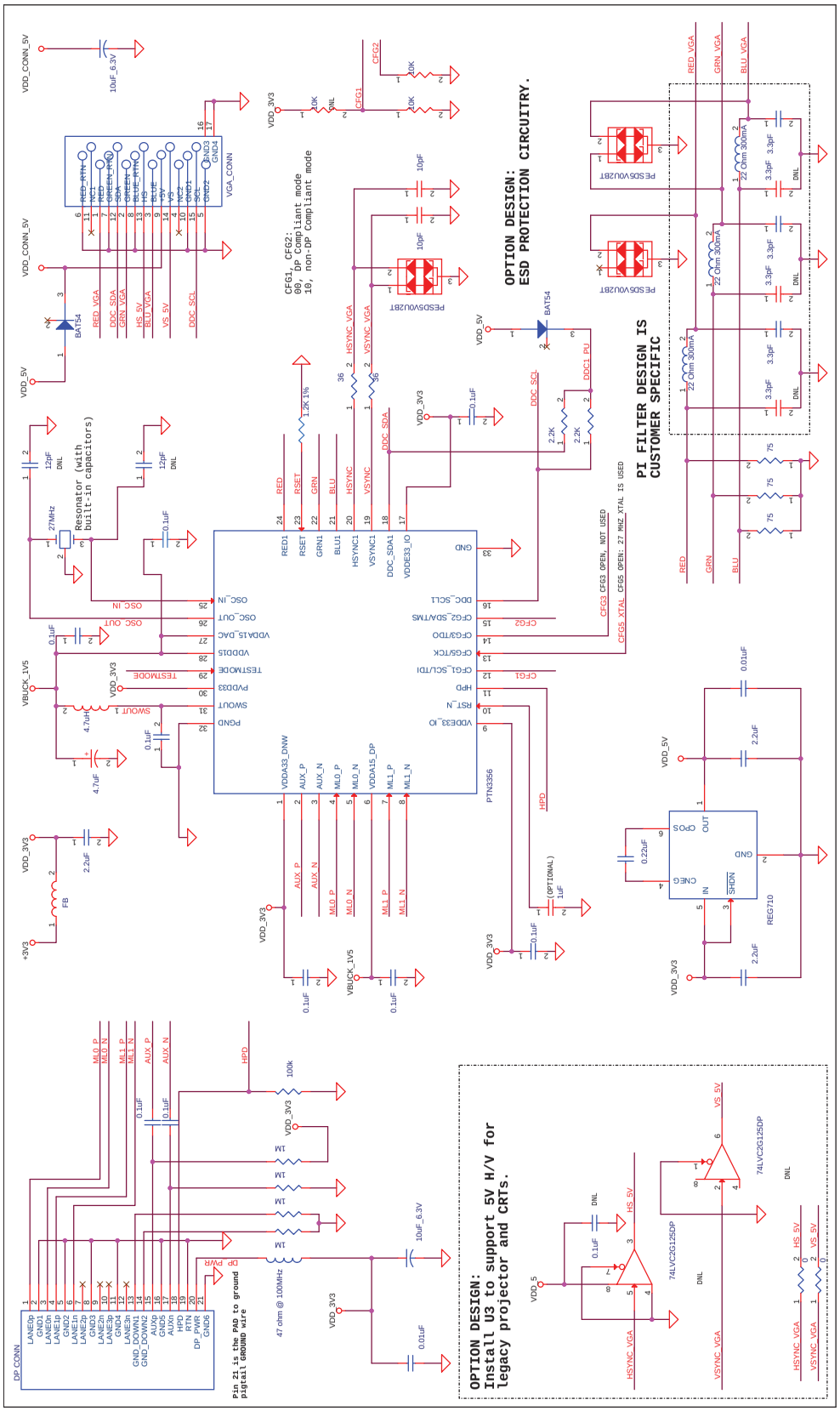

Fig 2. ULT DPVGA dongle reference design

2.3 Minimum BOM design

For cost conscious application, PTN3356 needs only a handful of components to function.

Below is a minimum BOM design for embedded or dongle design.

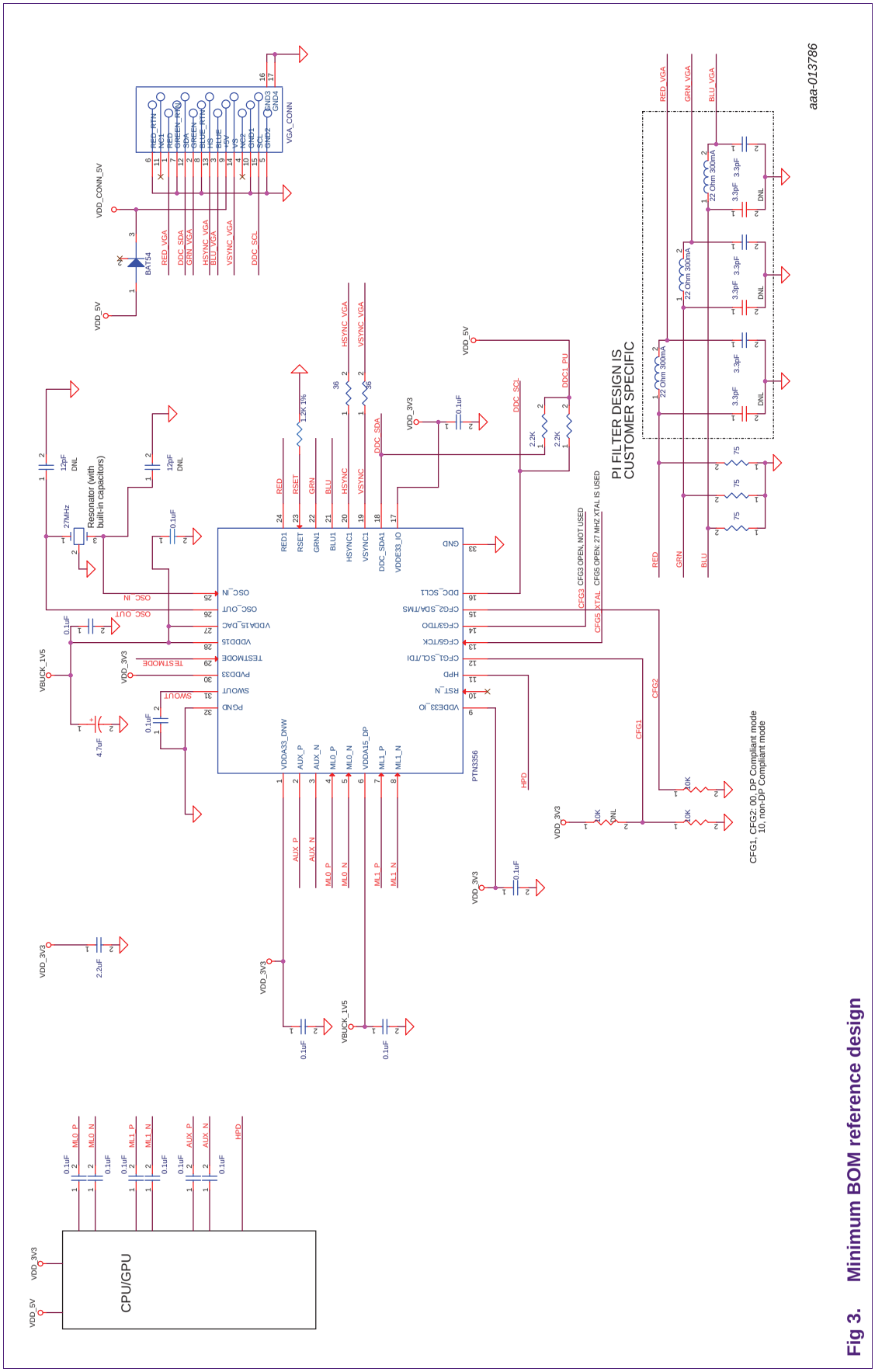

Fig 3. Minimum BOM reference design

3. Buck converter

3.1 Buck converter layout guideline

PTN3355 utilizes a switch mode power supply to deliver the power needed with highefficiency. Switch mode power supplies require careful attention to the PC board layout.

There are two switching high-current loops formed by the switching action of the buck converter. One loop is formed by the current that flows from the input capacitor through the PVDD pin of the part, through the internal PMOS High-side switch, out the SW pin, through the inductor and the load capacitor to the analog ground, and through the ground plane back to the ground connection of the input capacitor. A second switching high current loop is formed when the low-side NMOS switch is on.

The current flows from the PGND pin of the part through the internal NMOS switch, out the SW pin, through the inductor and the load capacitor, to the analog ground, and through the ground plane back to the PGND pin of the part.

Below is a minimum BOM design for embedded or dongle design.

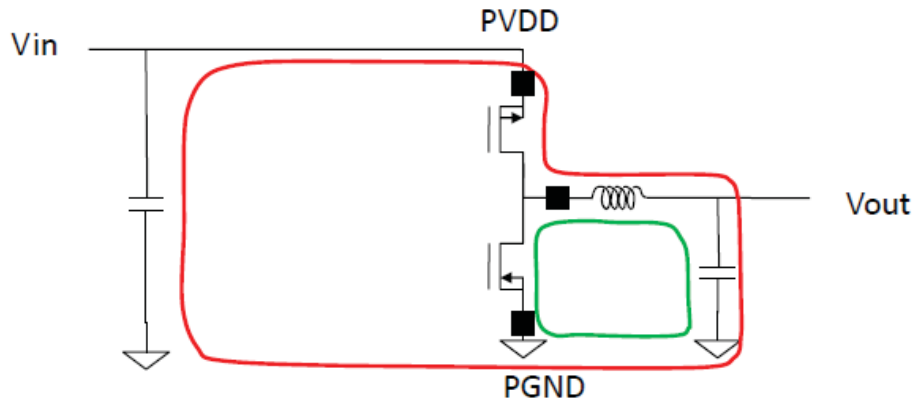

Fig 4. Switching High-current Loop1: PVDD - LC - PMOS -- GND

To minimize electromagnetic interference (EMI), it is essential to minimize the length and area of the switching high current loops. It is also critical that the two switching current paths are matched as closely as possible.

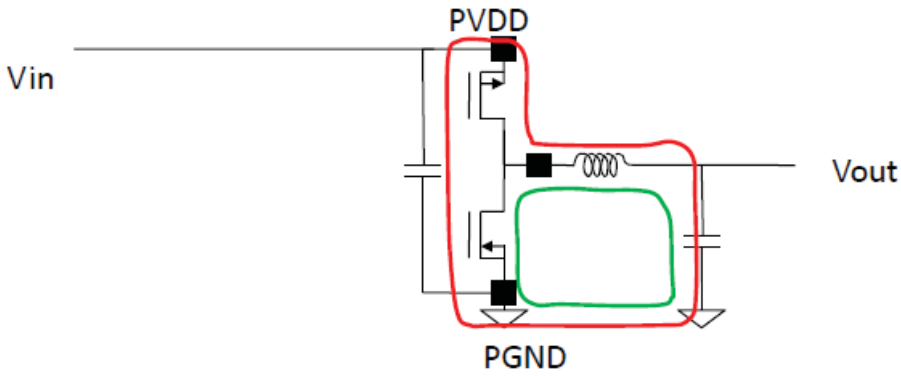

Fig 5. Switching high-current loop2 : PGND - NMOS - SW - LC - GND

Here are some guidelines for PC board design:

- Connect the exposed paddle of the IC to the PC board ground plane.
- Place the input capacitor as close to the PVDD pin as possible.
- Place the inductor and the load capacitor as close to the SW pin as possible.
- Keep the traces for the input capacitor, inductor and the output capacitor, short, direct and wide.
- Do not connect the PGND pin directly to the ground plane, instead, connect the PGND pin and the input capacitor's ground pin to the ground plane at the same point.
- Minimize the distance between the input capacitor's ground and the ground of the load capacitor.
- Keep the trace for the FB (Vout to VDD1V5) away from the switching high current paths.

The following is a proposed PC board layout scheme for the PTN3356 which minimizes the area of the two switching current loops and matches the current flow paths for the two loops as closely as possible.

Note the smaller capacitors are 0.1uF caps that must be place as close to the pin as possible.

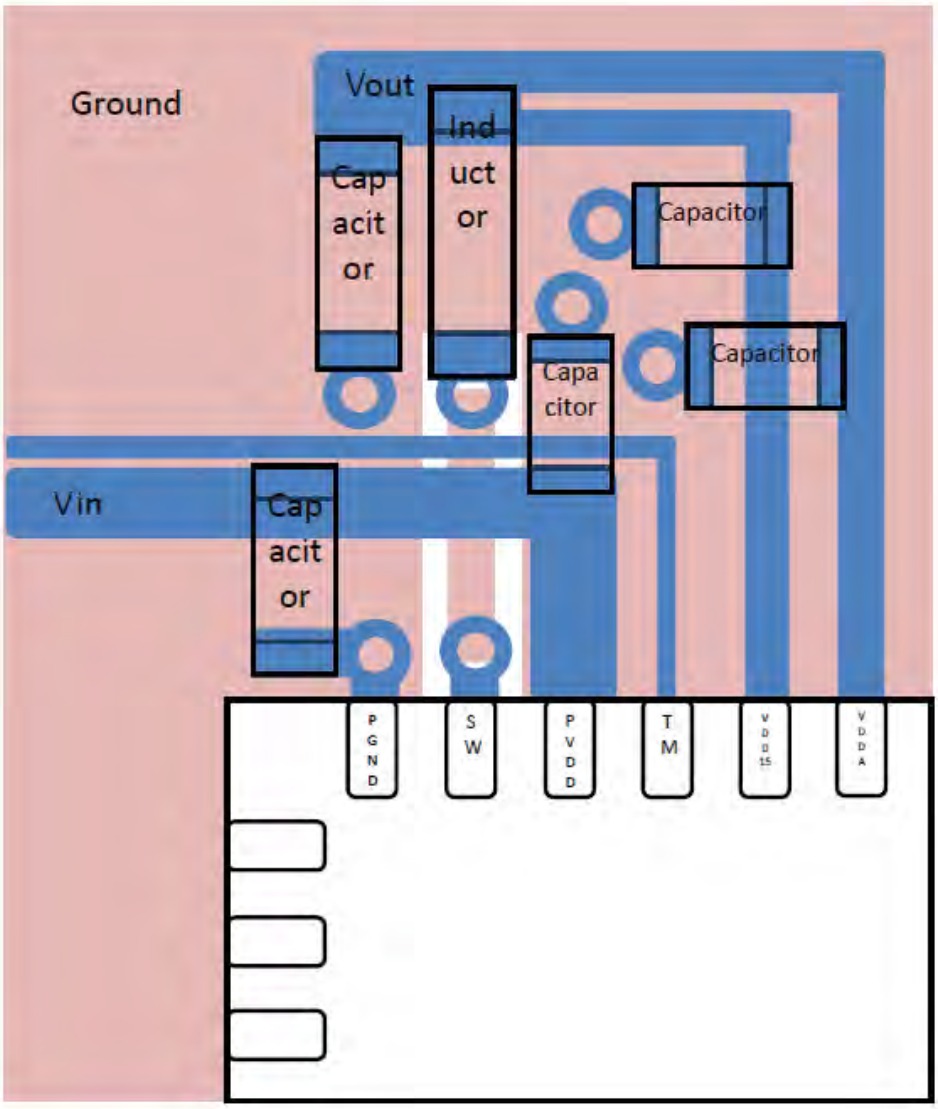

Fig 6. Buck converter component placement

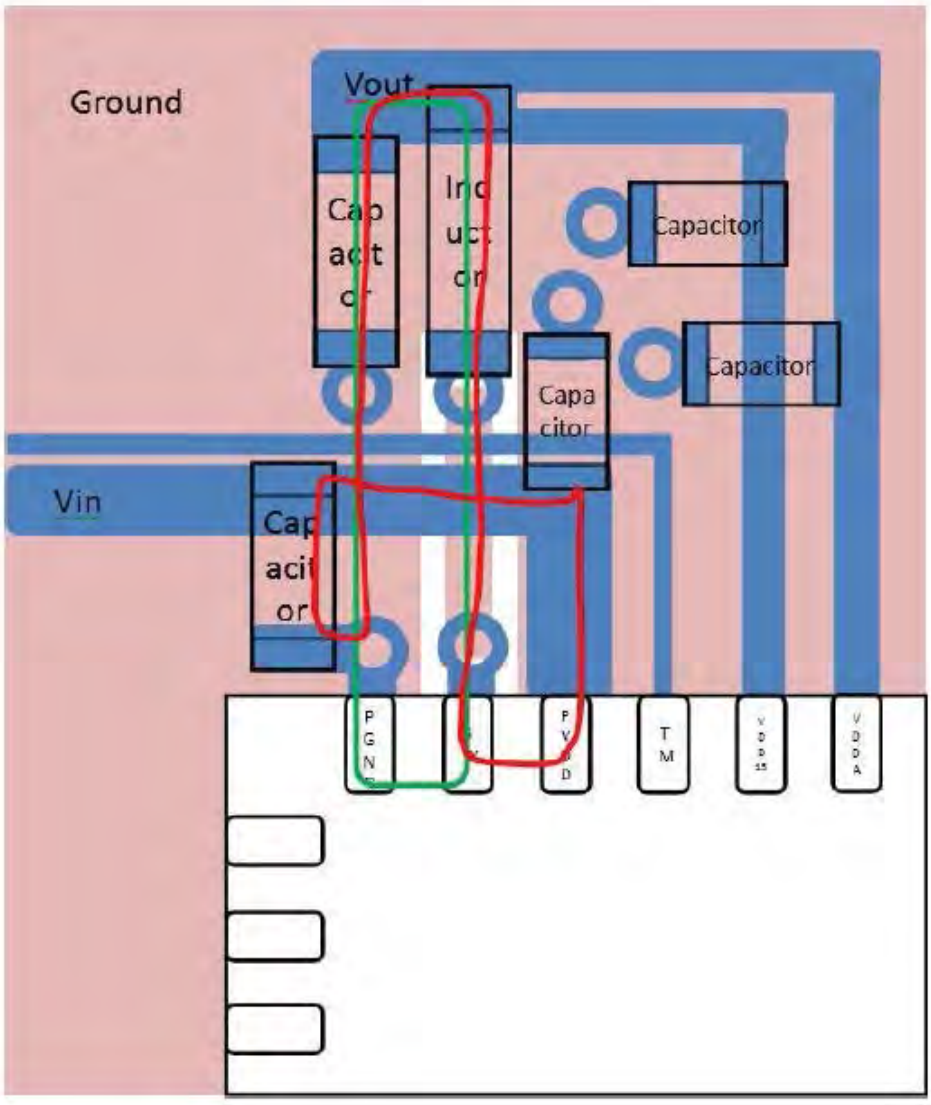

Fig 7. Buck converter switching current loops

3.2 Buck converter schematic

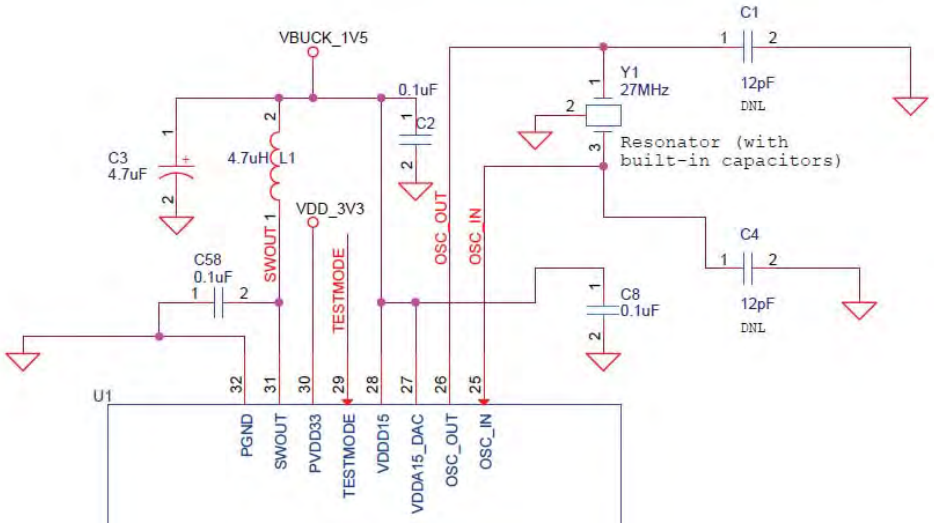

Fig 8. Buck converter schematics

4. Low EMI emission

DPVGA design was simulated by IC design team, in the following steps:

1. 3D simulations
   a. Obtain the Transfer function
   b. Obtain the S11 (S-parameters)
2. Circuit simulations
   a. Insert the S11 information (step 1 b)
   b. Compute and process the actual signal spectrum
3. Use Matlab to calculate the actual radiated emission spectrum by multiplying the transfer function (step 1 a) with the actual signal spectrum (step 2 b).

Pre-Compliance Test was measured following EMC standards and passed.

- CISPR 22: 2005-04; A1: 2005-07; A2: 2006-01
- EN 55022: 2006-09; A1: 2007-10

For information technology equipment, Criterion B is used, that is:

During application of the transient test, degradation of performance including loss of function is allowed provided that the EUT self-recovers to normal operation after testing without any operator intervention.

5. ESD protection

A crucial element in EMC/ESD immunity is a solid PCB design. Good practices such as decoupling power and I/O lines to ground, voltage and frequency (bandwidth) limiting, wave shaping (edge-rate control), using negative feedback, refresh cycling, WDT, and fault tolerant software-all play collectively an important role in improving EMC and ESD immunity.

PTN3356 is designed for 7.5 kV ESD HBM JEDEC.

Still, ESD protection diodes are recommended for RGB and H/V sync lines at VGA connector.

6. Reset circuitry

No external power-on reset circuitry is needed; this is been taken care of automatically by PTN3356. Its RESET pin (pin 11) allows for connection of a suitable capacitor to optimally time its internal power-on reset sequence.

7. Crystal oscillator

The Processor is clocked with the on-chip free-running oscillator or from the external 24/25/27 MHz crystal oscillator through a PLL. Video clock is generated from the crystal clock and DisplayPort main link with M/N relation transmitted over the link.

Crystal selection is done through CFG5 pin section:

- HIGH: 24 MHz
- LOW: 25 MHz
- OPEN: 27 MHz

The M and N are 24 bit values used for stream clock recovery.

External crystal is mainly used for processor and control, the precision of the crystal is not critical, +/- 50 ppm is good enough.

8. Bias, reference and tie-off

8.1 Video DAC bias

One external bias resistor to ground is required for video DAC outputs. This resistor sets the reference current which determines the analog output level.

Pin 23 Rset = External bias resistor value

1.2K Ohm +/- 1% is required, because non-linearity increases with larger bias resistors.

8.2 Internal LDO

PTN3356 internal LDO will be turned on to provide 1.5V to core and DAC when external 4.7uH inductor is not detected.

Note, the power consumption will increase two fold when internal LDO is used.

It is a trade-off; using buck converter will save power, add cost of 4.7 uH inductor; using internal LDO will save cost with the expense of power increase.

9. DP receiver interface

Main differential pairs and AUX channel are routed with 100 Ohm impedance. The important parameters to calculate the impedance are:

- PCB thickness
- Distance to ground plane
- Trace width
- Trace spacing
- PCB permittivity

Guard grounds are used to isolate the pair. This helps to eliminate cross talk between traces. Trace lengths are matched on the same pair to 0.01". Inter pair match to 1".

AC caps for DP lanes and AUX pair should be placed close to the DP interface.

When signals change plane, the ground plane need to move along to keep constant trace impedance. On DPVGA a ground island is inserted on the VCC plane for this purpose.

10. VGA interface

Table 1. Design guidelines for VGA connector, PWB to cable junction

Design guideline number	Design guideline description	Approximate impact on EMI decrease
1	Define the 2nd PWB layer as ground plane	
2	Connect the ground chassis pins of the VGA PWB-connector	25 dB
3	Use an upper ground plane around VGA connector pins This design guideline makes no sense when it is not combined with design guideline 4.	
4	Use enough vias to connect the upper ground plane with main ground plane in 2nd PWB layer. Enough means around every 3 mm (stitching)	20 dB
5	Ensure proper connection between PWB-connector chassis and upper ground plane by using contact springs (at least 3 contact points) Emission improvement when either 1 or 3 contacts were used was 10 dB!	10 dB
6	Apply ferrite bead around VGA cable (is already very common for typical cables available from the market)	3 dB

Following the recommended guidelines, all RGB traces on DPVGA board are routed with 75 Ohm impedance from PTN3356 to VGA connector. Ground fills are used to isolate these traces. Ground fills are connected to ground plane with vias.

11. PCB stack up

4-layer FR4 PCB is sufficient for PTN3356 DP-VGA layout. Suggested layers:

1. Signal layer 1 for DPs, with ground cover the entire buck converter area plus power islands or thick traces for Vin and Vout for buck converter.
2. Ground layer
3. Power layer with VDD_3V3 islands to cover entire PTN3356, except pin 31, 28, 27 and pin 6.
4. Signal layer 2

12. PTN3356 on notebook BOM

PTN3356 DPVGA Reference Design Revised: Modify, August 20, 2014
Revision: 0.3

NXP Semiconductors

Bill Of Materials August 20, 2014

Item	QTY	Reference	Value	PCB Footprint	Feature	Manufacturer	Manufacturer Number	Vendor N.	Load Option
2	13	C2,C8,C10,C11,C13,C19,C20,C21,C24,C58,C59,C60,C61	0.1uF	rc0201	CAP CER 0.1UF 10V 10% X5R 0201	TDK Corporation	C0603X5R1A104K	Digikey, 445-7318-2-ND	LOAD
4	1	C5	2.2uF	rc0603	CAP CER 2.2UF 10V 10% X5R 0603	Taiyo Yuden	LMK107BJ225KA-T	Digikey, 587-1253-2-ND	LOAD
7	3	C27,C29,C31	3.3pF	rc0402	CAP CER 3.3PF 50V NP0 0402	Murata	GRM1555C1H3R3CZ01D	Digikey, 490-1270-2-ND	LOAD
11	2	D4,D5	BAT54	SOT23	DIODE SCHOTTKY 30V 200MA SOT23-3	Diode	BAT54TA	Digikey, BAT54TR-ND	LOAD
12	1	J1	VGA_CONN	DB-15_HD	CONN D-SUB RCPT 15POS HD R/A	EDAC	634-015-274-992	Digikey, 151-1125-ND	LOAD
15	3	L3,L4,L5	22 Ohm 300mA	rc0402	FERRITE CHIP 22 OHM 300MA 0402	Murata	BLM15BB220SN	Digikey, 490-5187-2-ND	LOAD
16	1	R16	1.2K 1%	rc0402	RES 1.20K OHM 1/10W 1% 0402 SMD	Panasonic	ERJ-2RKF1201X	Digikey, P1.20KLTR-ND	LOAD
17	2	R21,R39	0	rc0201	RES 0 OHM 1/20W 5% 0201 SMD	Panasonic	ERJ-1GE0R00C	Digikey, P0.0AGTR-ND	LOAD
18	2	R29,R30	36	rc0402	RES 36 OHM 1/16W 5% 0402 SMD	Panasonic	ERA-2AKD360X	Digikey, P36DDTR-ND	LOAD
19	3	R31,R32,R33	75	rc0402	RES 75.0 OHM 1/10W 1% 0402 SMD	Panasonic	ERJ-2RKF75R0X	Digikey, P75.0LTR-ND	LOAD
20	2	R34,R35	2.2K	rc0402	RES 2.2K OHM 1/10W 5% 0402 SMD	Yageo	RC0402JR-072K2L	Digikey, 311-2.2KJRTR-ND	LOAD
23	1	U1	PTN3356	HVQFN32	DPVGA	NXP	NXP_PTN3356	NXP_PTN3356	LOAD
25	1	Y1	27MHz	2mm5x2mm	CER RESONATOR 27.00MHZ SMD/HZ 3225	ECS	ECS-HTR-27.00-B-TR	Digikey, XC1097TR-ND	LOAD
1	2	C1,C4	12pF	rc0402	CAP CER 12PF 50V 5% NP0 0402	Kemet	C0402C120J5GACTU	Digikey, 399-1013-1-ND	NO LOAD
3	1	C3	4.7uF	rc1206	CAP CER 4.7UF 16V 10% X7R 1206	TDK	C3216X7R1C475K/1.60	Digikey, 445-1385-2-ND	NO LOAD
5	1	C6	1uF	rc0603	CAP CER 1UF 10V 10% X5R 0603	Murata	GRM188R61A105KA61D	Digikey, 490-1548-2-ND	NO LOAD
6	3	C26,C28,C30	3.3pF	rc0402	CAP CER 3.3PF 50V NP0 0402	Murata	GRM1555C1H3R3CZ01D	Digikey, 490-1270-2-ND	NO LOAD
8	2	C32,C33	10pF	rc0402	CAP CER 10PF 50V 5% NP0 0402	Yageo	CC0402JRNPO9BN100	Digikey, 311-1014-2-ND	NO LOAD
9	1	C65	0.1uF	rc0402	CAP CER 0.1UF 10V 10% X5R 0402	Kemet	C0402C104K8PACTU	Digikey, PCC2146CT-ND	NO LOAD
10	3	D1,D2,D3	PESD5V0U2BT	SOT-23	DIODE ULOW ESD PROTECTION SOT-23	NXP	PESD5V0U2BT,215	Digikey, 568-4296-2-ND	NO LOAD
13	1	L1	4.7uH	rc1210	IND 4.7uH, 1210, 20%	Panasonic	ELJ-PA4R7MF2	Digikey, PCD2356TR-ND	NO LOAD
14	1	L2	FB	rc1206	FERRITE 3A 100 OHM 1206 SMD	Laird-Signal	HI1206N101R-10	Digikey, 240-2408-2-ND	NO LOAD
21	1	R36	100K	rc0402	RES 100K OHM 1/10W 5% 0402 SMD	Panasonic	ERJ-2GE0104X	P100KGTR-ND	NO LOAD
22	3	R57,R58,R59	10K	rc0201	RES 10K OHM 1/20W 5% 0201 SMD	Panasonic	ERJ-1GEJ103C	Digikey, P10KAGTR-ND	NO LOAD
24	1	U2	74LVC2G125DP	SOT505-2	IC BUS BUFF DVR TRI ST DL 8TSSOP	NXP	74LVC2G125DP,125	NXP_74LVC2G125DP	NO LOAD

Fig 9. BOM

13. HVQFN exposed center pad solder lands

PTN3356 uses HVQFN package.

The HVQFN package exposed center pad must be soldered to a corresponding solder land on the board for enhanced thermal, as well as electrical ground, performance.

During reflow soldering, solder paste melts and gas or trapped air is released, causing splattering or solder balling. Solder balling and splatter can be minimized if the solder paste is printed as a number of individual dots, instead of one large deposit, and if the solder paste is kept at a sufficient distance from the edge of the solder land.

The solder paste pattern area should cover 35 % of the solder land area. When printing solder paste on the exposed die pad solder land, the solder paste dot area should cover no more than 20 % of this solder land area. Furthermore, the paste should be printed away from the solder land edges. This is illustrated in 01; the solder paste pattern area lies within the boundary indicated by the red line and it is divided by the entire solder land area.

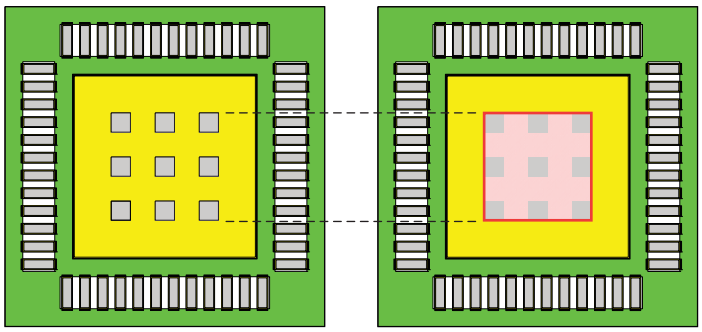

Fig 10. Solder paste dot area (left) and paste pattern area (right)

14. References

[1] PTN3356 preliminary datasheet, August, 2014

[2] PTN3356 Reference Design Schematics, rev 0.10

[3] AN10873.pdf, PTN3392 application design reference manual

[4] AN10798, DisplayPort PCB Layout Guidelines

[5] Intel Skylake Platform Design Guide, Rev. 0.7, May 2014

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