

AN11941

NTAG TagTamper products - Tamper loop design hints

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Application note
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Document information

Information	Content
Keywords	NTAG 213 TagTamper, Tamper loop, Tamper loop design, guidelines
Abstract	This document describes some guidelines which may be considered while designing a tamper loop for NXP NTAG 213 TagTamper and NTAG 424 DNA TagTamper product.



Revision

Revision history

Rev	Date	Description
1.1	20181031	NTAG 424 DNA TagTamper added
1.0	20170711	Initial version

1 General description

1.1 About this document

In this document, only the hints and notes for designing tamper loop, specific to NTAG 213 TagTamper and NTAG 424 DNA TagTamper are explained. All the antenna basics and design details are explained in AN11276 NTAG Antenna Design Guide [[Section 4](#)]. Use data sheet [[Section 4](#)] as the base document and apply wherever requires the notes mentioned here.

1.2 Abbreviations

Table 1. Abbreviations

Acronym	Description
PICC	Proximity Integrated Circuit Card
PCD	Proximity Coupling Device
DP	Detection Pin
GND	Ground Pin

2 Introduction

NTAG 213 TagTamper and NTAG 424 DNA TagTamper feature a novel tamper evidence function for identification of unauthorized access, manipulation of a product, package or system. Tampering attempts are detected and permanently stored into the chip's memory and subsequently reported to the cloud. Opened or closed status is mirrored into the tag's response (NDEF Message - URL).

NTAG 213 TagTamper and NTAG 424 DNA TagTamper ICs feature four (4) connection pads. Antenna is connected to the antenna pads of the IC (LA/LB). Tag tamper detection wire (Tamper loop) is connected the tamper pads (DP/GND). Tag tamper detection wire connection is checked at each startup.

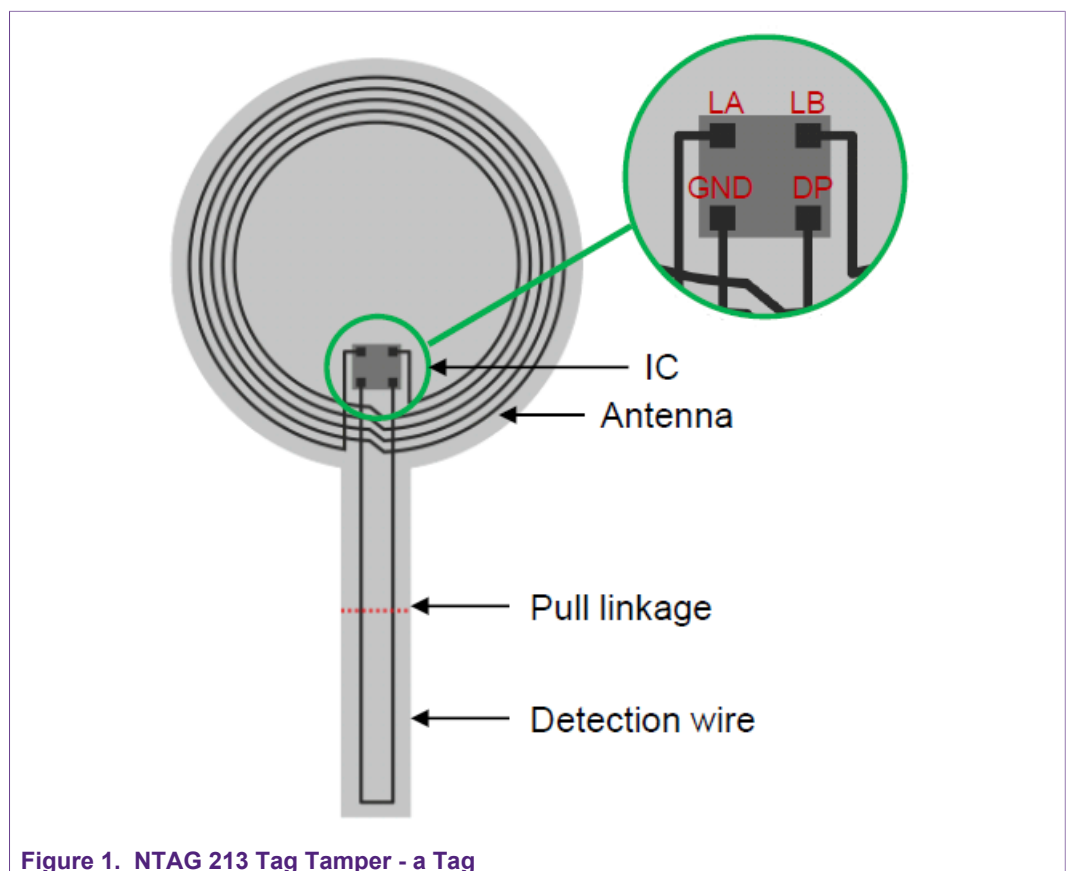


Figure 1. NTAG 213 Tag Tamper - a Tag

Current status of the wire can be read out by means of a special command. It has two (2) different tag responses based on open/close status of Tamper Loop.

3 Guidelines for designing

This chapter includes some guidelines which may be considered while designing a tamper loop. Final characterization of the design must be verified.

3.1 Requirements and conditions

Following points need to be considered when designing a Tamper Loop:

1. Requirement 1 - ON/OFF resistance shall not be exceeded. In state of CLOSED resistance shall be $R < 50 \text{ Ohm}$. In OPENED state $R > 1 \text{ MOhm}$
2. Requirement 2 - Induced voltage on Tamper Loop shall not exceed 0.5 V (peak)

3.2 Other considerations

3.2.1 Tamper loop material

Tamper loop is constructed from a conductive material. The material and the length of the loop, shall be chosen to meet requirement Requirement 1.

3.2.2 Overlapping area

Overlapping area can be calculated. This is an intersection area between the Tamper Loop conductors/wires and PCD's antenna outer track.

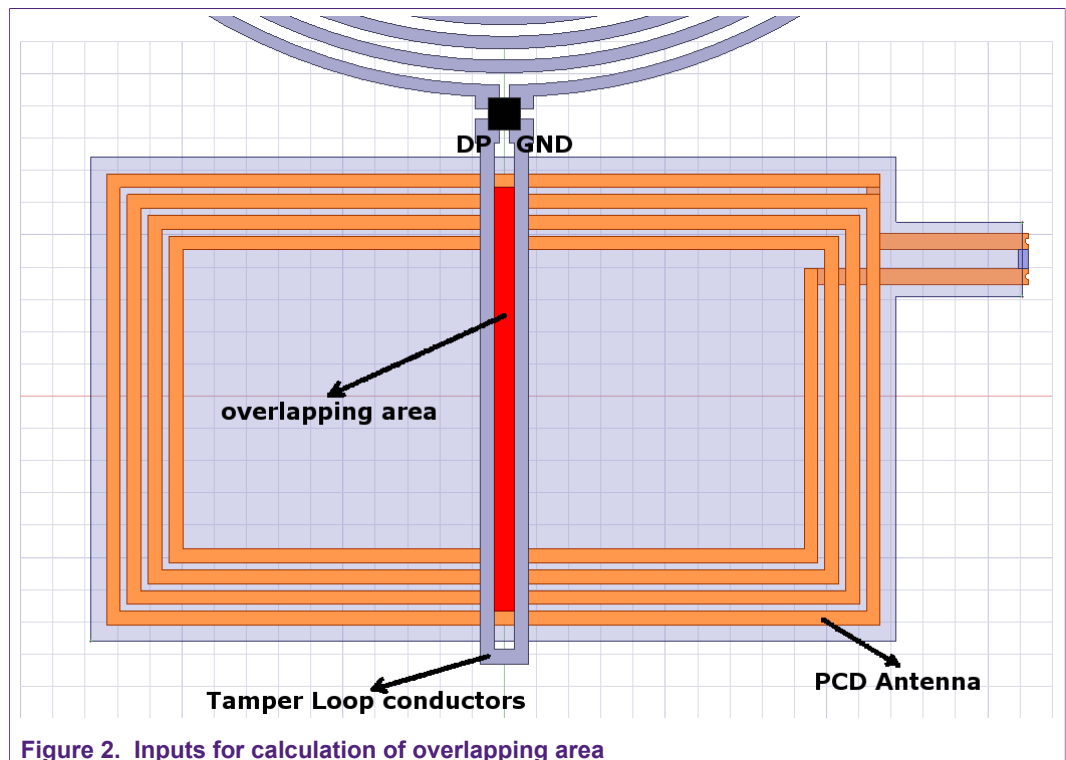


Figure 2. Inputs for calculation of overlapping area

The [Figure 3] below, shows how to calculate antenna coverage (overlapping) area between Tag's Tamper Loop wires/conductors.

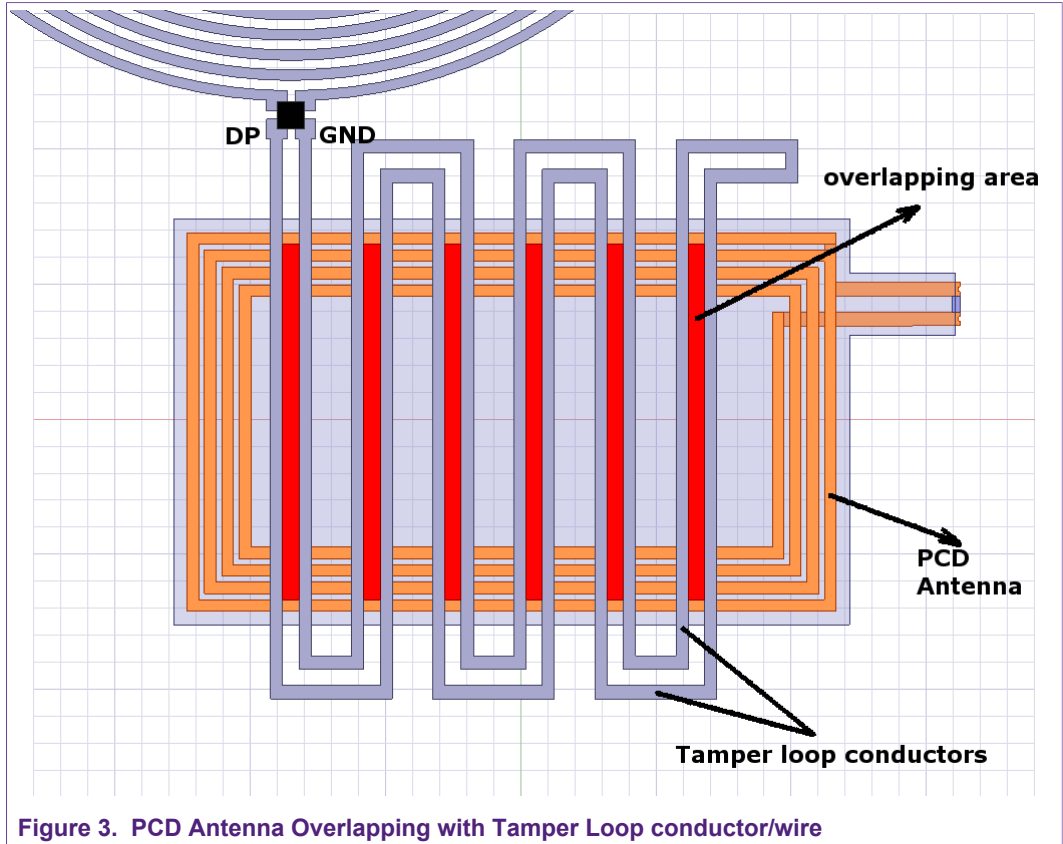


Figure 3. PCD Antenna Overlapping with Tamper Loop conductor/wire

Main target is to summarize all overlapping areas sizes. Sum of all overlapping areas shall not be larger than 2.5 cm², for PCD antenna size Class 6. See [Table 2] for other PCD antenna sizes.

3.2.3 PCD antenna sizes and mapped field strengths

In the [Table 2], there are values for PCD field strengths and applicable overlapping area which shall not be larger as stated. PCD field strengths are defined in [ISO/IEC 14443-1:2008/Amd.1:2012, 4.4 (alternating magnetic field)].

Table 2. PCD field strength

Antenna size	H _{MAX} [A/m (rms)]	Allowed overlapping area [cm ²]
Mobile devices' average/ estimated antenna size	1.5	15
Class 1	7.5	6
Class 2	8.5	5.5
Class 3	8.5	5.5
Class 4	12	3.8
Class 5	14	3.3
Class 6	18	2.5

3.2.4 Additional considerations

1. Avoid large open areas [Figure 4]
2. Avoid tamper loop circumferencing tag's antenna [Figure 5]
3. Tamper loop wires/conductors shall be positioned as close as possible [Figure 6]

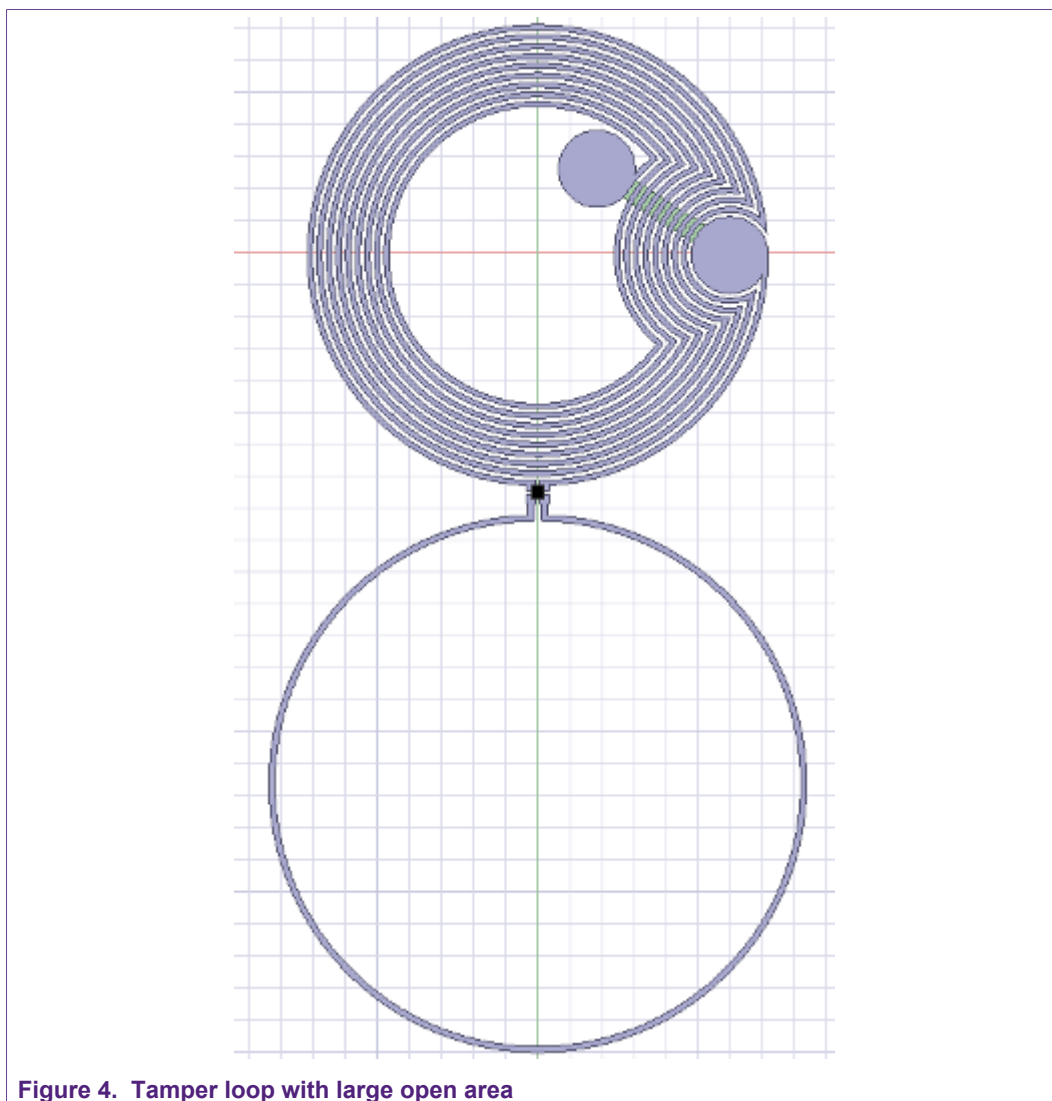


Figure 4. Tamper loop with large open area

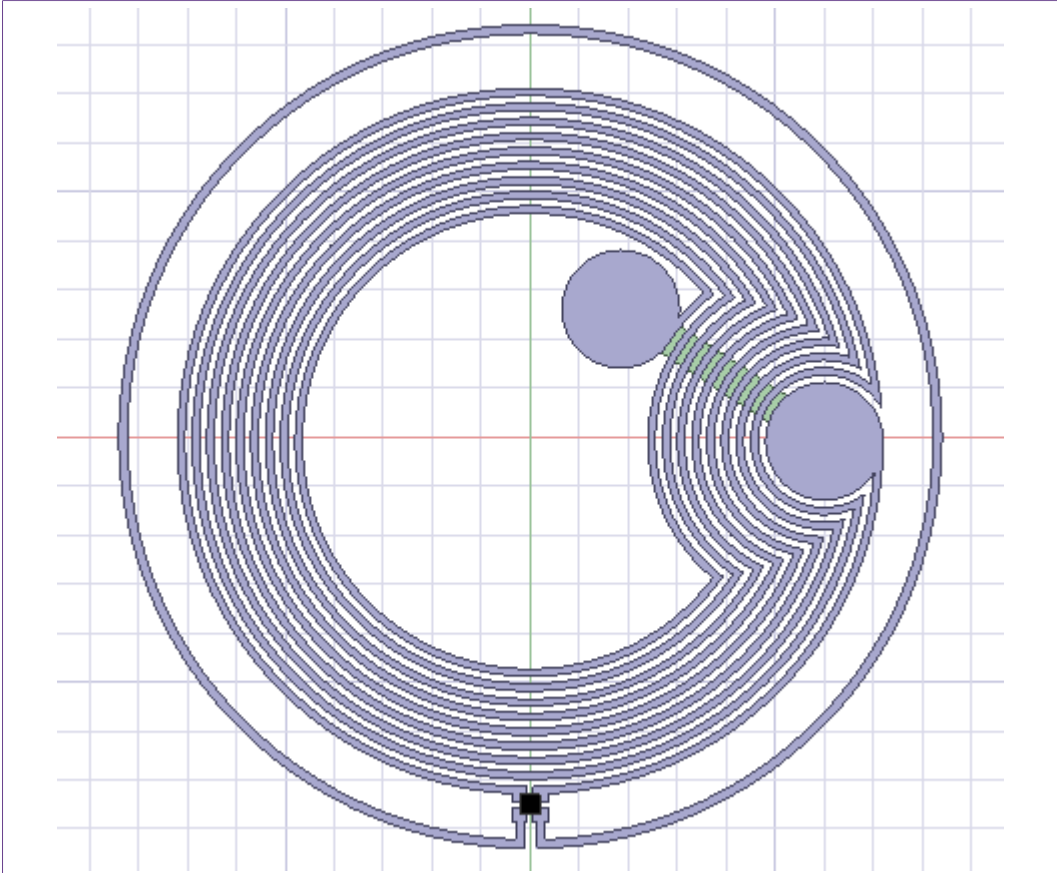


Figure 5. Tamper loop circumference

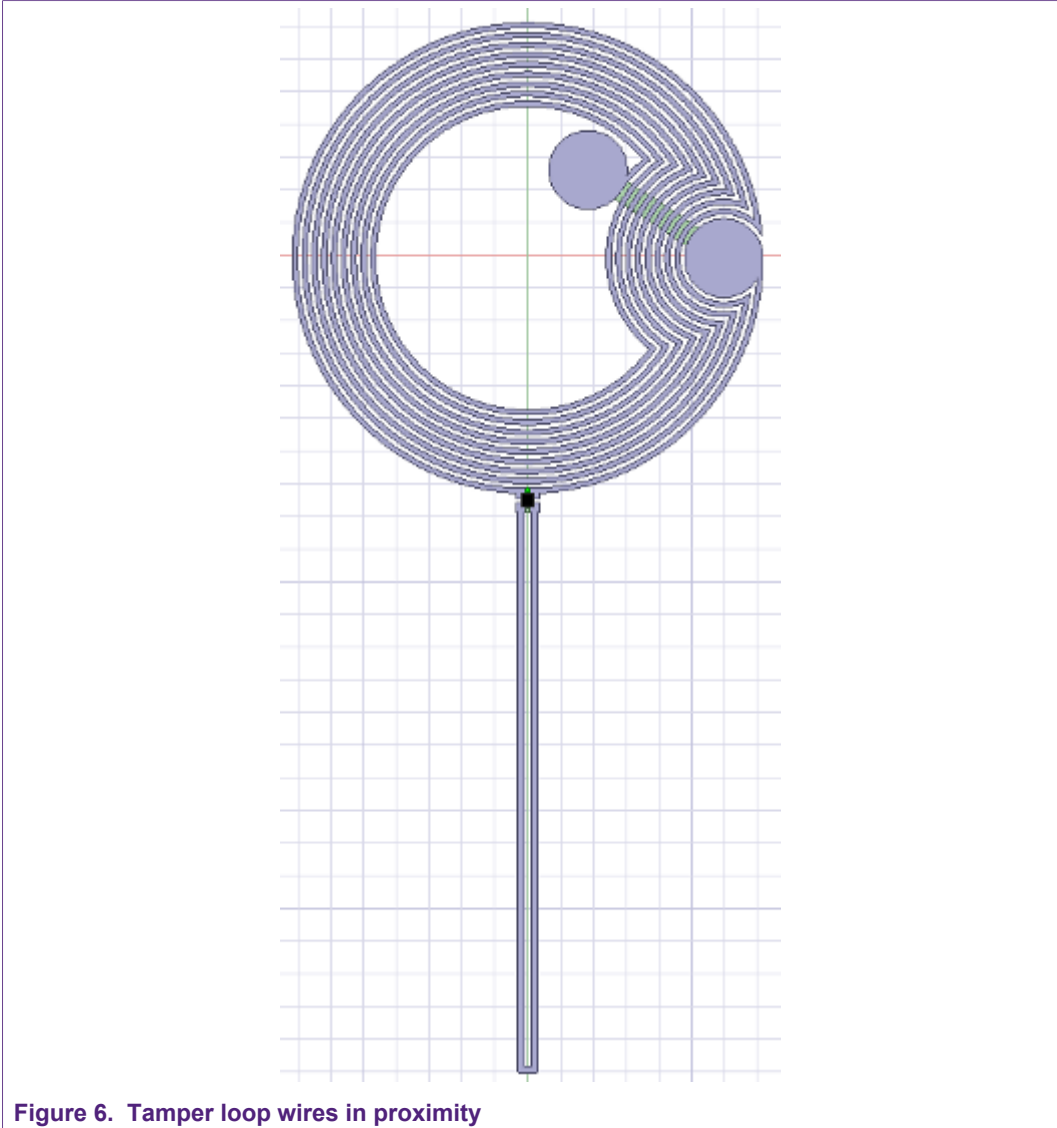


Figure 6. Tamper loop wires in proximity

4 References

- [1] **Data sheet** — NT2H1311TT NTAG 213 TT - NFC T2T Compliant IC With Tag Tamper Feature, Product data sheet, doc.nr. 3983**^[1]
- [2] **ISO/IEC 10373-6** — ISO/IEC 10373-6 standard, Identification cards — Test methods — Part 6: Proximity cards, 2013
- [3] **Application Note** — AN11276 NTAG Antenna Design Guide, Application Note, doc.nr. 2421**
- [4] **Data sheet** — NT4H2421G0, NTAG 424 DNA – Secure NFC T4T compliant IC, Product data sheet, doc.nr. 4654**

[1] ** ... document version number

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