Using a Linear Transistor Model for RF Amplifier Design

Introduction

The fundamental task of a power amplifier designer is to design the matching structures necessary to deliver power into the gate of the transistor and provide the required output power to a load. The linear model presented here is a simplified lumped-element model of the device intended for use in the design of power amplifier input and output PCB matching structures. The frequency usage of this model is for the HF and VHF operating bands.

This application note uses the MRFX1K80H (1800 W, 65 V LDMOS transistor) as an example and compares the linear model simulation results with measured circuit results.

This linear model is validated at 230 MHz and is usable at lower frequencies.

Warning: This model is linear and thus will not predict gain compression, drain efficiency, harmonics, distortion or breakdown effects of the junctions. For RF PA designers interested in nonlinear simulations, ADS and Microwave Office models are available from the NXP website.

Linear Model Components

The linear model presented here uses standard models for resistors, capacitors, inductors and a current source. Thus, such a linear model provides the advantage of being usable in any RF simulation program that has the capability of S-parameter and circuit-matching simulations.

The linear model is subdivided into sections that represent the device package, wire bond interconnects, on-chip stability network, simple gate model, device feedback capacitance, and drain power match model. Figure 1 and Table 1 show a transistor model for half of the MRFX1K80H.

C_{PKG} represents the capacitive effect of the gate and drain leads of the package. It is the same for both sides of the transistor.

L_G represents the inductive effect of the wires that connect the die to the gate and drain leads. It is the same for both sides of the transistor.

R_{STAB} and C_{STAB} are added to the die to provide low frequency device stability.

R_G represents the effective gate resistance.

The gate and drain model subsections are developed using data sheet parameter values, with simple calculations based on power and drain voltage. The linear model uses the forward transconductance and capacitance parameters from the product data sheet (see Table 2 for the MRFX1K80H; all parameters are for half of the device and assume 65 V drain voltage operation). The capacitances for this model (C_{gs}, C_{gd} and C_{ds}) are calculated using the following equations:

$$C_{gs} = C_{iss} - C_{rss} - C_{PKG}$$

$$C_{ds} = C_{oss} - C_{rss} - C_{PKG}$$

$$C_{gd} = C_{rss}$$

The g_{fs} value used in the linear model is cut in half for Class B operation and adjusted to agree with the small signal gain.

The r_{opt} optimum resistance value is calculated from the following equation, used for half device:

$$r_{opt} = \frac{V^2}{2P}$$

The r_{opt} value is adjusted for the model to provide a more accurate agreement with the measured output impedances.

The Complete Simple Linear Model

Figure 2 shows the complete four-port linear model for the MRFX1K80H. This complete model is a duplication of Figure 1 to represent the four-port MRFX1K80H device.

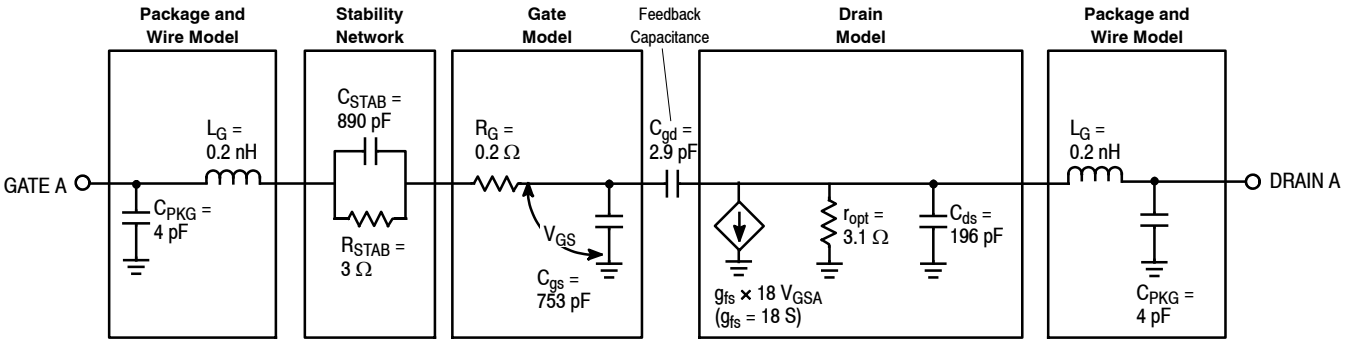

Figure 1. Linear Model for Half of the Device from the MRFX1K80H Data Sheet

Table 1. MRFX1K80H Linear Model Component Values

Package and Wire Bonds		Stability Network		Gate Model		Feedback	Drain Model		
C_{PKG}	L_G	R_{STAB}	C_{STAB}	R_G	C_{gs}	C_{gd}	g_{fs}	r_{opt}	C_{ds}
4 pF	0.2 nH	3 Ω	890 pF	0.2 Ω	753 pF	2.9 pF	18 mho	3.1 Ω	196 pF

Table 2. Capacitances and Forward Transconductance from MRFX1K80H Data Sheet

Characteristic	Symbol	Min	Typ	Max	Unit
On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 740 μAdc)	$V_{GS(th)}$	2.1	2.5	2.9	Vdc
Gate Quiescent Voltage (V_{DD} = 65 Vdc, $I_{D(A+B)}$ = 100 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.4	2.8	3.2	Vdc
Drain–Source On–Voltage (1) (V_{GS} = 10 Vdc, I_D = 2.76 Adc)	$V_{DS(on)}$	—	0.21	—	Vdc
Forward Transconductance (1) (V_{DS} = 10 Vdc, I_D = 43 Adc)	g_{fs}	—	44.7	—	S
Dynamic Characteristics (1)					
Reverse Transfer Capacitance (V_{DS} = 65 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2.9	—	pF
Output Capacitance (V_{DS} = 65 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	203	—	pF
Input Capacitance (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	760	—	pF

1. Each side of device measured separately.

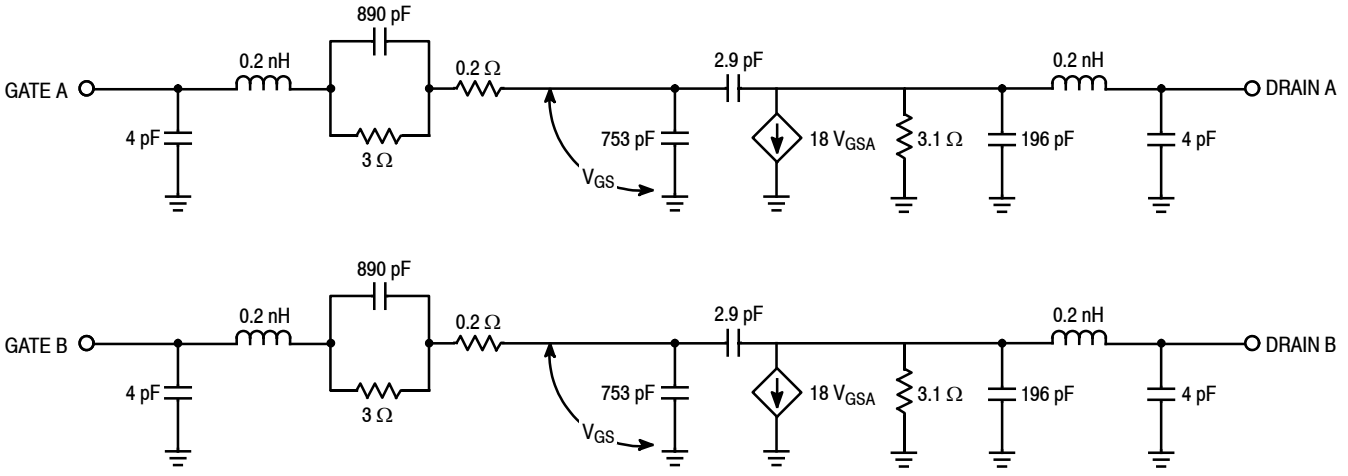

Figure 2. Simple Linear Model for the MRFX1K80H

Using the MRFX1K80H Simple Linear Model

Such a linear model can be used to design the input and output matching networks for developing an amplifier PCB. Figure 3 shows the basic block diagram from a top–level view of the power amplifier that includes the input PCB matching network, linear model and output PCB matching network. The two gate ports are connected to an input PCB matching network, and the two output ports are connected to the output PCB matching network. With the help of the linear model, the RF PA designer can determine the PCB impedance matching network to transform the linear model impedances to 50 ohms for the input and the output.

The following example uses the MRFX1K80H linear model and the MRFX1K80H 230 MHz PCB information and associated source and load impedances provided in the data sheet. The push–pull circuit shown in Figure 4 is modeled in the linear simulator using microstrip elements, capacitors, inductors, resistors, and coax cable models for input and output matching. Once information about the PCB matching structures and the linear model is entered into the linear simulator, the matching structures can be tuned to provide a good match for S11 and S22 of the combined two–port network; see Figure 3. It is recommended that the return loss be better than –20 dB to provide a good conjugate match between the device and the matching structures.

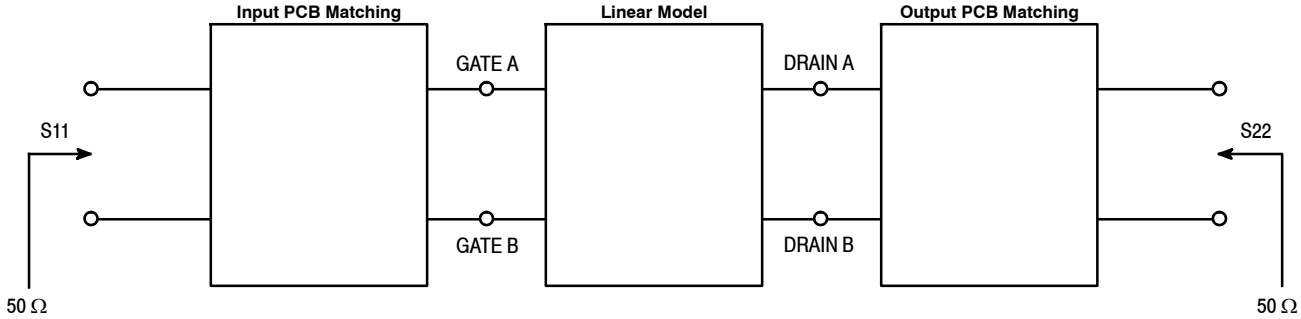

Figure 3. Computer Simulation Schematic for MRFX1K80H PCB Design

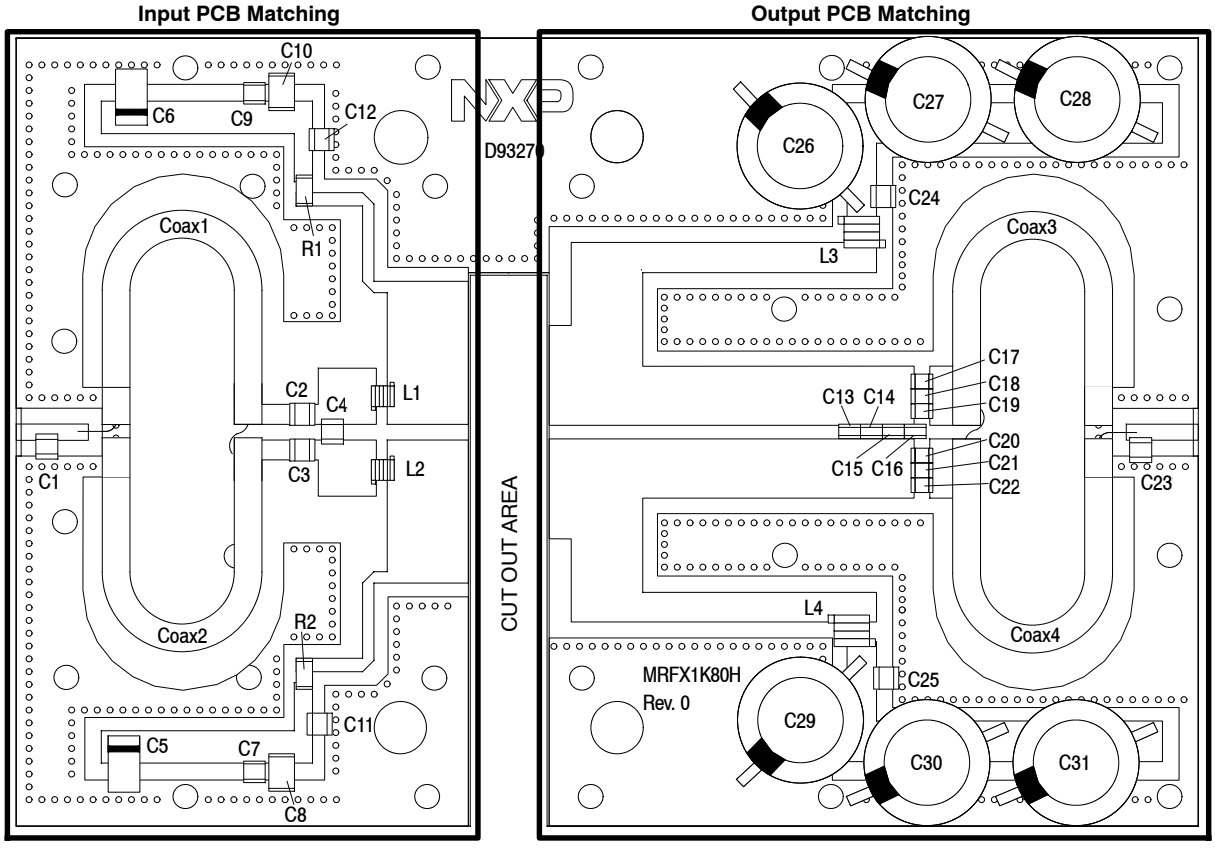

Figure 4. MRFX1K80H Push–Pull 230 MHz PCB

Figure 5 shows the simulation results for S11 and S22. Both S11 and S22 show the input return loss to be centered at 230 MHz. The S21 curve represents the small signal gain of the model. The final validation of the model is shown in Table 3 and provides a comparison of the measured and modeled impedances. These impedances are the source and load balanced impedances looking into the gate and drain PCB matching networks. This comparison shows agreement between modeled and measured balanced impedances.

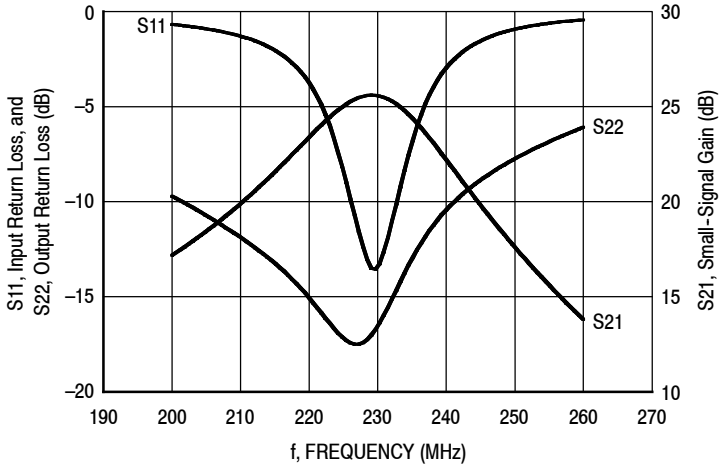

Figure 5. S–Parameter Simulation Results

Table 3. Measured versus Modeled Balanced Impedances

f MHz	Measured Impedance		Modeled Impedance	
	Z_{source} Ω	Z_{load} Ω	Z_{source} Ω	Z_{load} Ω
230	1.1 + j2.7	2.2 + j2.9	1.1 + j2.8	2.3 + j2.8

Note that the modeled S11 and S22 will not be the same as the measured S11 and S22 of the actual transistor, nor the S11 and S22 of the circuit PCB matched to the input and output of the transistor when looking from the amplifier's input and output connectors under large signal operation.

Conclusion

The fundamental task of an RF PA design engineer is to design the matching structures necessary to deliver power into the gate of the transistor and provide the required output power to a load. A linear model can be useful in the design of the PA PCB matching and can also be used in an inexpensive RF linear simulation tool. An example was presented for the MRFX1K80H linear model using the 230 MHz data sheet push–pull amplifier; simulation and measurement impedance results were compared and showed good alignment. As a reminder, this model is linear and thus will not predict gain compression, drain efficiency, harmonics, distortion or breakdown effects of the junctions. For RF PA designers interested in nonlinear simulations, ADS and Microwave Office models are available from the NXP website.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2018	• Initial release of application note

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