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NTAG 5 link - I²C master mode

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Application note
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Document information

Information	Content
Keywords	NTAG 5 I2C master mode, NTP5332, NTA5332, sensor, memory, I2C slaves
Abstract	NTP5332 and NTA5332 can act as a transparent I2C channel. NFC enabled devices can exchange data with I2C slaves without the help of an μ C.



Revision history

Rev	Date	Description
v.1.0	20200109	First official released version

1 Abbreviations

Table 1. Abbreviations

Acronym	Description
I ² C	Inter-IC communication
IC	Integrated Circuit
MCU	Microcontroller unit
NFC	Near Field Communication
POR	Power On Reset
VCD	Vicinity Coupling Device
VICC	Vicinity Integrated Circuit Card

2 Introduction

This document describes NTAG 5 link (NTP5332) and NTAG 5 boost (NTA5332) [[Data sheet](#)] capabilities of I²C master mode.

This mode enables a transparent I²C master channel between NFC and I²C interfaces. NTAG 5 can **power** [[Application note](#)] **and** act as **I²C Master** for any I²C slave device (e.g. sensor, external memory, LCD etc.) without a need of an MCU.

2.1 Potential applications

“Sensor IC”:

- Draw power from the NFC reader to supply sensors
- Configure sensors with an NFC enabled device
- Read out sensor information without an MCU
- Send the sensor data to the cloud “Memory tag”

“Memory IC”:

- Extend memory size to your needs
- Draw power from the NFC reader to supply external I²C memory
- Write Configuration data to the memory during production
- Read trace logs for maintenance or complaint handling

3 I²C Master functionality

I²C Master communication is initiated by RF interface. RF can initiate a READ or WRITE transaction to external I²C slaves. SRAM is used as intermediate storage of data (V_{CC} supply on NTAG 5 needed).

Session registers reflect the status of I²C Master transaction. Therefore an RF reader has to poll for the status bits related to I²C Master to know the status of the current I²C transaction.

Hints:

- Energy harvesting functionality can be used as power source [[Application note](#)].
- Maximum of 256 bytes/transactions can be sent/read at once.

Preconditions:

1. NTAG 5 must be the only I²C master acting device on the I²C-bus
2. NTAG 5 must be V_{CC} powered
3. USE_CASE_CONF in CONFIG_1 must be set to 01b (I²C master)
4. SRAM needs to be enabled.

3.1 I²C Master relevant registers

Table 2. Configuration registers - for I²C Master

NFC	I ² C	Byte 0	Byte 1	Byte 2	Byte 3	Description
ACh	10ACh	I2C_M_S_ADD_REG	I2C_M_LEN_REG	RFU	RFU	I ² C Master Configuration
ADh	10ADh	I2C_M_STATUS_REG	RFU	RFU	RFU	I ² C status Register

Below values have to be written in configuration memory to take effect after POR or Soft Reset.

Table 3. Configuration registers

NFC	I ² C	Byte 0	Byte 1	Byte 2	Byte 3
3Eh	103Eh	I2C_SLAVE_ADDR	I2C_SLAVE_CONFIG	I2C_MASTER_LOW	I2C_MASTER_HIGH

3.2 NFC command set for I²C Master

Table 4. NFC command set for I²C Master

Command Code	ISO/IEC 15693 command class.	NFC Forum T5T	Command name
D4h	Custom	Not defined	WRITE I2C
D5h	Custom	Not defined	READ I2C

READ I²C and WRITE I²C commands use as per I²C specification the 7-bit addressing. R/W bit is set automatically by NTAG 5.

3.3 I²C Baud rate configuration

I2C_MASTER_SCL_LOW and I2C_MASTER_SCL_HIGH are the coefficients and can be calculated by below formula.

$$I2C_Master_SCL_HIGH = \frac{Duty_Cycle \times 6,78MHz}{I2C_Frequency} - 5 \tag{1}$$

$$I2C_Master_SCL_LOW = \frac{(1 - Duty_Cycle) \times 6,78MHz}{I2C_Frequency} \tag{2}$$

Example:

400 kHz of I²C frequency with duty cycle of 50 %.

- Duty_Cycle = 0.53
- I2C_Frequency = 400 kHz
- I2C_MASTER_SCL_HIGH = (0.53 * 6.78 * 10⁶ / 400 * 10³) - 5
- I2C_MASTER_SCL_HIGH = 9 - 5 = 4
- I2C_MASTER_SCL_LOW = 0.53 * 6.78 * 10⁶ / 400 * 10³
- I2C_MASTER_SCL_LOW = 7

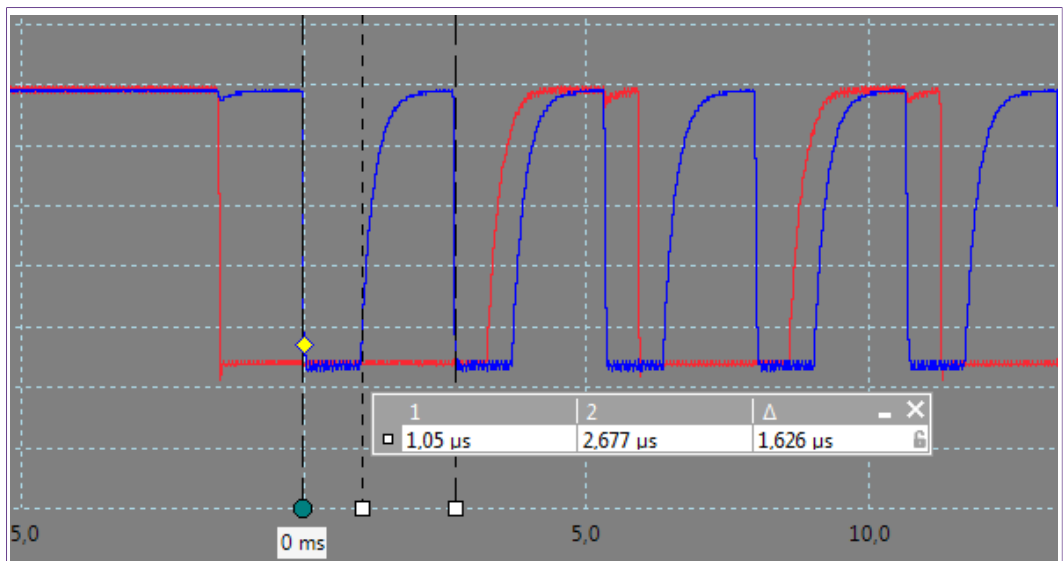


Figure 1. Duty cycle from EXAMPLE (400 kHz)

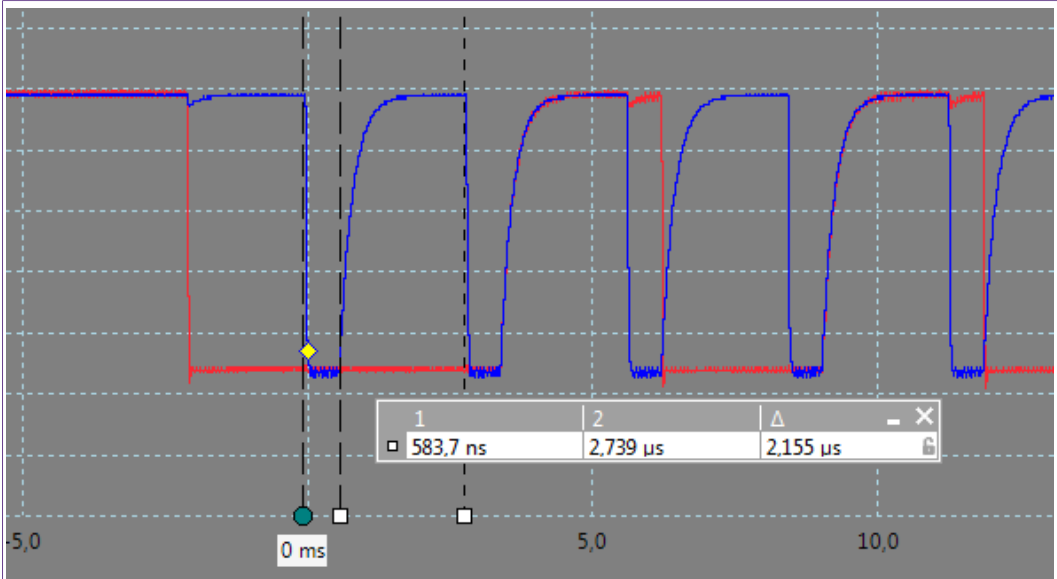


Figure 2. Duty cycle example 2

4 Implementation hints

4.1 I²C Repeated START communication

To shorten or to speed up the I²C communication, STOP condition can be left out for some I²C devices. It is often used where there is a need to first address the device and then read back values from the same device right away.

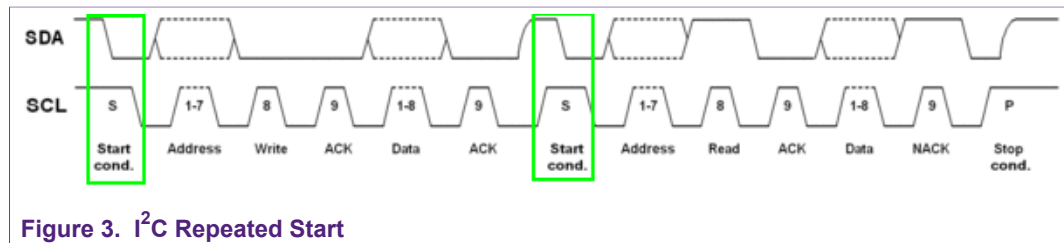


Figure 3. I²C Repeated Start

I²C Repeated START can be generated by I²C Master, when I²C_M_RS_EN = 1b.

4.2 I²C Master Data Length

How much data was sent over I²C in the last transaction (read or write), is reflected in I2C_M_LEN_REG byte.

4.3 Watch dog timer

This status bit reflects if WDT expired in the last transaction. This bit resets automatically, when new transaction is triggered. Watchdog Timer unlocks I²C, if NTAG is holding SDA down (both Master and Slave modes).

If WDT_EN = 1b (0b disables WDT):

- WDT Start:
 - WDT start at every memory access is initiated.
- WDT Stop:
 - WDT expires
 - I²C_IF_LOCKED = 0
 - I2C Reset.

WDT is not set or reset for register access.

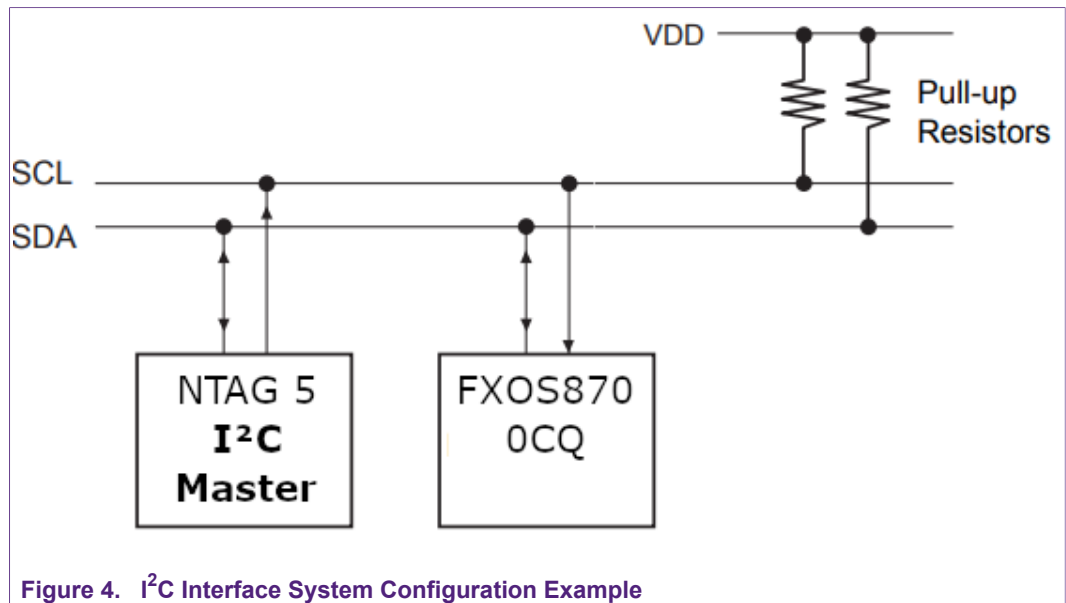
5 Example application

For the reference application with source code refer to [\[Application Note\]](#).

In following example application, NTAG 5 is configured as the I²C Master. NTAG 5 can also provide RF harvested energy (Energy harvesting) [\[Application Note\]](#). Configured as I²C Master, NTAG 5 link provides Clock (SCL) to the I²C-bus.

Following devices are used:

Device	Role	Description	I ² C command showcase	I ² C address	Description
NTAG 5	I ² C Master	In an I ² C master mode	READ/WRITE	n/a	[Datasheet]
NXP FXOS8700CQ	I ² C Slave	6-axis sensor with integrated linear accelerometer and magnetometer	READ	0x1E (7-bit address)	[Datasheet]



5.1 NTAG 5 configuration

Config I²C Master functionality can be configured from RF or I²C side.

Note: When I²C master is activated, access from I²C perspective is not possible anymore.

Desired behavior in following example:

1. NTAG 5 configured in I²C master mode
2. NTAG 5 Energy Harvesting enabled (Output voltage: 2.4 V, 0.3 A)
3. I²C Baud speed: 400 kHz (as calculated in [\[Section 3.3\]](#))

5.2 FXOS8700CQ configuration

1. Sensor's standby mode needs to be configured
VCD → VICC: 02 D4 04 1F 01 2A 00
2. Change to the hybrid mode so Accelerometer and Magnetometer are both active at the same time
VCD → VICC: 02 D4 04 1F 01 5B 1F
3. Configure Control register
VCD → VICC: 02 D4 04 1F 01 5C 20
4. Enters sensors active state / enable sensor
VCD → VICC: 02 D4 04 1F 01 2A 0D

5.3 Reading data - 6 axis sensor

Following procedure is taken:

1. Write I²C address + memory/register address with most significant bit set to 1b
2. Read byte by sending I²C address + num. bytes with MSb set to 0b
3. Data read from I²C slave is put to SRAM of NTAG. Read data from SRAM of NTAG (7 bytes in our example - length of answer is known)
4. (optional) Check proper I²C operation, I²C master status register 0xAD may be checked for debugging

Table 5. Example: Enable Gyroscope - RF Command: VCD to VICC

Flags	Command code	IC manuf. code	I ² C param	Data Length N	Data (Byte 1)	Data (Byte 2)	CRC 0	CRC 1
02	D4	04	1E	01	2A	0D	76	B1

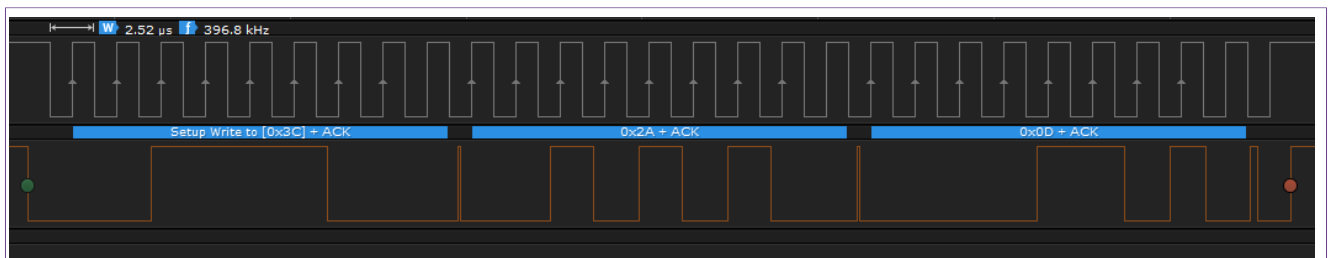


Figure 5. Signal generated by NTAG 5 on I²C-bus: Enable Gyroscope command sent to I²C Slave (FXOS8700CQ, address 1Eh) at 400 kHz

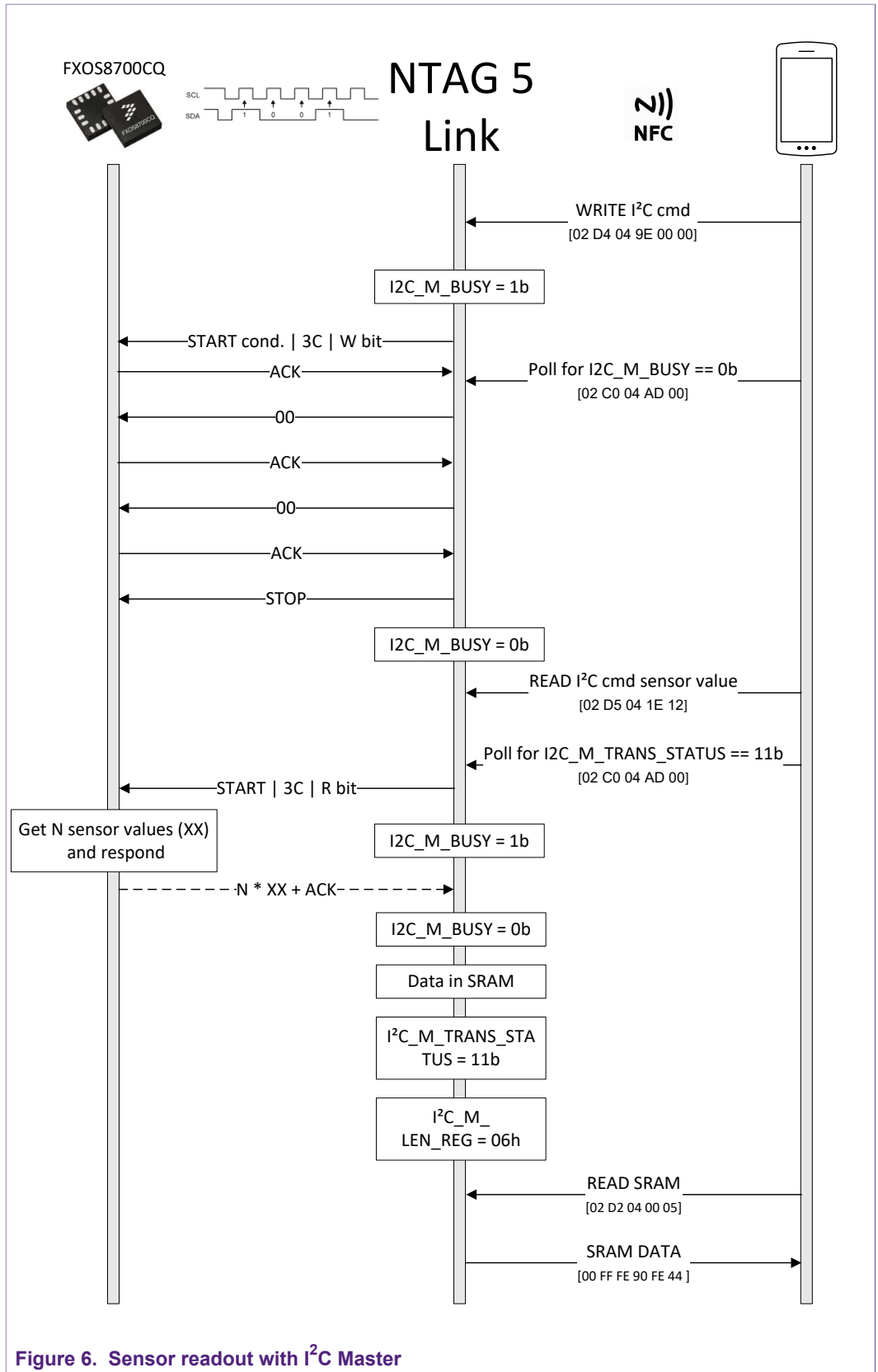


Figure 6. Sensor readout with I²C Master

6 References

- [1] NTP53x2 - NTAG 5 link, NFC Forum-compliant I²C bridge, doc.no. 5476xx
<https://www.nxp.com/docs/en/data-sheet/NTP53x2.pdf>
- [2] AN11201 - NTAG 5 How to use energy harvesting, doc.no. 5304xx
<https://www.nxp.com/docs/en/application-note/AN11201.pdf>
- [3] RM00221 - NTAG 5 Android Application development, doc.no. 5318xx
<https://www.nxp.com/docs/en/reference-manual/RM00221.pdf>

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