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MC33771C and MC33772C based system timing optimization

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Document information

Information	Content
Keywords	MC33771C, MC33772C, MC3377xC, timing, optimization
Abstract	The MC33771C and MC33772C find their natural application in a battery management system (BMS) performing safety-related functions up to ASIL D. The document explains how to achieve the fault detection time interval (FDTI) in a system with a high count of cells.

Revision history

Rev	Date	Description
v.4	20230418	Updated security status from "Company confidential" to "Public".
v.3	20210329	• Table 2 and Table 3 • Table 4 • Figure 3 and Figure 4 • Figure 5 and Figure 6 • Figure 7 • Figure 8 • Figure 9 • Figure 10 • Figure 11, Figure 13 and Figure 14 • Figure 17 • Table 5
v.2	20201028	addition of MC33772C
v.1	20200323	initial version

1 Introduction

MC33771C and MC33772C are mutually compatible, accurate remote sensors to handle up to, respectively, 14 cells or 6 cells. When a certain topic applies to both MC33771C and MC33772C, the name MC3377xC is used as shorthand to denote both ICs. The MC3377xC finds its natural application in a battery management system (BMS) performing safety-related functions up to ASIL D.

Meeting the fault detection time interval (FDTI) requirement is crucial. FDTI is the portion of the fault tolerant time interval (FTTI) considering fault detection but not fault reaction.

Following questions arise:

- How to schedule safety mechanisms (SM) in all nodes of the network to meet the FDTI?
- To which extent diagnostics execution limits the sample rate of the input channels?
- How does the MC3377xC internal digital filter settings affect the diagnostic time?
- How do the external anti-aliasing filter components influence the diagnostic time?
- To speed up the execution of safety mechanisms, which parts may be parallelized?

Such questions find answer in the present document.

To be able to adapt the information to a specific use case, the reader may request NXP a workbook [5] calculating system timing after configuring input parameters.

2 Safety mechanisms selection

The MC3377xC supports several system safety goals explained in documents [3] and [8] and listed in Table 1, where the ASIL and the FTTI given here are example values. The real MC3377xC ASIL capability is even better, as shown in references [4] and [9].

Table 1. System safety goals assignable to the MC3377xC

Label	Assumed safety goal	ASIL	FTTI
OV	The MC3377xC shall prevent the occurrence of an undetected overvoltage event on the Li-ion cells of the battery.	D	< 3 s
UV	The MC3377xC shall prevent the occurrence of an undetected undervoltage event on the Li-ion cells of the battery.	C	< 3 s
OT	The MC3377xC shall prevent the occurrence of an undetected overtemperature event on the Li-ion cells of the battery.	C	< 10 s
UT	The MC3377xC shall prevent the occurrence of an undetected undertemperature event on the Li-ion cells of the battery.	A	< 10 s
OC	The MC3377xC shall prevent the occurrence of an undetected overcurrent event in the battery.	C	< 1 s

The number of used SM impacts the system timing, which may be evaluated by using a tool, reference [5].

Shortening the list of used SM improves the system timing but may impact the metrics resulting from the safety analysis. It is always advice to follow all recommendations in documents [3], [4], [7], [8] and [9].

Then, the 'Used' column of 'Safety mech. & other activities' worksheet of document [5] may be configured, see Table 2.

Table 2. Partial view of 'Safety mech. & other activities' worksheet (timing is for MC33771C)

Item	Safety mechanism or other activity	Covered function	Used	Diag mode	t_IC [µs]	SG	Group	Constrained balance
M00	normal measurements	all measurements	yes	no	12823	n/a	M	yes
M01	application routines	SOC, SOH, others	yes	no	10000	n/a	G5	no
SM01	OV and UV functional verification	cell voltage measurement	no	yes	5262	OV/UV	G4	yes
SM02	CTx open detect and open detect functional verification	cell voltage measurement (EXT)	yes	yes	10047	OV/UV	G2	yes
SM03	cell voltage channel functional verification	cell voltage measurement	yes	yes	5817	OV/UV	G3	no
SM04	CTx cell terminal leakage monitor	cell voltage measurement (EXT)	yes	yes	11357	OV/UV	L0	yes
SM05	GPIOx OT/UT functional verification	temperature measurement	yes	yes	1471	OT/UT	G1	no
SM06	GPIOx open terminal diagnostics	temperature measurement (EXT)	yes	yes	408	OT/UT	G1	no
SM07	ADC1-a and ADC1-b functional verification	all measurements	yes	no	500	OV/UV/ OT/UT	G1	no
SM08	oscillator frequency monitor	all measurements	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM09	VCOM short/UV protection detection	power supply	yes	no	100	OV/UV/ OT/UT/OC	G1	no

Table 2. Partial view of 'Safety mech. & other activities' worksheet (timing is for MC33771C)*...continued*

Item	Safety mechanism or other activity	Covered function	Used	Diag mode	t_IC [µs]	SG	Group	Constrained balance
SM10	VANA short/UV protection detection	power supply	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM11	onboard temperature protection mode	all measurements	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM12	loss of ground detection	all measurements	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM13	fuses ECC	all measurements	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM14	FAULT pin heart beat feature (FAULT pin daisy chain operation)	communication	no	no	651	n/a	G1	no
SM15	VANA OV detection	power supply	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM16	exit diagnostic mode safety timer	all measurements	yes	yes	62	OV/UV/ OT/UT/OC	G1	no
SM17	register address identification frame	communication	yes	no	62	OV/UV/ OT/UT/OC	G1	no
SM18	check of register content	all measurements	yes	no	408	OV/UV/ OT/UT/OC	G1	no
SM19	eight-bit CRC with non-zero seed	communication	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM20	unique identifiable message start and stop bits	communication	no	no	0	n/a	G1	no
SM21	loss of communication fault	communication	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM22	n/a	n/a	no	n/a	0	n/a	n/a	no
SM23	VCOM OV detection	power supply	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM24	VPWR OV detection	power supply	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM25	VPWR UV detection	power supply	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM26	missing or wrong response detection	communication	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM27	main controller access to EEPROM data	all measurements	yes	no	1974	OV/UV/ OT/UT/OC	L0	no
SM28	FAULT pin level (FAULT pin daisy chain operation)	communication	no	no	1	n/a	G1	no
SM29	OV/UV internal detection	cell voltage measurement (EXT)	no	no	581	OV/UV	G1	no(*)
SM30	read data ready bit	all measurements	yes	no	31	OV/UV/ OT/UT/OC	G1	no

Table 2. Partial view of 'Safety mech. & other activities' worksheet (timing is for MC33771C)*...continued*

Item	Safety mechanism or other activity	Covered function	Used	Diag mode	t_IC [µs]	SG	Group	Constrained balance
SM31	fuses bit error flag	all measurements	yes	no	62	OV/UV/ OT/UT/OC	L0	no
SM32	use interleaved cyclic and on-demand conversion	all measurements	yes	no	674	OV/UV/ OT/UT	L0	no
SM33	plausibility check of redundant ANx in the pack controller	temperature measurement	yes	no	500	OT/UT	G1	no
SM34	OV/UV detection in the pack controller	cell voltage measurement (EXT)	yes	no	2647	OV/UV	G4	yes
SM35	message counter	communication	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM36	diagnostic of open between shunt and PGA	current measurement (EXT)	yes	yes	216	OC	G1	no
SM37	diagnostic of measurement chain offset with shorted PGA inputs	current measurement	yes	yes	1244	OC	G1	no
SM38	diagnostic of measurement chain with min PGA gain	current measurement	yes	yes	1244	OC	G1	no
SM39	use of AN5 and AN6 as current measurement input	current measurement (EXT)	yes	yes	2083	OC	G1	no
SM40	cell balance open load detection	cell balancing	yes	yes	1787	OV/UV	G4	yes
SM41	cell balance shorted resistor detection	cell balancing	no	no	638	n/a	G1	no
SM42	I2C_ERR_FLT detection	all measurements	yes	no	162	OV/UV/ OT/UT/OC	G1	no
SM43	n/a	n/a	no	n/a	0	n/a	n/a	no
SM44	cell voltage plausibility test at system level	cell voltage measurement (EXT)	yes	no	1500	OV/UV	G1	no(*)
SM45	VPWR comparison to sum of cell voltages	cell voltage measurement (EXT)	yes	no	1000	OV/UV	G1	no(*)
SM46	VCP UV detection	power supply	no	no	977	OV/UV/ OT/UT	G1	no

Safety mechanisms detection times, t_IC [µs], given in Table 2 correspond to a specific configuration of cell voltage and current filters. Tool [5] updates diagnostic times based on the configured parameters. Non-intrusive SMx (with x = 08, 09, 10, 11, 12, 13, 15, 21, 23, 24, 25, 26, 35) have by default t_IC = 100 µs. For M01, t_IC = 10000 µs has been set as default. The user may change it to a more convenient value.

Item M00 consist of both normal measurements execution and FAULTx_STATUS registers reading. Item M00 has constrained balance = yes, because measuring while balancing is forbidden. In both Table 2 and Table 3, safety mechanisms belonging to group G1 and having constrained balance = no(*) consist of calculations using input data obtained by item M00. Therefore, such safety mechanisms do not need any further suspension of the cell balancing.

Table 3. Partial view of 'Safety mech. & other activities' worksheet (timing is for MC33772C)

Item	Safety mechanism or other activity	Covered function	Used	Diag mode	t_IC [µs]	SG	Group	Constrained balance
M00	normal measurements	all measurements	yes	no	12823	n/a	M	yes
M01	application routines	SOC, SOH, others	yes	no	10000	n/a	G5	no
SM01	OV and UV functional verification	cell voltage measurement	no	yes	5262	OV/UV	G4	yes
SM02	CTx open detect and open detect functional verification	cell voltage measurement (EXT)	yes	yes	9801	OV/UV	G2	yes
SM03	cell voltage channel functional verification	cell voltage measurement	yes	yes	5077	OV/UV	G3	no
SM04	CTx cell terminal leakage monitor	cell voltage measurement (EXT)	yes	yes	10123	OV/UV	L0	yes
SM05	GPIOx OT/UT functional verification	temperature measurement	yes	yes	1471	OT/UT	G1	no
SM06	GPIOx open terminal diagnostics	temperature measurement (EXT)	yes	yes	408	OT/UT	G1	no
SM07	ADC1-a and ADC1-b functional verification	all measurements	yes	no	500	OV/UV/ OT/UT	G1	no
SM08	oscillator frequency monitor	all measurements	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM09	VCOM short/UV protection detection	power supply	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM10	VANA short/UV protection detection	power supply	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM11	onboard temperature protection mode	all measurements	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM12	loss of ground detection	all measurements	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM13	fuses ECC	all measurements	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM14	FAULT pin heart beat feature (FAULT pin daisy chain operation)	communication	no	no	651	n/a	G1	no
SM15	VANA OV detection	power supply	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM16	exit diagnostic mode safety timer	all measurements	yes	yes	62	OV/UV/ OT/UT/OC	G1	no
SM17	register address identification frame	communication	yes	no	62	OV/UV/ OT/UT/OC	G1	no
SM18	check of register content	all measurements	yes	no	408	OV/UV/ OT/UT/OC	G1	no
SM19	eight-bit CRC with non-zero seed	communication	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM20	unique identifiable message start and stop bits	communication	no	no	0	n/a	G1	no

Table 3. Partial view of 'Safety mech. & other activities' worksheet (timing is for MC33772C)*...continued*

Item	Safety mechanism or other activity	Covered function	Used	Diag mode	t_IC [µs]	SG	Group	Constrained balance
SM21	loss of communication fault	communication	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM22	n/a	n/a	no	n/a	0	n/a	n/a	no
SM23	VCOM OV detection	power supply	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM24	VPWR OV detection	power supply	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM25	VPWR UV detection	power supply	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM26	missing or wrong response detection	communication	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM27	main controller access to EEPROM data	all measurements	yes	no	1974	OV/UV/ OT/UT/OC	L0	no
SM28	FAULT pin level (FAULT pin daisy chain operation)	communication	no	no	1	n/a	G1	no
SM29	OV/UV internal detection	cell voltage measurement (EXT)	no	no	581	OV/UV	G1	no(*)
SM30	read data ready bit	all measurements	yes	no	31	OV/UV/ OT/UT/OC	G1	no
SM31	fuses bit error flag	all measurements	yes	no	62	OV/UV/ OT/UT/OC	L0	no
SM32	use interleaved cyclic and on-demand conversion	all measurements	no	no	674	OV/UV/ OT/UT	L0	no
SM33	plausibility check of redundant ANx in the pack controller	temperature measurement	yes	no	500	OT/UT	G1	no
SM34	OV/UV detection in the pack controller	cell voltage measurement (EXT)	yes	no	1907	OV/UV	G4	yes
SM35	message counter	communication	yes	no	100	OV/UV/ OT/UT/OC	G1	no
SM36	diagnostic of open between shunt and PGA	current measurement (EXT)	yes	yes	216	OC	G1	no
SM37	diagnostic of measurement chain offset with shorted PGA inputs	current measurement	yes	yes	1244	OC	G1	no
SM38	diagnostic of measurement chain with min PGA gain	current measurement	yes	yes	1244	OC	G1	no
SM39	use of AN5 and AN6 as current measurement input	current measurement (EXT)	yes	yes	2083	OC	G1	no
SM40	cell balance open load detection	cell balancing	yes	yes	1787	OV/UV	G4	yes
SM41	cell balance shorted resistor detection	cell balancing	no	no	638	n/a	G1	no

Table 3. Partial view of 'Safety mech. & other activities' worksheet (timing is for MC33772C)*...continued*

Item	Safety mechanism or other activity	Covered function	Used	Diag mode	t_IC [µs]	SG	Group	Constrained balance
SM42	I2C_ERR_FLT detection	all measurements	yes	no	162	OV/UV/ OT/UT/OC	G1	no
SM43	n/a	n/a	no	n/a	0	n/a	n/a	no
SM44	cell voltage plausibility test at system level	cell voltage measurement (EXT)	yes	no	1500	OV/UV	G1	no(*)
SM45	VPWR comparison to sum of cell voltages	cell voltage measurement (EXT)	yes	no	1000	OV/UV	G1	no(*)
SM46	VCP UV detection	power supply	yes	no	977	OV/UV/ OT/UT/OC	G1	no

3 Safety mechanisms execution strategies

Table 4 shows a possible grouping of safety mechanisms to handle them homogeneously. It considers the following aspects, where the first two are the most important:

1. Cell balancing constrained (yes/no). If yes, the cell balancing is forced to be either active or inactive; if no, the cell balancing may be arbitrarily active or inactive
2. Make execution times of groups as balanced as possible, an important property if using one of the strategies 2, 4 and 6 explained in Section 3.2, Section 3.4, and Section 3.6
3. Diagnostic mode activation (yes/no). If yes, it means diagnostics work only in diagnostic mode; if no, it means they work both in normal and diagnostic mode
4. Safety goals covered by safety mechanisms under consideration

Table 4. SM grouping

Group	Safety goals	Diagnostic mode activation	It includes	Cell balancing constrained
M	all	X[1]	V, T, I measurements[2] & FAULTx_STATUS analysis (x = 1, 2, 3) for all nodes of the daisy chain	yes
G1	OV/UV/OT/UT/OC	no	SM08, SM09, SM10, SM11, SM12, SM13, SM15, SM17, SM18, SM19, SM21, SM23, SM24, SM25, SM26, SM30, SM35, SM42	no
	OV/UV/OT/UT		SM07	
	OV/UV		SM29(opt), SM44, SM45	
	OT/UT		SM33	
		yes	SM05, SM06	
	OC		SM36, SM37, SM38, SM39	
	OV/UV/OT/UT/OC		SM16	
G2	OV/UV	yes	SM02 subprocedures	yes
G3	OV/UV	yes	SM03	no
G4	OV/UV	yes	SM01(opt), SM40	yes
		no	SM34	
G5	all	X[1]	application SW	no

[1] X = don't care
[2] I measurement includes coulomb counter.

Two different instances of G2 are needed, called G2a and G2b. These groups correspond to two separated calls to the same function, once to check the odd-numbered lines, the other time to check the even-numbered lines, as explained in documents [3] and [8]. To explain the parallelization of some BMS operations, some communication features are briefly recalled. The pack controller (PC) is the master node of the network. It sends write and read requests to a daisy chain of MC3377xC devices, which are the slave nodes. Write requests may be either global (directed to all slaves) or individual (directed to a single slave). In contrast, read requests are always individual. Read requests cause either single or multiple responses, while write requests do not cause any response. Thanks to the global command feature, it is possible to perform multiple operations in parallel. In TPL communication mode, it is possible to read multiple registers having adjacent addresses by using a single read request. The addressed slave responds with a burst of messages, each carrying the content of one of the requested adjacent addresses. The parallel operation may be applied to the execution of some procedural steps in an SM. For example, it is possible to measure simultaneously all nodes by sending a global write command and waiting only once for all the measurements to complete, rather than doing a sequence of measurements. This way, it is possible to save time. Likewise, waiting times necessary to let voltage signals settling after closing or opening diagnostic switches may be parallelized. In contrast, read commands need replication: the PC must address one node at the time to get the needed results. The CPU time is hard predicting, since it depends on too many factors, including HW features, real-time operating system implementation, compiler efficiency, and even programming style. Therefore, the analysis does not consider CPU time except for the specific example of illustrating SM02 parallelization. For each step in Figure 1, the question if it may be parallelized is asked. If the answer is yes, it means that there is no need to replicate the step by the number of nodes. If the answer is no, it means that the user must replicate the step N_{clust} times. N_{clust} is the number of clusters (node and cluster are used as synonyms throughout the document). For example, the write commands which are needed to close/open diagnostic switches or to start a sequence of ADC conversions may be global, they do not need replication; in those cases, the multi cluster TX time and the single cluster TX time are equal.

			SINGLE CLUSTER						MULTI CLUSTER					
Step	SM02 procedure	May be parallelized?	measurement time us	waiting time us	RX time us	TX time us	calculation time us	IC time us	measurement time us	waiting time us	RX time us	TX time us	calculation time us	IC time us
	Procedure SM02(Odd_Not_Even) // Odd_Not_Even, a Boolean parameter to close diagnostic switches		0		0	0	0	0	0	0	0	0	0	0
1	Write SYS_CFG1[GO2DIAG] bit to logic 1 to enter Diagnostic mode.	Yes	0		0	31	0	31	0	0	0	31	0	31
2	If Odd_Not_Even = 1 Then Write SYS_DIAG[CT_OL_ODD,CT_OL_EVEN] = 10 Else Write SYS_DIAG[CT_OL_ODD,CT_OL_EVEN] = 01	Yes	0		0	31	0	31	0	0	0	31	0	31
3	Wait for the diagnostic time $T_{wait} = K_{DIAG} \cdot \tau_{DIAG}$ (K_{DIAG} unitless, τ_{DIAG} diagnostic time constant)	Yes	0	6691	0	0	0	6691	0	6691	0	0	0	6691
4	Write ADC_CFG[AVG]=0000b and ADC_CFG[SOC]=1 to initiate a conversion	Yes	0		0	31	0	31	0	0	0	31	0	31
5	Wait for conversion time	Yes	520		0	0	0	520	520	0	0	0	0	520
6	Send Read Command to get results	No	0		0	31	0	31	0	0	0	247	0	247
7	Wait for the end of Reception	No	0		432	0	0	432	0	0	3454	0	0	3454
8	Determine fault mode according to the CT Open Detect and Functional Verification Table	No	0		0	0	25	25	0	0	0	0	200	200
9	Write SYS_DIAG[CT_OL_ODD, CT_OL_EVEN] field to 00 configuration to command all fault detect switches open	Yes	0		0	31	0	31	0	0	0	31	0	31
10	If Odd_Not_Even = 0 Then Vmean = mean(all the even cell voltage channels, excluded channel #14 and all the unused ones) If Voltage(channel #14)/Vmean > Ratio_threshold Then CT_14_shorted_to_VPWR = TRUE Else CT_14_shorted_to_VPWR = FALSE	No	0		0	0	25	25	0	0	0	0	200	200
11	Wait for the recovery time $T_{recv} = K \cdot \tau$ (K unitless, τ measurement time constant)	Yes	0	2128	0	0	0	2128	0	2128	0	0	0	2128
12	Clear CELL_OV_FLT and CELL_UV_FLT fault registers, as well as FAULT1_STATUS[CT_OV_FLT, CT_UV_FLT]	Yes	0		0	93	0	93	0	0	0	93	0	93
13	Exit Diagnostic Mode by writing SYS_CFG1[GO2DIAG] bit to logic 0.	Yes	0		0	31	0	31	0	0	0	31	0	31
	End Procedure		0		0	0	0	0	0	0	0	0	0	0
		Totals	520	8818	427	273	0	10097	520	8818	3454	493	400	13686
													Duration on 8 nodes if not parallelizing	80779
													timing reduction using parallelization	83.1%

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all times in µs

Figure 1. SM02 parallelization

Likewise, waiting time for conversions completion or for diagnostic voltage signals to settle do not need replication. In contrast, PC requests to read voltage channels must be replicated. In such case, the multi cluster RX time equals N_{clust} times the single cluster RX time. There are no time savings.

The purpose of Figure 1 and analogous tables applicable to other SM is informing SW developers to simplify their task. Waiting times appearing in such tables get automatically updated depending on the selected filter.

'single cluster' and 'multi cluster' columns have the same structure, including: 1) measurement time 2) pure waiting time 3) RX time 4) TX time 5) calculation time (TX/RX referred to the PC). The IC time is the sum of all these times. The effect of parallelizing in the SM02 is: 83.1 % execution time reduction regarding running N_{clust} times (N_{clust} = 8, in this specific example) its non-parallelized version. In absolute terms, 80779 µs runtime reduces to 13686 µs.

A very special parallelization case is the alternate procedure for SM36, which refers to the automatic I_{sense} open line detection capability while measuring the battery current through pin GPIO_5 and pin GPIO_6. These pins are connected to an analogous filter to that one which is connected to the I_{sense} pins; see Figure 21. Figure 2 shows the procedure and its timing. Instead of idling, the large waiting times associated to steps no. 4 and 7 may be used to measure. In fact, the diagnostic currents injected out of the I_{sense} pins do not affect the measurement via GPIO_5 and GPIO_6. Therefore, in the timing computations of Section 3.1 through Section 3.6, only the communication time (216 µs, in this example) is considered as duration of SM36. If a fault is present, it is detected in 69415 µs, but this time is not wasted, it may be used for running other measurements and diagnostics. The only required non-automatic step is reading the FAULT1_STATUS[IS_OL_FLT] error flag.

			SINGLE CLUSTER					
Step	SM36 alternate procedure as described in the safety manual	May be parallelized?	measurement time us	waiting time us	RX time us	TX time us	calculation time us	IC time us
			0		0	0	0	0
1	Write SYS_CFG1[GO2DIAG] bit to logic 1 to enter Diagnostic mode	Yes	0		0	31	0	31
2	Instruct the current measurement chain to use GPIO5,6 pins by writing the SYS_DIAG[I_MUX] field to 01 configuration	Yes	0		0	31	0	31
3	Configure the current measurement chain for the open detection check by setting the SYS_DIAG[ISENSE_OL_DIAG] bit to logic 1	Yes	0		0	31	0	31
4	Wait for the diagnostic time t_{diag}. During this time, SOC commands may be sent and current measurement values may be read	Yes	0	64000	0	0	0	64000
5	Read the flag FAULT1_STATUS[IS_OL_FLT]	No	0		31	31	0	62
6	Configure the current measurement chain for exiting the open detection check by setting the SYS_DIAG[ISENSE_OL_DIAG] bit to logic 0	Yes	0		0	31	0	31
7	Wait for K (*) times the current measurement time constant τ_f (see section 9.2 as a calculation example)	Yes	0	5200	0	0	0	5200
8	Exit Diagnostic mode SYS_CFG1[GO2DIAG] bit to logic 0.	Yes	0		0	31	0	31
		Totals	0	69199			0	69415

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Figure 2. SM36 alternate procedure timing

In the following sections, six different strategies are presented.

- Strategy 1 and strategy 2 do not use any parallelization feature.
- Strategy 3 and strategy 4 use parallelization: the pack controller waits during simultaneous measurements or during voltage settling after simultaneous closing/opening diagnostic switches. Simultaneous means occurring contemporarily in all nodes.
- Strategy 5 and strategy 6 are similar to strategy 3 and strategy 4; in addition, they use the direct memory access (DMA) feature to run calculations in parallel to communication.

3.1 Strategy 1

Figure 3 shows the timing diagram of a single node (cluster of cells).

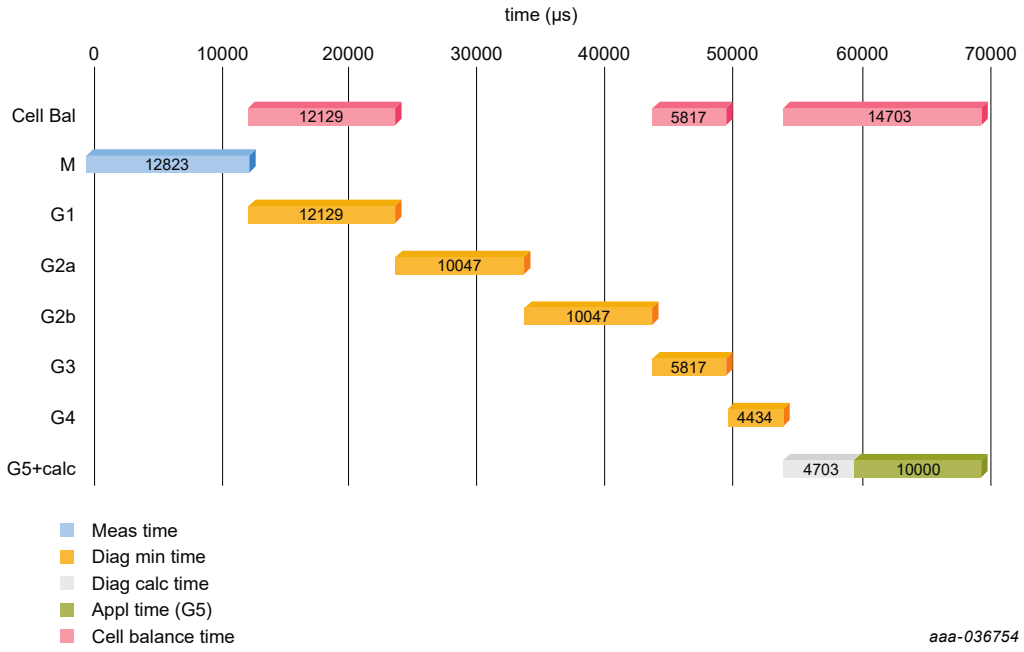


Figure 3. Strategy 1, timing within a single cluster

Each M-group includes the measurements of all nodes. All other groups are related to a specific cluster. Dark yellow bars represent time spent while running G1, G2a to G4, G5 in measuring, turning diagnostic switches on/off, and messaging, but not in running code. The gray bar represents the running code. It is just a residual time, that is the difference between A) chosen measurement period and B) sum of M, G1, G2a to G4, G5 durations. Red bars represent time slices for free balancing. There are N_{clust} (number of clusters) repetitions of Figure 3 diagram, one for each cluster (slave node); see Figure 4.

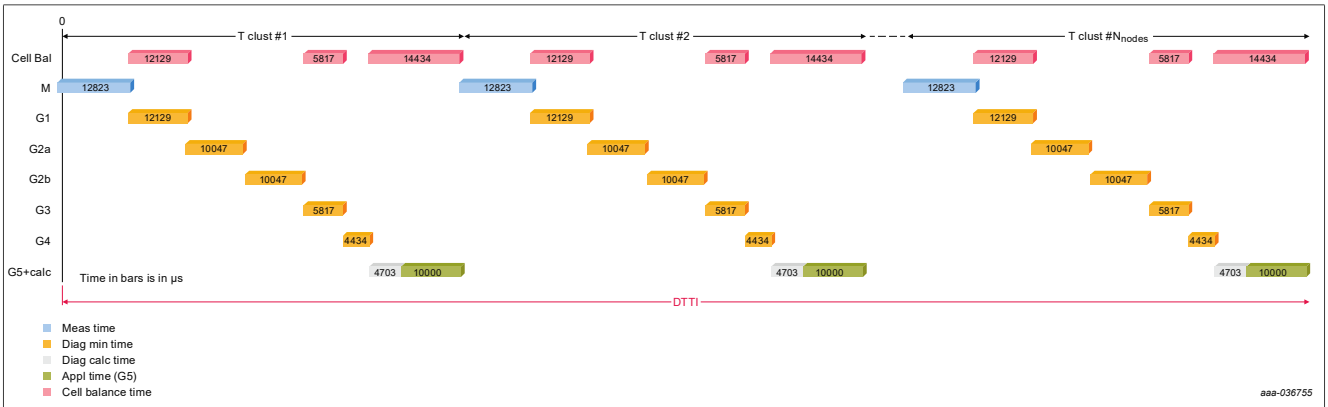


Figure 4. Strategy 1, system timing

3.2 Strategy 2

Strategy 2 interleaves the measurement of all nodes with the execution of two segments of code: A) a certain group of safety mechanisms, Gx, x = 1 to 4, related to a specific node, and B) the application SW, G5, must calculate, for example, SOC and SOH of the battery. More explicitly, following sequences are executed:

- For cluster #1: M, G1, G5; M, G2a, G5; M, G2b, G5; M, G3, G5; M, G4, G5
- For cluster #2: M, G1, G5; M, G2a, G5; M, G2b, G5; M, G3, G5; M, G4, G5
- …, and so on, for any of the N_{clust} clusters.

The term cluster means the series of max 14 cells handled by the MC3377xC. It should be evident, the frequency of both measurements (group M) and application software (group G5) is increased with respect to the case of strategy 1, which is a clear advantage. The drawback of strategy 2 is that the diagnostic test time interval (DTTI) increases. DTTI is the needed time to run once all safety mechanisms in all the nodes of the network.

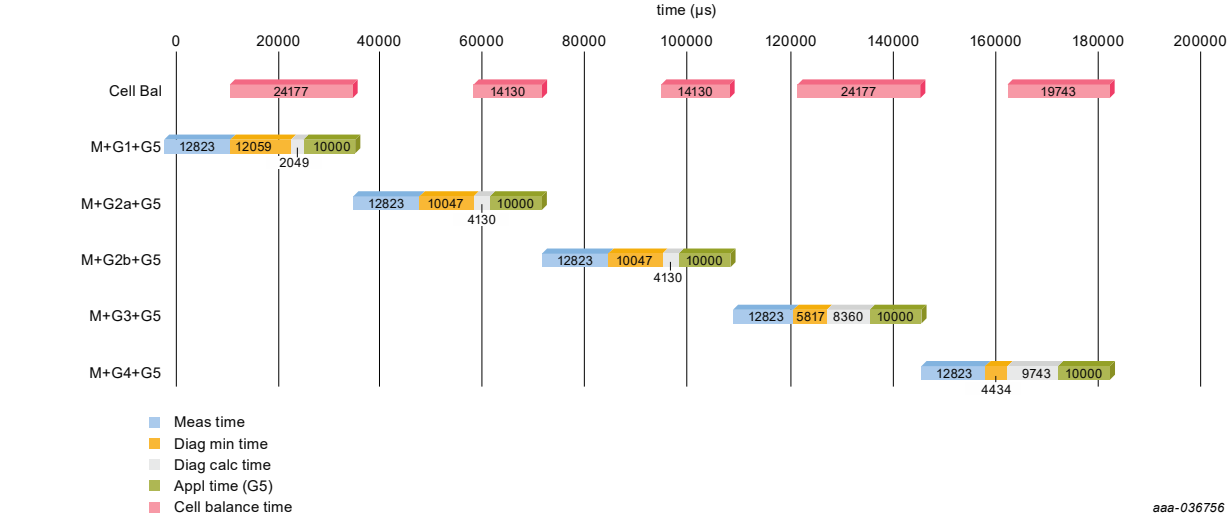


Figure 5. Strategy 2, timing within a single cluster

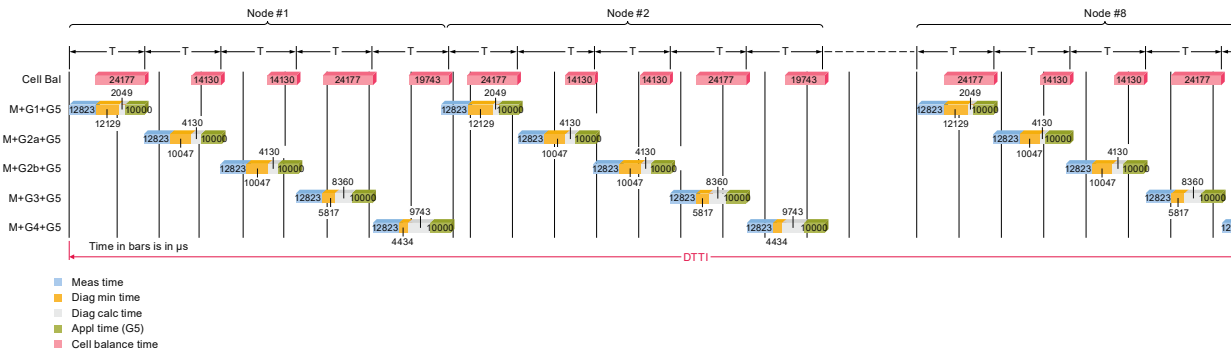


Figure 6. Strategy 2, system timing

3.3 Strategy 3

Strategy 3 looks very much like strategy 1, with the important difference that the former uses parallelized versions of safety mechanisms belonging to Gx groups, for x = 1 to 4. Each parallelized safety mechanism handles all clusters of cells within the system. Therefore, there is only one timing diagram like in Figure 7 for all clusters.

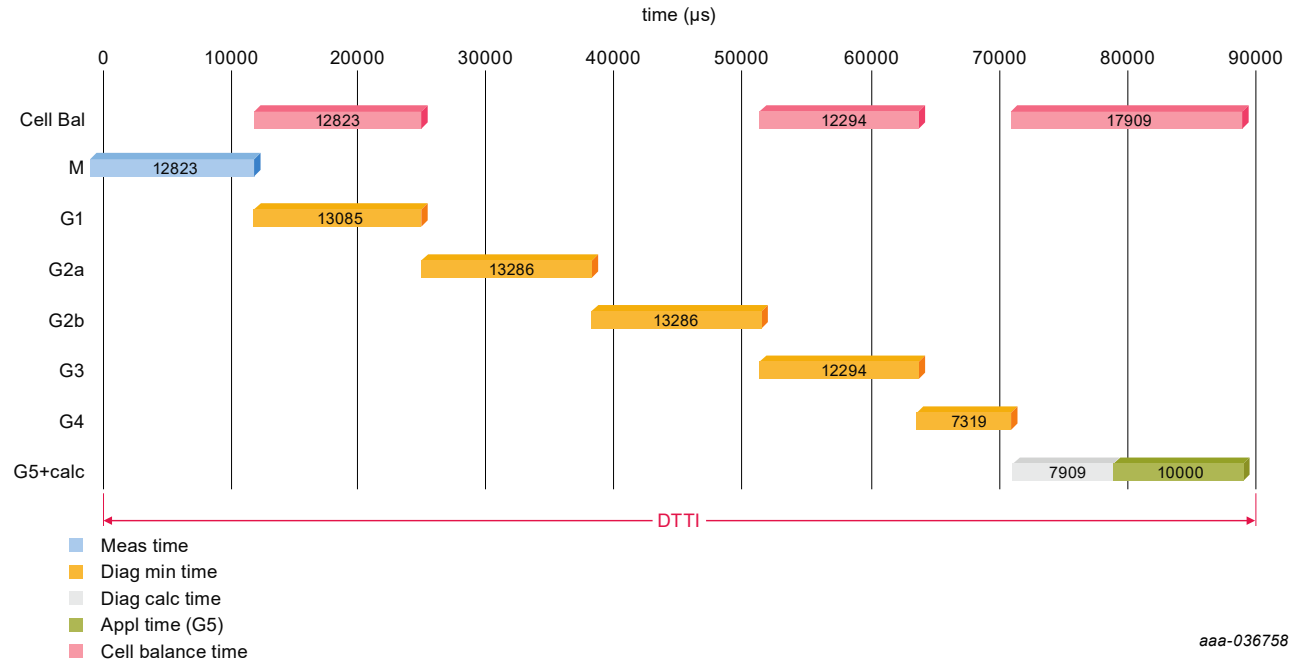


Figure 7. Strategy 3, system timing using parallelized versions of safety mechanisms

3.4 Strategy 4

Strategy 4 looks very much like strategy 2, the only difference being that the former uses parallelized versions of safety mechanisms. Therefore, there is a single diagram like in Figure 8 for all clusters.

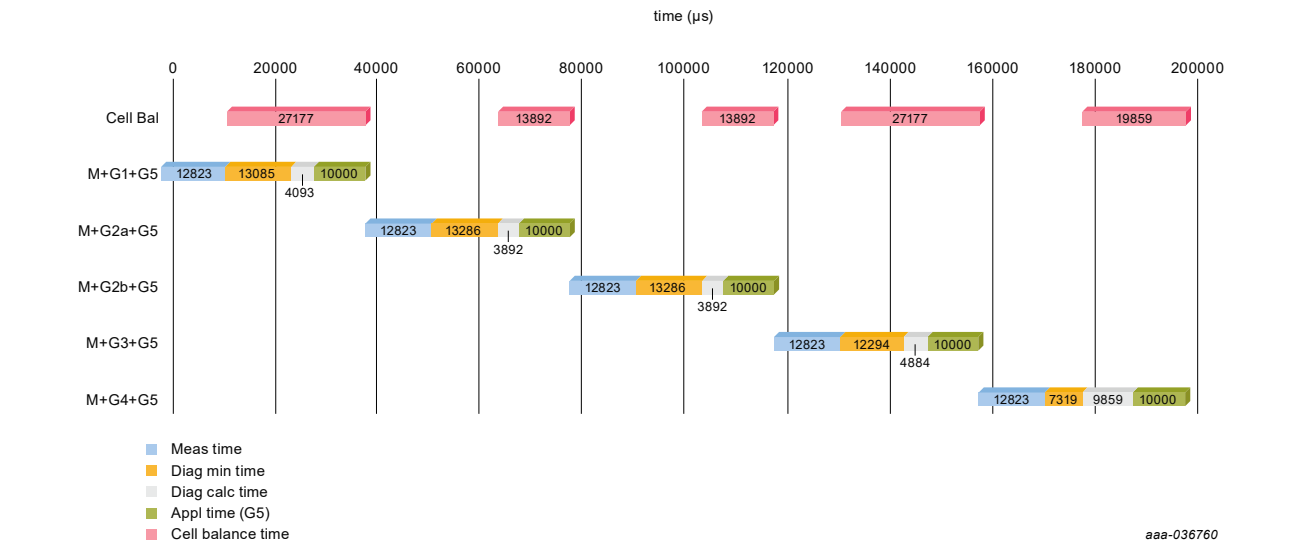


Figure 8. Strategy 4, system timing using parallelized versions of safety mechanisms

3.5 Strategy 5

Strategy 5 looks very much like strategy 3, the only difference being that, in the former case, the group G5 - standing for the application SW and represented by the green bar - runs in parallel to measurements and safety mechanisms, whose communication activities are assumed to be served by a DMA. The rest of the cycle time (DTTI) is used by the CPU to calculate safety mechanisms, represented by the gray bar, as if the SM execution time were concentrated at the end of G1 to G4 groups.

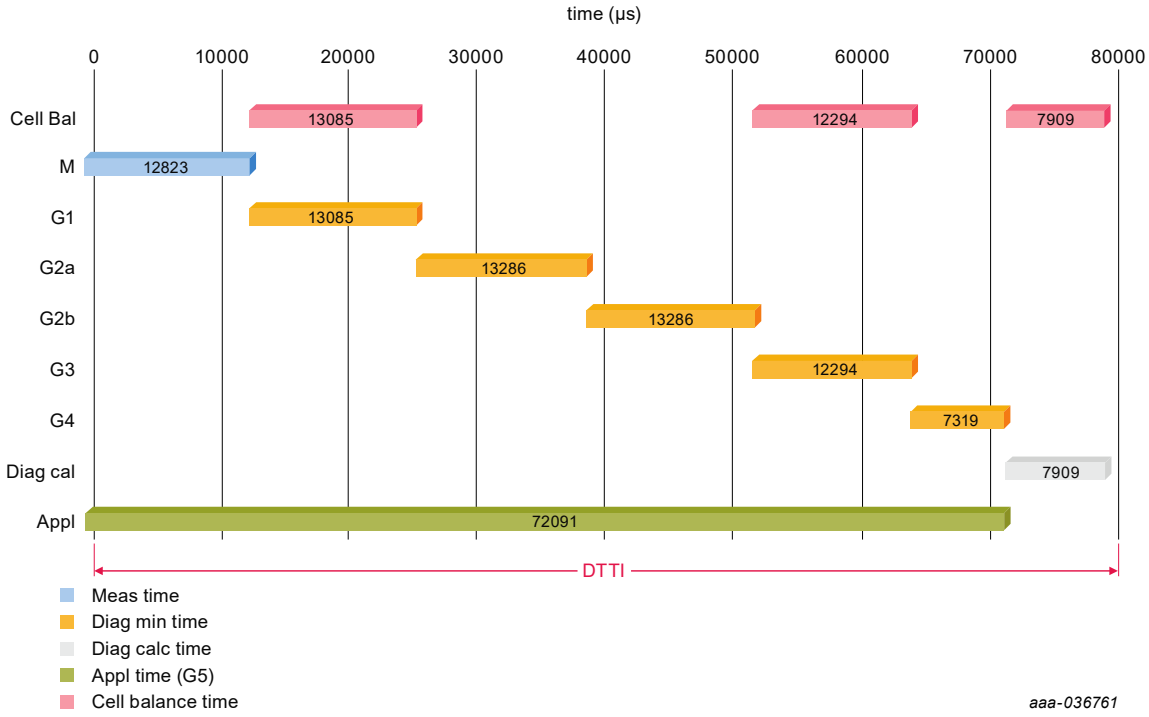


Figure 9. Strategy 5, system timing using both parallelized safety mechanisms, and DMA

3.6 Strategy 6

Strategy 6 looks very much like strategy 4. The only difference is that in the former case, group G5 - representing the execution of the application SW - runs in parallel to both measurements and safety mechanisms. Communication of such two activities is assumed to be served by a DMA. In Figure 10, the execution of the application SW (G5) is represented by green bars. The rest of the cycle time (DTTI) is represented by gray bars, as if the SM calculations were concentrated at the end of each group.

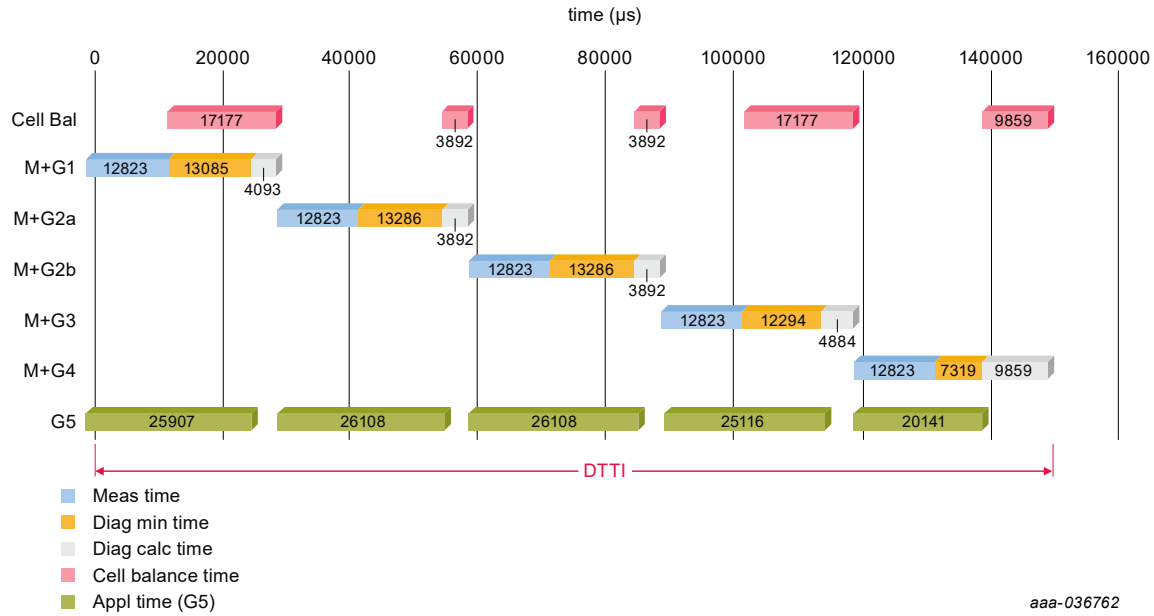


Figure 10. Strategy 6, system timing using parallelized versions of safety mechanisms, and DMA

3.7 How to achieve the best system timing

Document [5] is an Excel workbook whose main worksheet, named Global Parameters, looks like Figure 11. To use the tool, the first thing to do is configuring some input parameters shown in Figure 12. The latter being nothing but a zoom of a portion of Figure 11.

10.0 <Application SW reserved time in ms (G5) TPL <TPL/SPI MC33771C <IC TYPE

Users parameters (may be edited)

Number of Nodes of the system	Cell voltage LPF identifier	ADC1a,b #bits	Verr, mV	Cell volt. average length (via AVG)	Current LPF identifier	ADC2 #bits	Current average length (coulomb)	# current sensors	SM36 & SM39 together?	EEPROM?
8	ID_08	16	6	8	ID_01	16	110	1	Yes	No

Output Data (don't touch)

ADC1-a,b conversion time [us]	ADC2 conversion time [us]	Time to measure all nodes [us]	# PC TX msg to get measur. & faultx_sts	# PC RX msg to get measur. & faultx_sts	Time to read all nodes [us]
520	38	4157	17	264	8666

Users parameters (may be edited)

# meas. registers per clust. to read	# diagnost. registers per clust.	Safety goals			FDTI [ms]	Strategy?	Strategy 1 Measurement cycle [ms]	Strategy 2 Measurement cycle [ms]	Strategy 3 Measurement cycle [ms]	Strategy 4 Measurement cycle [ms]	Strategy 5 Measurement cycle [ms]	Strategy 6 Measurement cycle [ms]
		OV/UV	OT/UT	OC								
30	3	Yes	Yes	Yes	500	5	70	37	90	40	80	30

Output Data (don't touch)

Cell balance ratio	Communication rate [Mbps]	DTTI [ms]	Min LTI [ms]
42%	1.010	80.0	30.2

Output of grouping strategy 1 (don't touch)

t_M [ms]	t_G1 [ms]	t_G2 [ms]	t_G2 [ms]	t_G3 [ms]	t_G4 [ms]	t_G5 [ms]	t_G6 [ms]	t_G7 [ms]	Min DTTI clust [ms]	Min LTI clust [ms]	DTTI [ms]	LTI [ms]	# Pack Controller TX msg	# Pack Controller RX msg	TX mean bit rate by P.C. kbps	RX mean bit rate by P.C. kbps
12.8	12.1	10.0	10.0	5.8	4.4	10.0	0.0	0.0	65.3	12.1	560.0	96.7	184	433	126.2	296.9

Output of grouping strategy 2 (don't touch)

t_M+t_G5+ t_G1	t_M+t_G5+ t_G2	t_M+t_G5+ t_G2	t_M+t_G5+ t_G3	t_M+t_G5+ t_G4	t_M+t_G5+ t_G6	t_M+t_G5+ t_G7	TBD	Min meas. period [ms]	Min DTTI clust [ms]	Min LTI clust [ms]	DTTI [ms]	LTI [ms]	# Pack Controller TX msg	# Pack Controller RX msg	TX mean bit rate by P.C. kbps	RX mean bit rate by P.C. kbps
35.0	32.9	32.9	28.6	27.3	0.0	0.0		35.0	185.0	12.1	1480.0	96.7	2016	11912	65.4	386.3

Output of grouping strategy 3 (don't touch)

t_M [ms]	t_G1 [ms]	t_G2 [ms]	t_G2 [ms]	t_G3 [ms]	t_G4 [ms]	t_G5 [ms]	t_G6 [ms]	t_G7 [ms]	Min DTTI clust [ms]	Min LTI clust [ms]	DTTI [ms]	LTI [ms]	# Pack Controller TX msg	# Pack Controller RX msg	TX mean bit rate by P.C. kbps	RX mean bit rate by P.C. kbps
12.8	13.1	13.3	13.3	12.3	7.3	10.0	0.0	0.0	82.1	30.2	90.0	30.2	293	1391	156.3	741.9

Output of grouping strategy 4 (don't touch)

t_M+t_G5+ t_G1	t_M+t_G5+ t_G2	t_M+t_G5+ t_G2	t_M+t_G5+ t_G3	t_M+t_G5+ t_G4	t_M+t_G5+ t_G6	t_M+t_G5+ t_G7	TBD	Min meas. period [ms]	Min DTTI clust [ms]	Min LTI clust [ms]	DTTI [ms]	LTI [ms]	# Pack Controller TX msg	# Pack Controller RX msg	TX mean bit rate by P.C. kbps	RX mean bit rate by P.C. kbps
35.9	36.1	36.1	35.1	30.1	0.0	0.0		36.1	200.0	30.2	200.0	30.2	361	2447	86.6	587.3

Output of grouping strategy 5 (don't touch)

t_M [ms]	t_G1 [ms]	t_G2 [ms]	t_G2 [ms]	t_G3 [ms]	t_G4 [ms]	TBD	TBD	Min meas. period [ms]	Min DTTI clust [ms]	Min LTI clust [ms]	DTTI [ms]	LTI [ms]	# Pack Controller TX msg	# Pack Controller RX msg	TX mean bit rate by P.C. kbps	RX mean bit rate by P.C. kbps
12.8	13.1	13.3	13.3	12.3	7.3			72.1	80.0	30.2	80.0	30.2	293	1391	175.8	834.6

Output of grouping strategy 6 (don't touch)

t_M+ t_G1	t_M+t_G2	t_M+t_G2	t_M+t_G3	t_M+t_G4	t_M+t_G6	t_M+t_G7	TBD	Min meas. period [ms]	Min DTTI clust [ms]	Min LTI clust [ms]	DTTI [ms]	LTI [ms]	# Pack Controller TX msg	# Pack Controller RX msg	TX mean bit rate by P.C. kbps	RX mean bit rate by P.C. kbps
25.9	26.1	26.1	25.1	20.1	0.0	0.0		26.1	150.0	30.2	150.0	30.2	361	2447	115.5	783.0

aaa-036763

Figure 11. Global parameters

10.0 <Application SW reserved time in ms (G5) TPL TPL/SPI MC33771C <IC TYPE

Users parameters (may be edited)

Number of Nodes of the system	Cell voltage LPF identifier	ADC1a,b #bits	Verr, mV	Cell volt. average length (via AVG)	Current LPF identifier	ADC2 #bits	Current average length (coulomb)	# current sensors	SM36 & SM39 together?	EEPROM?	ADC1-a,b conversion time [us]	ADC2 conversion time [us]
8	ID_08	16	6	8	ID_01	16	110	1	Yes	No	520	38

Users parameters (may be edited)

# meas. registers per clust. to read	# diagnost. registers per clust.	Safety goals			FDTI [ms]	Strategy?	Strategy 1 Measurement cycle [ms]	Strategy 2 Measurement cycle [ms]	Strategy 3 Measurement cycle [ms]	Strategy 4 Measurement cycle [ms]	Strategy 5 Measurement cycle [ms]	Strategy 6 Measurement cycle [ms]
		OV/UV	OT/UT	OC								
30	3	Yes	Yes	Yes	500	5	70	37	90	40	80	30

aaa-036764

Figure 12. Input parameters

The meaning of the input parameters follows.

- Number of nodes of the system: number of daisy chained MC3377xC. Default is 8.
- Cell voltage LPF identifier: an item of 'Cell voltage analog filters' worksheet, see Figure 16. Default is ID_08.
- ADC1a,b #bits: the number of equivalent bits of ADC1-a, and ADC1-b. It shall be kept at value 16.
- Verr, mV: cell voltage max error, depending on cell voltage and temperature ranges. The 6 mV default value is suitable for most applications. Other values are given in documents [2] and [6].
- Cell volt. average length (via AVG): the cell voltage moving average length corresponding to the ADC_CFG[AVG] parameter, see documents [2] and [6]. If the parameter equals 0011b, the length is equal to 8, the default.
- ADC2 #bits: the number of equivalent bits of ADC2. It shall be kept at value 16.
- Current LPF identifier: it represents an item of 'Current LPF' worksheet, see Figure 22. Default is ID_01.
- Current average length (coulomb): number of current samples accumulated between any two consecutive readings of the coulomb counter. Default is 110.
- # current sensors: number of current sensors, it may be {0,1,2}, default is 1.
- SM36 & SM39 together?: If yes, it means SM36 and SM39 are combined, making SM36 not intrusive (the current is measured via GPIO_5 and GPIO_6 when SM36 injects the diagnostic current out of the ISENSE+/- pins). Set yes only if a double filter is used, see Figure 21, otherwise set no. Default is yes.
- EEPROM?: yes if an EEPROM connected to the MC3377xC holds its calibrations, else set no (default).
- # meas. registers per clust. to read: number of consecutive register addresses to be read for measurement purposes. Considering registers from CC_NB_SAMPLES to MEAS_VBG_DIAG_ADC1B - see documents [2] and [6] – the default is 30.
- # diagnost. registers per clust. to read: number of consecutive register addresses to be read for diagnostic purposes, default is 3, representing registers FAULTx_STATUS, x = 1, 2, 3.
- Safety goals
  - OV/UV: set no if both OV and UV safety goals are not applicable, else set yes. Default is yes.
  - OT/UT: set no if both OT and UT safety goals are not applicable, else set yes. Default is yes.
  - OC: set no if OC safety goal is not applicable, else set yes. Default is yes.
- FDTI [ms]: fault detection time interval, which is the amount of FTTI allocated to diagnose the daisy chain of slave nodes (clusters).
- Strategy?: selected strategy, it may assume one of {1,2,3,4,5,6} values.
- Strategy 1 Measurement cycle [ms]: period of group M when using strategy 1
- Strategy 2 Measurement cycle [ms]: period of group M when using strategy 2
- Strategy 3 Measurement cycle [ms]: period of group M when using strategy 3
- Strategy 4 Measurement cycle [ms]: period of group M when using strategy 4
- Strategy 5 Measurement cycle [ms]: period of group M when using strategy 5
- Strategy 6 Measurement cycle [ms]: period of group M when using strategy 6

If there is any doubt about the meaning of a parameter, point your mouse on the title of the parameter itself; the related comment shows up. Here are a few steps that one may want to follow:

1. Check IC type, communication type, number of nodes and fix it as needed.
2. Configure the number of current sensors (0,1,2) managed by the daisy chain of MC3377xC.
3. If GPIO_5 and GPIO_6 used as in Figure 21, set 'SM36 & SM39 together' = yes.
4. Configure if an EEPROM is connected to the MC3377xC: write yes only if it holds modified calibrations, for example, modified current channel gains, otherwise write no.
5. Check the applicable safety goals (SG) and fix them as needed.
6. Set the FDTI that is a fraction of the most stringent FTTI (in the example of Table 1, it would be a fraction of 1 s, the min FTTI).
7. If needed, change the cell voltage LPF identifier or the averaging length to achieve your target bandwidth and attenuation. Consider there are many ways to achieve such targets with very different SM02 timing implications; see Section 4.
8. If needed, change the current LPF identifier or the current average length (depending on the planned coulomb counter number of steps) to achieve your target bandwidth and attenuation. That impacts SM36 timing; see Section 5.
9. Select the strategy you want to focus on (but you also see other results).
10. Select the strategy x measurement cycle in ms, for x = 1 to 6.

After inputs configuration, it may happen that one of the 'DTTI [ms]' output parameter is highlighted in red color, meaning its value exceeds the value of the 'FDTI [ms]' input parameter. It may be fixed as explained in an exercise that follows. For strategies x = 1, 3, 5, the 'Strategy x Measurement cycle [ms]' value must be greater than the value of the 'Min DTTI clust [ms]' output parameter, otherwise a red colored highlight appears. The latter represents the minimum time to diagnose a cluster. For strategies x = 2, 4, 6, the 'Strategy x Measurement cycle [ms]' value must be greater than the value of the 'Min meas. period [ms]' output parameter, otherwise a red colored highlight appears. The latter represents the minimum time period to measure all nodes.

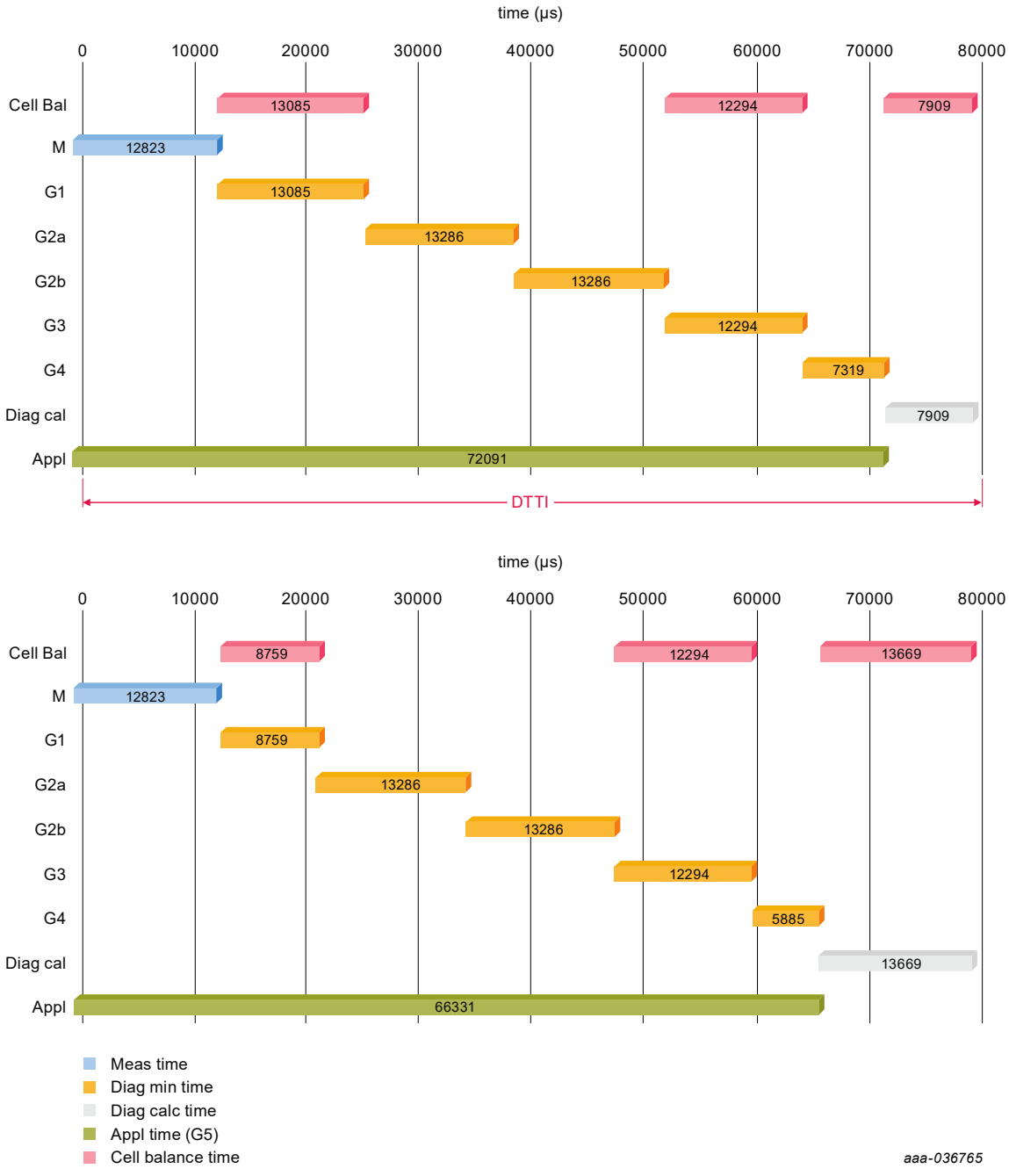


Figure 13. Strategy 5 timing change by removing SMx, x = 05, 06, 29, 30, 32, 36, 37, 40

Exercise: consider using strategy 5 and removing SM05, SM06, SM29, SM30, SM32, SM36, SM37, and SM40. This would change the residual time - Diag. calc. time in Figure 13 - from 7909 µs (top part of the figure) to 13669 µs (bottom part of the figure), giving the possibility to reduce the 'Strategy 5 Measurement cycle [ms]' parameter from 80 ms to 74 ms, see Figure 14. It leaves about the same CPU time for calculating all the diagnostics, implying the achievement of DTTI = 74 ms. Consider the assumption of FTTI given in Table 1, the most stringent of which is 1000 ms, and let the 'DTTI [ms]' parameter be 300 ms. There is room for running 4 consecutive times the safety mechanisms of all nodes, allowing for deglitching; for example, the user may ignore 1 false positive out of 4 consecutive DTTI to reduce the probability of false alarms occurrence.

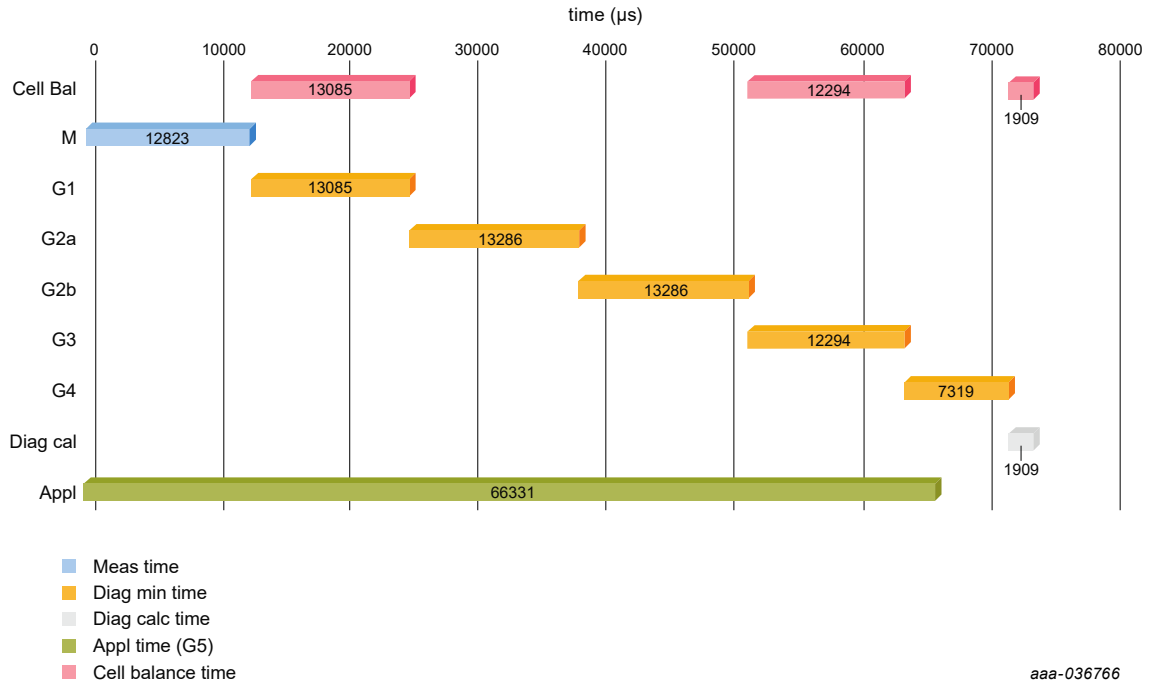


Figure 14. DTTI = 74 ms if strategy 5 and SM05, SM06, SM29, SM30, SM32, SM36, SM37, SM40 unused

4 Timing effects due to cell voltage filtering

The reference circuit is shown in Figure 15. SM01 or SM02 execution changes the circuit configuration by connecting internal resistors across adjacent CT_x and CT_x-1 pins, for x either odd or even number; this results in charging/discharging some capacitors of the external filter. Hence, different filter components result in different waiting times. If the MC3377xC senses fewer than the maximum number of cells, refer to document [7]; there can be found different filter topologies in the vicinity of the non-used channels. These are called type A, type B and type C. Different filter types or number of used cells also result in different timing; see Figure 16.

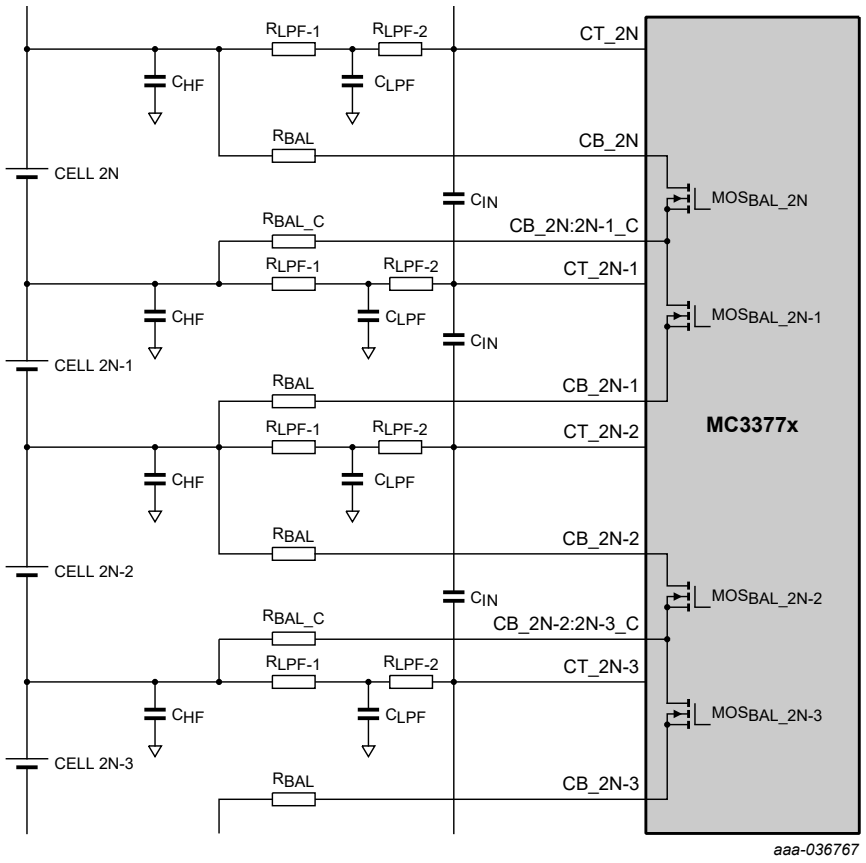


Figure 15. Cell voltage anti-aliasing filters

4.1 Anti-aliasing filter components selection

Figure 16 shows the appearance of the 'Cell voltage analog filters' worksheet. Such worksheet applies to the MC33771C. To handle the MC33772C, use the 'Cell voltage analog filters (2)' worksheet, having the same structure.

Warning: the worksheet is valid for filters types A, B and C. It provides the user guidance in calculating thresholds and timings for SM01 and SM02. However, always consider those results critically. This is by no

Max Ncell	SM02 tol mV	SM02 err recovery mV	SM01 tol	SM01 err recovery mV	SM01 Kdiag		R_{LPF-1} tolerance fraction	R_{LPF-2} tolerance fraction		Out of bounds probabilit
14	10	14.4	2.50%	14.4	5		100.0%	57.0%		1.1E-16

Editable columns — Warning: do not edit these columns

Item	Circuit	Ncell	min(Vcell) mV	max(Vcell) mV	R_{LPF-1} kΩ	C_{LPF} nF	R_{LPF-2} kΩ	R_{LPF-1} tolerance	R_{LPF-2} tolerance	C_{IN} nF	C_{HF} nF	Analog cutoff frequency Hz	SM02 threshold mV	SM02 Twait ms	SM02 Trecv ms	SM02 IC time ms	SM01 OV threshold mV	SM01 UV threshold mV	SM01 Trecv ms	SM01 Twait ms	SM01 IC time ms
ID_01	Type A	14	2200	4300	3	470	2	5.0%	5.0%	47	47	113	150	10.80	10.0	22.0	3601	1409	10.00	3.33	18.31
ID_02	Type A	12	2200	4300	3	470	2	5.0%	5.0%	47	47	113	150	28.20	10.0	39.5	3601	1409	10.00	3.33	18.31
ID_03	Type A	8	2200	4300	3	470	2	5.0%	5.0%	47	47	113	150	28.20	10.0	39.5	3601	1409	10.00	3.33	18.31
ID_04	Type A	14	1450	4300	3	100	2	10.0%	10.0%	10	47	530	90	3.96	2.1	7.3	2353	1468	2.13	0.71	5.20
ID_05	Type A	12	1450	4300	3	100	2	10.0%	10.0%	47	47	527	90	9.49	4.0	14.8	2353	1468	4.01	0.75	7.17
ID_06	Type A	8	1450	4300	3	100	2	10.0%	10.0%	10	47	529	90	8.18	2.1	11.6	2353	1468	2.13	0.71	5.20
ID_07	Type A	14	2200	4300	3	100	2	5.0%	5.0%	10	47	530	150	3.20	2.1	6.6	3601	1409	2.13	0.71	5.20
ID_08	Type A	12	2200	4300	3	100	2	5.0%	5.0%	10	47	530	150	6.69	2.1	10.1	3601	1409	2.13	0.71	5.20
ID_09	Type A	8	2200	4300	3	100	2	5.0%	5.0%	10	47	529	150	6.69	2.1	10.1	3601	1409	2.13	0.71	5.20
ID_10	Type A	14	2100	4300	3	100	2	5.0%	5.0%	10	47	530	142	3.27	2.1	6.7	3437	1409	2.13	0.71	5.20
ID_11	Type A	12	2100	4300	3	100	2	5.0%	5.0%	10	47	530	142	6.84	2.1	10.2	3437	1409	2.13	0.71	5.20
ID_12	Type A	8	2100	4300	3	100	2	5.0%	5.0%	10	47	529	142	6.84	2.1	10.2	3437	1409	2.13	0.71	5.20
ID_13	Type A	14	2100	4300	3	100	2	5.0%	5.0%	10	47	530	142	3.27	2.1	6.7	3437	1409	2.13	0.71	5.20
ID_14	Type A	12	2100	4300	3	100	2	5.0%	5.0%	10	47	530	142	6.84	2.1	10.2	3437	1409	2.13	0.71	5.20
ID_15	Type A	8	2100	4300	3	100	2	5.0%	5.0%	10	47	529	142	6.84	2.1	10.2	3437	1409	2.13	0.71	5.20
ID_16	Type B	14	2200	4300	3	470	2	5.0%	5.0%	10	47	113	150	9.87	8.4	19.5	3261	1149	8.43	3.30	16.67
ID_17	Type B	12	2200	4300	3	470	2	5.0%	5.0%	10	47	113	150	9.97	8.4	19.7	3261	1149	8.43	3.30	16.67
ID_18	Type B	8	2200	4300	3	470	2	5.0%	5.0%	10	47	113	150	10.19	8.4	19.9	3261	1149	8.43	3.30	16.67
ID_19	Type B	14	2200	4300	3	100	2	5.0%	5.0%	47	47	528	150	4.53	4.0	9.8	3261	1149	4.01	0.75	7.17
ID_20	Type B	12	2200	4300	3	100	2	5.0%	5.0%	47	47	527	150	5.03	4.0	10.3	3261	1149	4.01	0.75	7.17
ID_21	Type B	8	2200	4300	3	100	2	5.0%	5.0%	47	47	523	150	6.03	4.0	11.3	3261	1149	4.01	0.75	7.17
ID_22	Type B	14	2500	4300	6.8	100	2	5.0%	5.0%	47	47	233	94	7.16	8.2	16.6	3687	743	8.17	1.01	11.84
ID_23	Type B	12	2500	4300	6.8	100	2	5.0%	5.0%	47	47	233	94	7.68	8.2	17.1	3687	743	8.17	1.01	11.84

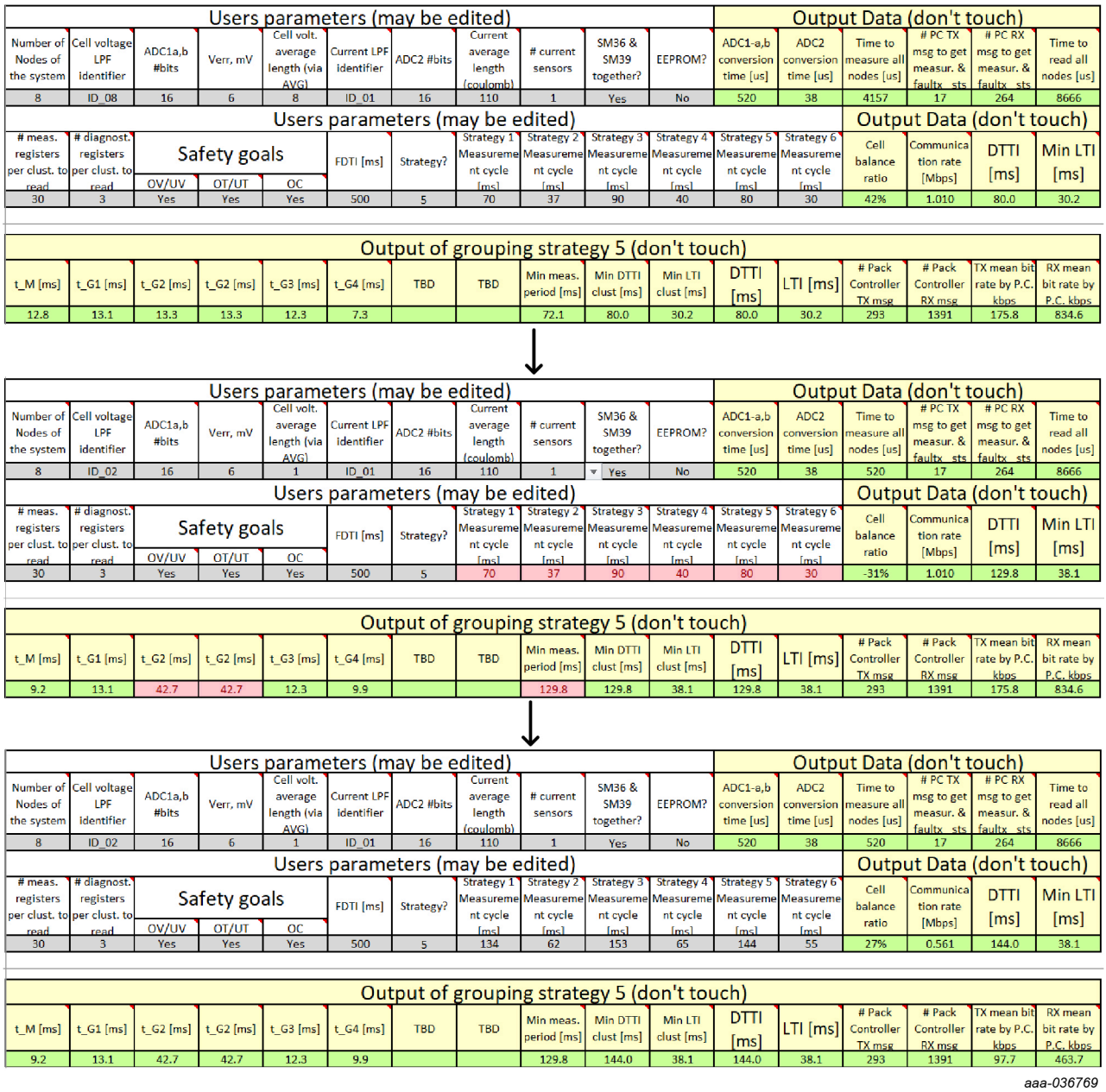
aaa-036768

Figure 16. Cell voltage analog filters

Depending on A) number of used cells, N_{cell}, which may be 14, 12 or 8, B) minimum and the maximum cell voltage, and C) resistance and capacitance values of PCB components, the user gets both SM01 and SM02 timing, which is considered in the DTTI calculation of each timing strategy.

For example, both T_{wait} and T_{recv} waiting times used in SM02 procedure, shown in Figure 1, come from Figure 16. The worksheet is also useful to calculate SM01 and SM02 thresholds. However, recall that SM01 is not needed in the MC3377xC safety concept, it is just an option for customer flexibility. The effect of the analog filter on the system timing is huge. For instance:

- Start with LPF identifier = ID_08 and moving average length = 8. Result is on the top of Figure 17: DTTI (strategy 5) = measurement cycle (strategy 5) = 80 ms
- Switch to LPF identifier = ID_02 and moving average length = 1. Result is in the middle of Figure 17: strategy 5 minimum measurement period is 129.8 ms while the used period is 80 ms, which is wrong, that is why they are highlighted red
- While keeping both LPF identifier = ID_02 and moving average length = 1, increase strategy 1 to 6 measurement cycles. Result is on the bottom of Figure 17: red color disappears, DTTI (strategy 5) = measurement cycle (strategy 5) = 144 ms. Maybe the DTTI is anyway good, but is the measurement cycle such?



Users parameters (may be edited) | Output Data (don't touch)

Number of Nodes of the system	Cell voltage LPF identifier	ADC1a,b #bits	Verr, mV	Cell volt. average length (via AVG)	Current LPF identifier	ADC2 #bits	Current average length (coulomb)	# current sensors	SM36 & SM39 together?	EEPROM?	ADC1-a,b conversion time [us]	ADC2 conversion time [us]	Time to measure all nodes [us]	# PC TX msg to get measur. & faultx_sts	# PC RX msg to get measur. & faultx_sts	Time to read all nodes [us]
8	ID_08	16	6	8	ID_01	16	110	1	Yes	No	520	38	4157	17	264	8666

Users parameters (may be edited) | Output Data (don't touch)

# meas. registers per clust. to read	# diagnost. registers per clust. to read	Safety goals			FDTI [ms]	Strategy?	Strategy 1 Measurement cycle [ms]	Strategy 2 Measurement cycle [ms]	Strategy 3 Measurement cycle [ms]	Strategy 4 Measurement cycle [ms]	Strategy 5 Measurement cycle [ms]	Strategy 6 Measurement cycle [ms]	Cell balance ratio	Communication rate [Mbps]	DTTI [ms]	Min LTI [ms]
		OV/UV	OT/UT	OC												
30	3	Yes	Yes	Yes	500	5	70	37	90	40	80	30	42%	1.010	80.0	30.2

Output of grouping strategy 5 (don't touch)

t_M [ms]	t_G1 [ms]	t_G2 [ms]	t_G2 [ms]	t_G3 [ms]	t_G4 [ms]	TBD	TBD	Min meas. period [ms]	Min DTTI clust [ms]	Min LTI clust [ms]	DTTI [ms]	LTI [ms]	# Pack Controller TX msg	# Pack Controller RX msg	TX mean bit rate by P.C. kbps	RX mean bit rate by P.C. kbps
12.8	13.1	13.3	13.3	12.3	7.3			72.1	80.0	30.2	80.0	30.2	293	1391	175.8	834.6

Users parameters (may be edited) | Output Data (don't touch)

Number of Nodes of the system	Cell voltage LPF identifier	ADC1a,b #bits	Verr, mV	Cell volt. average length (via AVG)	Current LPF identifier	ADC2 #bits	Current average length (coulomb)	# current sensors	SM36 & SM39 together?	EEPROM?	ADC1-a,b conversion time [us]	ADC2 conversion time [us]	Time to measure all nodes [us]	# PC TX msg to get measur. & faultx_sts	# PC RX msg to get measur. & faultx_sts	Time to read all nodes [us]
8	ID_02	16	6	1	ID_01	16	110	1	Yes	No	520	38	520	17	264	8666

Users parameters (may be edited) | Output Data (don't touch)

# meas. registers per clust. to read	# diagnost. registers per clust. to read	Safety goals			FDTI [ms]	Strategy?	Strategy 1 Measurement cycle [ms]	Strategy 2 Measurement cycle [ms]	Strategy 3 Measurement cycle [ms]	Strategy 4 Measurement cycle [ms]	Strategy 5 Measurement cycle [ms]	Strategy 6 Measurement cycle [ms]	Cell balance ratio	Communication rate [Mbps]	DTTI [ms]	Min LTI [ms]
		OV/UV	OT/UT	OC												
30	3	Yes	Yes	Yes	500	5	70	37	90	40	80	30	-31%	1.010	129.8	38.1

Output of grouping strategy 5 (don't touch)

t_M [ms]	t_G1 [ms]	t_G2 [ms]	t_G2 [ms]	t_G3 [ms]	t_G4 [ms]	TBD	TBD	Min meas. period [ms]	Min DTTI clust [ms]	Min LTI clust [ms]	DTTI [ms]	LTI [ms]	# Pack Controller TX msg	# Pack Controller RX msg	TX mean bit rate by P.C. kbps	RX mean bit rate by P.C. kbps
9.2	13.1	42.7	42.7	12.3	9.9			129.8	129.8	38.1	129.8	38.1	293	1391	175.8	834.6

Users parameters (may be edited) | Output Data (don't touch)

Number of Nodes of the system	Cell voltage LPF identifier	ADC1a,b #bits	Verr, mV	Cell volt. average length (via AVG)	Current LPF identifier	ADC2 #bits	Current average length (coulomb)	# current sensors	SM36 & SM39 together?	EEPROM?	ADC1-a,b conversion time [us]	ADC2 conversion time [us]	Time to measure all nodes [us]	# PC TX msg to get measur. & faultx_sts	# PC RX msg to get measur. & faultx_sts	Time to read all nodes [us]
8	ID_02	16	6	1	ID_01	16	110	1	Yes	No	520	38	520	17	264	8666

Users parameters (may be edited) | Output Data (don't touch)

# meas. registers per clust. to read	# diagnost. registers per clust. to read	Safety goals			FDTI [ms]	Strategy?	Strategy 1 Measurement cycle [ms]	Strategy 2 Measurement cycle [ms]	Strategy 3 Measurement cycle [ms]	Strategy 4 Measurement cycle [ms]	Strategy 5 Measurement cycle [ms]	Strategy 6 Measurement cycle [ms]	Cell balance ratio	Communication rate [Mbps]	DTTI [ms]	Min LTI [ms]
		OV/UV	OT/UT	OC												
30	3	Yes	Yes	Yes	500	5	134	62	153	65	144	55	27%	0.561	144.0	38.1

Output of grouping strategy 5 (don't touch)

t_M [ms]	t_G1 [ms]	t_G2 [ms]	t_G2 [ms]	t_G3 [ms]	t_G4 [ms]	TBD	TBD	Min meas. period [ms]	Min DTTI clust [ms]	Min LTI clust [ms]	DTTI [ms]	LTI [ms]	# Pack Controller TX msg	# Pack Controller RX msg	TX mean bit rate by P.C. kbps	RX mean bit rate by P.C. kbps
9.2	13.1	42.7	42.7	12.3	9.9			129.8	144.0	38.1	144.0	38.1	293	1391	97.7	463.7

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Figure 17. Switching to cell voltage LPF = ID_02 and cell voltage average length = 1

Replacing ID_08 with ID_02 gives much greater time constants, causing SM02 to take much longer, see Figure 18; while changing the length of the moving average (MA) from 8 to 1 reduces the duration of group M, but these effects in opposite directions do not compensate each other.

Max Ncell	SM02 tol mV	SM02 err recovery mV	SM01 tol	SM01 err recovery mV	SM01 Kdiag		R_{LPF-1} tolerance fraction	R_{LPF-2} tolerance fraction			Out of bounds probabilit									
14	10	14.4	2.50%	14.4	5		100.0%	57.0%			1.1E-16									
	Editable columns										Warning: do not edit these columns									
Item	Circuit	Ncell	min(Vcell) mV	max(Vcell) mV	R_{LPF-1} kΩ	C_{LPF} nF	R_{LPF-2} kΩ	R_{LPF-1} tolerance	R_{LPF-2} tolerance	C_{IN} nF	C_{HF} nF	Analog cutoff frequency Hz	SM02 threshold mV	SM02 Twait ms	SM02 Trecv ms	SM02 IC time ms	SM01 OV threshold mV	SM01 UV threshold mV	SM01 Trecv ms	SM01 Twait ms	SM01 IC time ms
ID_02	Type A	12	2200	4300	3	470	2	5.0%	5.0%	47	47	113	150	28.20	10.0	39.5	3601	1409	10.00	3.33	18.31
ID_08	Type A	12	2200	4300	3	100	2	5.0%	5.0%	10	47	530	150	6.69	2.1	10.1	3601	1409	2.13	0.71	5.20

aaa-036770

Figure 18. ID_02 vs ID_08, observe the differences in T_{wait} and T_{recv} diagnostic times

4.2 Digital filter parameter settings

The MA digital filter, in conjunction with the anti-aliasing LPF, shapes the final frequency response. Figure 19 and Figure 20 show two different ways of achieving about 100 Hz cut-off frequency with different effect on the system timing.

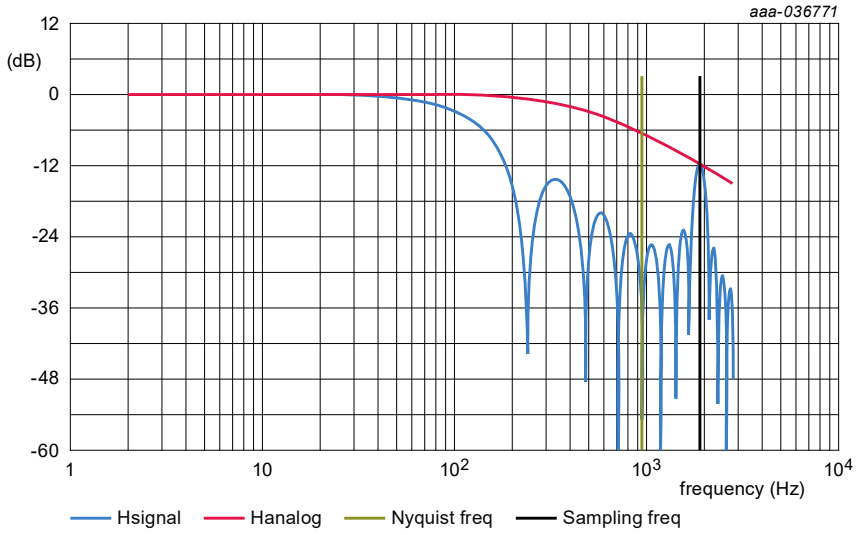


Figure 19. ID_08 analog LPF with length 8 moving average

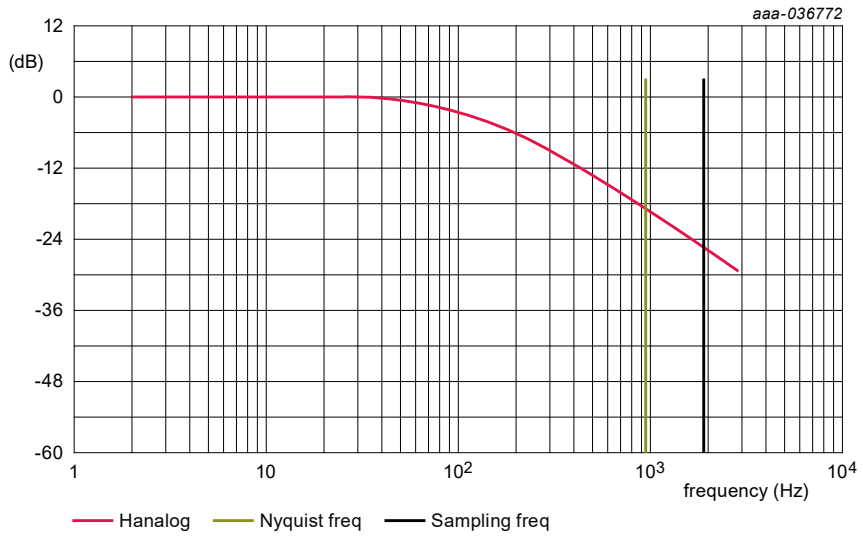


Figure 20. ID_02 analog LPF with length 1 moving average

Usage of analog LPF with ID_08 identifier gives 530 Hz bandwidth. The user can achieve the required 100 Hz bandwidth by digital filtering, setting MA length = 8; see Figure 19.

Using ID_02 already gives the requested analog bandwidth as shown in Figure 20, causing the MA filter to be not used, namely MA length = 1.

If the IC is an MC33771C, the frequency response may be obtained in 'Analog & digital LPF analysis' worksheet of the tool. If it is an MC33772C, the 'Analog & digital LPF analysis (2)' worksheet applies.

5 Timing effects due to current signal filtering

The external circuit for current measurement is shown in Figure 21. The filter is doubled for both SM39 implementation and to let SM36 run non-intrusively.

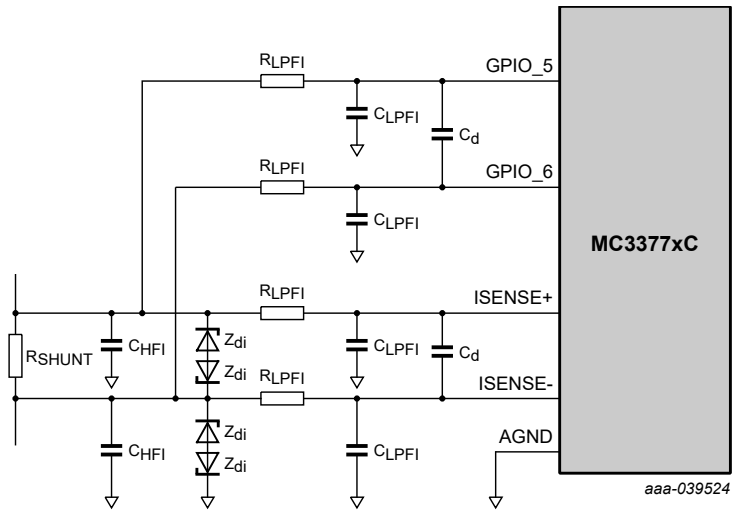


Figure 21. Battery current anti-aliasing filters

5.1 Anti-aliasing filter components selection

Two filters have been put in the current LPF worksheet. Others may be easily got by changing the input values of those columns whose titles are in white color. Very different bandwidths and SM36 detection times are achievable; see Figure 22.

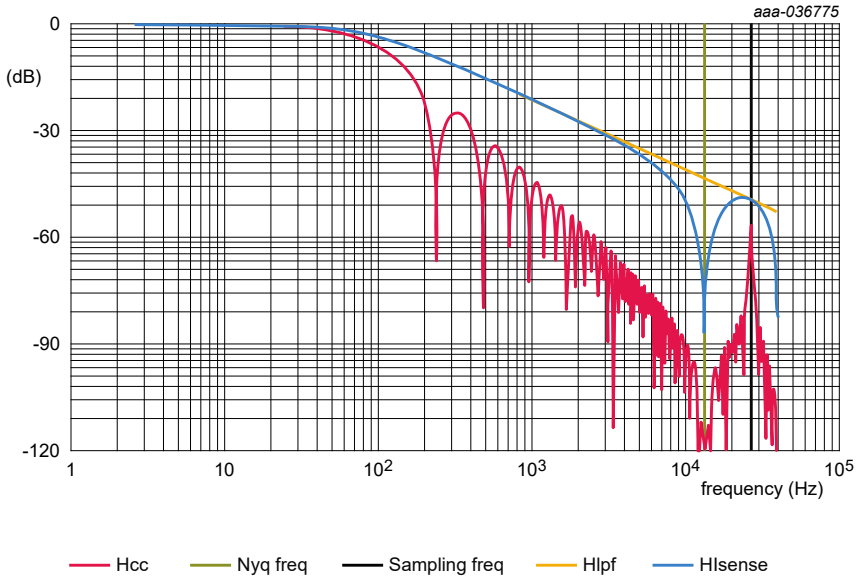
Item	C_{HFI} nF	R_{LPFI} Ω	C_{LPFI} nF	C_d nF	C_{HFI} tolerance	R_{LPFI} tolerance	C_{LPFI} tolerance	C_d tolerance	Analog cutoff frequency Hz	Open detection time ms
ID_01	47	127	47	6800	10.0%	5.0%	10.0%	10.0%	91.8	64.0
ID_02	47	150	47	1000	10.0%	5.0%	10.0%	10.0%	518.3	10.0

aaa-036774

Figure 22. Current signal analog filters

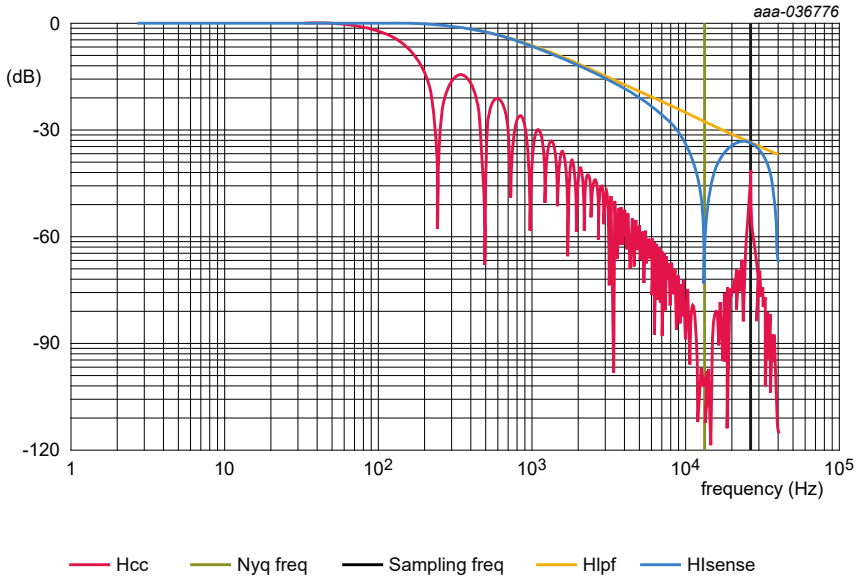
5.2 Digital filter parameter settings

The coulomb current mechanism embedded in the MC3377xC may be used equivalently to a moving average filter. The description may be found in documents [2] and [6], in the coulomb counting section.



average over 110 samples

Figure 23. LPF = ID_01 frequency response of I_{sense} and coulomb count



average over 110 samples

Figure 24. LPF = ID_02 frequency response of I_{sense} and coulomb count

It is worth noting the ≅ 90 Hz bandwidth of the current signal (I_{sense} signal) achieved with LPF = ID_01 can be obtained by using both coulomb counter (CC) and LPF = ID_02, which has ≅ 500 Hz bandwidth. Using the latter LPF gives much better diagnostic readiness but also more aliasing noise.

6 Achievable results and tradeoffs

The comparison of the six strategies as a function of the number of clusters is given below.

Table 5. Summary of the six strategies

Feature		Strategy 1	Strategy 2	Strategy 3	Strategy 4	Strategy 5	Strategy 6
	SM parallelism	no	no	yes	yes	yes	yes
	DMA usage	no	no	no	no	yes	yes
#clusters = 1	measurement period T [ms]	60	30	65	30	55	20
	DTTI [ms]	60	150	65	150	55	100
	communication rate CR [Mbit/s]	0.298	0.165	0.272	0.164	0.321	0.246
	cell balance ratio CBR [%]	54	66	46	64	48	50
#clusters = 8	measurement period T [ms]	70	37	90	40	80	30
	DTTI [ms]	560	1480	90	200	80	150
	CR [Mbit/s]	0.423	0.452	0.898	0.674	1.011	0.899
	CBR [%]	46	52	48	51	42	35
#clusters = 16	measurement period T [ms]	85	47	125	55	115	45
	DTTI [ms]	1360	3760	125	275	115	225
	CR [Mbit/s]	0.507	0.642	1.224	0.948	1.331	1.159
	CBR [%]	38	44	52	42	41	32
#clusters = 32	measurement period T [ms]	100	65	185	87	175	80
	DTTI [ms]	3200	10400	185	435	175	400
	CR [Mbit/s]	0.699	0.877	1.608	1.178	1.699	1.282
	CBR [%]	32	33	53	35	38	34
	Conclusion	- DTTI +CR	- - DTTI +CR	++ DTTI - - T	+ DTTI + T	++ DTTI - - T	+ DTTI ++ T

If the input parameters shown in Figure 12 are different, the numbers in Table 5 would change.

T = time interval for measuring all cells of all nodes. The lower, the better.

DTTI = diagnostic test time interval, that is time to run all SM of all nodes. The lower, the better.

CR = communication rate = (#TX bits + #RX bits)/(cycle time). The lower, the better. Note, the lower the communication rate, the lower the current consumption.

CBR = cell balance ratio = (usable time to balance)/(cycle time). The higher, the better.

-- prefix means significant drawback.

- prefix means drawback.

+ prefix means advantage.

++ prefix means significant advantage.

A few tradeoffs are possible:

- Short T & DTTI (strategies 4, 6) ↔ simplicity (strategies 1, 3)

- Short DTTI (strategies 3, 4, 5, 6) ↔ low CR (strategies 1, 2)

7 Conclusion

Six scheduling strategies, as well as a fully flexible calculation tool, have been presented. The properties of all strategies have been synthetically summarized.

Some possible tradeoffs in terms of working parameters have been highlighted.

The way of parallelizing the main safety mechanisms, namely SM03, SM04, SM05, SM06, SM34, SM36, SM37, SM38, SM39, SM40, as well as the optional SM01, is the same as the one shown for SM02. Details have not been presented in the present document but may be found in the tool itself. Safety mechanisms related to the overcurrent safety goal may need parallelization by the number of current sensors (typically no more than 2) not in terms of the total number of nodes.

The vast influence upon the diagnostic test time interval of analog and digital filter parameters has been highlighted.

8 Abbreviations

Table 6. Abbreviations

Acronym	Description
ADC	analog-to-digital converter
ASIL	Automotive Safety Integrity Level
BCC	battery cell controller
BMS	battery management system
CBR	cell balance ratio
CC	coulomb counter
CR	communication rate
CRC	cyclic redundancy check
DMA	direct memory access
DTTI	diagnostic test time interval
ECC	error correcting code
FDTI	fault detection time interval
FTTI	fault tolerant time interval
LPF	low-pass filter
MA	moving average
MCU	microcontroller unit
OC	overcurrent
OT	overtemperature
OV	overvoltage
PC	pack controller
PCB	printed-circuit board
PGA	programmable gain amplifier
SG	safety goal
SM	safety mechanism
SOC	start of conversion
	state of charge
SOH	state of health
SW	software
TPL	transformer physical layer
UT	undertemperature
UV	undervoltage
VCP	voltage charge pump

9 References

[1] Battery cell controllers page http://www.nxp.com/BATTERY-CELL-CONTROLLERS

[2] MC33771C data sheet; contact your sales representative or FAE

[3] MC33771C safety manual; contact your sales representative or FAE

[4] MC33771C FMEDA report; customizable FMEDA report workbook; contact your sales representative or FAE

[5] MC33771C and MC33772C SM optimization; safety mechanisms scheduling tool; contact your sales representative or FAE

[6] MC33772C data sheet; contact your sales representative or FAE

[7] AN12638; MC33771C and MC33772C functional safety; contact your sales representative or FAE

[8] MC33772C safety manual; contact your sales representative or FAE

[9] MC33772C FMEDA report; customizable FMEDA report workbook; contact your sales representative or FAE

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Figures

Contents

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