AN12840

PCA9450 application note

Rev. 1.0 — 26 June 2020 **Application note**

Document information

Information	Content
Keywords	PCA9450, I.MX 8M, PMIC
Abstract	This application note discusses the critical items needed in designing the PMIC PCA9450 in portable devices with an i.MX 8M application processor. It gives a guideline for component selection, placement, and routing the trace.

Revision history

Rev	Date	Description
v.1.0	20200626	Initial version

1 Introduction

The PCA9450 is a single chip Power Management IC (PMIC) specifically designed to support i.MX 8M family processor in both 1 cell Li-Ion and Li-polymer battery portable application and 5V adapter non-portable applications.

The device provides six high efficiency step-down regulators, five LDOs, one 400 mA load switch, 2-channel level translator and 32.768 kHz crystal oscillator driver. Three buck regulators support dynamic voltage scaling (DVS) feature along with programmable ramping up and down time; the buck regulators support remote sense to compensate IR drop to load. This device is characterized across -40°C to 105°C ambient temperature range.

Six step-down regulators are designed to provide power for i.MX 8M application processor and DRAM memory. Two LDOs (LDO1 and LDO2) feature very low quiescent current to provide power for Secure Non-Volatile Storage (SNVS) since these LDOs are always ON when input voltage is valid.

PCA9450 integrates logic translator which is a 2-bit, dual supply translating transceiver with auto direction sensing. It enables bidirectional voltage level translation. It can be used as I^2C level translator. 400 mA load switch is to supply 3.3 V power supply to SD card, which has internal discharge resistor.

PCA9450 has three versions: PCA9450A is companion PMIC for 845S (i.MX 8M Mini), PCA9450B is companion PMIC for 815S (i.MX 8M Nano) and PCA9450C is companion PMIC for 865S (i.MX 8M Plus).

The PCA9450 is offered in 56-pin HVQFN package, 7 mm x 7 mm, 0.4 mm pitch.

1.1 Features and benefits

- Six high-efficiency step-down regulators
  - Three 3 A buck regulators with DVS feature and remote sense
    - PCA9450A – Three 3 A buck regulators
    - PCA9450B – Two 3 A buck regulators
    - PCA9450C – 6 A dual-phase buck regulator and 3 A buck regulator
- One 3 A buck regulator
- Two 2 A buck regulators
- Five linear regulators
  - Two 10 mA LDOs
  - One 150 mA LDO
  - One 200 mA LDO
  - One 300 mA LDO
- Support various memory types: DDR4/LPDDR4/DDR3L via system UBOOT configuration, no hardware change required
- 400 mA load switch with built-in active discharge resistor
- 32.768 kHz crystal oscillator driver and buffer output
- Two channel logic level translator
- Power control IO
  - Power ON/OFF control
  - Standby/run mode control
- Fm+ 1 MHz I^2C-bus interface
- ESD protection

  - Human Body Model (HBM) : +/- 2000 V
  - Charged Device Model (CDM) : +/-500 V
- 7 mm x 7 mm, 56-pin HVQFN with 0.4 mm pitch

2 Block diagram

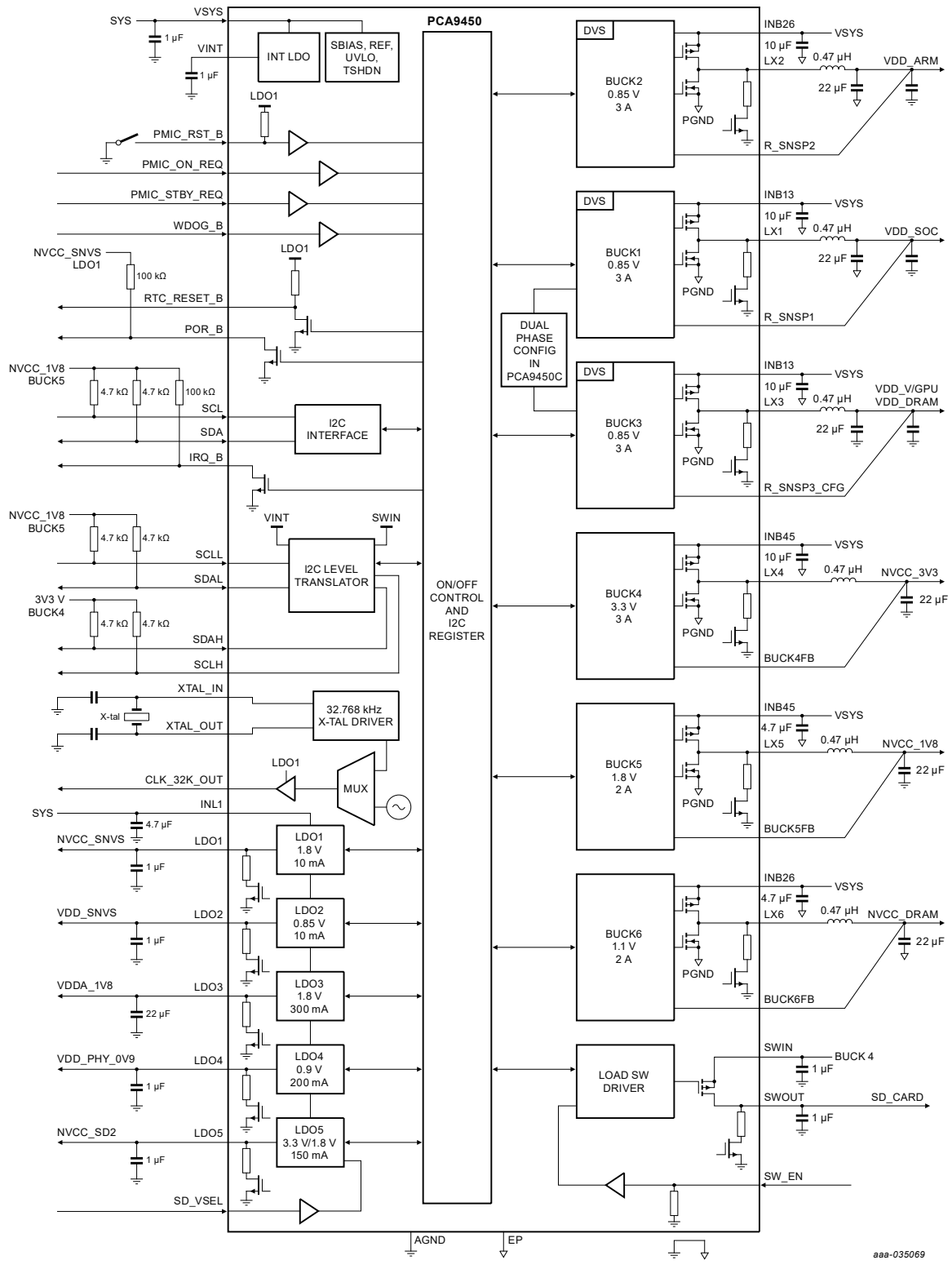


Figure 1. Block diagram

3 Pinning information

3.1 Pinning

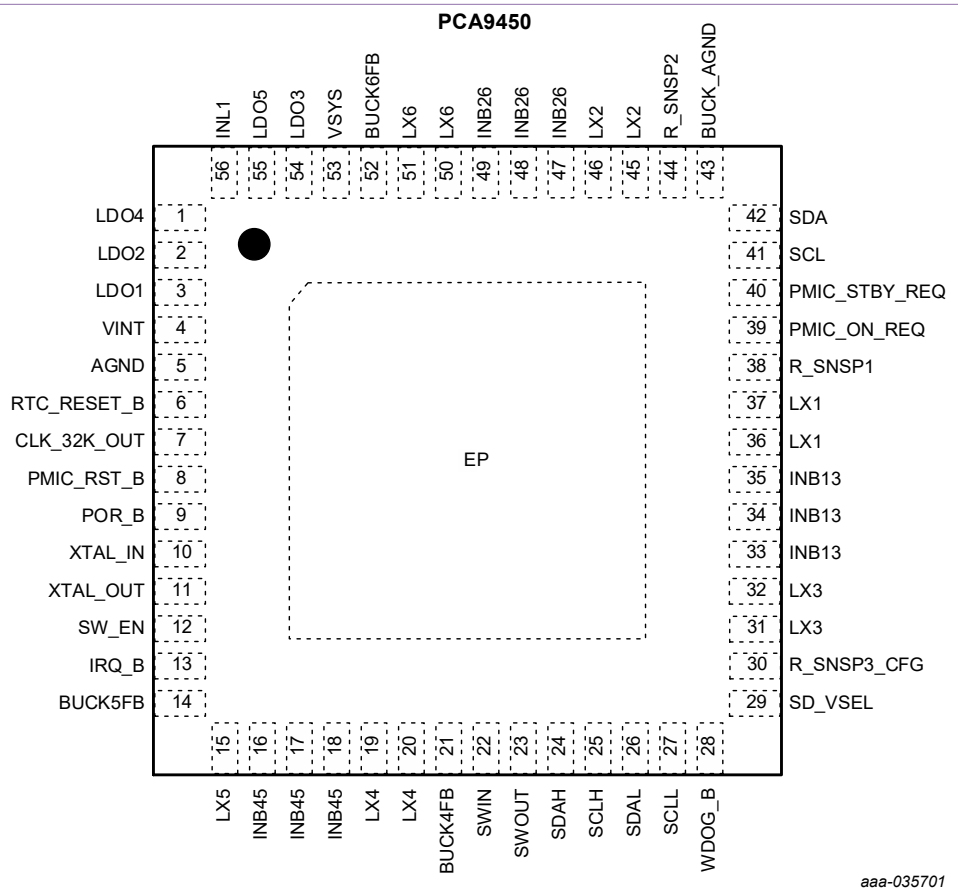


Figure 2. PCA9450 pin map – Top View

3.2 Pin description

Table 1. Pin description

Pin description			
Symbol	**Pin**	**Type**	**Description**
LDO4	1	P	LDO4 output. Bypass with a 1 µF to Ground.
LDO2	2	P	LDO2 output. Bypass with a 1 µF to Ground.
LDO1	3	P	LDO1 output. Bypass with a 1 µF to Ground.
VINT	4	P	Internal Power supply output pin. Bypass with 1 µF to Ground.
AGND	5	GND	Analog ground pin. It should be connected to ground plane through Via. Do not short to EP directly on top layer

Pin description			
Symbol	**Pin**	**Type**	**Description**
RTC_RESET_B	6	DO	Reset output pin. It is High-Z after both LDO1 and LDO2 voltage are good. It is internally pulled up with LDO1 power rail
CLK_32K_OUT	7	DO	32.768 kHz clock CMOS output with LDO1 power rail.
PMIC_RST_B	8	DI	PMIC reset input pin. It is internally pulled up with LDO1 power rail. Once it is asserted low, PMIC performs reset.
POR_B	9	DO	Power On reset output pin. Open drain output requiring external pull up resistor.
XTAL_IN	10	AI	32.768 kHz crystal oscillator input, tie to GND if X-tal is not used
XTAL_OUT	11	AO	32.768 kHz crystal oscillator output, leave floating if X-tal is not used
SW_EN	12	DI	Load switch enable input pin. It has internal 1.5 MΩ pull down resistor.
IRQ_B	13	DO	Open drain output to indicate Interrupt issued. It requires external pull up resistor.
BUCK5FB	14	AI	BUCK5 output voltage sensing pin. If BUCK5 is not used, tie to INB45.
LX5	15	P	BUCK5 switching node. If BUCK5 is not used, leave it floating.
INB45	16,17,18	P	BUCK4 / BUCK5 Input pins. Bypass with 10 µF and 4.7 µF to Ground
LX4	19,20	P	BUCK4 switching node. If BUCK4 is not used, leave them floating.
BUCK4FB	21	AI	BUCK4 output voltage sensing pin. If BUCK4 is not used, tie to INB45.
SWIN	22	P	Load switch input pin, Bypass with a 1 µF to Ground. Leave it floating if not used.
SWOUT	23	P	Load switch output pin, Bypass with a 1 µF to Ground. Leave it floating if not used.
SDAH	24	DIO	Level translator high voltage IO pin, SDA referenced to SWIN, 3.3 V
SCLH	25	DO	Level translator high voltage IO pin, SCL referenced to SWIN, 3.3 V
SDAL	26	DIO	Level translator low voltage IO pin, SDA referenced to VINT, 1.8 V
SCLL	27	DO	Level translator low voltage IO pin, SCL referenced to VINT, 1.8 V
WDOG_B	28	DI	Active low watchdog reset input pin from application processor.
SD_VSEL	29	DI	LDO5 voltage selection input pin. LDO5 output is 3.3 V when it is driven low and 1.8 V when driven high. VSEL pin should be tied low or high. Do not leave it floating.

Pin description			
Symbol	**Pin**	**Type**	**Description**
R_SNSP3_CFG	30	AI	BUCK3 output voltage remote sense pin in PCA9450A. Logic input pin in PCA9450B/C. This pin should be tied to SYS in PCA9450B, where BUCK3 is disabled. This pin is tied to GND in PCA9450C, where BUCK1 and BUCK3 are configured as dual phase buck regulator.
LX3	31,32	P	BUCK3 switching node If BUCK3 is not used by shorting R_SNSP3_CFG to VSYS, leave LX3 pins floating.
INB13	33,34,35	P	BUCK1 / BUCK3 Input. Bypass with two 10 µF to Ground
LX1	36,37	P	BUCK1 switching node. Leave it floating if not used.
R_SNSP1	38	AI	BUCK1 output voltage remote sensing pin. Tie to INB13 if not used.
PMIC_ON_REQ	39	DI	PMIC ON input from Application processor. When it is asserted high, the device starts power on sequence.
PMIC_STBY_REQ	40	DI	Standby mode input from Application processor. When it is asserted high, device enters STANDBY mode.
SCL	41	DI	I2C serial clock pin
SDA	42	DIO	I2C serial data pin
BUCK_AGND	43	GND	Buck reference GND for BUCK1,2,3. It should be connected to ground plane through Via. Do not short to EP directly on top layer
R_SNSP2	44	AI	BUCK2 output voltage remote sensing pin. Tie to INB26 if not used.
LX2	45,46	P	BUCK2 switching node. Leave them floating if not used.
INB26	47,48,49	P	BUCK2 / BUCK6 Input. Bypass with 10 µF and 4.7 µF to Ground
LX6	50,51	P	BUCK6 switching node. Leave it floating if not used.
BUCK6FB	52	AI	BUCK6 output voltage sensing pin. Tie to INB26 if not used.
VSYS	53	P	Internal power input. Bypass with a 1 µF to Ground
LDO3	54	P	LDO3 output. Bypass with a 2.2 µF to Ground.
LDO5	55	P	LDO5 output. Bypass with a 1 µF to Ground.
INL1	56	P	Power input pin for LDO1, LDO2, LDO3, LDO4 and LDO5. Bypass with a 4.7 µF to Ground.
EP		GND	Exposed PAD. All buck PGNDs are internally connected.

4 PCA9450 Selection Guide

Table 2. PCA9450 selection guide

Part number	AP Platform	Buck1	Buck3	LDO4	R_SNSP3_CFG
PCA9450A	i.MX 8M Mini (845S)	3A for SOC (ON by default)	3A for VPU/ GPU/DRAM (ON by default)	0.9V for VDDA (ON by default)	R_SNSP3_CFG is feedback of BUCK 3
PCA9450B	i.MX 8M Nano (815S)	3A for SOC / VPU/GPU/DRAM (ON by default)	Disabled	OFF by default	R_SNSP3_CFG = VSYS
PCA9450C	i.MX 8M Plus (865S)	6A Dual phase for SOC/VPU/GPU/DRAM (ON by default)		OFF by default	R_SNSP3_CFG = GND

5 Application design-in information

5.1 Reference schematic

5.1.1 PCA9450A reference schematic

PCA9450A reference schematic with i.MX 8M Mini is illustrated in Figure 3.

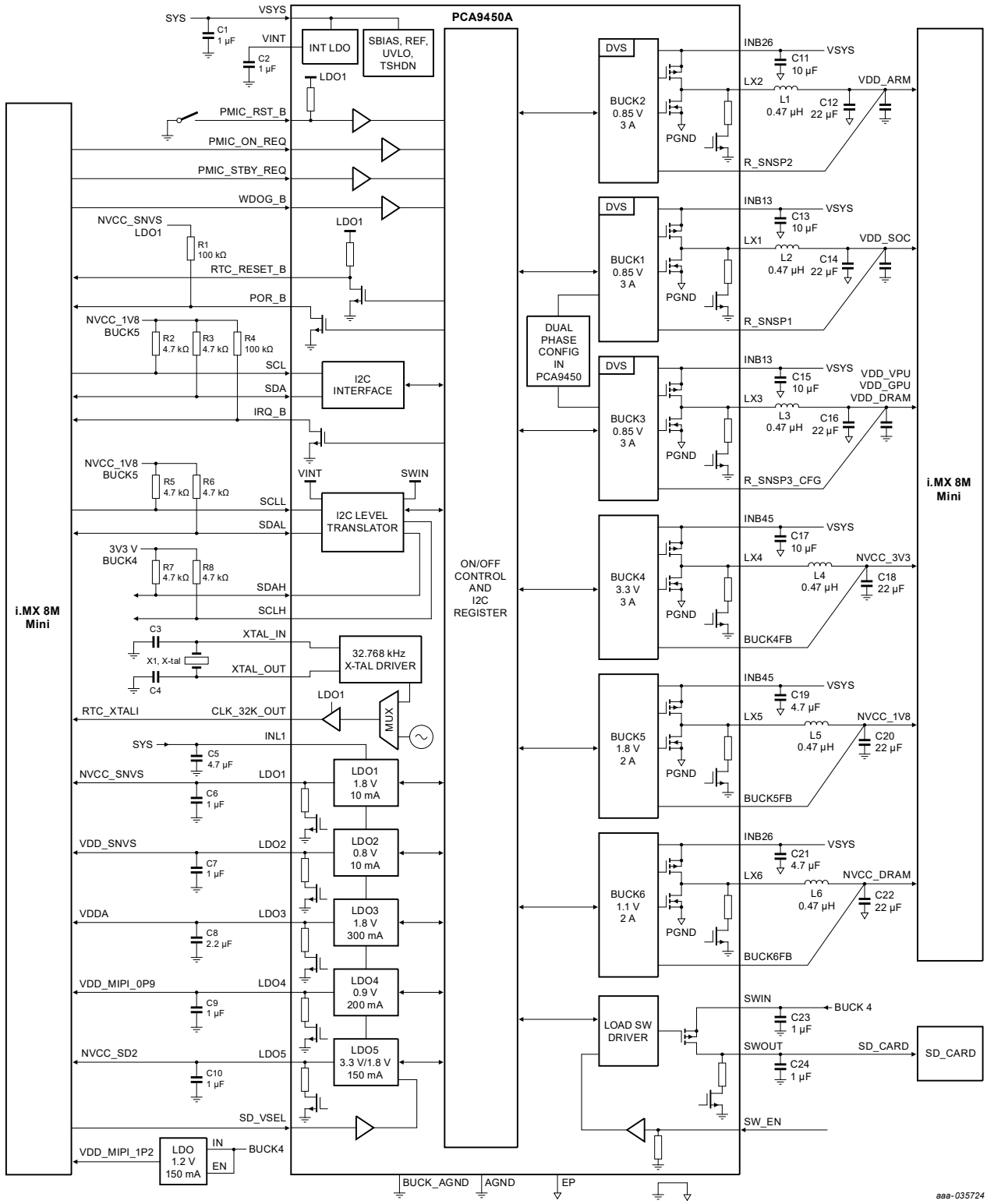


Figure 3. PCA9450A application schematic

5.1.2 PCA9450B reference schematic

PCA9450B reference schematic with i.MX 8M Nano is illustrated in Figure 4.

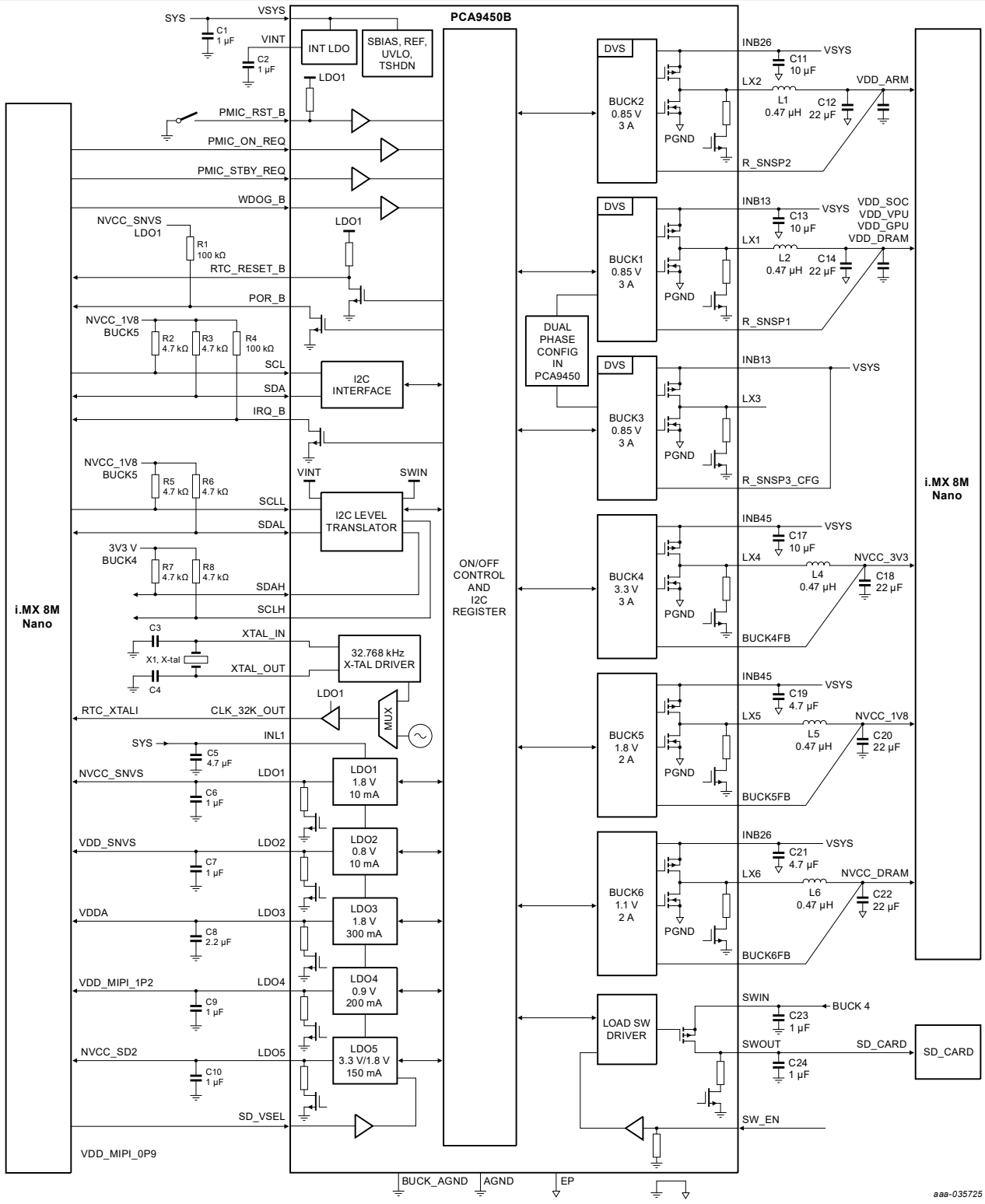


Figure 4. PCA9450B application schematic

5.1.3 PCA9450C reference schematic

PCA9450C reference schematic with i.MX 8M Plus is illustrated in Figure 5

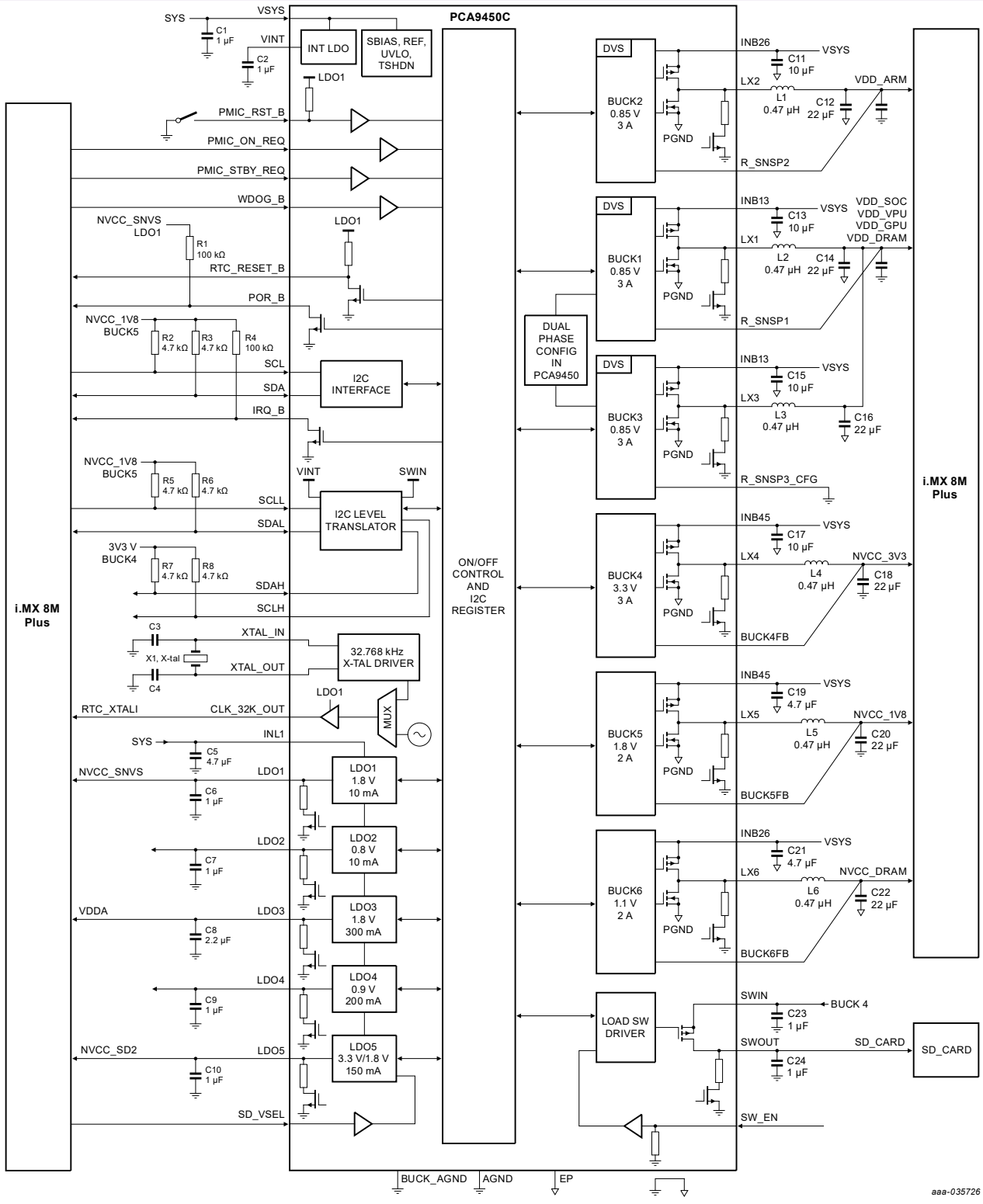


Figure 5. PCA9450C application schematic

5.2 Typical application

The PCA9450 devices have only a few design requirements. Use the following parameters for the design.

- 1 µF bypass capacitor on VINT and VSYS, located as close as possible to those pins to ground
- Input capacitors must be present on the INB and INL supplies if used
- Output inductors and capacitors must be used on the outputs of the BUCK converters if used
- Output capacitors must be used on the outputs of the LDOs

5.2.1 Inductor selection for buck converters

Each of the converters in the PCA9450 typically use a 0.47 µH output inductor which has to be rated for its DC resistance and saturation current. The DC resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest DC resistance must be selected for highest efficiency.

Equation 1 calculates the maximum inductor current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current as calculated with Equation 2. This is needed because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vinmax}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{out.max} + \frac{\Delta I_L}{2} \quad (2)$$

Where:

- f = switching frequency (2 MHz)
- L = Inductance
- ΔI_L = Peak to peak inductor ripple current
- $I_{L.max}$ = Maximum inductor current

A conservative approach is to select the inductor current rating just for the maximum switch current of the PCA9450.

Table 3 shows possible inductors list.

Table 3. Tested inductor list

Buck	Vendor	Part number	Size	DCR [mΩ]	Isat [A]	Itemp [A]
BUCK1, BUCK2, BUCK3, BUCK4	Sunlord	WPN252012HR47MT	2520	29	5.6	4.0
	Murata	1239AS-H-R47M	2520	39	3.8	3.7
BUCK5, BUCK6	Sunlord	WPN201610UR47MT	2016	28	5.0	4.1
	Murata	1286AS-H-R47M	2016	52	3.4	3.2

5.2.2 Output capacitor selection for buck converters

The fast response adaptive constant ON time control scheme of the buck converters implemented in the PCA9450 allows the use of small ceramic capacitors with a typical value of 22 µF for each converter without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended. See Table 4 for recommended list of capacitors.

Table 4. Recommended list of capacitors

BUCK	Vendor	Part number	Capacitor value	Size	Voltage
BUCK1, BUCK2, BUCK3, BUCK4, BUCK5, BUCK6	TDK	C1608X5R1A226M080AC	22 µF	CC0603	10 V
BUCK1, BUCK2, BUCK3, BUCK4, BUCK5, BUCK6	TDK	C1608JB1A226M080AC	22 µF	CC0603	10 V

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. Just for completeness, the RMS ripple current is calculated in Equation 3.

$$I_{RMS.COUT} = \text{Vout} \times \frac{1-\frac{\text{Vout}}{\text{Vin}}}{\text{L} \times \text{f}} \times \frac{1}{2\sqrt{3}} \quad (3)$$

At nominal load current, the inductive converters operate in PWM mode. The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta\,\text{Vout} = \text{Vout} \times \frac{1-\frac{Vout}{Vin}}{\text{L} \times \text{f}} \times \left(\frac{1}{8 \times Cout \times f} + ESR\right) \quad (4)$$

Where:

- The highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents, the converters operate in PFM mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1 % of the nominal output voltage.

5.2.3 Input capacitor selection for buck converters

Low ESR input capacitor is highly recommended for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes because of the nature of buck converter. Each DC-DC converter requires a 10µF ceramic input capacitor on its input pins. The input capacitor could be increased without any limit for better input voltage filtering.

6 Layout guide

6.1 Placement

Layout guide is shown in Figure 6.

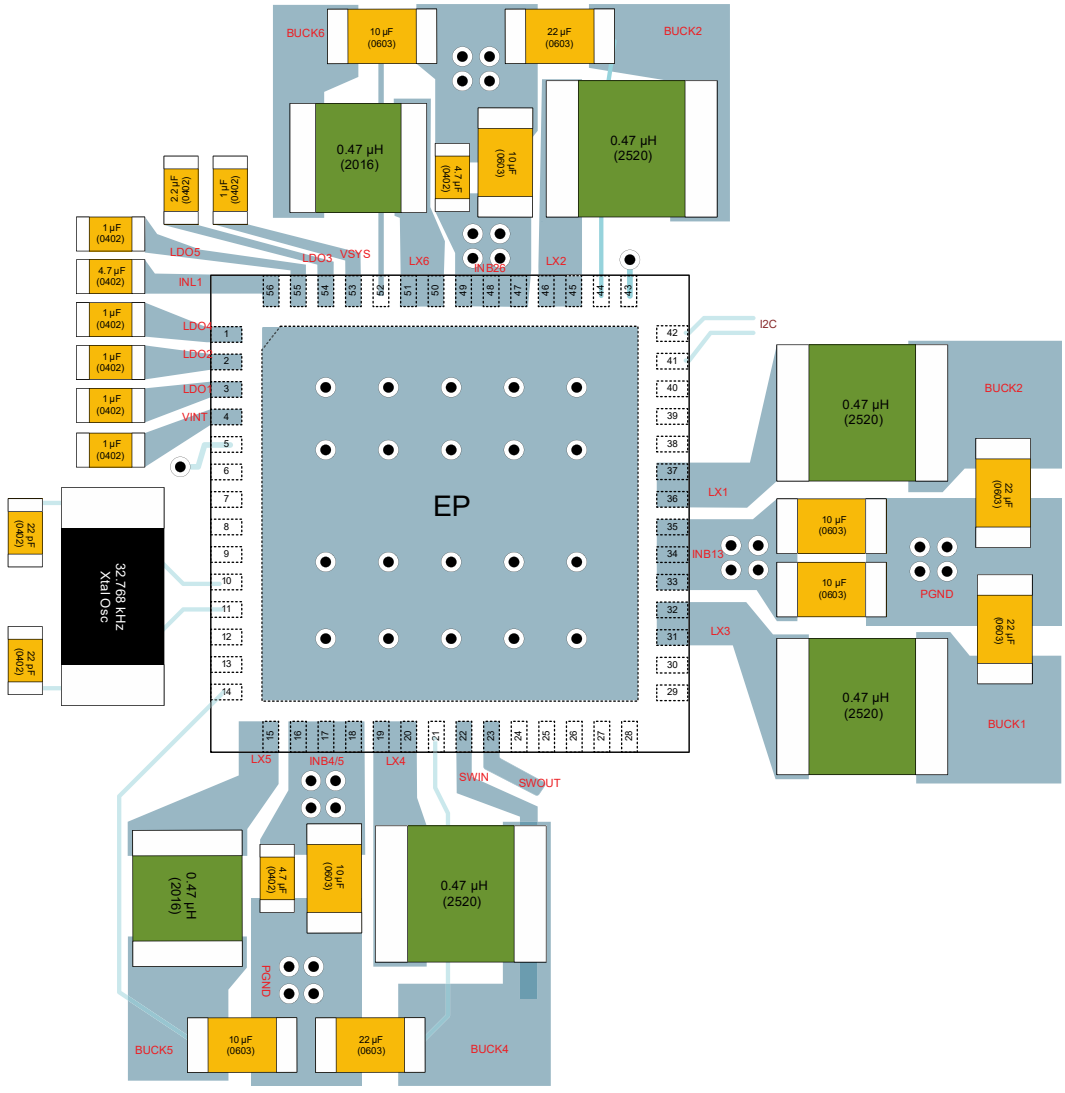


Figure 6. PCA9450 layout

6.2 Buck layout

6.2.1 Schematic

Figure 7 shows the critical path in buck converter which has high di/dt.

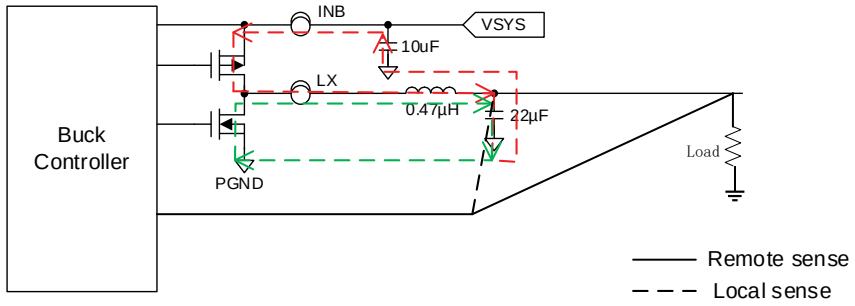


Figure 7. Buck schematic

The biggest challenge in buck layout is EMI. To minimize the EMI requires the minimum loop area of two high di/dt path as shown in Figure 7. The area in red is input power charging the inductor when high side FET is on; the area in green is inductor discharge energy to output capacitor (load) when low side FET is on.

6.2.2 Layout

Put the input/output capacitor and inductor as close to chip as possible to minimize the loop area. If using the high frequency bypass capacitor to filter the EMI, make sure this high frequency capacitor is close to the chip.

Use the shortest path to route the trace including the return path (ground). Make sure the trace is capable of handling the maximum current in the application. Maximum current on Lx pin to inductor is around 1.4 times maximum loading current by quick estimation.

Keep enough vias to connect the ground pad to main ground; this not only reduces the parasitic inductance but also helps with heat dissipation.

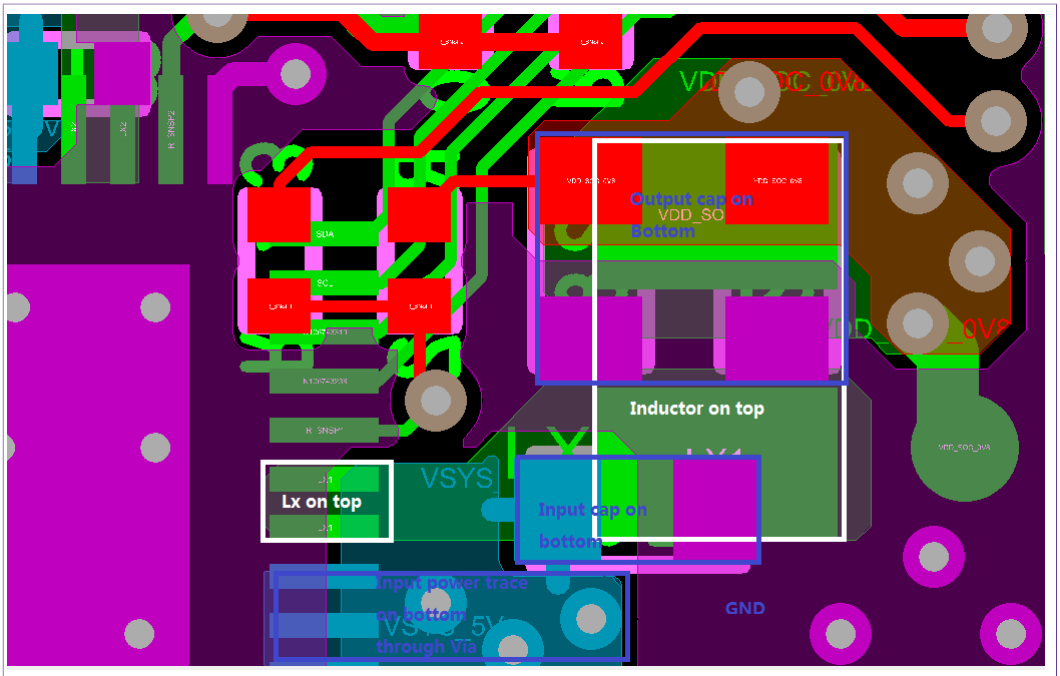


Figure 8. Buck layout example

6.2.3 Local sense and remote sense

All six bucks of PCA9450 have sense feedback. Bucks 1, 2, and 3 are remote sense; Bucks 4, 5, and 6 are local sense. The difference between local and remote sense in application is that local sense senses the voltage on buck output capacitor, and remote sense senses the voltage on load (application processor) power pin.

As sense pin doesn't carry current but only senses the voltage, 5 mils wide trace is good enough. Buck controller fine tunes the output voltage according to the voltage sensed, and it is very noise sensitive. It requires noise source far away from the sense trace.

6.2.4 Dual phase buck

PCA9450C buck 1 and buck 3 can be configured as dual phase buck by connecting R_SNSP3_CFG pin to ground. In order to balance the current on two traces, the routing on LX1 to inductor to load and LX3 to inductor to load needs be as symmetrical as possible.

6.3 LDO

PCA9450 integrates five LDOs with different output current capability for different purposes. The output capacitor needs to be as close as possible to the chip. Make sure the trace is wide enough to carry the maximum current in the application.

6.4 GND

The exposed pad (EP) is the power ground of all bucks which is relatively noisy. AGND is the analog ground. **Do not connect AGND to EP on the top layer!** Connect AGND to main ground by via.

Avoid separating the main ground under PCA9450 which may increase the return path. Make sure there are enough vias to connect EP to system main ground.

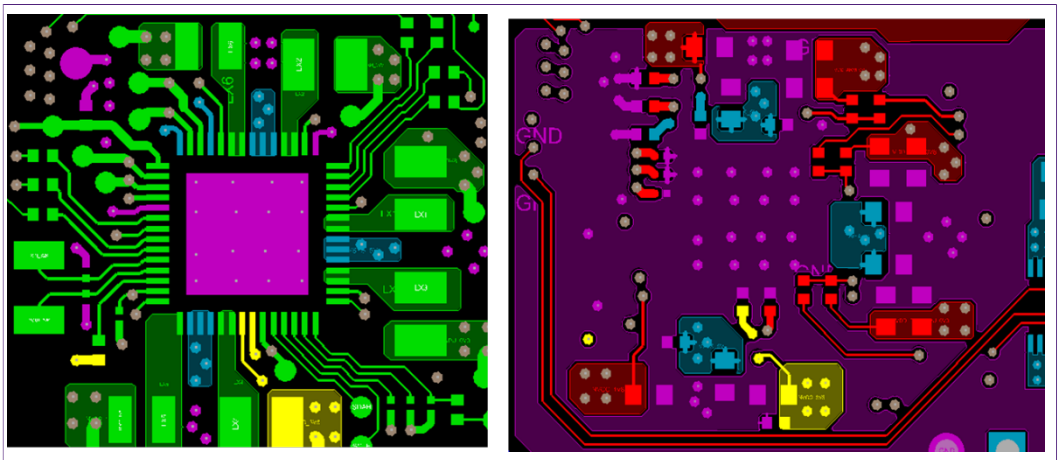
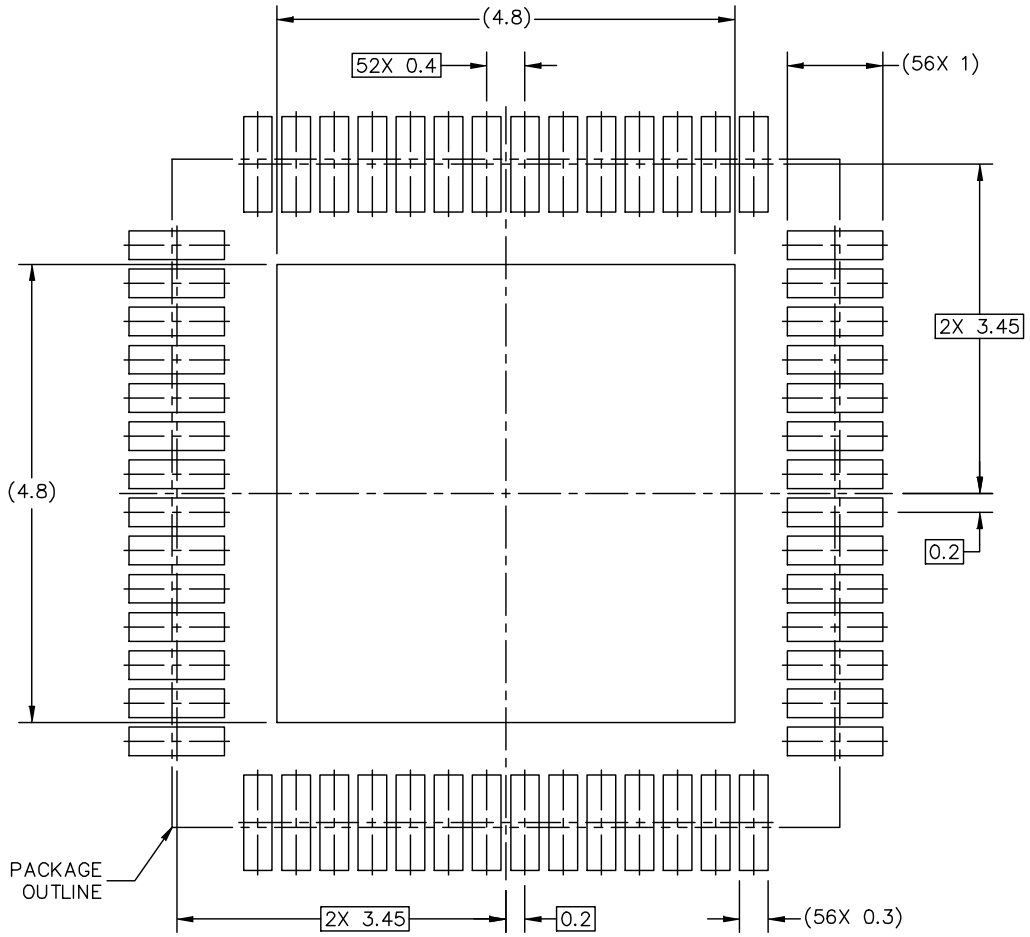


Figure 9. GND layout example

7 PCB design guidelines



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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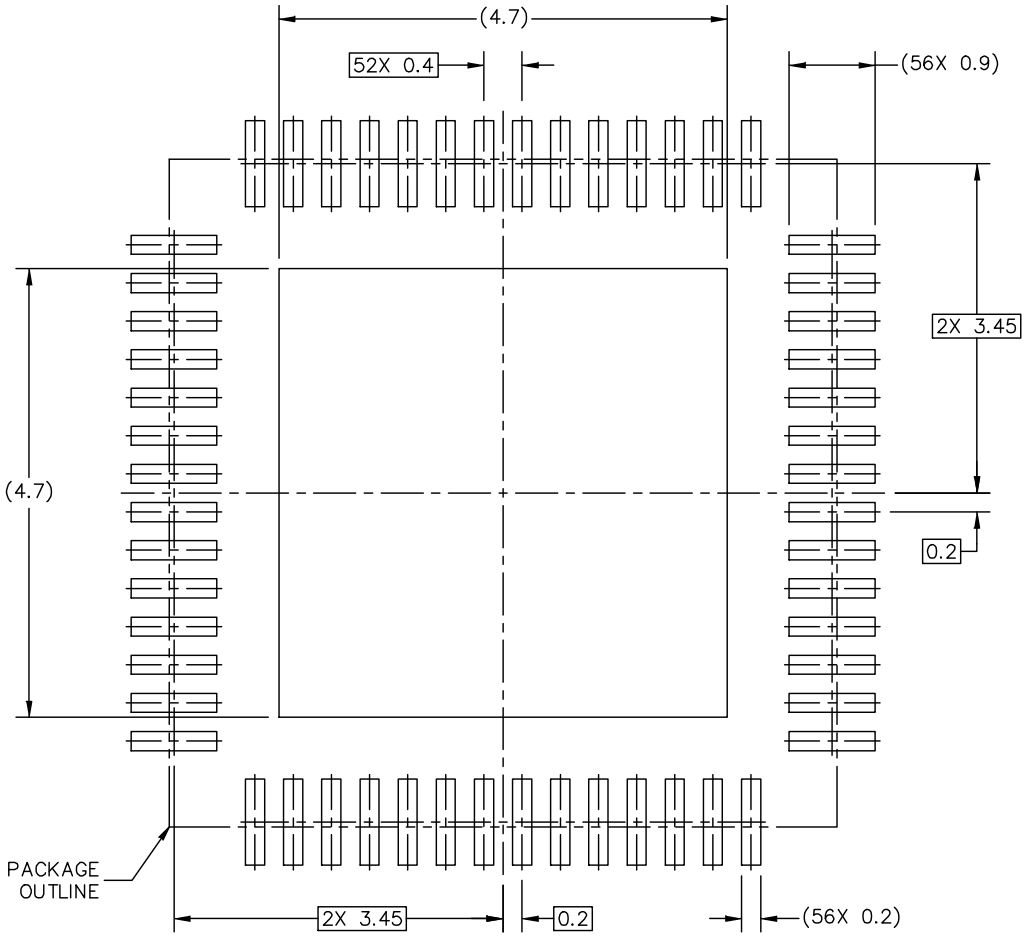
DATE: 01 MAR 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01369D	REVISION: A	

Figure 10. PCB Design Guidelines – Solder Mask Opening Pattern



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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Figure 11. PCB Design Guidelines - I/O PADS AND SODERABLE AREA

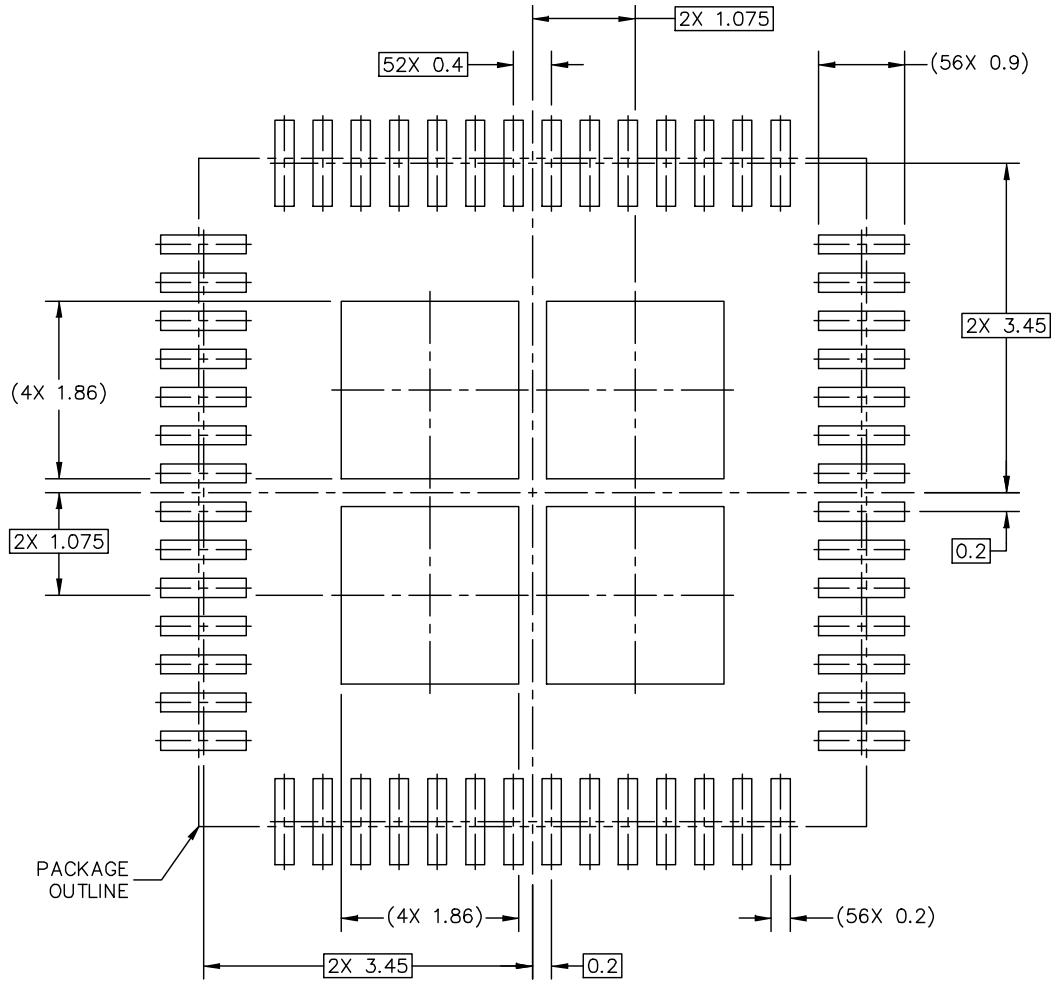

Figure 12. PCB Design Guidelines – Solder Paste Stencil

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