AN12864

PCB design and layout guidelines for CBTU02044

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Document information

Information	Content
Keywords	high-speed signal, PCB, layout, loss, jitter
Abstract	This document provides a practical guideline for PCB design and layout in CBTU02044 applications

Revision history

Rev	Date	Description
v.1.0	20200521	Initial version

1 Introduction

CBTU02044 is a high-speed 2-differential channels, 1-to-2 switching chip optimized to interface with PCIe Gen4 for server and client applications. This high performance switch chip could be used for other high-speed interfaces such as MIPI, DisplayPort1.4, and DDR.

CBTU02044 offers numerous benefits, such as a wide VDD range (1.62 V to 3.63 V), low insertion loss, low crosstalk, low return loss, and a 17GHz typical -3dB bandwidth.

CBTU02044 is a small package with optimized footprint for smaller real estate occupancy.

This document provides PCB design guidelines and considerations while using CBTU02044.

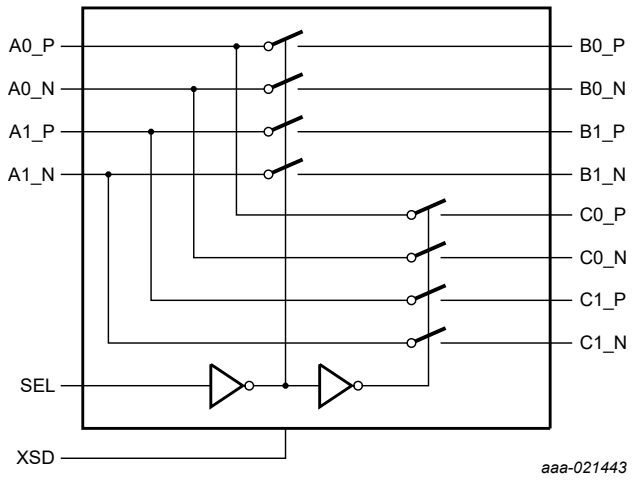

Figure 1. CBTU02044 functional block diagram

2 AC coupling and DC bias

PCIe, DP and other high-speed serial signals require AC coupling between the transmitter and receiver. The AC coupling capacitors are usually placed close to the transmitter.

CBTU02044 requires a bias voltage, less than 2 V or VDD, whichever is lower, applied to its switches.

The following figures illustrate several AC coupling capacitor placement options.

In Figure 2, the capacitors are placed between the MUX and the downstream controller, and the MUX is biased by the upstream controller.

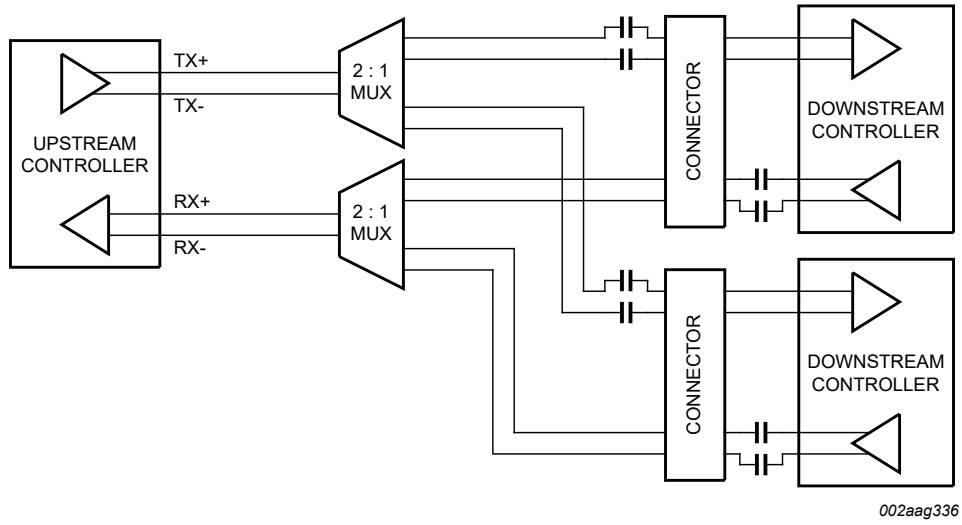

Figure 2. The capacitors are placed between MUX and downstream controller

In Figure 3, the capacitors are placed between the upstream transmitter and the MUX. RX signals on the motherboard sides usually do not require AC coupling capacitors since those capacitors are located on the add-in card. The TX MUX is biased by the downstream controller, and the RX MUX is biased by the upstream controller.

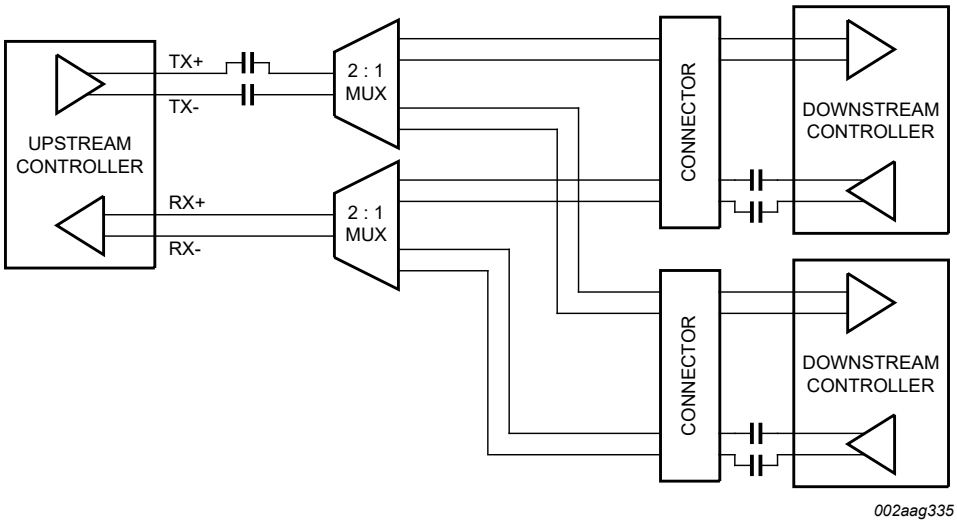

Figure 3. The capacitor is located in between upstream TX and MUX

Remark: Do not place capacitors at both side of MUX, unless a bias voltage is provided.

A bias voltage less than 2 V or VDD, whichever is lower, is needed for CBTU02044 if both upstream and downstream controllers' common-mode voltage is higher than 2 V or VDD, whichever is lower. Figure 4 shows an implementation in this case.

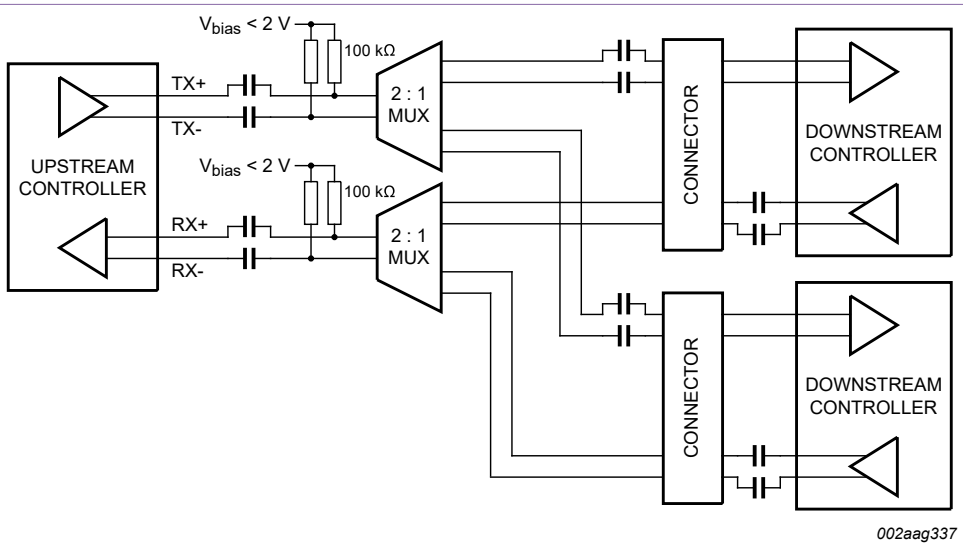

Figure 4. A bias voltage is applied to CBTU02044 MUX

3 PCB layout guidelines

3.1 Traces

3.1.1 Impedance

To minimize loss and jitter, the most important considerations are to design the PCB to a target impedance and to keep tolerances small. PCIe, and other high-speed serial link traces need to maintain 100 Ω differential / 50 Ω singled-ended impedance.

3.1.2 Width and spacing

The coupling of the intra-pair differential signals and increased spacing to neighboring signals help to minimize harmful crosstalk impacts and ElectroMagnetic Interference (EMI) effects. The differential trace width and air gap spacing between the two traces of the pair need to be elected to achieve the impedance target.

The spacing between pairs and to all non-PCIe signals should be at least four times the dielectric height. If the non-PCIe signals have significantly higher voltage levels or edge rate than the PCIe signal, the space should increase to ever further in order to avoid cross coupling.

3.1.3 Length and length matching

Trace length greatly affects the loss and jitter budgets of the interconnection. The PCB trace may introduce 1 ps to 5 ps of jitter and 1.0 dB to 1.2 dB of loss per inch (2.54 cm) at PCIe Gen4 speed.

CBTU02044 also brings in extra insertion loss to the system. CBTU02044 has -1.5 dB loss at 8 GHz, which is equivalent to about 1.5 inch (3.81 cm) PCB loss. The system designers need to take this MUX insertion loss into account when planning the system loss budget.

Long distance traces should be routed at an off-angle to the X-Y axis of a PCB layer, in order to distribute the effects of fiberglass bundle weaves and resin-rich areas of the dielectric.

The two traces of a pair should be symmetrically routed, and trace length needs to match. Any asymmetric or mismatch will cause common mode distortion.

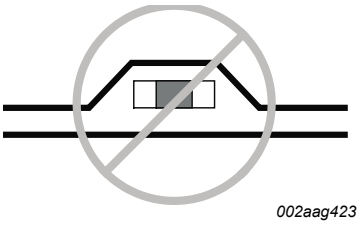

Figure 5. Non-symmetrical routing should be avoided

The length mismatching between a differential pair should be limited to 5 mils (0.127 mm) maximum. Length matching is required per segment, and any length added (typically a

'serpentine' section) for the sake of matching a pair should be added near the location where the mismatch occurs.

The length matching between TX pair and RX pair is not required.

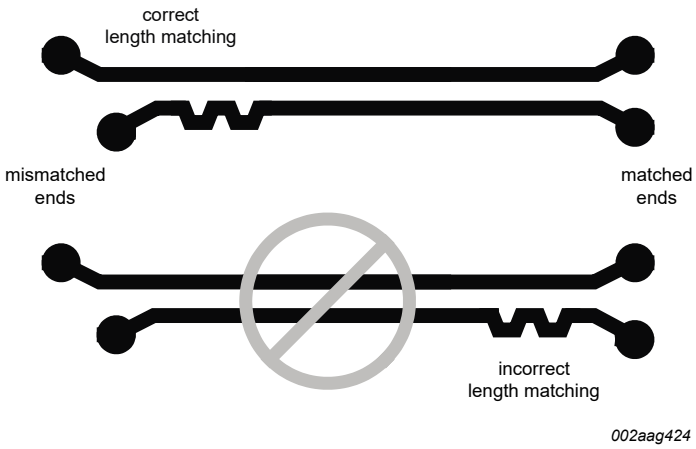

Figure 6. Length matching near location of mismatch

3.2 Test points, vias and pads

Signal vias affect the overall loss and jitter budgets. Each via pair may contribute 0.25 dB of loss in some corner cases. Vias may limit the achievable maximum routing length.

A maximum of two via pairs can be used on a differential pair. Vias should have a pad size of 25 mils (0.635 mm) or less, and a finished hole size of 14 mils (0.356 mm) or less. Two vias must be placed as a symmetric pair in the same location.

Test points and probe pads should be placed symmetrically in series. Stubs should not be introduced on differential pairs. Refer to Figure 7 for illustrations of correct and incorrect placements.

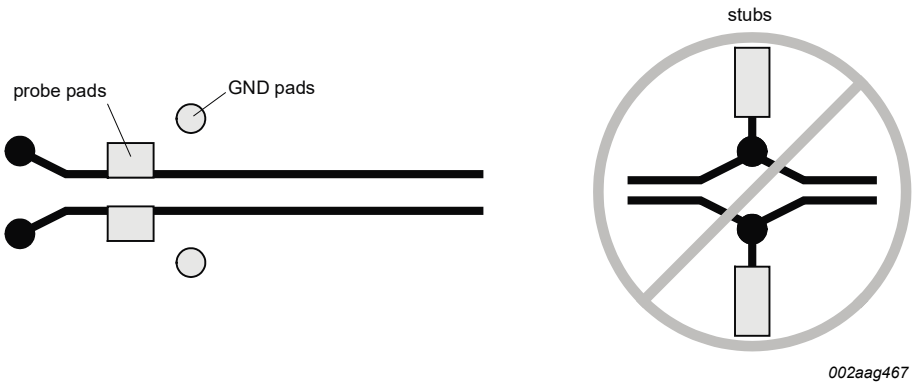

Figure 7. Test points and probe pads

3.3 AC coupling capacitors

PCIe, DP and other high-speed serial signals require AC coupling between transmitter and receiver. The AC coupling capacitors for both differential pair signals must be the

same value, same package size, and have symmetric placement. If possible, TX traces should route on the top layer.

The 0402 or smaller package size is preferred, and 0603 is acceptable. C-pack is not allowed. The breakout into and out of capacitors should be symmetrical for both signal lines in a differential pair. The trace separation for routing to pads must be minimized in order to optimize tight coupling between the signal pairs.

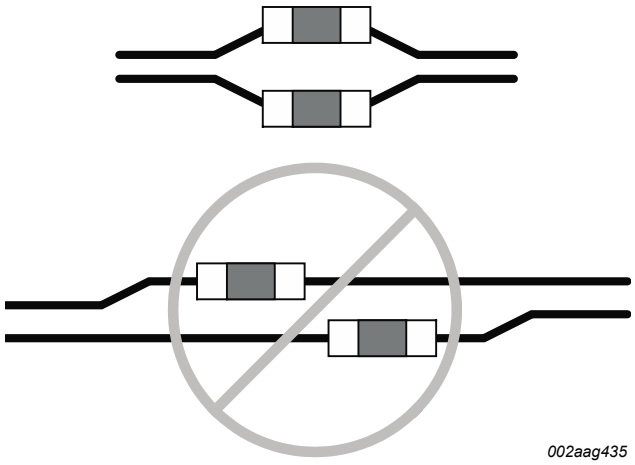

Figure 8. Placement of AC coupling capacitors

3.4 Reference plane

The high-speed differential signals should be referenced to the ground plane. Any discontinuities in the reference plane, such as splits and voids, should be avoided. Never route a trace so that it straddles a plane split.

If it is necessary to change reference to power plane, capacitors with low ESR values should be placed at locations where the PCIe signals are changing layers, and between power and ground planes to minimize the negative impact of EMI and signal integrity performance caused by reference plane changing.

When a signal changes layers, the ground stitching vias should be placed close to the signal vias to provide a current return path. A minimum of 1 to 3 stitching vias per pair of signals is recommended.

Do not route high-speed traces under power connectors, other interface connectors, crystals, oscillators, clock synthesizers, or magnetic devices that use and/or duplicate clocks.

4 Summary

NXP's CBTU02044 is a high bandwidth multiplexer/de-multiplexer specially designed for switching the high-speed serial interface signals, such as PCIe Gen4, DisplayPort 1.4, MIPI, and DDR. The high data rate requires some specific implementations in the PCB design. The following is the summary of guideline:

- Maintains 50 Ω ± 15 % single-ended and 100 Ω ± 20 % differential impedance.
- The differential pair must be routed symmetrically. The length mismatching within the differential pair should be less than 5 mils (0.127 mm).
- Do not route high speed signals over any plane split; avoid any discontinuities in the reference plane.
- Avoid any discontinuity for signal integrity. Differential pairs should be routed on the same layer. The number of vias on the differential traces should be minimized. Test points should be placed in series and symmetrically. Stubs should not be introduced on the differential pairs.
- PCB design should account for the insertion loss by the multiplexer, and plan the total trace length accordingly.
- Implement AC coupling capacitors for high-speed link, and provide bias voltage, less than 2 V or VDD, whichever is lower, to the MUX.

5 Abbreviations

Table 1. Abbreviations

Acronym	Description
DP	DisplayPort
EMI	ElectroMagnetic Interference
ESR	Equivalent Series Resistance
MUX	multiplexer
PCB	Printed-Circuit Board
PCIe	PCI Express
PCI	Peripheral Component Interconnect
RX	Receive
TX	Transmit

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