AN12950

Optimizing Serial Interface Equalization Settings for 25 GbE on LX216xA Processor

Rev. 1 — 12/2020 Application Note

Contents

1 Introduction

The QorIQ® LX216xA product family supports a variety of Ethernet speeds and interfaces. Serial and parallel interface selections are determined by the reset configuration word (RCW). This application note focuses on the three serial Ethernet point-to-point protocols supported by a single or multiple 25.78125 Gbit/s SerDes lanes. The LX216xA supports 25 GbE, 50 GbE, and 100 GbE. These protocols utilize 64b/66b line coding as defined in *IEEE 802.3-2018, Clause 107* [1]. The LX216xA also adheres to the electrical specifications for 25GAUI, 50GAUI-2, and CAUI-4.

Careful consideration should go into the design of an Ethernet high-speed serial interface based system. The transmit and receive IBIS-AMI models in conjunction with the board's channel characteristics help to meet the channel operating margin (COM), as defined in *IEEE 802.3-2018, Annex 93A* [1].

This document is intended to serve as a guide to help users configure SerDes equalization settings that are optimal for 25 GbE, 50 GbE, and 100 GbE protocols with an emphasis on tuning transmit equalization parameters. An overview of CAUI-4 is discussed because it serves as a superset for the two-lane implementation for 50 GbE and the single-lane implementation for 25 GbE. CAUI-4 chip-to-chip (C2C) and CAUI-4 chip-to-module (C2M) electrical interfaces are also discussed. I/O Buffer Information Specification Algorithmic Modeling Interface (IBIS-AMI) simulations are key to understanding the channel response to factors, such as interconnects, vias, PCB trace materials and lengths, and others. Forward error correction (FEC) details are beyond the scope of this document but mentioned because LX216xA supports two implementations of FEC. LX216xA Repeater Mode and the QorIQ Configuration and Validation Suite (QCVS) are included because they serve as useful debugging aids. You are recommended to obtain a copy of *IEEE 802.3-2018* [1] to easily follow its references made within this document.

In addition, this document assumes that the reader understands how to perform reads and writes to memory-mapped registers and internal MII management registers within the LX216xA.

NOTE

- The supplied SerDes differential reference clock must be 161.1328125 MHz
- Spread-spectrum clocking is not supported for Ethernet related serial protocols
- Only MACs 3, 4, 5, 6, 9, and 10 support 25 GbE. Only MACs 1 and 2 support 50 GbE and 100 GbE.
- MAC offsets used in this document are only an example. See the reference manuals for the MAC offsets associated with the SerDes protocols selected in the design.

1.1 CAUI-4 overview

The 100 Gigabit Attachment Unit Interface (CAUI-4) operates utilizing 4 x 25.78125 Gbit/s links.

NOTE

The Roman numeral for 100 is **C**.

1.1.1 CAUI-4 C2C channel insertion loss

The channel operating margin (COM) for CAUI-4 chip-to-chip (C2C) is defined in *IEEE 802.3-2018, Annex 83D.4* [1]. The informative CAUI-4 C2C insertion loss equation is shown in Equation 83D-1 of *IEEE 802.3-2018, Annex 83D* [1]. Based on the equation, the channel insertion loss is 20 dB at the fundamental frequency of 12.89 GHz.

The CAUI-4 C2C channel insertion loss graph is shown in Figure 83D-3 of *IEEE 802.3-2018, Annex 83D* [1].

1.1.2 CAUI-4 C2M channel insertion loss

The CAUI-4 chip-to-module (C2M) electrical characteristics are defined in *IEEE 802.3 Annex 83E.3* [1]. The electrical characteristics specify the amount of loss for the transmit side of the connector, the connector, and the receive side of the connector.

The informative CAUI-4 C2M insertion loss equation is shown in Equation 83E-1 of *IEEE 802.3-2018, Annex 83E-1* [1]. The CAUI-4 C2M channel insertion loss graph is shown in Figure 83E-3 of *IEEE 802.3-2018, Annex 83E-3* [1].

1.2 Receive equalization

The continuous time linear equalization (CTLE) function on the LX216xA receiver is adaptive and is enabled by default.

See Adaptive receive equalization to see the available options for applying the recommended optimal settings for the SerDes receiver for 25 GbE operation.

1.3 Transmit equalization

For CAUI-4, the LX216xA SerDes transmitter implements a 3-tap feed forward equalization (FFE) circuit to compensate for the frequency-dependent loss of the channel and to facilitate data recovery at the receiver. The pre-cursor c(-1), main cursor c(0), and post-cursor c(1) are available to help shape the data stream. A functional model of a 3-tap transmit equalizer can be found in Figure 83D-4 of *IEEE 802.3-2018* [1].

To explain the pre-cursor and post-cursor, take as an example a single pulse (1 bit) that is sent through a lossy channel. This bit is called the main cursor. As the bit traverses the channel, it develops "tails" on either side of the received pulse. The losses in the interconnects spread the energy into the subsequent bit time, for example, post-cursor. Some of the energy can spread into the previous bit time, for example, pre-cursor. In a stream of many pulses, these tails start to affect the bits on either side of the main cursor, making it difficult or impossible for the receiver to recover the data stream. The spreading of the energy is known as inter-symbol interference (ISI). The data eye, which is an overlay graph of all data samples collected, would not have the desired openness. With equalization, the effects of the lossy channel can be negated, resulting in an increased eye opening and improved bit error rate (BER). An example of no equalization and with optimized transmit equalization is shown in Figure 1.

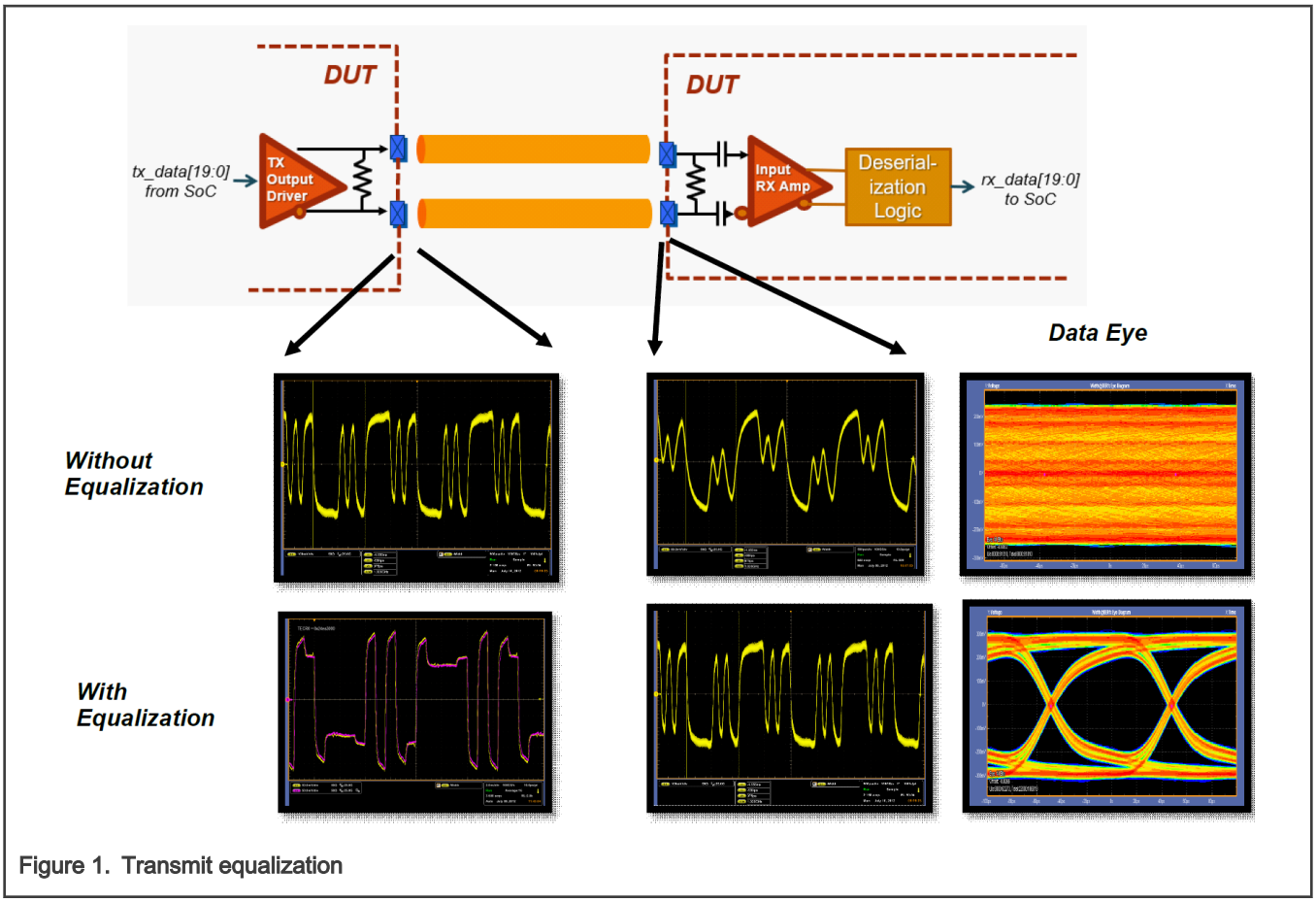

Figure 1. Transmit equalization

1.3.1 Important parameters, registers, and bits for transmit link optimization

This section describes the transmit equalization parameters and the corresponding LX216xA registers and bits.

Transmitter output waveform can be found in Figure 72-12 of *IEEE 802.3-2018, Clause 72* [1]. In this waveform:

- T = Symbol period
- *t1* = Zero-crossing point of the first rising edge of the AC-coupled signal
- *t2* = Zero-crossing point of the first falling edge of the AC-coupled signal
- V1 = Maximum voltage measured in the interval from *t1* to *t1* + T
- V2 = Postive steady-state voltage measured as the average voltage in the interval from *t1* + 2T to *t2* - 2T
- V3 = Maximum voltage measured in the interval from *t2* - T to *t2*

The **pre-cursor** amplitude is the peak amplitude before a transition. The peak amplitude before the transition at *t2* is V3.

The **post-cursor** amplitude is the peak amplitude after a transition. The peak amplitude after the transition at *t1* is V1.

The pre- and post-cursor coefficient ratios, Rpre and Rpost, are derived from the following equations:

- Rpre = V3 / V2
- Rpost = V1 / V2
- $Rpre_{dB}$ = 20 log (V3 / V2)
- $Rpost_{dB}$ = 20 log (V1 / V2)

1.3.1.1 Pre-cursor equalization settings

CAUI-4 pre-cursor equalization is defined in Table 83D-2 of *IEEE 802.3-2018, Annex 83D* [1]. Table 1 shows the CAUI-4 transmitter equalization settings from the industry specification translated into LX216xA parameters.

Table 1. Pre-cursor equalization settings

LNmTECR0[EQ_PREQ]	C(-1) ratio[1]	Drive strength of full swing transition bit to pre-cursor	
		Amplitude ratio	dB
0000b	0.0	1.0x	0
0001b	0.02	1.04x	0.34
0010b	0.04	1.09x	0.75
0011b	0.06	1.14x	1.14
0100b	0.08	1.20x	1.58
0101b	0.10	1.26x	2.0
0110b	0.12	1.33x	2.48
0111b	0.15	1.40x	2.9
1000b	0.18	1.50x	3.5
1001b	0.20	1.60x	4.1
1010b	0.23	1.71x	4.7
1011b	0.26	1.84x	5.3
1100b	0.30	2.00x	6.0

1. C(-1) ratio = c(–1) / (|c(–1)|+|c(0)|)

1.3.1.2 Post-cursor equalization settings

CAUI-4 post-cursor equalization is defined in Table 83D-3 of *IEEE 802.3 -2018, Annex 83D* [1]. Table 2 shows the CAUI-4 transmitter equalization settings from the industry specification translated into LX216xA parameters.

Table 2. Post-cursor equalization settings

LNmTECR0[EQ_POST1Q]	C(1) ratio[1]	Drive strength of full swing transition bit to post-cursor	
		Amplitude ratio	dB
00000b	0.0	1.0x	0
00001b	0.02	1.04x	0.34
00010b	0.04	1.09x	0.75
00011b	0.06	1.14x	1.14
00100b	0.08	1.20x	1.58
00101b	0.10	1.26x	2.0
00110b	0.12	1.33x	2.48
00111b	0.15	1.40x	2.9
01000b	0.18	1.50x	3.5

Table continues on the next page...

Table 2. Post-cursor equalization settings (continued)

LNmTECR0[EQ_POST1Q]	C(1) ratio[1]	Drive strength of full swing transition bit to post-cursor	
		Amplitude ratio	dB
01001b	0.20	1.60x	4.1
01010b	0.23	1.71x	4.7
01011b	0.26	1.84x	5.3
01100b	0.30	2.00x	6.0
01101b	0.34	2.18x	6.8
01110b	0.38	2.40x	7.6
01111b	0.42	2.66x	8.5
10000b	0.48	3.00x	9.5

1. C(1) ratio = c(1) / (|c(1)|+|c(0)|)

1.4 IBIS-AMI simulation

IBSI-AMI modeling provides a way to simulate the system design before the prototype phase of development. Simulations help to understand what happens to the signal as it goes through the channel. The equalizer tap settings in the models allow signal observation after equalization.

This section provides examples of IBIS-AMI simulations using the LX2160A for both the Tx AMI model and the Rx AMI model. It shows examples of how different transmit pre-cursor and post-cursor settings on the LX2160A transmit side affect the eye diagram of another LX2160A device on the receive side.

The three values are the pre-cursor, main cursor, and post-cursor.

In Figure 2, no transmit equalization is applied, for example, no pre-cursor and no post-cursor.

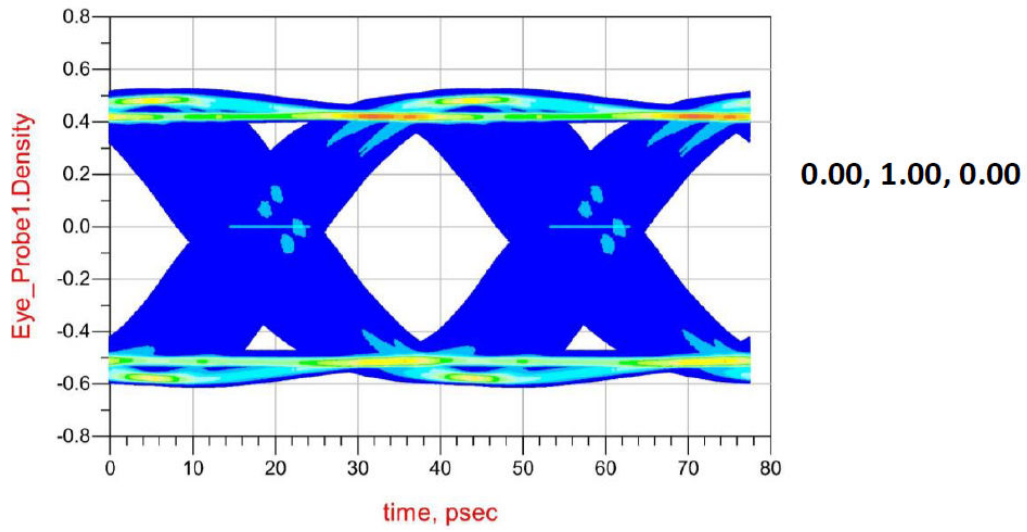

Figure 2. Transmit equalization: No pre-cursor, no post-cursor

In Figure 3, the pre-cursor is adjusted to 0.22 (1.67x or 4.4 dB), resulting in an increased eye opening.

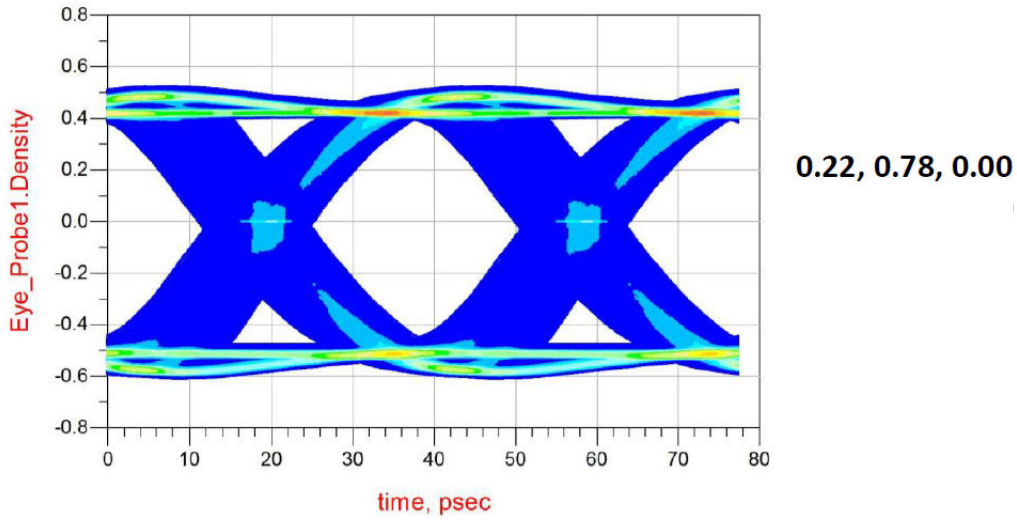

Figure 3. Transmit equalization: Pre-cursor 0.22, post-cursor 0

In Figure 4, the pre-cursor is adjusted to 0.04 (1.09x or 0.75 dB) and the post-cursor is adjusted to 0.28 (1.9x or 5.6 dB), resulting in a decreased eye opening.

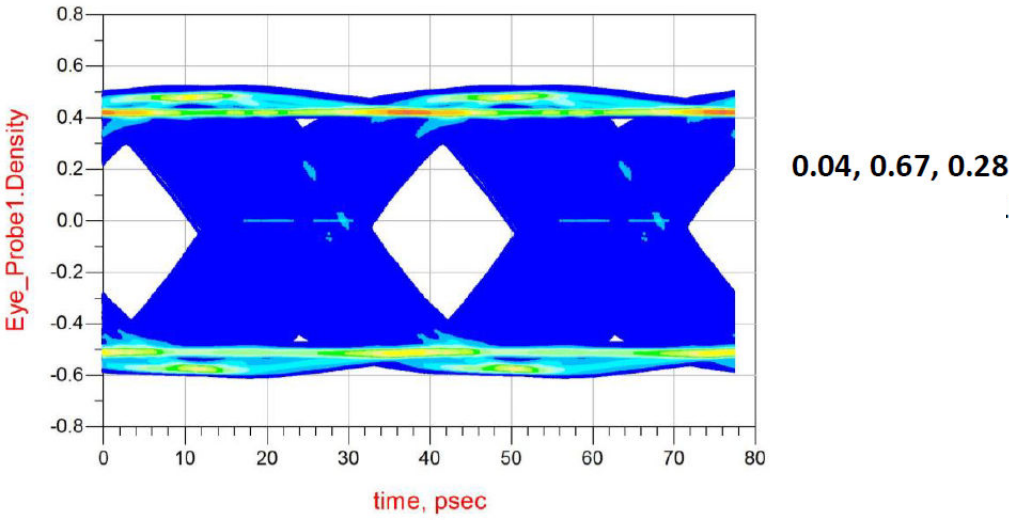

Figure 4. Transmit equalization: Pre-cursor 0.04, post-cursor 0.28

2 Link optimization

After performing simulations and determining a range of pre-cursor and post-cursor values, use those values as the starting point for sweeping transmit equalization settings on the LX216xA.

2.1 Ingress

This section discusses link optimization when traffic is directed towards the LX216xA.

2.1.1 Adaptive receive equalization

The SerDes receiver logic provides adaptive equalization. Receiver tuning is not required but optimal settings are recommended before link establishment. Use one of the following options to apply the fixed settings for a one-time initialization of the SerDes receiver:

- Use MC firmware 10.23.0 or later. To get the latest MC firmware release, see https://github.com/NXP/qoriq-mc-binary [2].
- Use PBI commands via the RCW:

NOTE

Any support, information, and technology (“Materials”) provided by NXP are provided AS IS, without any warranty express or implied, and NXP disclaims all direct and indirect liability and damages in connection with the Material to the maximum extent permitted by the applicable law. NXP accepts no liability for any assistance with applications or product design. Materials may only be used in connection with NXP products. Any feedback provided to NXP regarding the Materials may be used by NXP without restriction.

```
.pbi
 /* Lane H specific settings */
write 0x01EA0F44, 0x03000330
write 0x01EA0F48, 0x10000000
write 0x01EA0F50, 0x00000085
write 0x01EA0F58, 0xA1000023
write 0x01EA0F74, 0x00002020
write 0x01EA0F28, 0x00000000

/* Lane G specific settings */
write 0x01EA0E44, 0x03000330
write 0x01EA0E48, 0x10000000
write 0x01EA0E50, 0x00000085
write 0x01EA0E58, 0xA1000023
write 0x01EA0E74, 0x00002020
write 0x01EA0E28, 0x00000000

/* Lane F specific settings */
write 0x01EA0D44, 0x03000330
write 0x01EA0D48, 0x10000000
write 0x01EA0D50, 0x00000085
write 0x01EA0D58, 0xA1000023
write 0x01EA0D74, 0x00002020
write 0x01EA0D28, 0x00000000

/* Lane E specific settings */
write 0x01EA0C44, 0x03000330
write 0x01EA0C48, 0x10000000
write 0x01EA0C50, 0x00000085
write 0x01EA0C58, 0xA1000023
write 0x01EA0C74, 0x00002020
write 0x01EA0C28, 0x00000000

/* Common setting */
write 0x01EA0428, 0x03100000
.end
```

- Run the following sequence of commands per Ethernet lane configured for 25GbE, 50GbE, or 100GbE operation; after booting or at some point before traffic is received:

```
write LNmRRSTCTL[HLT_REQ]=1
write offset 0x1EA0844 + m*0x100 = 0x03000330
write offset 0x1EA0848 + m*0x100 = 0x10000000
```

```
write offset 0x1EA0850 + m*0x100 = 0x00000085
write offset 0x1EA0858 + m*0x100 = 0xA1000023
write offset 0x1EA0874 + m*0x100 = 0x00002020
write offset 0x1EA0428 = 0x03100000
write offset 0x1EA0828 + m*0x100 = 0x00000000
write LNmRRSTCTL[RST_REQ]=1
```

NOTE

For the multi-lane protocols, 50G and 100G, SW, HLT_REQ needs to be done first on all the lanes of a port, with 'lane 0' of the port halted last, and the reconfiguration waiting until 'lane 0' is halted. Similarly, RST_REQ needs to be done on all lanes of a port after all lanes are reconfigured, with 'lane 0' of the port reset last.

2.1.2 Connected device transmit equalization tuning

Since the LX216xA's receiver is adaptive, tuning the connected device's transmitter equalization settings is recommended to ensure good signal integrity for proper operation. Whether the LX216xA is connected to a retimer, an FPGA, or another LX216xA device, transmit equalization tuning of the link partner is required.

As an example, if the LX216xA is connected to a retimer that supports programmable transmit equalization, adjust the transmit equalization pre- and post-cursor coefficient settings for each 25 Gbit/s lane if the default pre- and post-cursor coefficients result in link instability or a high BER. Test each pre- and post-cursor coefficient combination to find the optimal values that result in best performance in terms of link stability, robustness, and number of bit errors.

To observe how the LX216xA receiver behaves with connected device's transmit equalization settings, see QVCS SerDes tool BIST error indication.

2.1.3 QVCS SerDes tool BIST error indication

The QCVS SerDes tool supports the LX216xA Built-In Self Test (BIST), which includes a pattern generator in the transmit path and a pattern checker in the receive path. There are three operating modes: *Digital Loopback*, *External Loopback*, and *External*.

- Digital Loopback: The pattern is generated by the SerDes block and internally looped back into the serial receiver path (internal loopback). Transmit or receive equalization does not affect the results of BIST in Digital Loopback mode because there is no lossy channel.
- External Loopback: The pattern is generated by the SerDes block to the Tx pin, which is connected to the Rx pin through an external user-supplied connection
- External: The pattern is generated from an external source. The pattern must match one of the BIST internal patterns.

When the SerDes tracking loop locks onto the data, the error counting starts. A BIST pattern sync is asserted when the serial received data matches the selected BIST pattern.

The BIST analyzer operates on four consecutive input serial bits. The number of received errors is incremented each time an error or multiple errors are detected within the four bit wide pattern. The number of received errors is limited to 255 errors. Additional errors are not reported in the error counter.

An example of the QCVS SerDes tool BIST is shown in Figure 5. Lane E of the LX216xA is running BIST in External mode, while its link partner is transmitting the mixed frequency test pattern (MFTP). All received bits from the link partner matches the bits in the repeating MFTP pattern and the BIST passes.

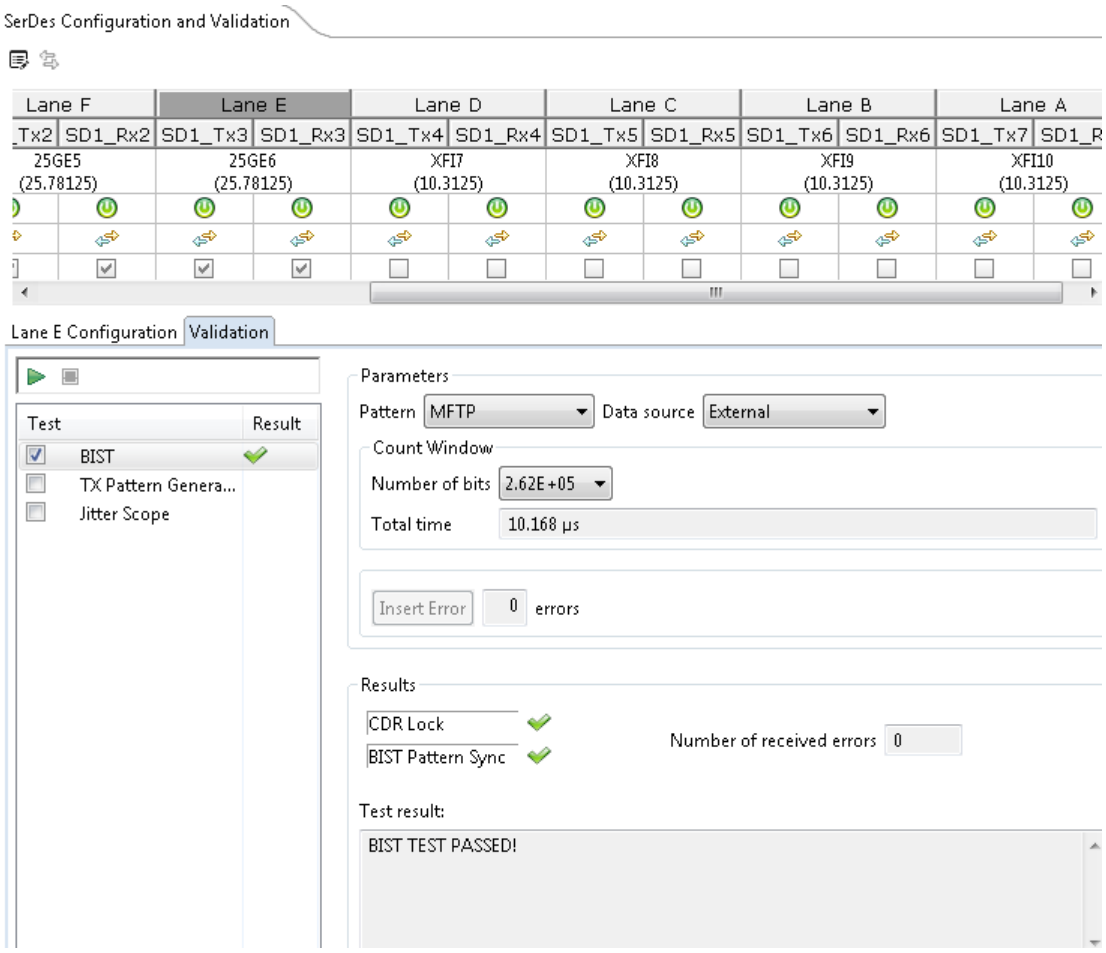

Figure 5. QCVS SerDes tool BIST example 1

In Figure 6, the link partner transmit equalization settings result in the LX216xA BIST to fail. In this case, tune the link partner transmit equalization settings for correct operation with the LX216xA.

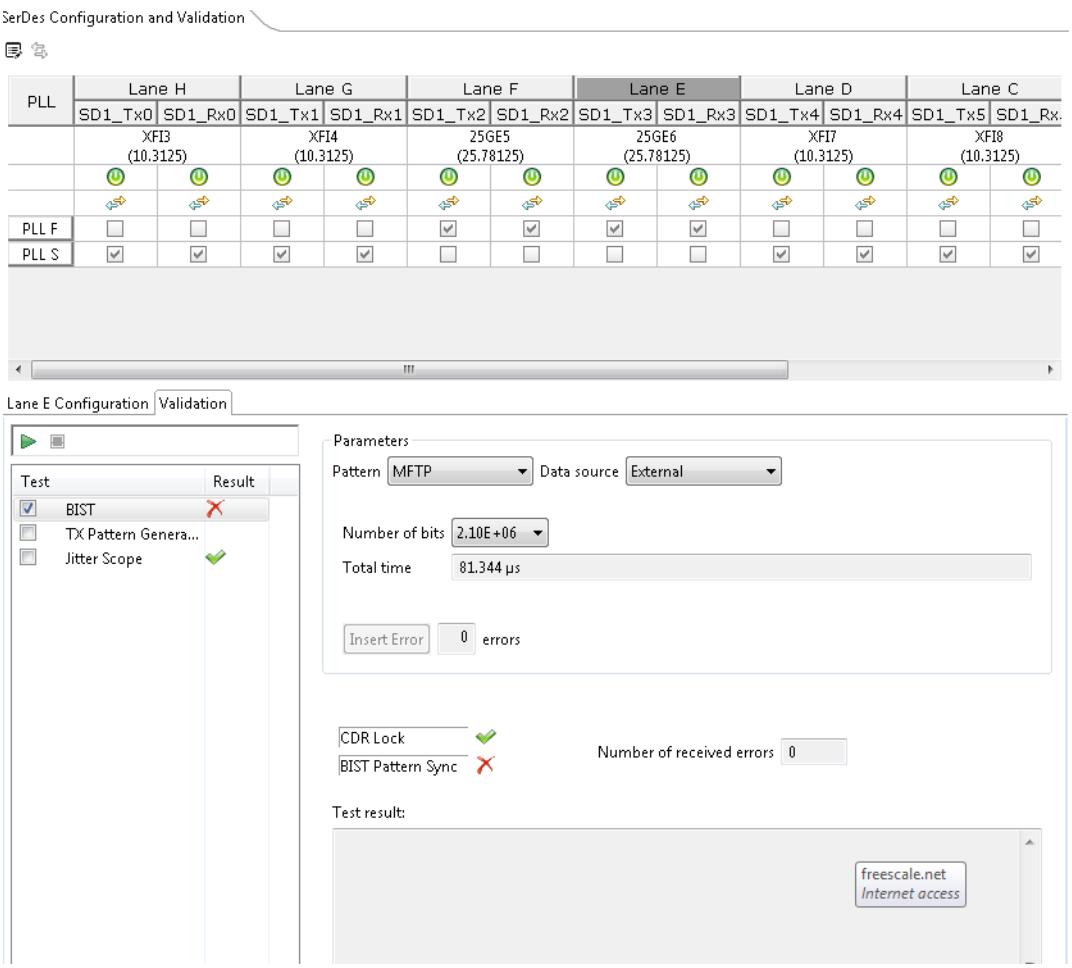

Figure 6. QCVS SerDes tool BIST example 2

2.1.4 Forward error correction (FEC)

Forward error correction (FEC) is a method of detecting and correcting errors in transmitted data, without retransmission. In this method, redundant data, called error-correcting code, is sent along with data frames by the sender to help the receiver detect and ignore erroneous data frames. FEC is useful in scenarios where retransmission is very costly or not possible, for example, when sending data to multiple receivers or during transmission over a one-way communication link.

Enabling FEC can help fix errors at the Physical Coding Sublayer (PCS). The LX216xA supports both *IEEE 802.3-2018* [1] Clause 91 Reed-Solomon FEC (RS-FEC) and Clause 74 Fire code FEC (FC-FEC).

In the Open Systems Interconnection (OSI) model, the FEC layer is placed above the Physical Medium Attachment (PMA) layer and below the PCS layer. For more details, see Figure 108-1 of *IEEE 802.3-2018* [1] .

NOTE

FEC mode programming requires modifying SerDes memory-mapped registers and 25G PCS MII management registers. See *QorIQ LX216xA Reference Manual* and *DPAA2 User Manual* for more details.

2.1.4.1 RS-FEC enablement

Memory-mapped register

Setting E25G*a*CR2[FEC91_ENA] enables RS-FEC (FEC91) for the channel. Enabling or disabling FEC91 can occur at any time during operation. This link coding change will cause a link restart.

The register offset is 1B08h + (*a* × 10h), where *a* is lane A to H (0 to 7).

```
write E25GaCR2[FEC91_ENA] = 0b1
```

MII management registers

For MAC3, MAC5, and MAC9, perform the following writes to the associated MAC's 25G PCS registers:

```
write 0x3.0x8010 = 0x0307
write 0x3.0x8002 = 0x4FFF
write 0x3.0x8008 = 0x68C1
write 0x3.0x8009 = 0x0021
write 0x3.0x0 = 0x8000
```

For MAC4, MAC6, and MAC10, perform the following writes to the associated MAC's 25G PCS registers:

```
write 0x3.0x8010 = 0x0307
write 0x3.0x8002 = 0x4FFF
write 0x3.0x0 = 0x8000
```

2.1.4.2 FC-FEC enablement

Memory-mapped register

Setting E25G*a*CR2[FEC_ENA] enables FC-FEC (FEC74) for the channel. Enabling or disabling FEC74 can occur at any time during operation. This link coding change will cause a link restart.

The register offset is 1B08h + (*a* × 10h), where *a* is lane A to H (0 to 7).

```
write E25GaC2[FEC_ENA] = 0b1
```

MII management registers

For MAC3, MAC5, and MAC9, perform the following writes to the associated MAC's 25G PCS registers:

```
write 0x3.0x8010 = 0x0005
write 0x3.0x8002 = 0x4FFF
write 0x3.0x8008 = 0x68C1
write 0x3.0x8009 = 0x0021
write 0x3.0x0 = 0x8000
```

For MAC4, MAC6, and MAC10, perform the following writes to the associated MAC's 25G PCS registers:

```
write 0x3.0x8010 = 0x0005
write 0x3.0x8002 = 0x4FFF
write 0x3.0x0 = 0x8000
```

2.1.5 Repeater mode for debugging

If the connected device has the capability to generate PRBS patterns or data, the LX216xA has a Repeater mode feature that echoes back whatever is received without modification from other on-chip logic, for example, Media Access Control (MAC).

This may be a useful debug mode if the connected device has a way to evaluate errors on its receiver.

NOTE

For Repeater mode operation, the SerDes reference clock and the clock to the connected devices must be the same.

The steps to enable Repeater mode on the LX216xA are as follows:

For a = Lane A to H (0 to 7):

1. For TRSTCTL register (0x820 + (a x 0x100)):
    a. Set Tx output to Common mode by setting bit 8 (OUT_CM) to 1.
    b. Reset Tx by setting bit 5 (TX_RESET_B) to 0.
    c. Disable Tx side by setting bit 4 (TX_LANE_EN) to 0.
2. For RRSTCTL register (0x840 + (a x 0x100)):
    a. Reset Rx by setting bit 5 (RX_RESET_B) to 0.
    b. Disable Rx side by setting bit 4 (RX_LANE_EN) to 0.
3. For TCSR0 register (0x8A0 + (a x 0x100)):
    a. Set bits 13:12 (RPTR_MODE_SEL) to 01.
    b. Reset repeater FIFO by setting bit 10 (RPTR_FIFO_RESET_B) to 0.
4. Again for RRSTCTL register (0x840 + (a x 0x100)):
    a. Reset Rx by setting bit 5 (RX_RESET_B) to 0.
    b. Enable Rx side by setting bit 4 (RX_LANE_EN) to 1.
    c. Wait for 240 µs.
    d. Take Rx out of reset by setting bit 5 (RX_RESET_B) to 1.
    e. Enable Rx side by setting bit 4 (RX_LANE_EN) to 1.
    f. Wait for 9 ms for CDR lock (see step i).
    g. Take Rx out of reset by setting bit 5 (RX_RESET_B) to 1.
    h. Enable Rx side by setting bit 4 (RX_LANE_EN) to 1.
    i. Ensure that bit 12 (CDR_LOCK) is set to 1.
5. Now, again for TCSR0 register (0x8A0 + (a x 0x100)):
    a. Set bits 13:12 (RPTR_MODE_SEL) to 01.
    b. Take repeater FIFO out of reset by setting bit 10 (RPTR_FIFO_RESET_B) to 1.
6. Now, again for TRSTCTL register (0x820 + (a x 0x100)):
    a. Set Tx output to Common mode by setting bit 8 (OUT_CM) to 1.
    b. Reset Tx by setting bit 5 (TX_RESET_B) to 0.
    c. Enable Tx side by setting bit 4 (TX_LANE_EN) to 1.
    d. Set Tx output to Common mode by setting bit 8 (OUT_CM) to 1.
    e. Take Tx out of reset by setting bit 5 (TX_RESET_B) to 1.
    f. Enable Tx side by setting bit 4 (TX_LANE_EN) to 1.
    g. Disable Common mode by setting bit 8 (OUT_CM) to 0.
7. Monitor bit 8 of TCSR0 register (0x8A0 + (a × 0x100)). If set, then the LX216xA SerDes reference clock does not match the reference clock for the other end of the link.

2.2 Egress

This section discusses link optimization when traffic is directed from the LX216xA to a connected device.

2.2.1 Transmitter equalization tuning

The goal of the transmit equalization tuning is to identify the optimal settings as per the requirements of the link partner's receiver and meet the required system bit error rate. Tuning requires sweeping of the pre- and post-cursor coefficients discussed in Important parameters, registers, and bits for transmit link optimization.

The following steps show an example of LX216xA transmit equalization tuning by utilizing the QCVS SerDes tool. The LX216x transmit pre- and post-cursor parameters are adjusted, and a pattern is transmitted to the connected device. If the pre- and post-cursor combination results in link instability or a high bit error rate on the receiver, this indicates non-optimal equalization settings and further adjustments are needed.

1. Set LNmTECR0[EQ_TYPE] = 010b for 3-tap equalization.
2. Set LNmTECR0[EQ_PREQ] = 0 to initialize the pre-cursor. Make sure LNmTECR0[EQ_SGN_PREQ] = 1 for a positive pre-cursor sign.
3. Set LNmTECR0[EQ_POST1Q] = 0 to initialize the post-cursor. Make sure LNmTECR0[EQ_SGN_POST1Q] = 1 for a positive post-cursor sign.
4. Start the QCVS SerDes tool Transmit Pattern Generator.
5. When the QCVS SerDes tool displays the message "Pattern Generation STARTED", start BIST on the link partner's receiver and record the bit error count.
6. Increment the EQ_POST1Q to increase the post-cursor.
7. Check if EQ_POST1Q > 16 ?
    - Yes
        - Increment the EQ_PREQ to increase the pre-cursor
        - Check if EQ_PREQ > 12 ?
            - Yes - Done
            - No - Go to step 3
    - No
        - Go to step 4

Figure 7 explains how to configure transmit equalization parameters in the QCVS SerDes tool.

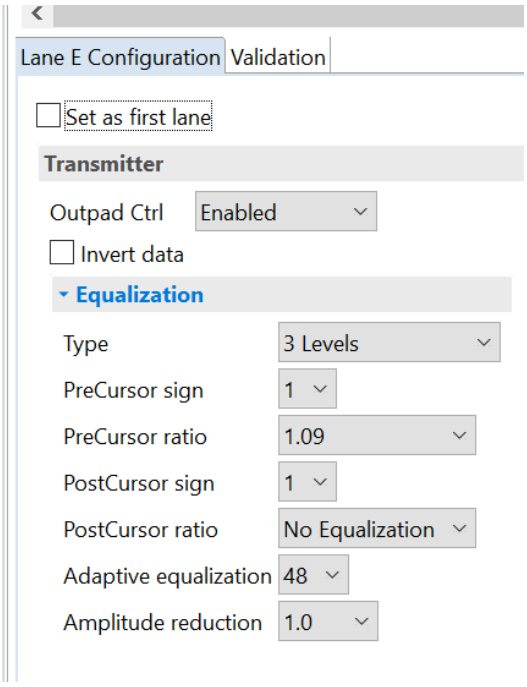

Figure 7. QCVS SerDes transmit equalization configuration

The transmit pattern generator of QCVS SerDes tool (shown in Figure 8) can be used to transmit a pattern.

NOTE

The pattern selected for transmission must be supported by the receiving device.

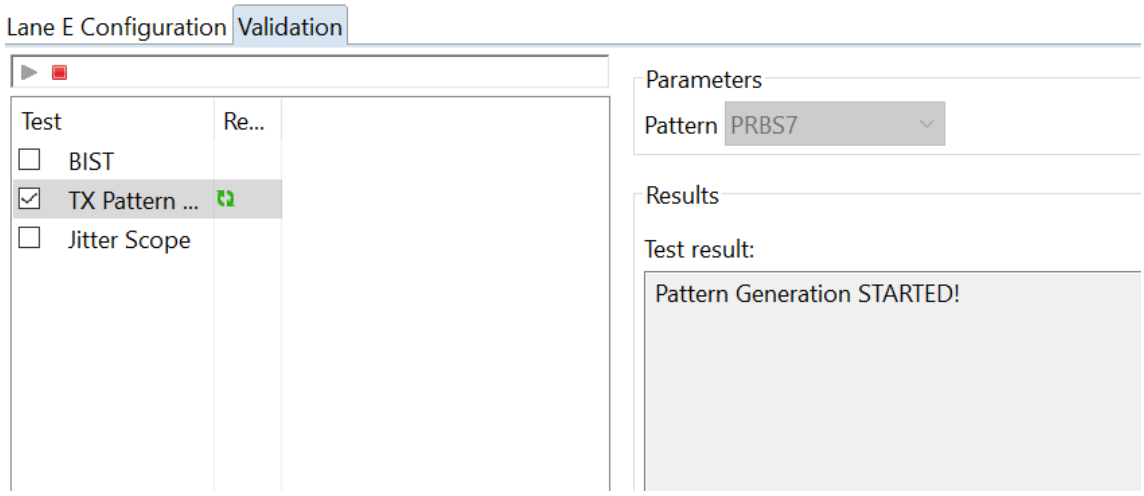

Figure 8. QCVS SerDes transmit pattern generator

2.2.2 Connected device receive response

In step 5 of Transmitter equalization tuning, testing is performed to determine how the connected device receiver responds to the LX216xA transmit equalization settings. The goal is to find the LX216xA settings that result in meeting the bit error rate requirement. Constructing a matrix plot as shown in Figure 9 may be useful in analyzing how the connected device responds to the pre- and post-cursor combinations. The red cells indicate pre- and post-cursor settings that result in link up failures. The yellow cells indicate high bit/frame errors, while the green cells meet the bit error requirement.

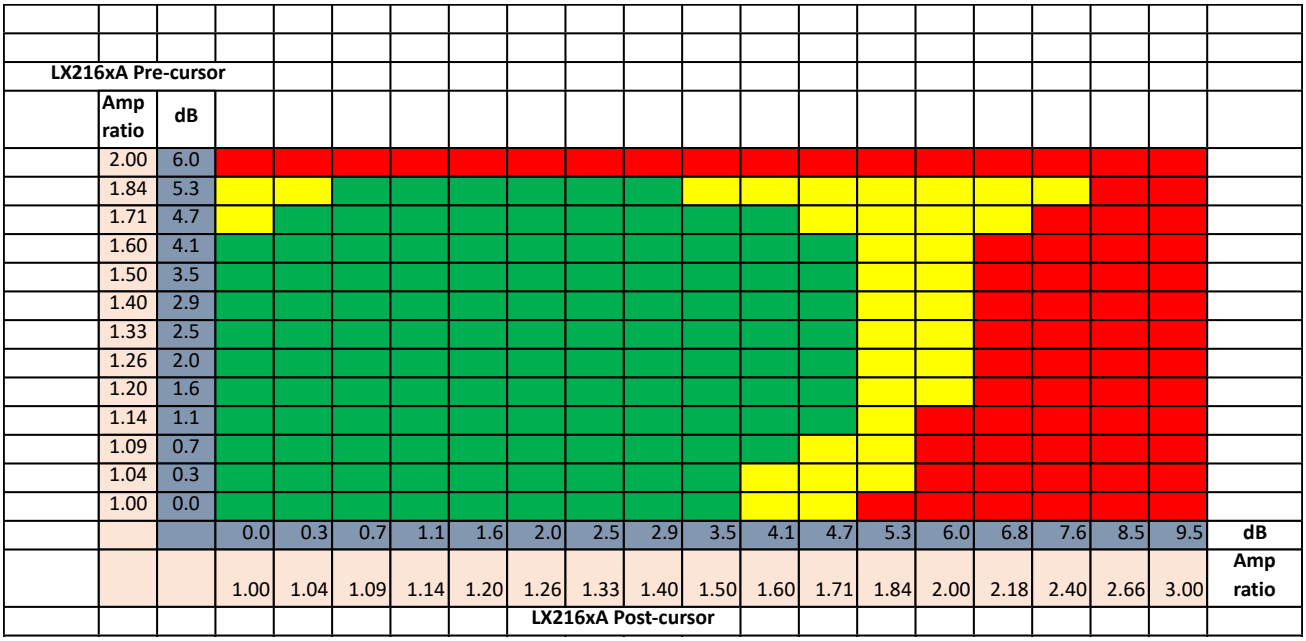

Figure 9. Example of a connected device response to LX216xA transmit equalization tuning

3 Summary

Link optimization is key in ensuring adequate margin to electrical specifications to avoid link establishment and operation issues. Receive and transmit equalization help compensate for lossy channels. IBIS-AMI modeling is a useful aid in determining a range of equalization values that are specific to a particular channel.

Apply the optimal settings to LX216xA's adaptive receiver that are defined in Adaptive receive equalization before link establishment. Assuming the channel is compliant to IEEE 802.3 CAUI-4 C2C and C2M specifications, tuning the transmit equalizer may improve the data eye at the receiver. An open data eye helps improve the robustness of the link across process, voltage, and temperature variations which leads to near error-free operation at line speed. Low-level link errors are further reduced if FEC is also enabled.

4 References

The table below lists additional resources that can be referred for additional information.

Table 3. Reference documentation and tools

ID	Name of related collateral / information to refer	Location
[1] IEEE Std 802.3-2018	IEEE Standard for Ethernet • Annex 83D Chip-to-Chip CAUI-4 • Annex 83E Chip-to-Module CAUI-4 • Clause 108 Reed-Solomon Forward Error Correction sublayer for 25GBASE-R PHYs	standards.ieee.org
[2] LSDK Open Source	MC Firmware	lsdk.github.io
LX2160ARM	QorIQ LX2160A Reference Manual	www.nxp.com

Table continues on the next page...

Table 3. Reference documentation and tools (continued)

ID	Name of related collateral / information to refer	Location
DPAA2UM	DPAA2 User Manual	www.nxp.com
AN5407	LX2160A Design Checklist	Contact your local NXP field applications engineer (FAE) or sales representative
LX2160ACE	LX2160A Chip Errata	Contact your local NXP FAE or sales representative
AN5119	SerDes Configuration and Validation Tool Companion Application Note	www.nxp.com
	High-Speed SERDES Modeling for the PCB and System Environment	www.nxp.com
	QCVS SerDes Tool User Guide	www.nxp.com
	QCVS Getting Started Guide	www.nxp.com

5 Revision history

The table below summarizes the revisions to this document.

Table 4. Revision history

Revision	Date	Topic cross-reference	Change description
Rev. 1	12/2020	Introduction	Changed "25G-AUI" to "25GAUI" and "CAUI-2" to "50GAUI-2"
Rev. 0	09/2020		Initial public release

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 12/2020

Document identifier: AN12950

arm