AN13260

PTN38007/38003A/3816/3944 USB Type-C USB3.2, DisplayPort v2.0, Thunderbolt 3, and USB4 v1.0 combo redriver design guidelines

Rev. 1.0 — 14 June 2021 **Application note**

Document information

Information	Content
Keywords	PTN38007 PTN38003A, PTN3816, PTN3944, PTN5150A, PTN5110, NX5P3090, USB Type-C, CC Logic, Orientation Detection, USB3.2, SuperSpeed, DisplayPort, USB4 v1.0, Thunderbolt3 redriver
Abstract	This application note presents design guidelines for PTN38007/38003A/3816/3944 in a system.

Revision history

Rev	Date	Description
v.1.0	20210614	Initial version

1 Introduction

PTN38007 is a high-performance Type-C USB3.2/ DP1.4/Thunderbolt3/USB4 v1.0 combo linear redriver that is optimized for USB3.2, DisplayPort 1.4 and Thunderbolt3/ USB4 v1.0 applications on either the Downstream Facing Port (DFP) or Upstream Facing Port (UFP) application.

PTN38007 can be used in different system configurations (DFP, UFP or Dongle), and can be configured through I^2C. This document discusses in detail how each design can be achieved, in terms of schematics and layout.

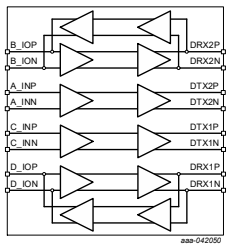
2 Connections to a Type-C Receptacle or a Type-C Plug

PTN38007 can be used in a DFP, UFP, or Dongle configuration. In each configuration, each pin has its specific connection in the system.

2.1 DFP system with Type-C receptacle

In a DFP system, a USB3/USB4 v1.0/DisplayPort/Thunderbolt controller is placed on the left side of the PTN38007, and a Type-C receptacle is placed on the right side of PTN38007. Table 1 illustrates the connection in a DFP system.

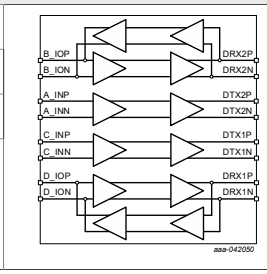
Table 1. Connection in a DFP system

DP Controller		USB3/USB4 v1.0 Controller		PTN38007			Type-C Receptacle	
Normal	Reversed	Normal	Reversed				Pin #	Pin name
ML0	ML3	SSRX2	SSRX1	B_IO		DRX2	A11/A10	RX2
ML1	ML2	SSTX2	SSTX1	A_IN		DTX2	B3/B2	TX2
ML2	ML1	SSTX1	SSTX2	C_IN		DTX1	A2/A3	TX1
ML3	ML0	SSRX1	SSRX2	D_IO		DRX1	B10/B11	RX1

2.2 UFP system with Type-C receptacle

In a UFP system, a Type-C receptacle is placed on the left side of the PTN38007, and a USB3/USB4 v1.0/DisplayPort/Thunderbolt controller is placed on the right side of PTN38007. Table 2 illustrates the connection in a UFP system.

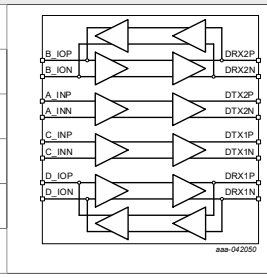
Table 2. Connection in a UFP system

Type-C Receptacle		PTN38007			USB3/USB4 v1.0 Controller		DP Controller	
Pin #	Pin name				Normal	Reversed	Normal	Reversed
A2/A3	TX1	B_IO		DRX2	SSTX1	SSTX2	ML3	ML0
B10/B11	RX1	A_IN		DTX2	SSRX1	SSRX2	ML2	ML1
A11/A10	RX2	C_IN		DTX1	SSRX2	SSRX1	ML1	ML2
B3/B2	TX2	D_IO		DRX1	SSTX2	SSTX1	ML0	ML3

2.3 UFP dongle with Type-C plug

Similar to a UFP system, a UFP dongle has a USB3/USB4 v1.0/DisplayPort/Thunderbolt controller placed on the right side of PTN38007, but a Type-C plug is placed on the left side of the PTN38007. Table 3 illustrates the connection in a UFP dongle system. (This design is based on normal orientation with CC1 connected to PD controller, and only CC1 pin is connected to PD controller).

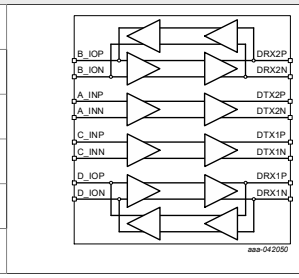
Table 3. Connection in a UFP dongle system

Type-C plug		PTN38007			USB3/USB4 v1.0 controller		DP controller	
Pin #	Pin Name				Normal	Reversed	Normal	Reversed
A11/A10	RX2	B_IO		DRX2	SSTX2	SSTX1	ML0	ML3
B3/B2	TX2	A_IN		DTX2	SSRX2	SSRX1	ML1	ML2
A2/A3	TX1	C_IN		DTX1	SSRX1	SSRX2	ML2	ML1
B10/B11	RX1	D_IO		DRX1	SSTX1	SSTX2	ML3	ML0
A8	SBU1	AUXP					AUXP	
B8	SBU2	AUXN					AUXN	
A5	CC1	Connect to PD controller's CC1						
B5	CC2	VCONN or NC						

2.4 Type-C cable with Type-C plugs on both sides

A Type-C cable has plugs on both sides of PTN38007. Table 4 illustrates the connection in a cable. For DisplayPort interface, since the signal is unidirectional (from source to sink only), it is important to plug left side of the cable to a host PC, and plug right side of the cable to a device or monitor.

Table 4. Type-C cable connection

Type-C plug (to host)		PTN38007			Type-C plug (to device)	
Pin #	Pin name				Pin #	Pin name
A11/A10	RX2	B_IO		DRX2	A2/A3	TX1
B3/B2	TX2	A_IN		DTX2	B10/B11	RX1
A2/A3	TX1	C_IN		DTX1	A11/A10	RX2
B10/B11	RX1	D_IO		DRX1	B3/B2	TX2
A8	SBU1	AUXP			B8	SBU2
B8	SBU2	AUXN			A8	SBU1
A5	CC1	Connect across the cable			B5	CC2
B5	CC2	VCONN or NC			A5	CC1

2.4.1 High-speed switches

PTN38007 itself does not have any built-in switch to multiplex USB3/USB4 v1.0/ DisplayPort/Thunderbolt signals. The controllers or application processors should include a high-speed crossbar switch that is capable of multiplexing different signal standards to four differential input pins of PTN38007. If the controllers or application processors don't have a crossbar switch integrated, NXP has the following high-speed switches available for selection:

- To cover up to 10 Gbps (USB3.2 Gen 2, DisplayPort HBR3)
  - Simple 2:1 switch: CBTU02043, CBTL01023, CBTL02043, CBTL04083
  - Integrated Type-C switch: CBTL08GP053
- To cover up to 20 Gbps (USB4 v1.0, DisplayPort v2.0, Thunderbolt 3, PCIe Gen 3)
  - Simple 2:1 switch: CBTU02043, CBTU02044

2.4.2 AC capacitor location

PTN38007's TX or RX DC common mode voltage might be different from the chipset's or device's DC common mode voltage; AC caps should be placed on all high-speed lanes on both left and right sides of PTN38007. Between the chipset and last redriver or retimer before the Type-C connector, 0.1 µF capacitors should be placed on the high-speed lanes. Between last redriver or retimer and Type-C connector, 0.22 µF capacitors should be placed on TX channels, and 0.33 µF capacitors should be placed on the RX channels.

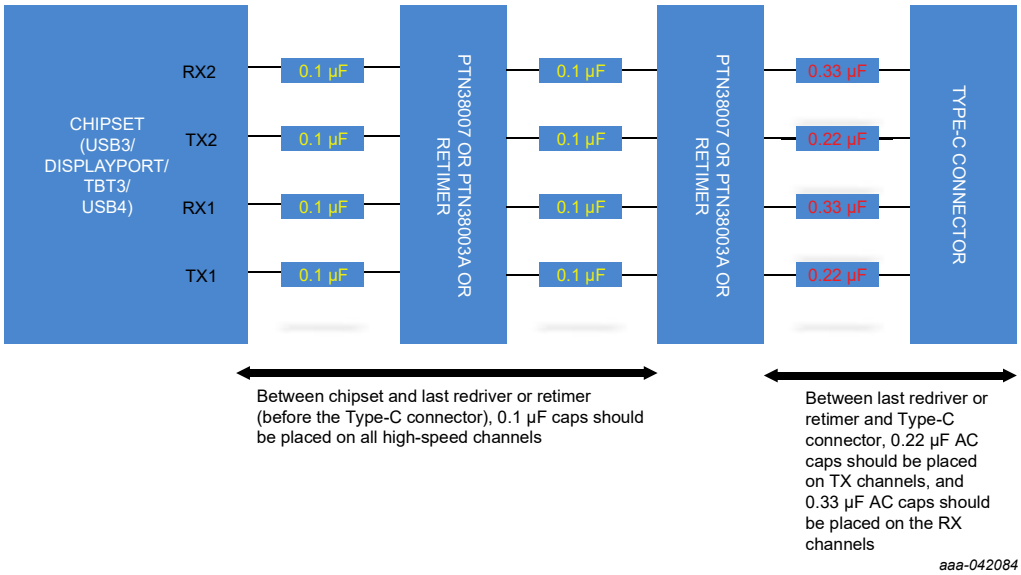


Figure 1. AC cap values on left/right side of the redriver

2.5 High-speed P and N signal assignment

PTN38007's high-speed lanes are agnostic to the polarity of the signal, and it is okay to swap the P and N signal polarity to achieve better layout result. However, when the polarity the left side is inverted, the polarity of the corresponding signal pair on the right side should be inverted at the same time.

2.6 AUXP and AUXN signal connection

PTN38007's AUX monitor circuit is used to decode AUX transactions, and connections to a DisplayPort's AUX channel polarity should follow the pin name assignments. In the case of SBU signals on the type-C connector, the AUXP and AUXN polarity changes according to the orientation of the cable plugging in.

Table 5. AUX polarity hardware wiring connection orientation

	DFP Type-C connector	UFP Type-C connector
Normal Orientation	SBU1 = AUXP SBU2 = AUXN	SBU1 = AUXN SBU2 = AUXP
Reversed Orientation	SBU1 = AUXN SBU2 = AUXP	SBU1 = AUXP SBU2 = AUXN

Usually the AUX P and N polarity hardware wiring connection follows the normal orientation in Table 5, and PTN38007's I^2C register 0x04 bit 3 can be used to follow the orientation of the cable plugging in, which is register 0x04 bit 4. When in normal orientation, set Reg[0x04].Bit[4:3]=[0, 0]; when in reversed orientation, set Reg[0x04].Bit[4:3]=[1, 1].

3	b'0	AUX snooping polarity control bit • When 0, AUXP/AUXN signal polarities follow pin naming: – Pin 18 = AUXP – Pin 17 = AUXN • When 1, AUXP/AUXN signal polarities are reverse of the pin naming: – Pin 17 = AUXP – Pin 18 = AUXN

For PTN3816, the AUX polarity assignment is NOT reversible, because there is no I^2C control to set the orientation of the AUX signaling. User should always connect AUX's positive signal to AUXP pin, and AUX's negative signal to AUXN pin.

2.7 AUX and LS connections options

There are various ways AUX and LS can connect to PTN38007 for snooping purposes. PTN38007 has two registers to configure AUX polarity, and pin sharing of AUX and LS signals.

- Reg[0x04][3] controls the polarity of AUXP/N

3	b'0	AUX snooping polarity control bit • When 0, AUXP/AUXN signal polarities follow pin naming: – Pin 18 = AUXP – Pin 17 = AUXN • When 1, AUXP/AUXN signal polarities are reverse of the pin naming: – Pin 17 = AUXP – Pin 18 = AUXN

- Reg[0x05][1] allows the use of AUXP/AUXN pins for both AUX/LS inputs

1	b'0	AUX/LS snooping pin muxing When 0, AUX and LS snooping are done through separate interface pairs. • AUX snooping using AUXP/AUXN pins • LS snooping using LSTX/LSRX pins When 1, AUX and LS snooping are done through the same AUXP/AUXN pins. • AUXP/AUXN snooping using AUXP/AUXN pins • LS snooping using AUXP/AUXN pins PTN38007 decodes the protocols based on the respective mode that is enabled.

Depending on these bit settings, AUX/LS connections are illustrated in Figure 2.

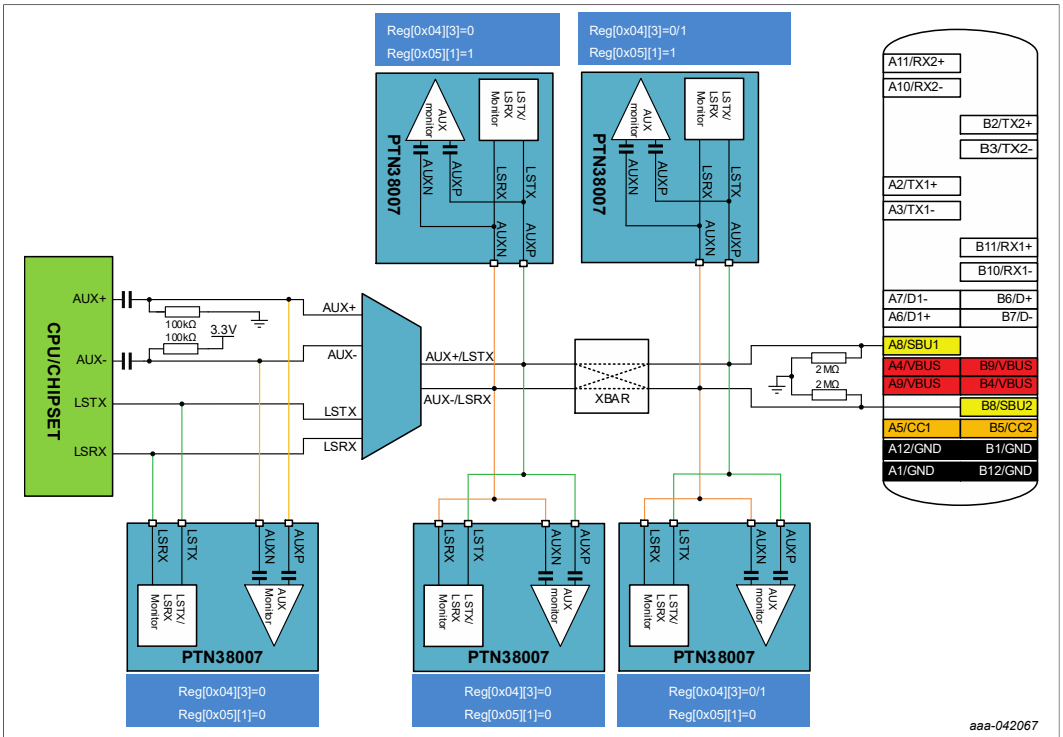


Figure 2. AUX and LS connection options

2.8 PTN3816 main lane assignments

DisplayPort's main lane number assignments are not interchangeable. Corresponding lanes are turned off or placed in low power mode when the link is in D3 mode or number of operating lanes are less than four. When setting LANE_ORDER to 0, PTN3816's lane number assignment should match with the DisplayPort connector's lane assignment.

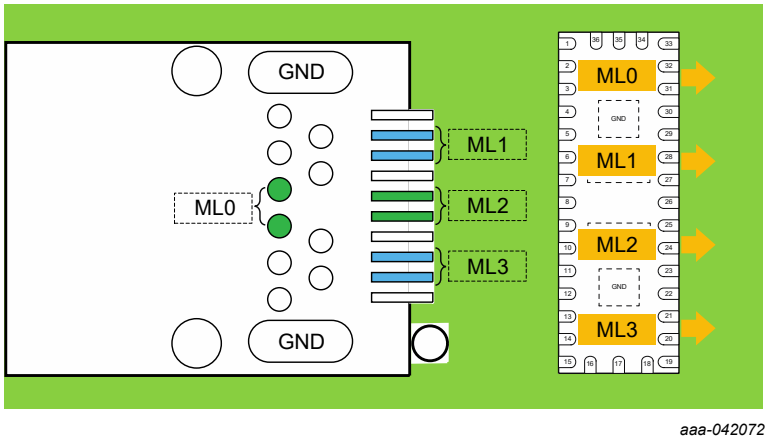


Figure 3. Mini DisplayPort connector, sink side

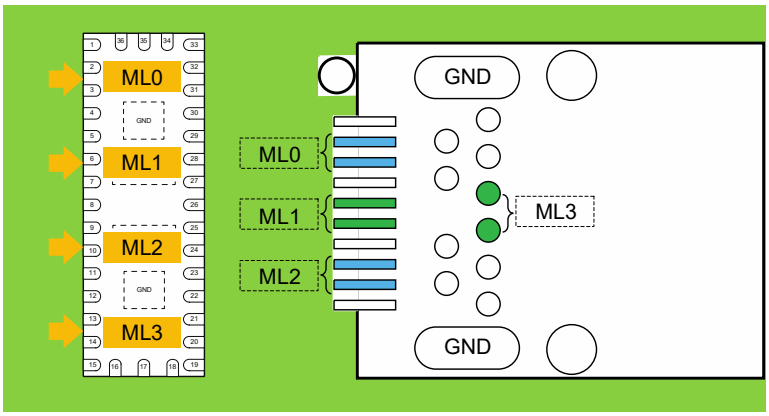


Figure 4. Mini DisplayPort connector, source side

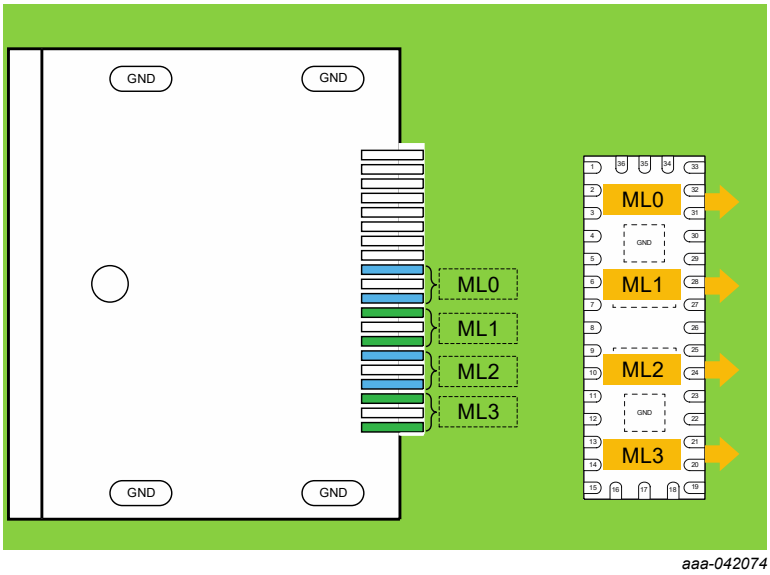


Figure 5. Full-size DisplayPort connector, sink side

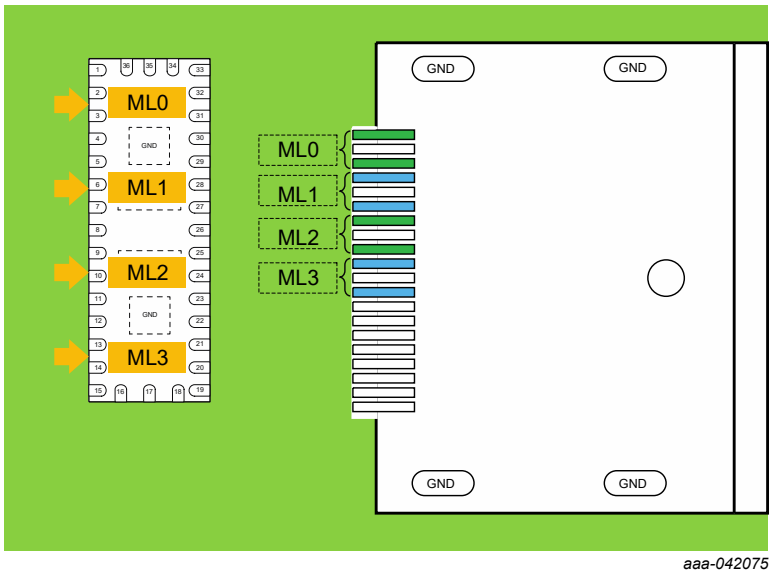


Figure 6. Full-size DisplayPort connector, source side

2.9 Number of power supply decoupling capacitors required

PTN38007 has five power supply pins. VCCA/VCCB/VCCC/VCCD are analog power supplies to each transmitter/receiver path. VDD pin is the power supply to the digital circuits. Ideally, there should be a 0.1 µF decoupling capacitor on each power supply pin; if there is limitation on number of capacitors that can be placed for each PTN38007 on the PCB, at least two capacitors should be used.

2.10 ADDR resistor tolerance

PTN38007's I^2C slave address can be configured through resistor options on the ADDR pin. During manufacturing, if it is very difficult to have exact resistor value placed in the BOM, the following table shows a range of resistors values that can be placed at the ADDR pin to achieve the same setting result.

Table 6. ADDR pin resistor options

I^2C Address	Datasheet recommendation	Minimum	Maximum
0x33	Connect to 1.8 V directly	0 Ω	1.1 kΩ
0x32	Connect to 1.8 V with 56 kΩ	50.4 kΩ	61.6 kΩ
0x31	Connect to 1.8 V with 200 kΩ	180 kΩ	220 kΩ
0x30	Connect to GND directly	0 Ω	Open

2.11 ESD recommendation

The following ESD devices are used on NXP's PTN38007/PTN3944 evaluation boards:

- PESD3V3R1BSF
- PESD2V8R1BSF

ESD protection diodes are placed between PTN38007 and the AC caps on the USB Type-C connector facing side. For more details about the ESD products, please contact Nexperia for more information.

2.12 PCIe mode I^2C address assignments

There are 32 possible I^2C slave addresses that can be assigned to PTN3944, including eight of which are reserved slave addresses in the I^2C standard. User should avoid using the reserved I^2C slave addresses. Below is a list of I^2C address assignments to each PCIe bus' TX/RX group that are being predefined on the PTN3944 Add-In Card. This is not mandatory, but if the user follows the assignments, the GUI can be used.

Table 7. PCIe mode I^2C address assignments

		ADDR4	ADDR3	ADDR2	ADDR/ADDR1	7-Bit Address	7-Bit Address						
BUS0 x16	TX[0:3]	0	0	0	VDD1V8 (0x33)	23	0	1	0	0	0	1	1
	TX[4:7]	0	0	0	56K Pull Up (0x32)	22	0	1	0	0	0	1	0
	TX[8:11]	0	0	0	200K Pull Up (0x31)	21	0	1	0	0	0	0	1
	TX[12:15]	0	0	0	GND (0x30)	20	0	1	0	0	0	0	0
	RX[0:3]	0	0	1	VDD1V8 (0x33)	2B	0	1	0	1	0	1	1
	RX[4:7]	0	0	1	56K Pull Up (0x32)	2A	0	1	0	1	0	1	0
	RX[8:11]	0	0	1	200K Pull Up (0x31)	29	0	1	0	1	0	0	1
	RX[12:15]	0	0	1	GND (0x30)	28	0	1	0	1	0	0	0
BUS1 x16	TX[0:3]	0	1	0	VDD1V8 (0x33)	33	0	1	1	0	0	1	1
	TX[4:7]	0	1	0	56K Pull Up (0x32)	32	0	1	1	0	0	1	0
	TX[8:11]	0	1	0	200K Pull Up (0x31)	31	0	1	1	0	0	0	1
	TX[12:15]	0	1	0	GND (0x30)	30	0	1	1	0	0	0	0
	RX[0:3]	0	1	1	VDD1V8 (0x33)	3B	0	1	1	1	0	1	1
	RX[4:7]	0	1	1	56K Pull Up (0x32)	3A	0	1	1	1	0	1	0
	RX[8:11]	0	1	1	200K Pull Up (0x31)	39	0	1	1	1	0	0	1
	RX[12:15]	0	1	1	GND (0x30)	38	0	1	1	1	0	0	0
BUS2 x16	TX[0:3]	1	0	0	VDD1V8 (0x33)	63	1	1	0	0	0	1	1
	TX[4:7]	1	0	0	56K Pull Up (0x32)	62	1	1	0	0	0	1	0
	TX[8:11]	1	0	0	200K Pull Up (0x31)	61	1	1	0	0	0	0	1
	TX[12:15]	1	0	0	GND (0x30)	60	1	1	0	0	0	0	0
	RX[0:3]	1	0	1	VDD1V8 (0x33)	6B	1	1	0	1	0	1	1
	RX[4:7]	1	0	1	56K Pull Up (0x32)	6A	1	1	0	1	0	1	0
	RX[8:11]	1	0	1	200K Pull Up (0x31)	69	1	1	0	1	0	0	1
	RX[12:15]	1	0	1	GND (0x30)	68	1	1	0	1	0	0	0
BUS3 x16	TX[0:3]	1	1	0	VDD1V8 (0x33)	73	1	1	1	0	0	1	1
	TX[4:7]	1	1	0	56K Pull Up (0x32)	72	1	1	1	0	0	1	0
	TX[8:11]	1	1	0	200K Pull Up (0x31)	71	1	1	1	0	0	0	1
	TX[12:15]	1	1	0	GND (0x30)	70	1	1	1	0	0	0	0
	RX[0:3]	1	1	1	VDD1V8 (0x33)	7B	1	1	1	1	0	1	1
	RX[4:7]	1	1	1	56K Pull Up (0x32)	7A	1	1	1	1	0	1	0
	RX[8:11]	1	1	1	200K Pull Up (0x31)	79	1	1	1	1	0	0	1
	RX[12:15]	1	1	1	GND (0x30)	78	1	1	1	1	0	0	0

3 Redriver placement

Depending on the use cases, PTN38007/PTN3816/PTN3944 should be placed with some pre-channel length and post-channel length in the system. The following sections depicts the most common configurations.

3.1 PTN3816/PTN3944 (single direction outputs)

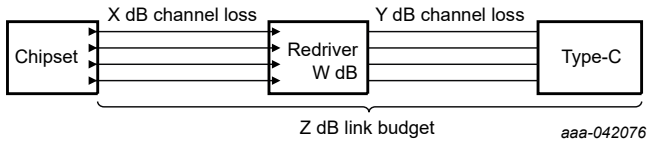


Figure 7. PTN3816/PTN3944 (single direction outputs)

- Pre-Channel (X) length: minimum: 2 inches, maximum 9 inches.
- Post-Channel (Y) length: about 1.5-2.0 inches

3.2 PTN3816/PTN3944 (single direction inputs)

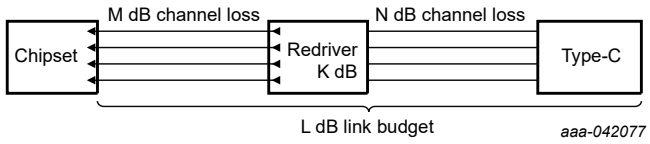


Figure 8. PTN3816/PTN3944 (single direction inputs)

- Pre-Channel (N) length: about 1.5-2.0 inches
- Post-Channel (M) length: minimum: 2 inches, maximum 9 inches.

3.3 PTN38007/PTN38003A (bidirectional input/outputs)

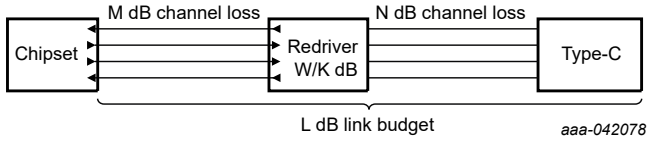


Figure 9. PTN38007/PTN38003A (bidirectional input/outputs)

- Pre-Channel (M) length: minimum: 2 inches, maximum 9 inches.
- Post-Channel (N) length: about 1.5-2.0 inches

3.4 PTN38007/PTN38003A (bidirectional input/outputs) with retimer

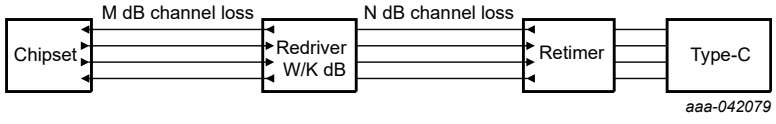


Figure 10. PTN38007/PTN38003A (bidirectional input/outputs) with retimer

- Pre-Channel (M) length: minimum: 2 inches, maximum 9 inches.
- Post-Channel (N) length: minimum: 2 inches, maximum 9 inches.

4 Layout guidelines

4.1 General differential layout guideline

Please refer to AN10798 for general differential layout guidelines.

High-speed transmission lines need to be designed with impedance matching in mind. These traces should be designed with 90Ω differential impedance. Signal trace length within the same differential pair should be equal. If it is difficult to achieve exact same length within the same differential pair, the mismatch in length should be minimized to no more than 3 mils.

High-speed signals should be routed over the top or bottom layer of a multi-layer PCB because signals travel faster on the buried microstrips than striplines. These signals should also not to be routed on the internal power/ground layers, or in the internal signal layers to avoid stubs created by the vias.

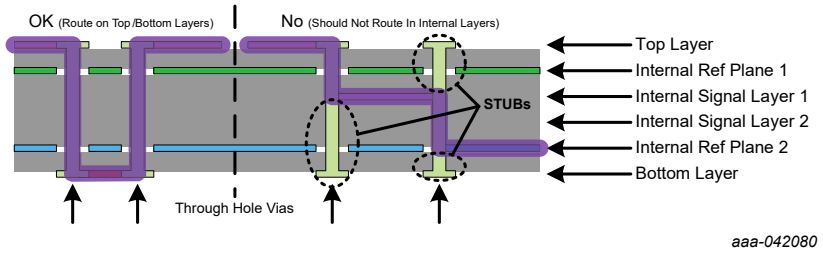


Figure 11. High-speed signal routing

Solid internal reference ground planes should be designed immediately underneath or above the high-speed transmission lines. The distance between the two differential traces should be kept equal as long as possible. Try to avoid vias in the transmission lines themselves. If it is required to use a via, make sure the trace branches to the vias are symmetrical, and oval-shape anti-pads should be used on all internal planes for transitional vias as shown below.

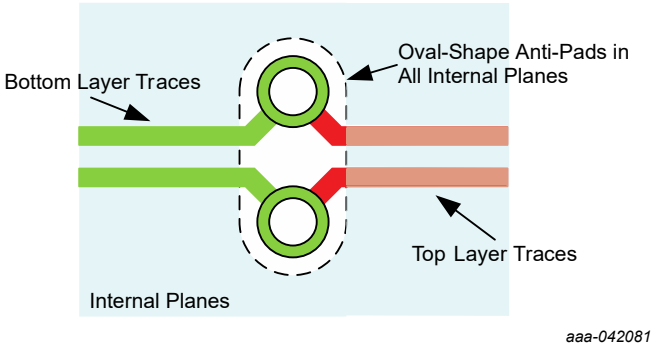


Figure 12. Transitional via routing

4.2 High-speed signal routing

PTN38007 pin assignments are defined in such a way that connection to Type-C connector can be minimized. High-speed traces should be routed between PTN38007 and Type-C connector with minimum layer transition. Whenever possible, route signals on the same layer.

In the layout example below, orange color traces are on the top layer, and blue traces are on the bottom layer. The AC caps can be placed on the same side as PTN38007, close to the chip. For traces connecting to RX2 and TX1 on the Type-C connector, the trace can be routed all on the top layer. For traces connecting to TX2 and RX1 on the Type-C connectors, because it is very difficult to fan out these signals only on the top layer, and vias are usually required. Try to minimize the total number of vias used on the traces. Usually two vias for each trace should be enough to complete the routing.

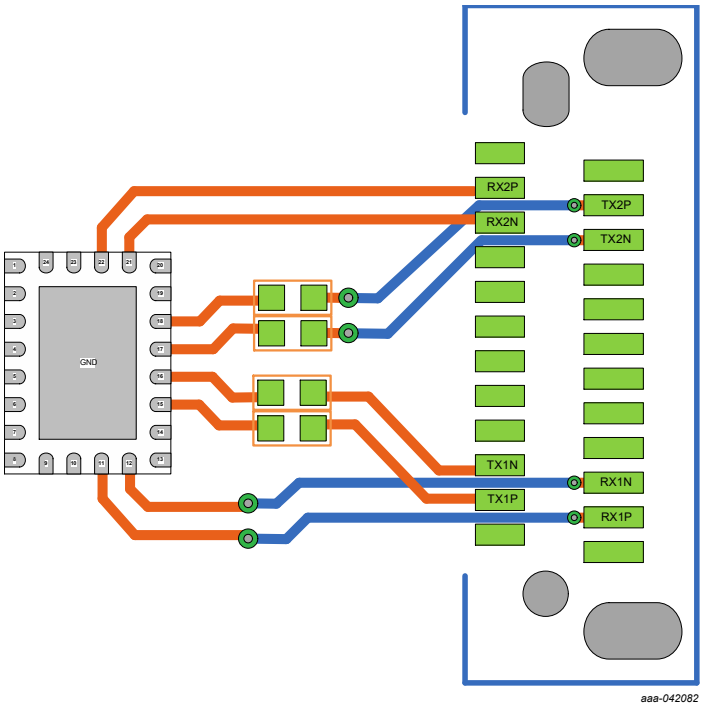


Figure 13. Layout example 1

In the next layout example below, even the RX1 signal pairs are routed with minimum number of vias, but the vias are not placed at the optimum position. This layout causes TX1 signal traces to have 2 extra vias that will impact the signal integrity. This should be avoided.

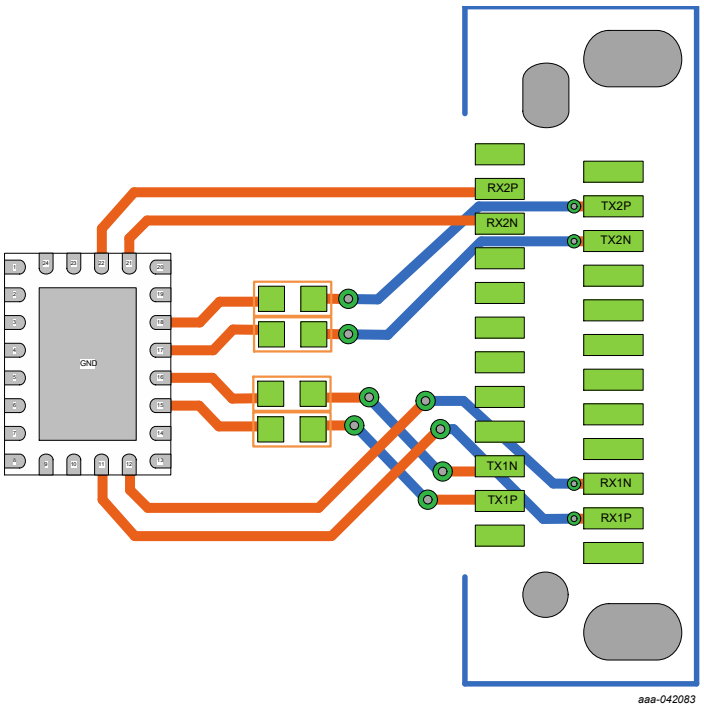


Figure 14. Layout example 2

4.3 Impedance matching across the AC capacitors

When these AC-Coupling capacitors are placed on the high-speed signals, impedance of the trace changes across these AC-Coupling capacitors. To minimize the impedance change, a void in the adjacent reference ground plane is required. The size of the void should be the same size of the capacitor's pad size.

In the below figure, the picture on the left side illustrates the top layer routing, with component pads showing in green color. The picture on the right side illustrates the inner ground layer. Directly under the component pads that are connected to high-speed signals, a void with same shape and same size of the pad are created in the inner ground layer. This void can also be applied under connector pads, or PTN38007's high-speed signal pin pads.

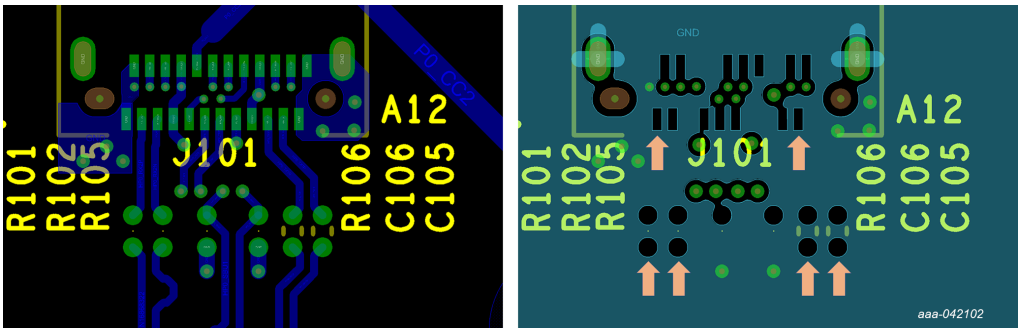


Figure 15. Top layer routing (left), inner ground layer (right)

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Tables

Figures

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