AN13320

NXP PMIC solution for XILINX UltraScale+ MPSoC ZU2/ZU3 Processor

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Document information

Information	Content
Keywords	Power solution, PMIC, FS56, FS85, PF81, PF71, PF5020, PF5024 Functional safety, Xilinx Zynq UltraScale+ MPSoC, ZU2, ZU3
Abstract	This application note shows two NXP PMIC solutions for powering a Xilinx Zynq UltraScale+ MPSoC ZU2/ZU3. The first one is a cost-optimized power solution using the FS56 and PF81. The second is a full performance power solution using the FS85, PF71, PF5024, and PF5020.

Revision History

Table 1. Revision history

Revision	Date	Description
AN13320 v.2	20220127	Minor update and corrections
Modifications	• Correct Figure 1 • Correct Table 3 • Add BYLink System Power Platform to list of references	
AN13320 v.1	20210901	Initial Release
Modifications	NA	

1 Introduction

The Xilinx Zynq UltraScale+ MPSoC ZU2/ZU3 is a high-performance smart-processing platform aimed at deep learning applications such as autonomous driving systems. Given the high number of power rails required, ZU2 and ZU3 systems present challenging power management demands. These conditions are further complicated by the need to meet additional power requirements for other components in the system. NXP's flexible Power Management ICs (PMIC) offer a total power solution that fully meets ZU2/ZU3 system requirements in a way that simplifies design and development.

NXP PMICs feature a built-in one-time programmable (OTP) memory that stores key startup configurations. Users define the OTP configuration based on their specific application requirements. The PMICs also feature a dedicated functional block for synchronizing power-up sequences from multiple PMICs. Thus, NXP Multi-PMICs function as “one chipset” in the system. This simplifies the design effort and reduces system complexity by eliminating the need for an external controller for system default voltage configurations and power-up sequence configurations.

This application note introduces two typical NXP PMIC designs for a ZU2/ZU3 device and its system. Table 2 shows the power solutions. Detailed PMIC power tree configurations, power-up sequences, and functional safety features are described in the sections that follow. Because of the PMIC's OTP capabilities, PMIC configurations can be customized to meet a customer's specific system requirements.

Table 2. Xilinx ZU2/U3 power solutions

Power supply consolidation	Functional safety level	NXP PMIC solution	
		Xilinx ZU2/ZU3 power supply	System power supply
Cost optimized power solution	QM	PF81	FS56 and PF81
Full performance power solution	ASIL-D/ASIL-B	PF71, PF5024 and PF5020	FS85, PF71, PF5024 and PF5020

2 Cost Optimized Power Solution

A cost-optimized power solution is a goal for always-on, Functional Safety QM-level applications. Table 3 defines a PF81 configuration for powering ZU2/ZU3 designs. PF81 is a low voltage input PMIC that includes seven buck outputs and four LDO outputs. The PF81 is capable of meeting all the power supply requirements for ZU2/ZU3 and DDR systems. For the PF81, maximum output currents are 2.5 A for each buck and 0.4 A for each LDO. PF81 Buck1, Buck2, and Buck3 are configured as three-phase buck regulators that support 7.5 A continuous current. The PF81's output voltage and power-up sequence are configured in OTP.

Table 3. Xilinx ZU2/ZU3 Cost-optimized power solution with PF81

Xilinx ZU2/ZU3 power rail		PF81 output power configuration			
Rail	Symbol	Output channel	Output/voltage/ V	Current Capability/A	Power-up sequence
Rail 1	VCCINT, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR, VCINT_IO, VCCB RAM	BUCK1 – BUCK3	0.85	7.5	1

Table 3. Xilinx ZU2/ZU3 Cost-optimized power solution with PF81*...continued*

Xilinx ZU2/ZU3 power rail		PF81 output power configuration			
Rail	**Symbol**	**Output channel**	**Output/voltage/ V**	**Current Capability/A**	**Power-up sequence**
Rail 2	VCC_PSAUX, VCC_PSADC, VC_PSDDR_PLL, VCCAUX, VCCAUX_IO, VCCAD	BUCK7	1.8	2.5	2
Rail 3	VCC_PSPLL	BUCK5	1.2	2.5	2
Rail 4	VCCO_PSDDR	BUCK5	1.2	2.5	2
Rail 5	VCC_PSIO[0:3]	LDO3	1.8	0.4	3
Rail 6	VPS_MGTRAVCC	BUCK4	0.85	2.5	2
Rail 7	VPS_MGTRAVTT	LDO2	1.8	0.4	3
NA	VPP(DDR)	BUCK6	0.6	2.5	3
NA	VTT(DDR)	LDO1	2.5	0.4	3

Normally, an MCU is used in ZU2/ZU3 automotive autonomous driving applications. Figure 1 shows an NXP PMIC solution using an FS56 and a PF81 to power an MCU in a ZU2/ZU3 system. The FS56 is a high voltage PMIC that supports 12 V vehicle battery systems. It includes two buck outputs, one powering the MCU and the other powering the PF81. The MCU uses the I^2C interface to configure the FS56 and the PF81 registers. Both the FS56 and the PF81 have a PGOOD pin that notifies the MCU whether the PMIC power supply output is good. The MCU controls the power on request for the PF81 through the PF81's PWRON pin. FS56 and PF81 are QM-level for this design. NXP also offers P2P-compatible ASIL-B level devices.

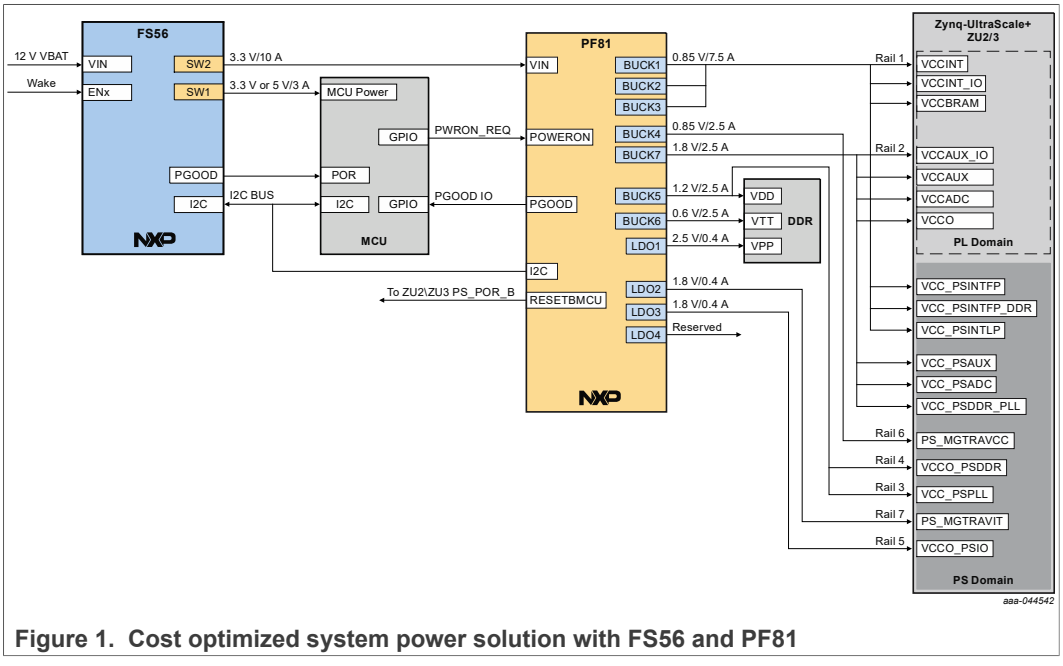

Figure 1. Cost optimized system power solution with FS56 and PF81

3 Full Performance Power Solution

Some ZU2/ZU3 applications must be capable of entering an ultra-low power/reduced function state in order to maximize battery life or to reduce overall power consumption. In addition, autonomous driving applications require Functional Safety features. A full performance power solution must support low power mode requirements and must meet

the Functional Safety requirements for ASIL-D/B systems. The FS85/PF71/PF5020/PF5024 PMIC solutions presented in this section are intended to aid designers in meeting those requirements for ZU2/ZU3-based systems.

3.1 Power solution

Table 4 defines a PF71/PF5024/PF5020 power supply configuration for a Xilinx ZU2/ZU3 design. PF71 contains five high-efficiency buck converters and two LDOs with load switch options. PF5020 contain three buck converters and one LDO. PF5024 has four buck converters. Each PF71, PF5020 and PF5024 buck converter is rated up to 2.5 A and the linear regulator is rated up to 0.4 A. By using dedicated regulators for different rails, this power solution separates the ZU2/ZU3 power rails, thereby allowing different low power modes of operation and reducing power consumption.

Table 4. Xilinx ZU2/ZU3 full performance power solution with PF71/PF5024/PF5020

Xilinx ZU2/ZU3 power rail		PMIC output power configuration			
Rail	**Symbol**	**Output channel**	**Output/voltage/V**	**Current Capability/A**	**Power-up sequence**
Rail 1	VCC_PSINTLP	PF71 BUCK1	0.85	2.5	1
Rail 2	VCC_PSAUX, VCC_PSADC	PF71 BUCK2	1.8	2.5	2
Rail 3	VCC_PSPLL	PF71 LDO1	1.2	0.4	2
Rail 4	VCC_PSIO[0:3]	PF71 LDO2	1.2	0.4	3
Rail 5	VCC_PSINTFP, VCC_PSINTFP_DDR	PF5024 BUCK3 – BUCK4	0.85	5.0	1
Rail 6	VCC_PSDDR_PLL	PF5020 LDO1	1.8	0.4	2
Rail 7	VCCO_PSDDR	PF71 BUCK3	1.2	2.5	3
Rail 8	VCCINT, VCCINT_IO, VCCBRAM	PF5024 BUCK1 – BUCK2	0.85	5.0	1
Rail 9	VCCAUX, VCCAUX_IO, VCCADC	PF5020 BUCK3	1.8	2.5	2
Rail 10	VPS_MGTRAVCC	PF5020 BUCK1	0.85	2.5	2
Rail 11	VPS_MGTRAVTT	PF5020 BUCK2	1.8	2.5	3
NA	VTT(DDR)	PF71 BUCK4	0.6	2.5	3
NA	VPP(DDR)	PF71 BUCK5	2.5	2.5	3

Figure 2 shows a typical architecture for an autonomous driving ECU that requires Functional Safety. The FS85 and the ASIL-D MCU are the ASIL-D domain for the decision and control function. The PF71/PF5024/PF5020 combination powers the ZU2/ZU3 in the ASIL-B domain. The FS85 is a high-voltage PMIC that supports 12 V or 24 V battery systems. It is designed for ASIL-D systems that power and secure an ASIL-D MCU. The FS85 has multiple outputs for powering the MCU and its peripherals (e.g. CAN, Ethernet and Memory). In addition, the FS85 provides input power to low-voltage PMICs through the Vpre pin. PF71,PF5024,PF5020 are ASIL-B ready for this design. All PMICs in this solution have Functional Safety features integrated within the device, which significantly reduces the Functional Safety system development effort.

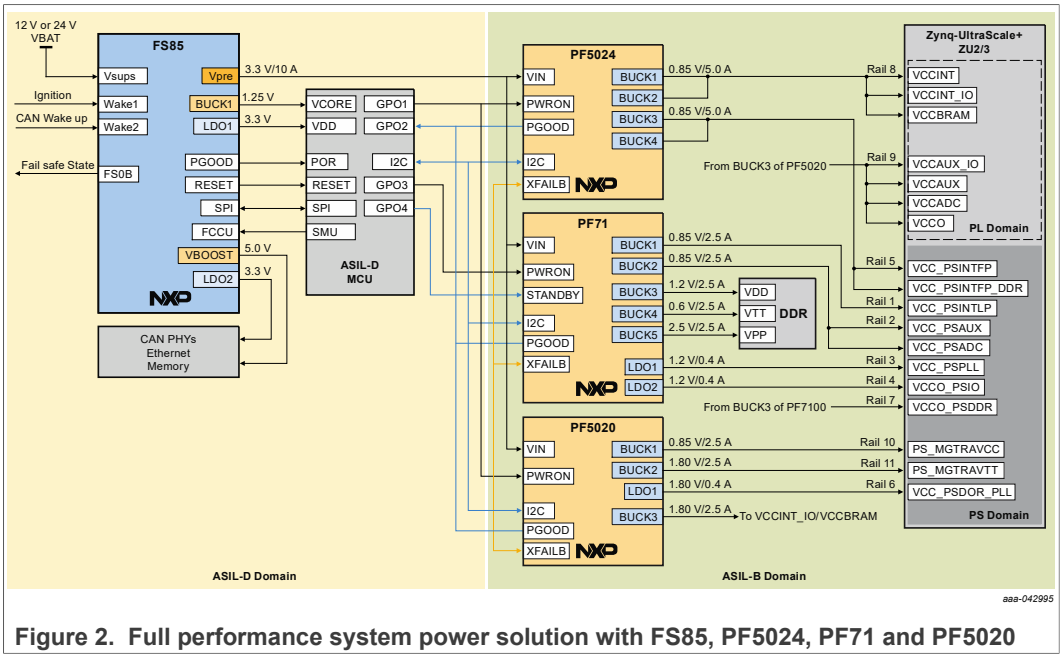

Figure 2. Full performance system power solution with FS85, PF5024, PF71 and PF5020

Table 5 details the I/O connection between the PMIC and the ASIL-D MCU. The PF71, PF5020 and PF5024 power-ups are triggered by the ASIL-D MCU with the PMIC PWRON pin. This combination of devices acts as “one PMIC” for power up/down sequences through the NXP PMIC internal power-up sequencer PWRON and XFAILB functions. The multiple PMICs effectively synchronize accurate power-up and power-down sequencing for all power rails by the PMIC itself without the need for MCU control.

Table 5. Xilinx ZU2/ZU3 connection with PF71, PF5024 and PF5020

PMIC	ASIC-D MCU	Block	Function
FS85 PGOOD	POR	IO	FS85 power good output that connects to MCU hardware reset
FS85 RESET	RESET		FS85 reset output that connects to MCU software reset
FS85 FCCU	SMU		FS85 monitor MCU hardware fault
PF5024 & PF5020 PWRON	GPIO1		PF5024 and PF5020 power-on input request by MCU
PF5024 & PF5020 & PF71 PGOOD	GPIO2		PF5024, PF5020 and PF71 input indicator
PF71 PWRON	GPIO3		PF5024&PF5020&PF71 power good indicator
PF71 STANDBY	GPIO4		PF71 standby mode input request by MCU
FS85 SPI	SPI	Communication	SPI bus communication for FS85 and MCU
PF5024 & PF5020 & PF71 I2C	I2C		I^2C bus communication for PF5024, PF5020 and MCU

4 Functional Safety

NXP PMICs are developed in compliance with the ISO26262 standard. All FS85, PF71, PF5024 and PF5020 devices have embedded safety mechanisms that include the following functional safety features:

- **Independent voltage monitoring and fault detection**: The PMICs listed above offer independent fault monitoring per regulator. UV, OV and ILIM faults are monitored by

the PMIC fault monitor block. The PMICs indicate the output state of each regulator through the PGOOD pin

- **I^{2}C CRC and write protection**: The I^{2}C secure write function provides safety mechanisms that protect secure registers against invalid operations.
- **Analog built-in self-test (ABIST)**: Each time the ZU2/ZU3 system powers up, the PMICs initiate an ABIST process on all output voltage monitors before allowing the power-up sequence to proceed. ABIST checks the state of the voltage monitoring block (OV/UV) of each regulator to assure that it is functioning normally. If a failure on the OV/UV monitor is detected during the ABIST, the PMIC asserts the corresponding ABIST flag.
- **Functional safety output**: When the PMIC detects a critical fault, such as an incorrect regulator output or a WD failure, the FS85's FSOB pin is used to transition the system into a safe state.
- **Logic build-in self-test (LBIST, FS85 only)**: LBIST verifies the functionality of the safety logic monitoring functions. The FS85 performs an LBIST after power-up or wake up from Standby mode.
- **External voltage monitor (FS85 only)**: The FS85 contains up to four voltage monitors that can be used to monitor FS85 supply rails or PF device regulators. Depending on the safety requirements, VMON can be used to monitor PF device for each of the system ASIL-D safety levels.
- **MCU failure monitoring (FS85 only)**: The FS85 features two input pins (FCCU1 and FCCU2) dedicated to monitoring safety hardware failures in the MCU. The FCCU pins connect to the MCU's fault output I/O. When the FS85 detects an MCU hardware failure through the FCCU pins, the FS85 FS0B\RSTB pin is asserted.
- **External IC monitoring (FS85 only)**: The FS85 features an ERRMON input pin for monitoring the application's external safety IC.
- **Challenger watchdog monitoring (FS85 only)**: The challenger watchdog uses a question/answer strategy to monitor MCU safety.

Figure 3 shows a functional safety signal configuration based on ASIL-D/B safety requirements for a ZU2/ZU3 system.

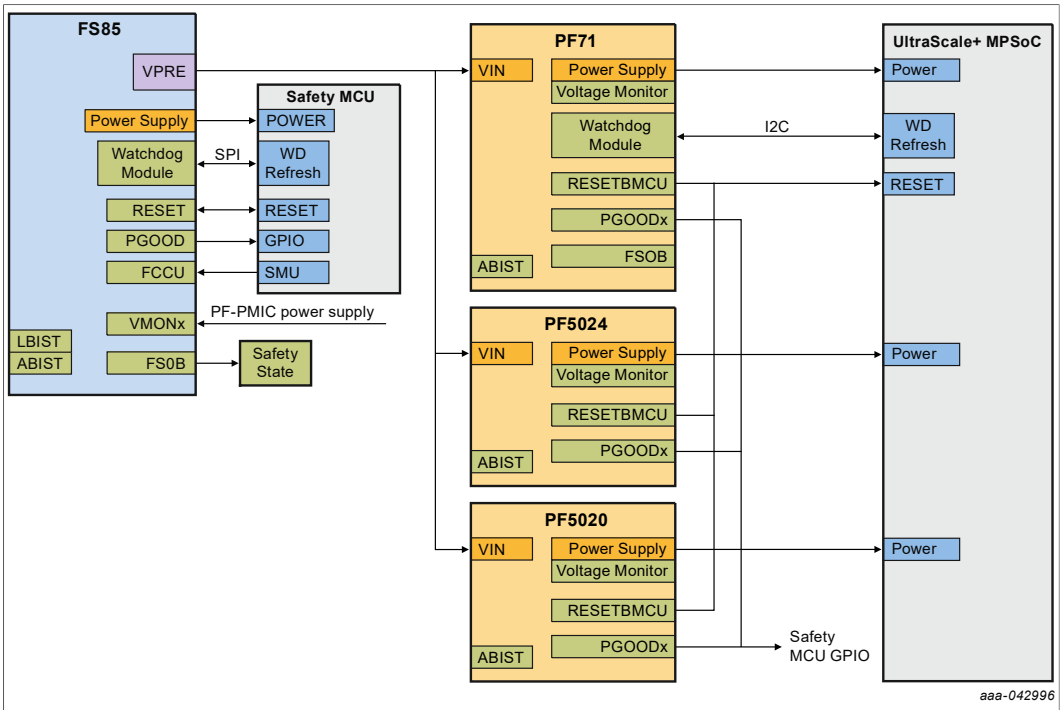

Figure 3. ASIL-D/B functional safety operation for Xilinx ZU2/ZU3

5 References

[1] FS56 webpage — includes documentation and tools (Data sheet, Safety Manual, FMEDA, SW driver)

[2] FS85 webpage — includes documentation and tools (Data sheet, Safety Manual, FMEDA, SW driver)

[3] PF81 webpage — includes documentation and tools (Data sheet, Safety Manual, FMEDA, SW driver)

[4] PF71 webpage — includes documentation and tools (Data sheet, Safety Manual, FMEDA, SW driver)

[5] PF5020 webpage — includes documentation and tools (Data sheet, Safety Manual, FMEDA, SW driver

[6] PF5024 webpage — includes documentation and tools (Data sheet, Safety Manual, FMEDA, SW driver

[7] Power Management Community

[8] BYLink System Power Platform

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