AN13462

PTN3222 layout guidelines

Rev. 1.0 — 13 December 2021 Application note

Document information

Information	Content
Keywords	PTN3222, eUSB2 Redriver, eUSB2 to USB2, Layout Guideline
Abstract	PTN3222 is a 1-port eUSB2 to USB2 redriver IC that performs translation between eUSB2 and USB2 signaling schemes. It is meant to be used in systems that have eUSB2 interface on one side and USB2 interface on the other side. It supports host role only, device role only or dual role repeater function. This application note details the layout guidelines to ensure the optimal operation of the device.

Revision history

Rev	Date	Description
v.1.0	20211213	Initial version

1 Introduction

As silicon technology continues to scale down and device dimensions get smaller, the manufacturing cost for an advanced process technology to support 3.3 V IO signaling has grown exponentially. A low voltage eUSB2 solution is introduced to address the following:

- Eliminates the need for the USB2.0 on the SoC to support 3.3V IO.
- Reduces the PHY analog content - digital mechanisms are employed for PHY functions such as disconnect detect.
- A mechanism is defined to convert eUSB2 signaling to USB2.0 signaling. eUSB2 redriver such as the PTN3222 is designed specifically to use such a mechanism to allow eUSB2 to support USB2.0 connections.
  This application note details the general PCB layout guidelines for PTN3222 eUSB2 to USB2.0 redrive application to minimize signal integrity issues.

2 PTN3222 eUSB2 redriver layout guidelines

To ensure optimal performance and reliability of the device, the following PCB layout guidelines are recommended.

2.1 Power and ground

- A minimum four-layer PCB stack-up is required.
- The eUSB2 redriver should be placed top of a solid, continuous ground plane.
- Preferably, the power for the eUSB2 redriver should come directly from the power plane underneath it, but if the power trace must be used then the trace should be at least 20 mil wide.

2.2 Bypass capacitors

Bypass capacitors of 0.47 µF and a 33 pF should be placed as close as possible to VDD1V8 and VDD3V3 pins with a very short PCB trace.

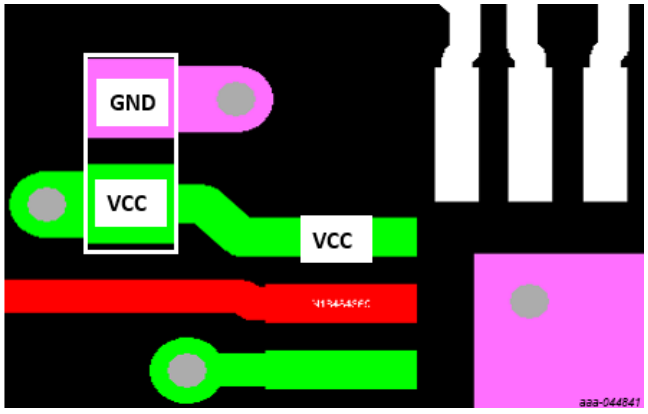

Figure 1. Bypass capacitor placement

2.3 AGND and DGND pins connection

Connect AGND and DGND pins of the PTN3222 to the same ground plane.

2.4 eUSB2 electrical specifications

Table 1. eUSB2 electrical specification

Parameter	Min	Typical	Max	Unit
Transmit source termination impedance	32	40	80	ohm
Receiver differential termination (repeater)	72	80	88	ohm
PCB trace differential impedance		85		ohm
PCB trace differential impedance tolerance			15	%
Host to repeater insertion loss			-1.2	dB
Repeater to connector insertion loss			-2.0	dB

Table 2. USB2.0 electrical specification

Parameter	Min	Typical	Max	Unit
PCB trace differential impedance		90		ohm
PCB trace differential impedance tolerance			15%	

2.5 eUSB2 and USB2.0 PCB trace routing

eUSB2 specification specifies PCB trace differential impedance of 85 Ω ±15 %, and USB2.0 specification specifies 90 Ω ± 15 %. To use the same PCB stack-up, trace width and trace to trace spacing it is recommended to route the differential trace of 85 Ω for both eUSB2 and USB2.0.

The eUSB2 PCB trace insertion loss between the host and the repeater, between the repeater and the connector are listed in Table 1. The PCB trace length must be kept such that the insertion loss is lower than specified. In general, the PCB trace length should be kept to less than 10 inches.

The PTN3222 eUSB2 and USB2.0 differential pins are optimized to allow direct PCB routing to eUSB2 host/peripheral without any via. Therefore, it is strongly recommended to not place any via in the path.

When routing PCB traces, it is critical to keep the trace width the same to keep the trace impedance constant from the driver and the receiver. Any trace width deviation will create impedance mismatch and will create signal reflection. Avoid using 90-degree angle and use 45-degree bend when the trace must be routed perpendicularly.

Maintain the same differential spacing between the differential traces at all time. Failure to maintain the same differential spacing will result in impedance mismatch, hence reflection.

Minimize the length of high-speed clock and periodic signal traces that run parallel to the high-speed eUSB2 and USB2.0 lines to minimize crosstalk. The spacing (D) between

pairs and to all other signals should be at least four times the dielectric height (h). If the other signals have significantly higher voltage levels or edge rate than the differential signal, the space should increase to 30 mil in order to avoid coupling.

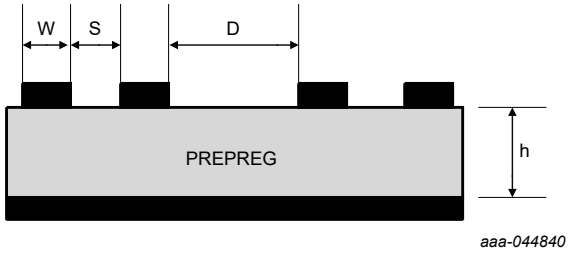

Figure 2. Differential pair to pair spacing

2.6 eUSB2 PCB trace length matching

eUSB2 specification Rev 1.1 specifies differential skew of 500 pS max for the transmitter. Subtracting the transmitter output driver skew and allow to allow skew guard band, the differential length should be matched within 50 mil. When serpentine is used to match the length, the matching should be made as close as possible to the point where the mismatch occurred

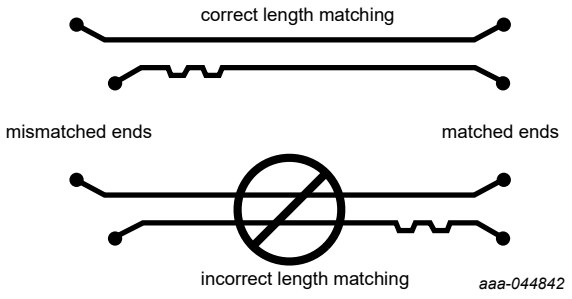

Figure 3. Length matching near location of the mismatch

3 Summary

Proper PCB layout is critical for the success of the PTN3222 operation. All high-speed PCB rules, techniques, component placement and trace routing must be followed and taken into consideration during the PCB layout phase. The following is the summary of the guideline:

- The differential pair must be routed symmetrically. Keep all differential signal traces the same length. The difference in trace length should be less than 20 mils.
- Maintains 85 Ω differential impedance.
- Do not route high speed signals over any plane split; use only one ground plane underneath the differential signals.
- Avoid any discontinuity for signal integrity. Differential pairs should be routed on the same layer. The number of vias on the differential traces should be minimized (preferably none). Test points should be placed in series and symmetrically. Stubs should not be introduced on the differential pairs.

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