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NXP PMIC solution for TI Sitara AM62x and AM62Ax processors

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Document information

Information	Content
Keywords	Power solution, power management integrated circuit (PMIC), PF71, FS86, Texas Instruments (TI) Sitara, AM62x, AM62Ax, processor, Industrial, Automotive, Security, Functional Safety
Abstract	NXP offers a complete power solution with PF71/(FS86+PF71) for TI Sitara AM62x/AM62Ax processors. This document details power tree, functional safety to simplify customer design with PF71 from 3.3 V/5 V or with FS86+PF71 from 12 V/24 V batteries.

Revision history

Revision	Date	Description
1	20231026	Initial version

1 Introduction

This application note presents the NXP PF7100 PMIC solution for TI Sitara AM62x and AM62Ax processors. This application note introduces PF7100 key features and functions to work with the TI processor, which includes a power tree with DDR4/LPDDR4 and functional safety. The detailed connections between the Sitara and PMIC are also highlighted. Furthermore, if the customer wants to use the AM62x/AM62Ax with 12 V/24 V input, this document also introduces a system power solution using FS86+PF7100.

2 PF7100 PMIC

The PF7100 device is an NXP multichannel PMIC device designed to be used for high-performance automotive and industrial applications. The PF7100 is also highly configurable, making it an appropriate companion and fit for various system-level power requirements. The PF7100 integrates independent voltage monitoring circuits to ensure compliance with ISO 26262 standard and functional safety up to ASIL B. The PF7100 is also available as a standard non-safety device for industrial applications.

The PF7100 is a PMIC with less than 5 V input. The PF7100 is suitable for a variety of applications including infotainment, ADAS, vision, and radar, either as a standalone power solution or as a companion to another NXP PMIC, such as the FS86.

The PF7100 supports customized OTP (one time programmable) definition to fit for processors' and peripherals' power and safety requirements.

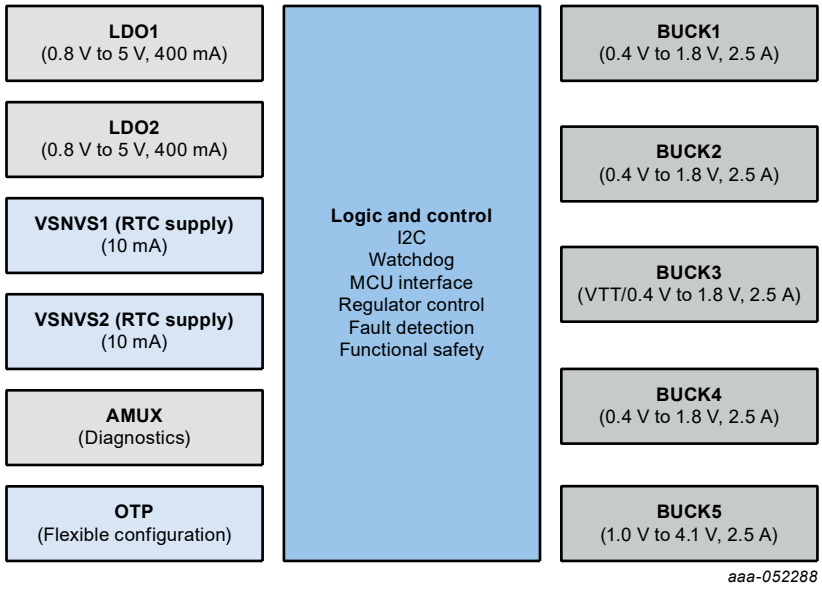

Figure 1. PF7100 PMIC block diagram

3 FS86 PMIC

The FS86 PMIC family is an automotive, functionally safe multi-output power supply integrated circuit. It includes multiple switch modes and linear voltage regulators, enhanced safety features with fail-safe outputs. This makes it a full part of a safety-oriented system to ASIL B, or even ASIL D. The device can operate at a maximum of 60 V input.

The FS86 is part of a complete family of devices that offers scalability in power and safety. FS86 is developed in compliance with the ISO 26262 standard and is qualified according to AEC-Q100 requirements.

The FS86 family also supports customized OTP (one time programmable) definition fit for processors' and peripherals' power and safety requirements.

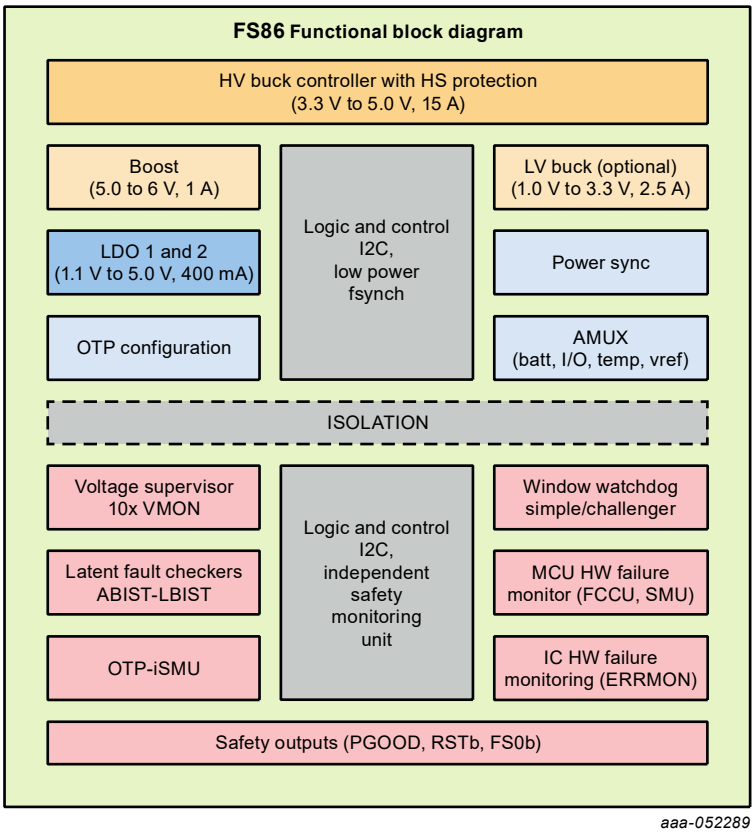

Figure 2. FS86 family devices function block diagram

4 TI Sitara AM62x and AM62Ax processors

The TI AM62x Sitara family of application processors is built for Linux application development, with scalable Arm Cortex-A53 performance and embedded features, such as dual-display support and 3D graphics acceleration, along with an extensive set of peripherals. These features make the AM62x device well suited for a broad range of industrial and automotive applications, while offering intelligent features and optimized power architecture, as well.

The AM62Ax is an extension of the TI Sitara automotive-grade family of heterogeneous Arm processors with embedded deep learning, video and vision processing acceleration, display interface, extensive automotive peripheral, and networking options. The AM62Ax is built for a set of cost-sensitive automotive applications, including driver and in-cabin monitoring systems, next generation eMirror systems, multiple sensor modalities in standalone electronic control units (ECU), as well as a broad set of industrial applications in factory automation, building automation, and other markets.

Table 1. Description of AM62x and AM62Ax

Device	Description
AM62x	A53: Single/Dual/Quad Core, M4F: Single core as functional safety optional, 3D graphics engine
AM62Ax	A53: Single/dual/quad core, MCU_R5F: Single core as functional safety optional, hardware security module, deep learning accelerator is up to 2 TOPS

5 Power solutions

In designing, from the AM62x/AM62Ax point of view, there are several considerations to take account, for example, the input system voltage, the memory type, the SD card participation, low-quiescent current supporting and functional safety, and so on. For the many different configurations, NXP PMICs have an OTP function to customize each configuration and play roles, designing a robust power solution.

If the input is intermediate voltage (3.3 V/5 V), the PF7100 can meet AM62x/AM62Ax series processors' requirement of power supply and functional safety goal. If the input is battery (12 V/24 V) using in vehicle, putting an FS86 in front is an appropriate selection.

5.1 Case 1: VIN = 3.3 V/5 V, LPDDR4 memory

Figure 3 shows the PF7100 powering the AM62x/AM62Ax processors on-system with a 5 V/3.3 V input supply and LPDDR4 memory. The VDD_CORE needs 3500 mA maximum current in the automotive application at 125 °C. The BUCK1 and BUCK2 can be configured as dual phase that can support 5 A maximum. For the power supply of LPDDR4, the BUCK4 should be configured as 1.1 V. If the input is 5 V, LDO1 of PF7100 should be configured as a load switch in the second power sequence. If the input is 3.3 V, the LDO is OK for the output. If using an SD card, a switch reserve is needed in the circuit. The switch can be controlled by a GPIO of AM62x/AM62Ax.

The sequence of each power rail can be configured as below in the OTP.

With regard to the interface, PF71 supports I^2C communication, and has an interrupt control, MCU reset pin, PGOOD, and so on. The STANDBY pin can be controlled by the AM62x/AM62Ax, when the system enters Low-Power mode. The VSELECT pin is an input pin used to select the output voltage of LDO2. When configured, the bit VSELECT_EN = 1 could select the LDO2 as 3.3 V/1.8 V. The WDI pin is an input pin to the PF7100 and is intended to operate as an external watchdog monitor. The pin can work with RESETSTATz of AM62x/AM62Ax to warm reset.

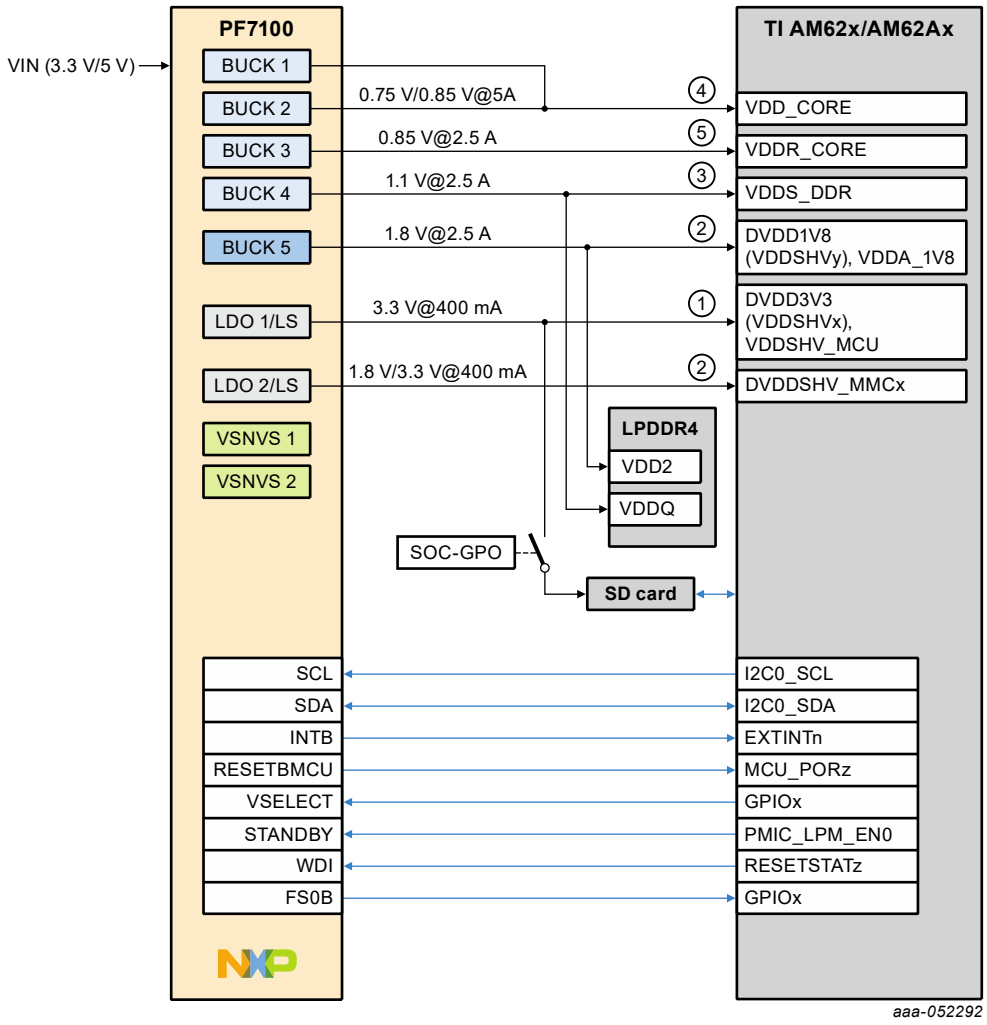

Figure 3. PF7100 powering AM62x/AM62Ax with LPDDR4

5.2 Case 2: VIN = 3.3 V/5 V, DDR4 memory

Figure 4 shows the PF7100 powering the AM62x/AM62Ax processor on-system with 5 V/3.3 V input supply and DDR4 memory. For the power supply of DDR4, the BUCK4 should be configured as 1.2 V as the DDR4 VDDQ power supply, and the voltage reference (VREF) can be divided the 1.2 V by the same impedance of R1 and R2. In this solution, the VPP should be powered by an external LDO, which is enabled by the LDO1 of PF7100. Other power rails are the same as Case 1.

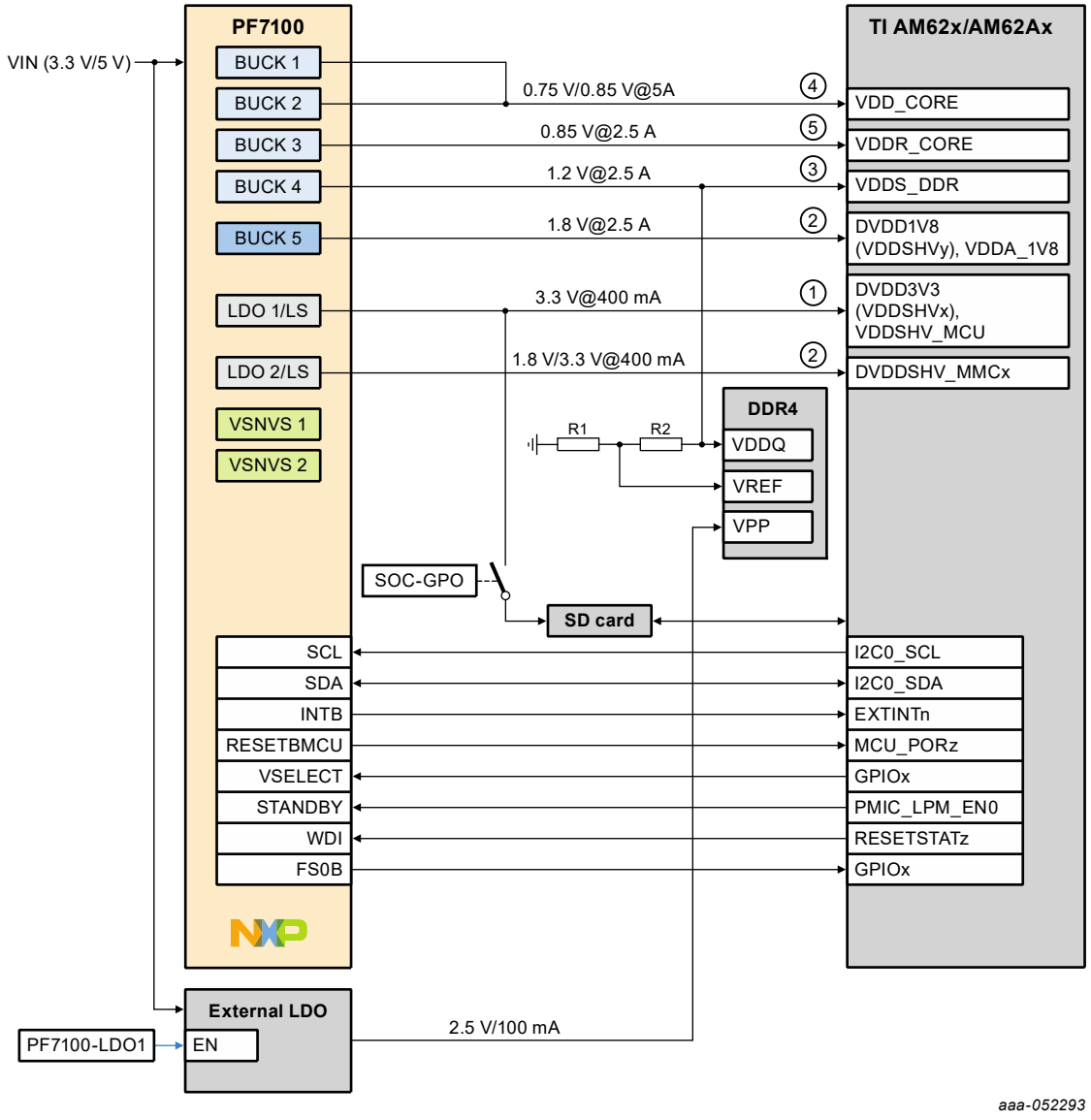

Figure 4. PF7100 powering AM62x/AM62Ax with DDR4

5.3 Case 3: VIN = 12 V/24 V, LPDDR4 memory

Figure 5 shows the FS86+PF7100 powering the AM62x/AM62Ax processor on-system level with 12 V/24 V input supply and LPDDR4 memory. The FS86 can support both 12 V or 24 V battery input directly. The FS86 has 2*LDO, that one LDO can power the SD card directly. No switcher is needed. Another LDO can operate as the peripheral's power supply.

The FS86 family of devices has many interfaces. The FS86 can support both I^2C and serial peripheral interface (SPI) communications. The FS86 has interrupt control, an MCU reset pin, PGOOD, and so on. The FS86 has an XFAILB function that can be used to synchronize the power-up and power-down sequences with the PF7100.

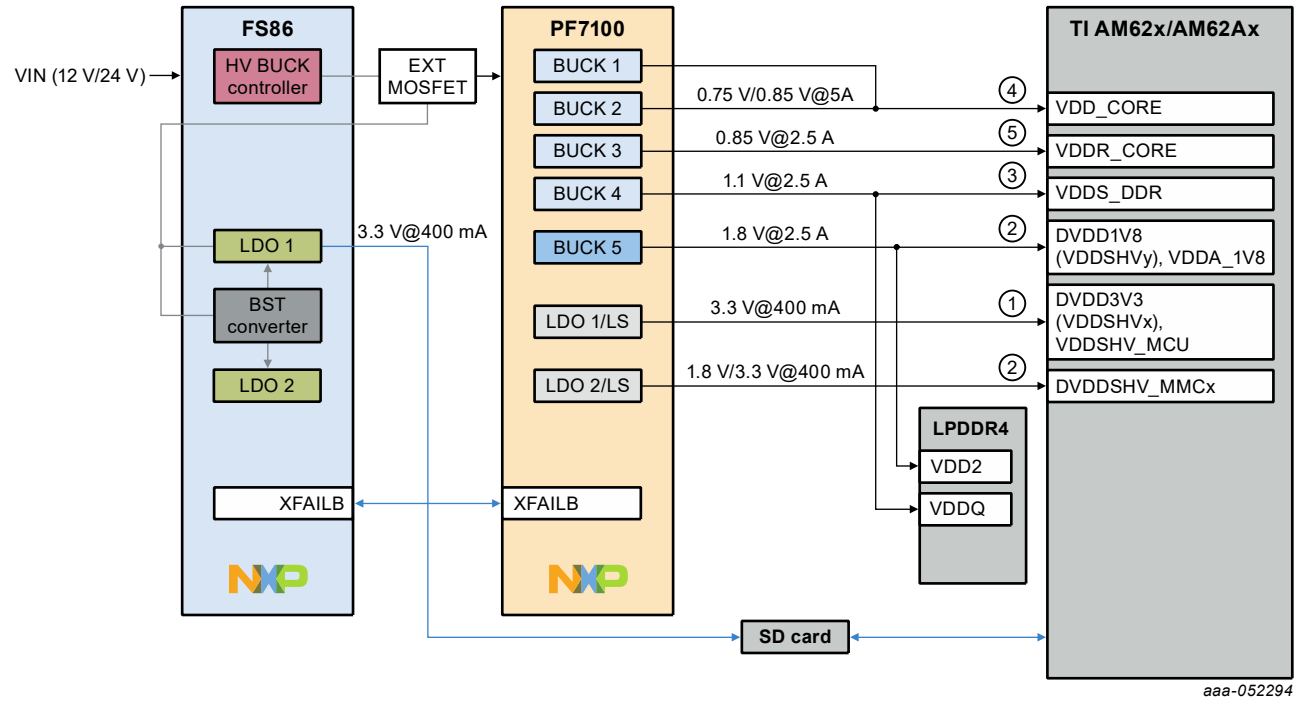

Figure 5. FS86+PF7100 powering AM62x/AM62Ax with LPDDR4

5.4 Case 4: VIN = 12 V/24 V, DDR4 memory

Figure 6 shows the FS86+PF7100 powering the AM62x/AM62Ax processor on-system level with 12 V/24 V input supply and DDR4 memory. The two low dropouts (LDO) can supply power to SD card, and also supply power to the VPP of DDR4. In this way, the external LDO is not needed.

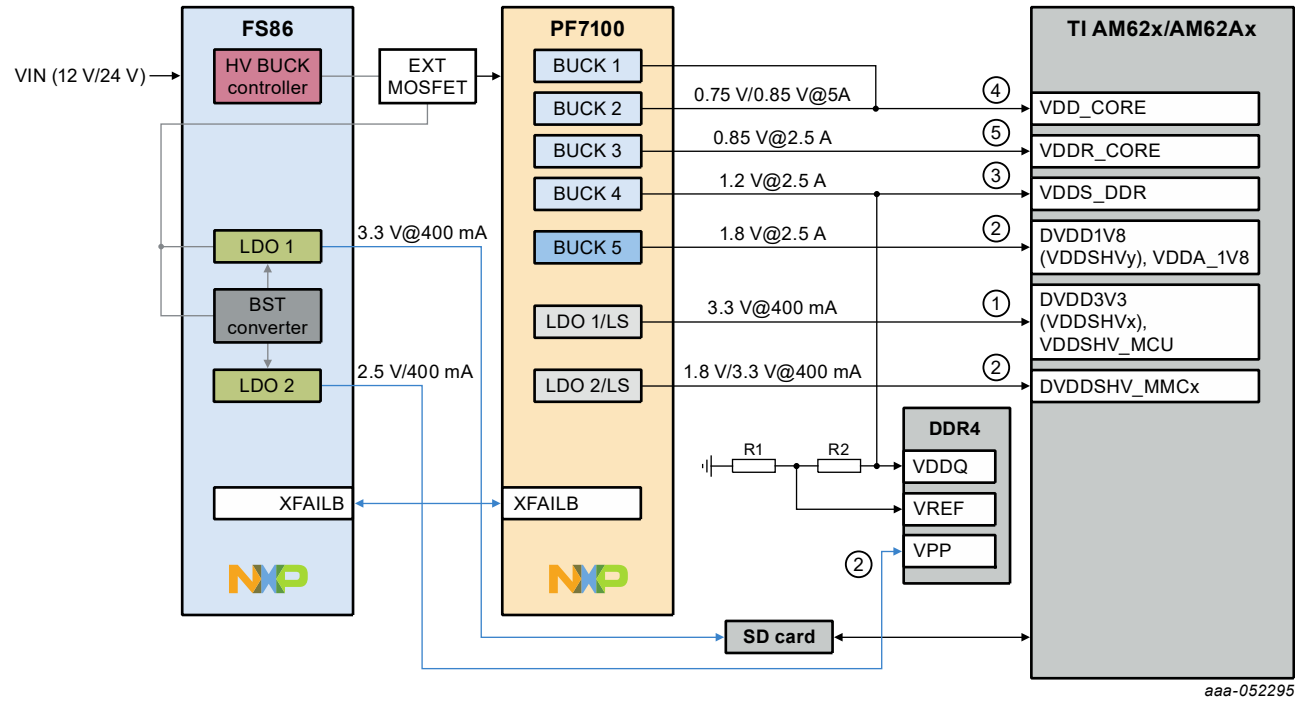

Figure 6. FS86+PF7100 powering AM62x/AM62Ax with DDR4

5.5 Power-up and power-down sequence

AM62x/AM62Ax have fixed power-up and power-down sequences according to different work modes. Refer to the AM62x/AM62Ax data sheet. FS86+PF7100 can be arranged in different configurations. For most applications, its power-up and power-down sequences follow Figure 7 and Figure 8. When the system is powered by below 5 V, the FS86 sequence can be ignored.

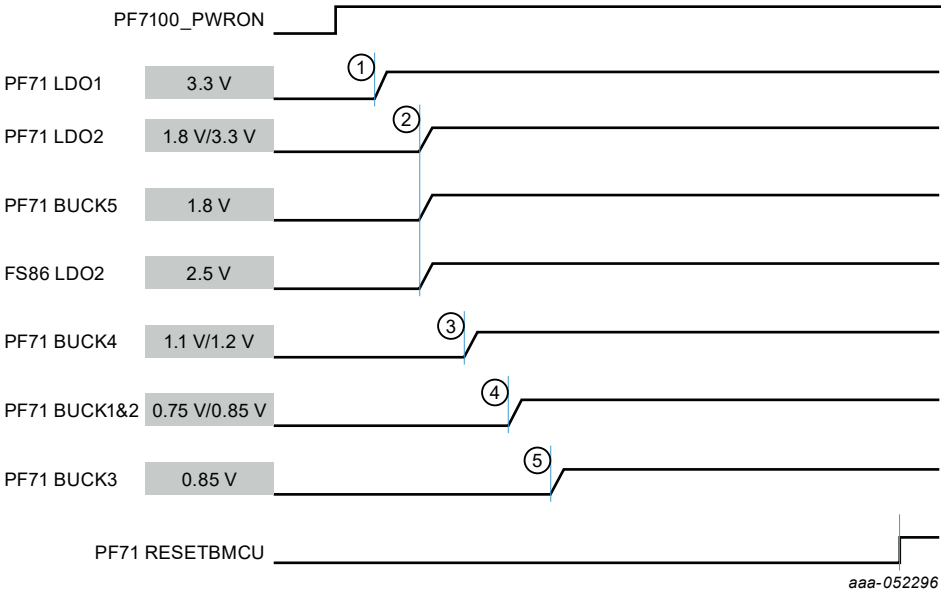

Figure 7. FS86+PF7100 powering AM62x/AM62Ax power-up sequence

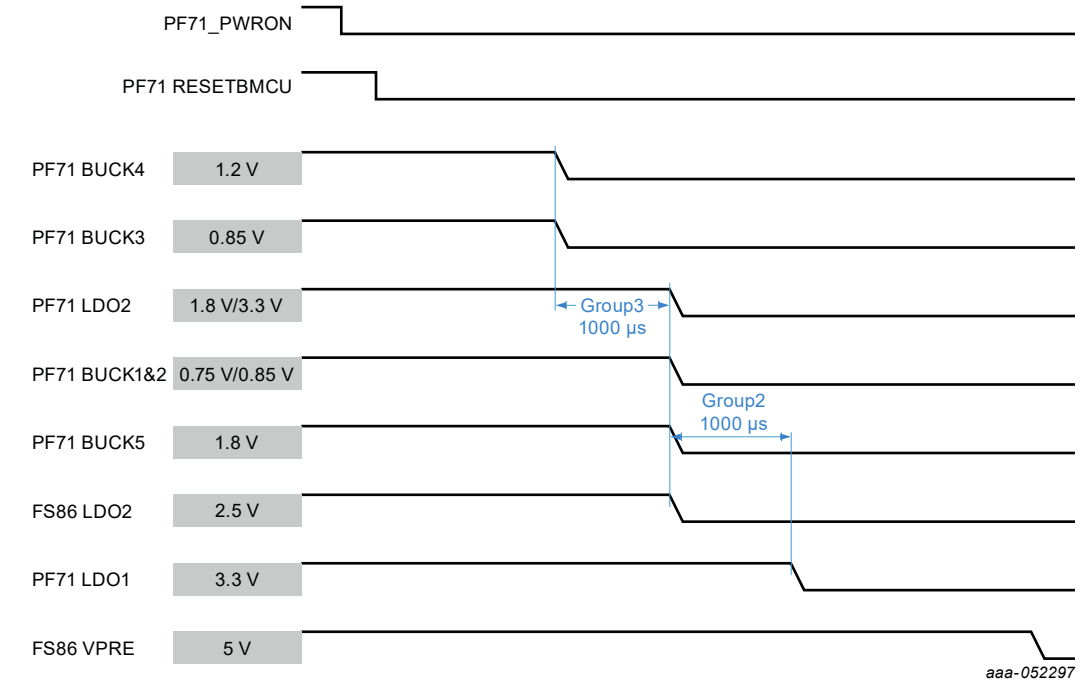

Figure 8. FS86+PF7100 powering AM62x/AM62Ax power-down sequence

6 Functional safety

The FS86 family and PF7100 devices are embedded safety mechanism and NXP PMICs that meet ISO 26262 standard. The PF7100 is up to ASIL B. The FS86 is up to ASIL D. The safety mechanism includes the following functional safety features:

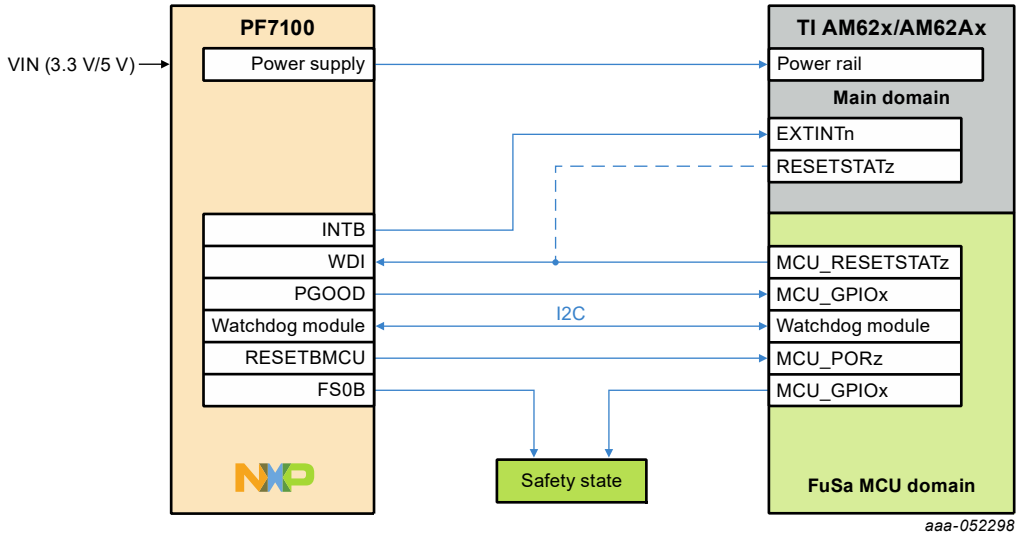

Figure 9. System ASIL B safety mechanism

Table 2. Low voltage input connection with system ASIL B

	PF7100	TI AM62x/AM62Ax	Function
1	INTB	EXTINTn	Interrupt event occurs from PF71
2	WDI	RESETSTATz/MCU_RESETSTATz	Main/MCU Domain warm reset
3	PGOOD	MCU_GPIOx	Indicator of power good
4	I2C	I2C	Communication and Watchdog Module
5	RESETBMCU	MCU_PORz	MCU and Main Domain cold reset
6	FS0B	MCU_GPIOx	Safety state output

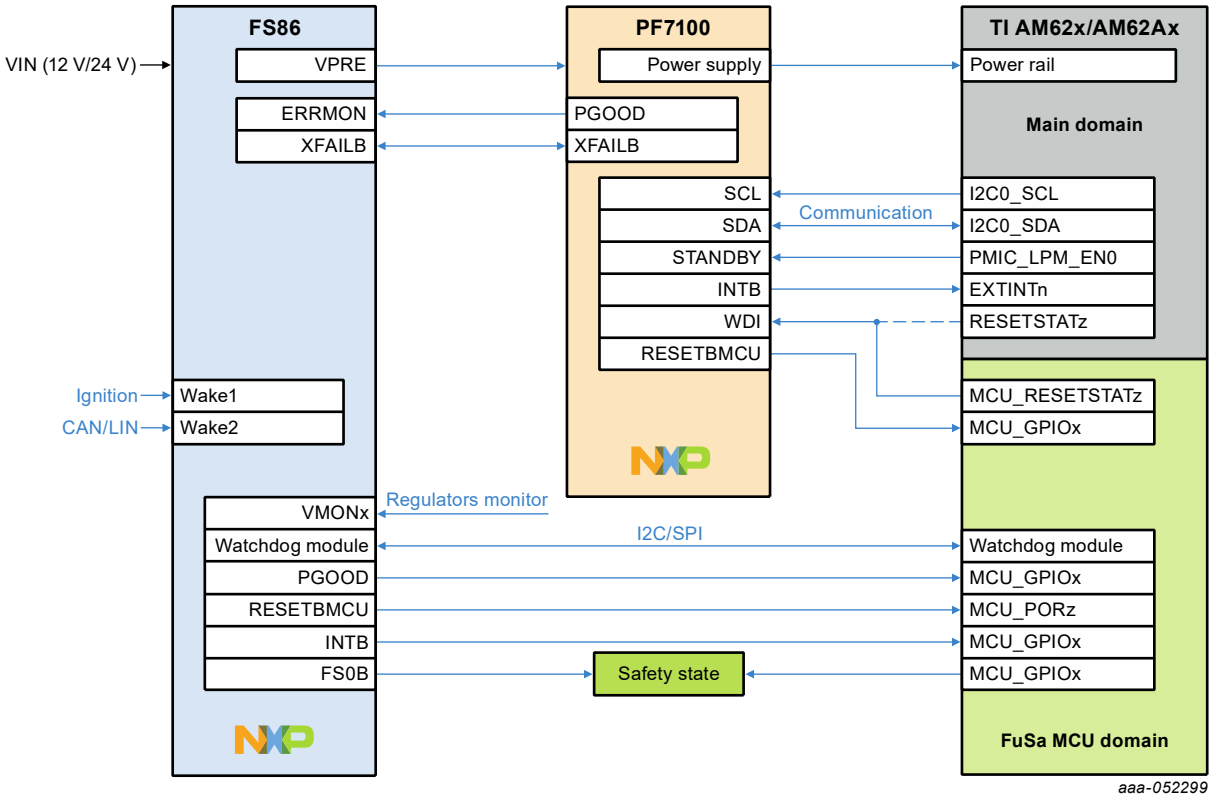

Figure 10. System ASIL D safety mechanism

Table 3. Battery input connection with system ASIL D

	FS86	PF7100	TI AM62Ax	Function
1	ERRMON	PGOOD	-	PF7100 power good monitor
2	XFAILB	XFAILB	-	PMICs power sequencing synchronization
3	-	INTB	EXTINTn	Interrupt event occurs from PF71
4	-	WDI	RESETSTATz/MCU_ RESETSTATz	Main/MCU Domain warm reset
5	PGOOD	-	MCU_GPIOx	Indicator of system power good
6	I2C/SPI	I2C	I2C/SPI	Communication and Watchdog Module
7	RESETBMCU	-	MCU_PORz	MCU and Main Domain cold reset
8	FS0B	-	MCU_GPIOx	Safety state output

- Independent voltage monitoring and fault detection: The PMIC features independent fault monitoring function for each regulator. UV, OV, and ILIM are the three types of faults monitored by the PMIC fault monitor block. The PMIC can indicate the output state for each regulator through a PGOOD signal.
- Watchdog monitoring and internal watchdog counter: The PMIC features an internal watchdog counter for monitoring a watchdog event happening from the processor. If the PMIC internal watchdog expiration counter reaches the maximum value, a reset event is performed by PMIC. ASIL B level devices have a sample watchdog. ASIL D devices have a challenged watchdog. The watchdog can be disabled if not needed.
- I^2C cyclic redundancy check (CRC) and write protection: The fuses are loaded into the functional I^2C registers of the PMIC. The fuse circuits have a CRC error check routine that reports and protects against register

loading errors on the PMIC registers. If a register loading error is detected, the corresponding flag is asserted. The I^2C secure write is to protect the secure registers from an incorrect operation.

- Functional safety output: When a fault is detected by the PMIC, such as an incorrect regulator output or WD failure, the PMIC can reset the AM62Ax MPU through the RESETBMCU pin. Also, the PMIC can trigger the FSOB pin to transition the system into safe state.
- Fail-safe state: Fail-safe state works as a safety lock down in the event of a critical device/system failure. If a fail-safe bypass is disabled, the device moves to the fail-safe state when the proper condition is met. The device can exit the fail-safe state only after a power-cycle event is present.
- Built-in self-test (BIST): When turning on the power system, the PMIC routinely implements ABIST (analog built-in self-test) and LBIST (logical built-in self-test) processes of all output voltage monitors before starting the power-up sequence. ABIST is for checking the state of the voltage monitoring block (OV/UV) for each regulator, whether normal or not. If a failure on the OV/UV monitor is detected during the ABIST on-demand request, the PMIC asserts the corresponding ABIST flags. The LBIST verifies the correct functionality of the safety logic monitoring. The LBIST is performed after each POR, or after each wake-up from standby. The LBIST is only performed in ASIL D devices.

7 References

[1] **PF7100 webpage include documentation and tools(Datasheet,Safety Manual, FMEDA, SW driver)**

[2] **FS86 webpage include documentation and tools(Datasheet,Safety Manual, FMEDA, SW driver)**

[3] **Power Management Community**

[4] **BYLink System Power Platform**

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