Exception Table Relocation and Multi-Processor Address Mapping in the Embedded PowerPC™ MPC5XX Family

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ABSTRACT

This application note presents a way to compress the eight Kbytes of exception vector table (according to the PowerPC architecture) into a 32-bit branch instruction (jump-table), allowing the compiler/linker to use this valuable space in on-chip memory.

In each multi-MPC5XX processor system that shares the same external bus, where each processor has its own internal space (4 Mbytes), each processor can access any memory or peripheral even if located within another processor on that system. The implemented exception table relocation allows each processor to have its own exception vector at any address space in the system.

This application note is organized as follows. **1 Motivation** gives motivation to this method. An introduction to the method is given in **2 The Relocation Solution**. **3 Multi-Processor Systems** describes the multi-processor system. **4 Using Table Relocation in the MPC5XX Family** describes both the principle of operation and other features of the exception relocation of the MPC5XX family. In **5 Implementation**, a hardware implementation of a PowerPC-based controller is considered for this method.

1 Motivation

Integrated circuits, like microprocessors or microcontrollers, can be found in almost any data processing system. Besides controlling the main flow of the system, the ICs must provide a pre-determined behavior response to external signals, errors, or unusual conditions arising during execution of instructions.

When exceptions occur, the processor ceases normal instruction execution and begins executing a specific exception routine. This routine is programmed by the user to handle any particular event. Each application requires its own exception set, such as: reset, overflow, storage_error, machine_check, system_call, etc.

The address space for all these exceptions in the PowerPC architecture is eight Kbytes, where each of the possible 32 exceptions occupies a 0x100 word space. This address space can be in volatile memory (SRAM, DRAM) or non-volatile memory (EPROM, flash), and in either on-chip memory or on-board memory. The consideration of which memory to use is generally a question of cost.

In PowerPC architecture each exception has its own pre-determined address for implementing the exception routine. This pre-determined arrangement of exception addresses may result in wasting valuable memory space. There are cases in which the exception routine does not require all the 0x100 space, and others where more than this space is needed (in this last case, it is common to put in a

branch instruction and use another location for the exception routine).

This address space is very important in cases where the memory space is on-chip memory, which is the case in a typical embedded system.

In **Figure 1**, a basic microcontroller configuration with an internal flash is shown. On-chip memories are generally limited (small and very expensive). This configuration will save eight Kbytes of memory.

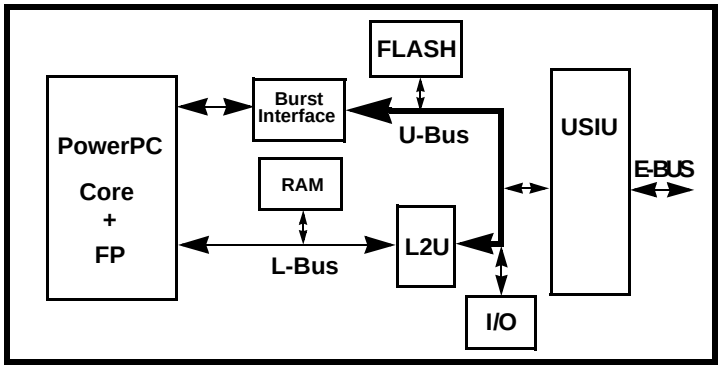

Figure 1 Block Diagram of the MPC5XX

2 The Relocation Solution

The solution to the on-chip memory problem is exception table relocation. Each exception entry that the controller/processor issues generates an address which goes to the burst buffer and then to the flash/external memory. This address will then be re-mapped to the corresponding entry in a jump-table.

The 8-Kbyte address space of the exception table is replaced with a 32-bit consecutive branch instruction. Each instruction branchs to the actual exception routine that has been placed anywhere in the address space, in any memory device either internal or external.

This method gives flexibility to the user and saves valuable memory space.

NOTE

When using exception table relocation, an additional branch instruction is executed due to one extra branch instruction corresponding to the jump-table. **Figure 2** illustrates exception table mapping entries.

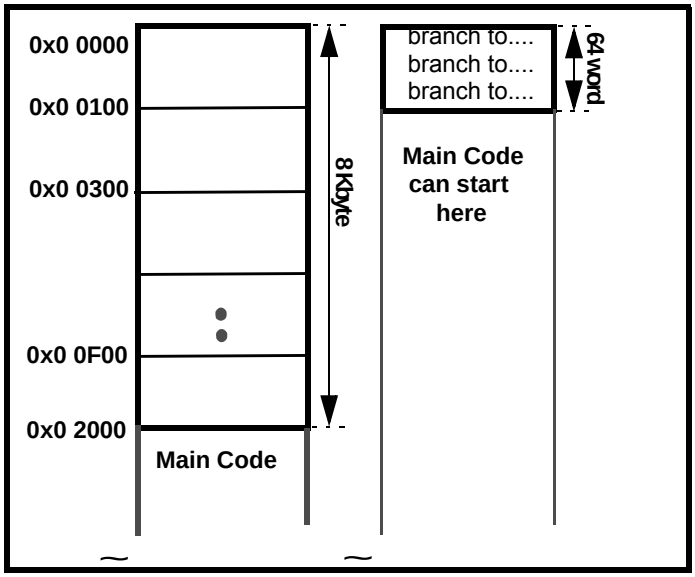

Figure 2 Exception Table Mapping Entries

3 Multi-Processor Systems

In multi-processing systems (more then one master device on the external bus) all address space is shared by all the processors. Each processor has its own internal flash/RAM/EPROM for instructions and dates. In order to distinguish between all the processors, each has a 4-Mbyte internal map (according to the INT_MAP[0:2] control bits, which set on the RESET configuration word). Each processor can access any internal address among its own four Mbytes (flash/RAM), or any address in one of the processors in the system.

When using exception table relocation, each processor has selected internal memory space as well as its own exception sets. The exceptions of each processor are re-mapped according to the jump-table of each internal map (as can be seen in **Figure 3**).

Up to eight processors with different jump-tables may be used. More then one processor with the same internal map (INT_MAP[0:2] control bits) is also allowed. This means that processors can share the same jump-table. If more then one processor has the same internal map, only one flash can be enabled.

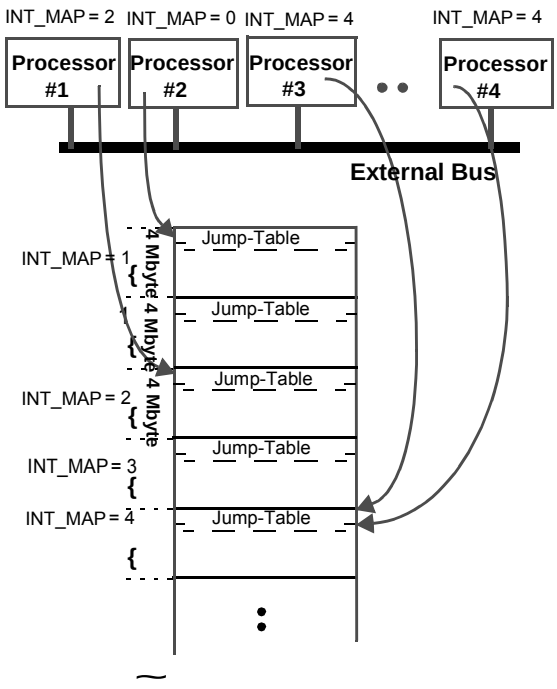

Figure 3 Re-Mapping Exceptions According to Internal Address Space

4 Using Table Relocation in the MPC5XX Family

In order to activate the exception table relocation feature in MPC5XX family, the following steps are required:

1. Set MSR(IP) bit, RESET configuration word
2. Set ETRE bit, RESET configuration word
3. Set INT_MAP[0:2] bits, RESET configuration word
4. Set OERC bit, programing bit

The PowerPC architecture allows offset of the exception to be 0000_0000 or FFF0_0000. The exception relocation method works only with F's prepended offset, and this done by setting the IP bit.

The enable table relocation exception (ETRE) bit maps each exception address to the appropriate jump-table instruction. The user should put a 32-bit branch instruction at the beginning of the internal memory (according to INT_MAP[0:2] control bits), plus, one space word between each branch to support compression code, (see **Figure 4**).

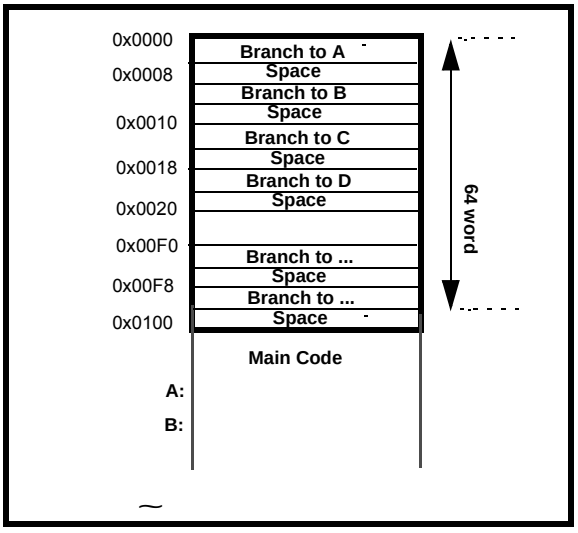

Figure 4 Jump-Table

4.1 OERC (Other Exception Relocation Control)

The MPC5XX supports distributing the exception jump-table into two different flash blocks. The OERC bit (other exception relocation control) is used to control the start address offset of the jump-table (if needed):

1. Start address of the internal memory, or
2. Start address + 32 Kbytes

The 32-Kbyte size is the block size of the flash.

When setting the OERC bit, all exceptions but the reset exception, will be mapped to the second page of the internal flash (for debugging purposes). There are two jump-tables (one for each internal map) according to programing bit OERC.

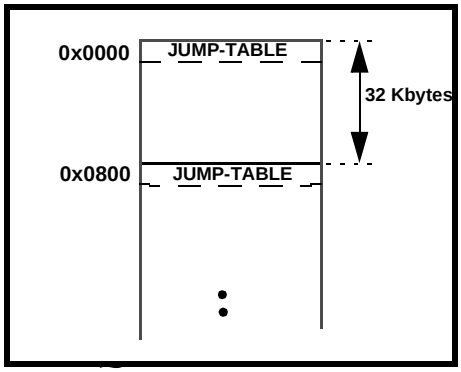

Figure 5 Two Jump-Tables

5 Implementation

This method of exception table relocation was first implemented successfully on a 32-bit PowerPC MPC5XX family microcontroller, for automotive controller application.

This method was invented and designed at MSIL (Freescale Semiconductor Israel).

6 References

[1] ***"PowerPC Microprocessor Family: The Programming Environments for 32-Bit Microprocessors"*, MPCFPE32B/AD** REV. 1, 1997.

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