

HCS12XD Family Compatibility Considerations

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1 Introduction

The HCS12XD family offers pin-compatible packaged devices to assist with system development and to accommodate expansion of applications. Applications with minor modifications can work across all of the HCS12XD family devices when memory map and module differences are considered (see [Section 5, “Module Summary”](#) and [Section 6, “Memory Configuration and Access”](#)).

When migrating among different HCS12XD family members, evaluate the appropriate device errata sheets to ensure no errata may affect compatibility. If there are errata, the work-around is generally compatible amongst the HCS12XD family members. Also, evaluate application-specific parameters such as EMC behavior and IDD levels when migrating to a different family member.

The purpose of this document is to help you maintain compatibility when considering the differences amongst members of the HCS12XD family, as shown in [Table 1](#).

Contents

1	Introduction	1
2	Overview	2
3	Part ID Assignments & Maskset Numbers	4
4	Pin Locations and Functionality	4
5	Module Summary	13
5.1	Analog-to-Digital Converter	14
5.2	Inter IC Interface (IIC)	14
5.3	Serial Communication Interface (SCI)	14
5.4	Serial Peripheral Interface (SPI)	15
5.5	Controller Area Network (CAN)	15
5.6	XGATE	15
6	Memory Configuration and Access	15
6.1	RAM Memory	16
6.2	EEPROM Memory	16
6.3	Flash Memory	17
7	Modes of Operations	17
7.1	Normal Expanded Mode	18
7.2	Normal Single-Chip Mode	18
7.3	Special Single-Chip Mode	18
7.4	Emulation of Expanded Mode	18
7.5	Emulation of Single-Chip Mode	18
8	Resets and Interrupts	19

This document does not replace any specification for the HCS12XD family devices and should be used with documents on the product summary page for HCS12X products at <http://freescale.com>.

2 Overview

The HCS12XD family includes standard on-chip peripherals up to:

- 512 Kbytes of Flash EEPROM
- 32 Kbytes of RAM
- 4 Kbytes of EEPROM
- 5 control area network 2.0 A, B software compatible modules (MSCAN12)
- 2 inter-integrated circuit bus blocks (IIC)
- 6 asynchronous serial communications interfaces (SCI)
- 3 serial peripheral interfaces (SPI)
- One 16-channel, 10-bit analog-to-digital converter (ATD)
- One 8-channel, 10-bit analog-to-digital converter (ATD)
- One 8-channel IC/OC enhanced capture timer (ECT)
- One 8-channel pulse-width modulator (PWM)
- One periodic interrupt timer (PIT)

Table 1. Package Peripheral and Memory Options of HCS12XD Family Devices

	Pins	I/O ¹	Modules									Memory				XGATE
			CAN	SCI	SPI	IIC	ECT	PIT	ATD0	ATD1	PWM	Flash	RAM	EEPROM	ROM	
9S12XDP512	144	119	5	6	3	2	1	4ch	8ch ²	16ch ³	8ch	512K	32K	4K		YES
	112	91	5	4	3	1	1	4ch	8ch ²	8ch ⁴	8ch		20K			
9S12XDT512	144	119	3	6	3	1	1	4ch	8ch ²	16ch ³	8ch	384K	20K	4K		YES
	112	91	3	4	3	1	1	4ch	8ch ²	8ch ⁴	8ch					
	80	59	3	2	2	1	1	4ch	8ch ²		8ch					
9S12XDT384	144	119	3	4	3	1	1	4ch	8ch ²	16ch ³	8ch	256K	16K	4K		YES
	112	91	3	4	3	1	1	4ch	8ch ²	8ch ⁴	8ch					
	80	59	3	2	2	1	1	4ch	8ch ²		8ch					
9S12XDQ256	144	119	4	4	3	1	1	4ch	8ch ²	16ch ³	8ch	14K	16K	4K		YES
	112	91	4	4	3	1	1	4ch	8ch ²	8ch ⁴	8ch					
	80	59	4	2	2	1	1	4ch	8ch ²		8ch					
9S12XDT256	144	119	3	4	3	1	1	4ch	8ch ²	16ch ³	8ch	16K	16K	4K		YES
	112	91	3	4	3	1	1	4ch	8ch ²	8ch ⁴	8ch					
	80	59	3	2	2	1	1	4ch	8ch ²		8ch					
9S12XD256	144	119	1	4	2	1	1	4ch	8ch ²	16ch ³	8ch	16K	16K	4K		YES
	112	91	1	4	2	1	1	4ch	8ch ²	8ch ⁴	8ch					
	80	59	1	2	2	1	1	4ch	8ch ²		8ch					
3S12XDG256	144	119	2	4	2	1	1	4ch	8ch ²	16ch ³	8ch	128K	12K	2K	128K	YES ⁶
	112	91	2	4	2	1	1	4ch	8ch ²	8ch ⁴	8ch					
	80	59	2	2	2	1	1	4ch	8ch ²		8ch					
9S12XDG128	112	91	2	2	2	1	1	4ch		16ch ⁵	8ch	8K	2K		YES ⁶	
	80	59	2	2	2	1	1	4ch		8ch ⁷	8ch					
3S12XDG128	112	91	2	2	2	1	1	4ch		16ch ⁵	8ch	64K	4K	1K	YES ⁶	
	80	59	2	2	2	1	1	4ch		8ch ⁷	8ch					
9S12XD128	112	91	1	2	2	1	1	4ch		16ch ⁵	8ch	8K	2K		YES ⁶	
	80	59	1	2	2	1	1	4ch		8ch ⁷	8ch					
9S12XD64	80	59	1	2	2	1	1	2ch		8ch ⁷	8ch	64K	4K	1K		YES ⁶

¹ I/O is the sum of ports capable to act as digital input or output

² ATD0 routed to PAD[7:0]

³ ATD1 routed to PAD[23:8]

⁴ ATD1 routed to PAD[15:8]

⁵ ATD1 routed to PAD[15:0] instead of PAD[23:8]

⁶ XGATE has no access to flash

⁷ ATD1 routed to PAD[7:0] instead of PAD[15:8]

NOTE

Three different dies (MC9S12XDP512, MC9S12XDQ256, and MC9S12XDG128) with a super set of features support all devices shown in [Table 1](#).

3 Part ID Assignments & Maskset Numbers

The part ID is located in two 8-bit read-only registers, PARTIDH and PARTIDL (addresses 0x001A and 0x001B). Each device has a unique identifier value specifying major and minor revisions encoded in the part ID registers. Consider decoding the part ID value in existing applications when migrating between HCS12XD family devices with different minor family identifiers. [Table 2](#) shows the assigned part ID number and mask set number.

Table 2. Part Names, Masksets, and Assigned Part ID Numbers¹

Part Names	Mask Set Number	Part ID ²
9S12XDP512	0L15Y/1L15Y	0xC410/0xC411
9S12XDT512	0L15Y/1L15Y	0xC410/0xC411
9S12XDT384	0L15Y/1L15Y	0xC410/0xC411
9S12XDQ256	xM84E	0xC000
9S12XDT256	xM84E	0xC000
9S12XD256	xM84E	0xC000
9S12XDG128	0M42E/1M42E	0xC100/0xC101
9S12XD128	xM42E	0xC100/0xC101

¹ Part IDs for all other XD devices are TBD

² The coding is as follows:

Bit 15–12: Major family identifier

Bit 11–8: Minor family identifier

Bit 7–4: Major mask set revision number, including fab transfers

Bit 3–0: Minor — non full — mask set revision

NOTE

The part names throughout this document correspond with the assigned part ID numbers shown in [Table 2](#).

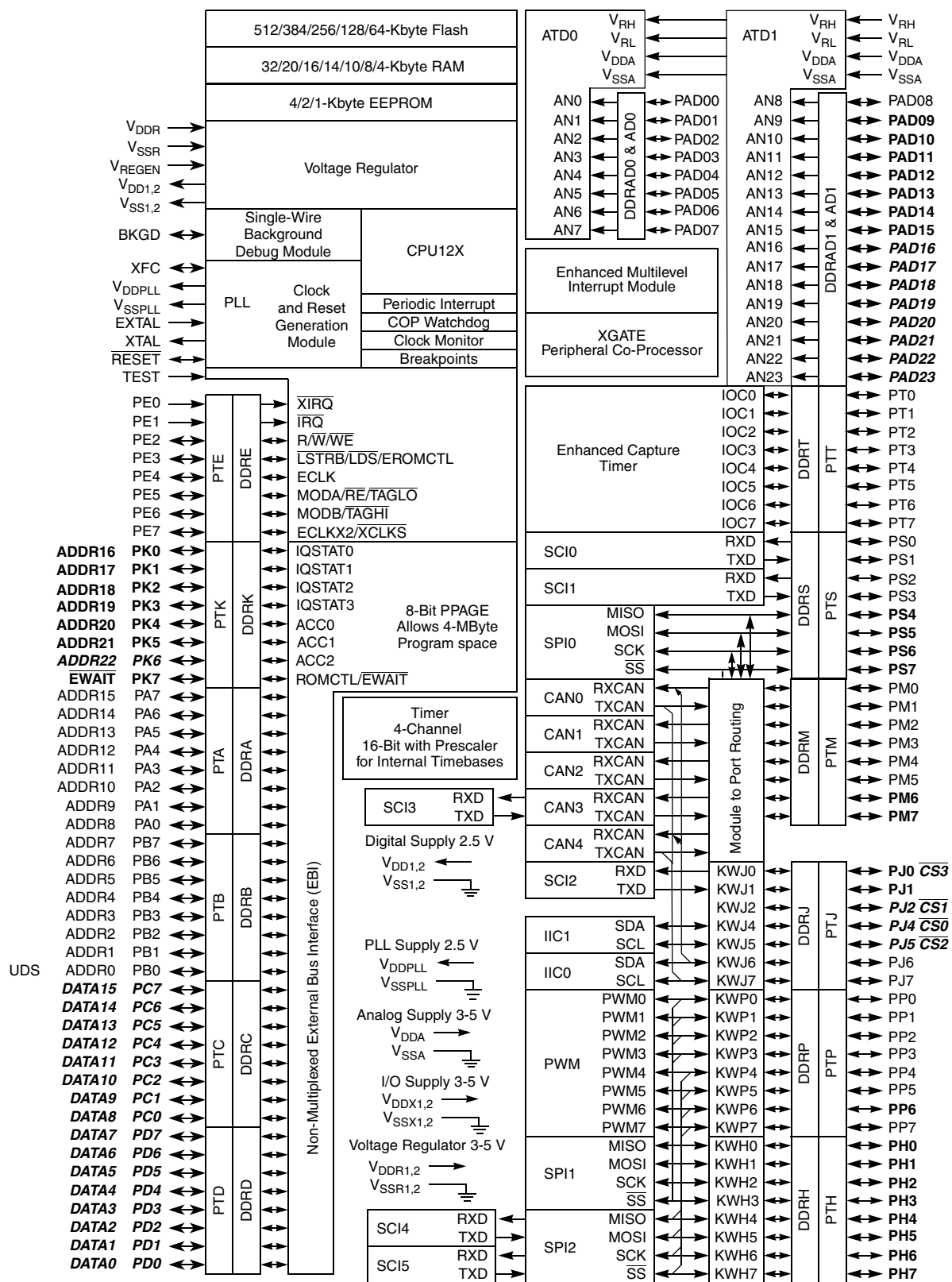
4 Pin Locations and Functionality

The pinout across the HCS12XD family is compatible, and each package option has comparable I/O pins and supply connections. [Figure 1](#) shows a block diagram for devices under the MC9S12XDP512 umbrella, including part IDs 0xC410/0xC411 and 0xC000. [Figure 2](#) shows blocks integrated on devices under the 9S12XDG128 umbrella, including part IDs 0xC100/0xC101. These block diagrams show all modules available in the HCS12XD family. See [Table 1](#) for specific availability of modules and memory options for all family members.

NOTE

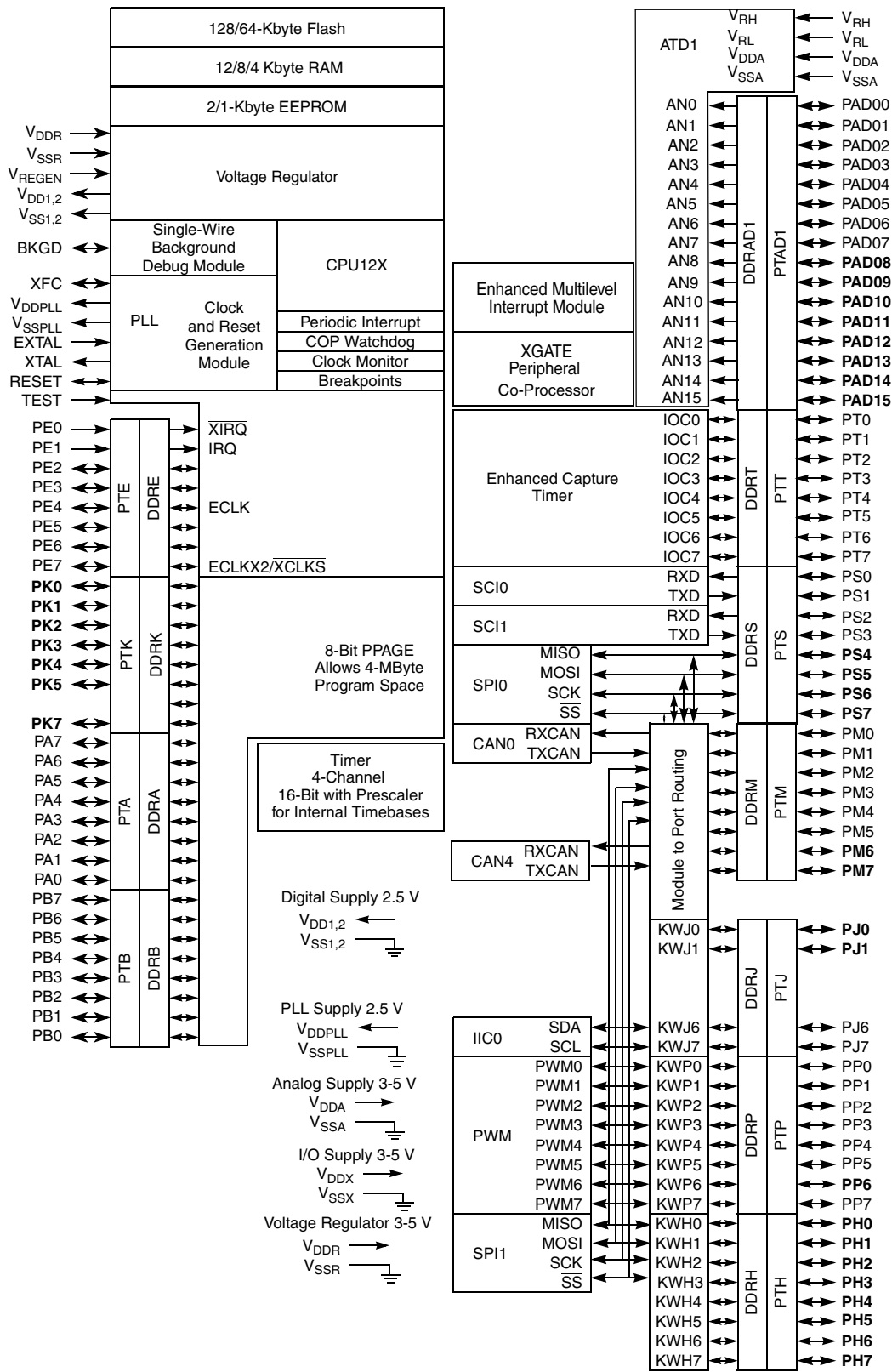
The analog-to-digital converter block is a major difference between the two diagrams. [Figure 1](#) shows two ATD blocks (ATD0 and ATD1) with up to 24 ATD signals. [Figure 2](#) shows one ATD block (ATD1) with up to 16 signals. The flexibility of the ATD module makes it straight forward in most cases to develop code for the different configurations. See [Section 5.1, “Analog-to-Digital Converter,”](#) for specific details on compatibility considerations among family members.

Pin Locations and Functionality



Signals shown in **Bold-Italics** are neither available on the 112-pin nor on the 80-pin package option
 Signals shown in **Bold** are not available on the 80-pin package

Figure 1. Part ID 0xC410/0x0C411/0xC000 Block Diagram



Signals shown in **Bold** are not available on the 80-pin package

Figure 2. Part ID 0xC100/0xC101 Block Diagram

Table 3 shows the number of general-purpose I/O pins available on each HCS12XD family package.

Table 3. HCS12XD Family GPIO Availability by Package Option

	144-pin Package ¹	112-pin Package ²	80-pin Package ³
Port A	8 pins	8 pins	8 pins
Port B	8 pins	8 pins	8 pins
Port C	8 pins		
Port D	8 pins		
Port E	8 pins (2 input only)	8 pins (2 input only)	8 pins (2 input only)
Port H	8 pins	8 pins	
Port J	7 pins	4 pins	2 pins
Port K	8 pins	7 pins	
Port M	8 pins	8 pins	6 pins
Port P	8 pins	8 pins	7 pins
Port S	8 pins	8 pins	4 pins
Port T	8 pins	8 pins	8 pins
Port AD	24 pins	16 pins	8 pins
V_{DDX}	4 pins	3 pins	2 pins
V_{SSX}	4 pins	3 pins	2 pins

¹ 25 inputs provide interrupt capability (H = 8, P = 8, J = 7, IRQ, XIRQ)

² 22 inputs provide interrupt capability (H = 8, P = 8, J = 4, IRQ, XIRQ)

³ 11 inputs provide interrupt capability (P = 7, J = 2, IRQ, XIRQ)

Pinout explanations:

IIC

- Versions with one IIC module have IIC0.
- IIC0 pins are shared among CAN4 pins.

SCI

- Versions with four SCI modules have SCI0, SCI1, SCI2 and SCI4.
- Versions with two SCI modules have SCI0 and SCI1.

SPI

- Versions with two SPI modules have SPI0 and SPI1.
- SPI0 can be routed to PS[7:4] or PM[5:2].
- SPI1 pins are shared with PWM[3:0]; in 144 and 112-pin versions, SPI1 can be routed under software control to PH[3:0].
- SPI2 pins are shared with PWM[7:4]; in 144 and 112-pin versions, SPI2 can be routed under software control to PH[7:4]. In 80-pin packages, the SS signal of SPI2 is not bonded out.

CAN

- Versions with four CAN modules have CAN0, CAN1, CAN2, and CAN4.
- Versions with three CAN modules have CAN0, CAN1, and CAN4.
- Versions with two CAN modules have CAN0 and CAN4.
- Versions with one CAN modules have CAN0.
- CAN0 can be routed under software control from PM[1:0] to pins PM[3:2], PM[5:4], or PJ[7:6].
- CAN4 pins are shared with IIC0 pins.
- CAN4 can be routed under software control from PJ[7:6] to pins PM[5:4] or PM[7:6].

NOTE

See [Section 5, “Module Summary,”](#) for specific details on module compatibility considerations among family members.

When migrating between 144, 112, and 80-pin package options, consider developing applications only using pins available with the smallest planned package. [Table 4](#) shows the pin-out summary with function details for each available package in the HCS12XD family.

Table 4. Table Pin-Out Summary¹ (Sheet 1 of 5)

LQFP 144	LQFP 112	QFP 80	Pin	2nd Function	3rd Function	4th Function	5th Function
1	1	1	PP3	KWP3	PWM3	SS1	–
2	2	2	PP2	KWP2	PWM2	SCK1	–
3	3	3	PP1	KWP1	PWM1	MOSI1	–
4	4	4	PP0	KWP0	PWM0	MISO1	–
5	–	–	PJ2	KWJ2	CS1	–	–
6	–	–	PK6	ADDR22	NOACC	–	–
7	5	–	PK3	ADDR19	–	–	–
8	6	–	PK2	ADDR18	IQSTAT2	–	–
9	7	–	PK1	ADDR17	IQSTAT1	–	–
10	8	–	PK0	ADDR16	IQSTAT0	–	–
11	9	5	PT0	IOC0	–	–	–
12	10	6	PT1	IOC1	–	–	–
13	11	7	PT2	IOC2	–	–	–
14	12	8	PT3	IOC3	–	–	–
15	13	9	V _{DD1}	–	–	–	–
16	14	10	V _{SS1}	–	–	–	–
17	15	11	PT4	IOC4	–	–	–
18	16	12	PT5	IOC5	–	–	–
19	17	13	PT6	IOC6	–	–	–
20	18	14	PT7	IOC7	–	–	–
21	19	–	PK5	ADDR21	–	–	–
22	20	–	PK4	ADDR20	–	–	–

Table 4. Table Pin-Out Summary¹ (Sheet 2 of 5)

LQFP 144	LQFP 112	QFP 80	Pin	2nd Function	3rd Function	4th Function	5th Function
23	21	–	PJ1	KWJ1	TXD2	–	–
24	22	–	PJ0	KWJ0	RXD2	$\overline{\text{CS3}}^2$	–
25	23	15	BKGD	MODC	–	–	–
26	–	–	V _{DDX2}	–	–	–	–
27	–	–	V _{SSX2}	–	–	–	–
28	–	–	PC0	DATA8	–	–	–
29	–	–	PC1	DATA9	–	–	–
30	–	–	PC2	DATA10	–	–	–
31	–	–	PC3	DATA11	–	–	–
32	24	16	PB0	ADDR0	$\overline{\text{UDS}}$	–	–
33	25	17	PB1	ADDR1	–	–	–
34	26	18	PB2	ADDR2	–	–	–
35	27	19	PB3	ADDR3	–	–	–
36	28	20	PB4	ADDR4	–	–	–
37	29	21	PB5	ADDR5	–	–	–
38	30	22	PB6	ADDR6	–	–	–
39	31	23	PB7	ADDR7	–	–	–
40	–	–	PC4	DATA12	–	–	–
41	–	–	PC5	DATA13	–	–	–
42	–	–	PC6	DATA14	–	–	–
43	–	–	PC7	DATA15	–	–	–
44	32	–	PH7	KWH7	$\overline{\text{SS2}}$	TXD5	–
45	33	–	PH6	KWH6	SCK2	RXD5	–
46	34	–	PH5	KWH5	MOSI2	TXD4	–
47	35	–	PH4	KWH4	MISO2	RXD4	–
48	36	24	PE7	$\overline{\text{XCLKS}}$	ECLKX2	–	–
49	37	25	PE6	MODB	$\overline{\text{TAGHI}}$	–	–
50	38	26	PE5	MODA	$\overline{\text{TAGLO}}$	$\overline{\text{RE}}$	–
51	39	27	PE4	ECLK	–	–	–
52	40	28	V _{SSR}	–	–	–	–
53	41	29	V _{DDR}	–	–	–	–
54	42	30	$\overline{\text{RESET}}$	–	–	–	–
55	43	31	V _{DDPLL}	–	–	–	–
56	44	32	XFC	–	–	–	–
57	45	33	V _{SSPLL}	–	–	–	–
58	46	34	EXTAL	–	–	–	–
59	47	35	XTAL	–	–	–	–
60	48	36	TEST	–	–	–	–
61	49	–	PH3	KWH3	$\overline{\text{SS1}}$	TXD7	–

Table 4. Table Pin-Out Summary¹ (Sheet 3 of 5)

LQFP 144	LQFP 112	QFP 80	Pin	2nd Function	3rd Function	4th Function	5th Function
62	50	–	PH2	KWH2	SCK1	RXD7	–
63	51	–	PH1	KWH1	MOSI1	TXD6	–
64	52	–	PH0	KWH0	MISO1	RXD6	–
65	–	–	PD0	DATA0	–	–	–
66	–	–	PD1	DATA1	–	–	–
67	–	–	PD2	DATA2	–	–	–
68	–	–	PD3	DATA3	–	–	–
69	53	37	PE3	$\overline{\text{LSTRB}}$	$\overline{\text{LDS}}$	EROMCTL	–
70	54	38	PE2	$\overline{\text{RW}}$	$\overline{\text{WE}}$	–	–
71	55	39	PE1	$\overline{\text{IRQ}}$	–	–	–
72	56	40	PE0	$\overline{\text{XIRQ}}$	–	–	–
73	57	41	PA0	ADDR8	–	–	–
74	58	42	PA1	ADDR9	–	–	–
75	59	43	PA2	ADDR10	–	–	–
76	60	44	PA3	ADDR11	–	–	–
77	61	45	PA4	ADDR12	–	–	–
78	62	46	PA5	ADDR13	–	–	–
79	63	47	PA6	ADDR14	–	–	–
80	64	48	PA7	ADDR15	–	–	–
81	–	–	V _{DDX3}	–	–	–	–
82	–	–	V _{DDX3}	–	–	–	–
83	–	–	PD4	DATA4	–	–	–
84	–	–	PD5	DATA5	–	–	–
85	–	–	PD6	DATA6	–	–	–
86	–	–	PD7	DATA7	–	–	–
87	65	49	V _{DD2}	–	–	–	–
88	66	50	V _{SS2}	–	–	–	–
89	67	51	PAD00	AN0	–	–	–
90	68	–	PAD08	AN8	–	–	–
91	69	52	PAD01	AN1	–	–	–
92	70	–	PAD09	AN9	–	–	–
93	71	53	PAD02	AN2	–	–	–
94	72	–	PAD10	AN8	–	–	–
95	73	54	PAD03	AN3	–	–	–
96	74	–	PAD11	AN11	–	–	–
97	75	55	PAD04	AN4	–	–	–
98	76	–	PAD12	AN12	–	–	–
99	77	56	PAD05	AN5	–	–	–
100	78	–	PAD13	AN13	–	–	–

Table 4. Table Pin-Out Summary¹ (Sheet 4 of 5)

LQFP 144	LQFP 112	QFP 80	Pin	2nd Function	3rd Function	4th Function	5th Function
101	79	57	PAD06	AN6	–	–	–
102	80	–	PAD14	AN14	–	–	–
103	81	58	PAD07	AN7	–	–	–
104	82	–	PAD15	AN15	–	–	–
105	–	–	PAD16	AN16	–	–	–
106	–	–	PAD17	AN17	–	–	–
107	83	59	V _{DDA}	–	–	–	–
108	84	60	V _{RH}	–	–	–	–
109	85	61	V _{RL}	–	–	–	–
110	86	62	V _{SSA}	–	–	–	–
111	–	–	PAD18	AN18	–	–	–
112	–	–	PAD19	AN19	–	–	–
113	–	–	PAD20	AN20	–	–	–
114	–	–	PAD21	AN21	–	–	–
115	–	–	PAD22	AN22	–	–	–
116	–	–	PAD23	AN23	–	–	–
117	87	–	PM7	TXCAN3	TXCAN4	TXD3	–
118	88	–	PM6	RXCAN3	RXCAN4	RXD3	–
119	89	63	PS0	RXD0	–	–	–
120	90	64	PS1	TXD0	–	–	–
121	91	65	PS2	RXD1	–	–	–
122	92	66	PS3	TXD1	–	–	–
123	93	–	PS4	MISO0	–	–	–
124	94	–	PS5	MOSI0	–	–	–
125	95	–	PS6	SCK0	–	–	–
126	96	–	PS7	$\overline{SS0}$	–	–	–
127	97	67	V _{REGEN}	–	–	–	–
128	98	68	PJ7	KWJ7	TXCAN4	SCL0	–
129	99	69	PJ6	KWJ6	RXCAN4	SDA0	–
130	–	–	PJ5	KWJ5	SCL1	$\overline{CS2}$	–
131	–	–	PJ4	KWJ4	SDA1	$\overline{CS0}$	–
132	100	70	PM5	TXCAN2	TXCAN0	TXCAN4	SCK0
133	101	71	PM4	RXCAN2	RXCAN0	RXCAN4	MOSI0
134	102	72	PM3	TXCAN1	TXCAN0	$\overline{SS0}$	–
135	103	73	PM2	RXCAN1	RXCAN0	MISO0	–
136	104	74	PM1	TXCAN0	–	–	–
137	105	75	PM0	RXCAN0	–	–	–
138	106	76	V _{SSX1}	–	–	–	–
139	107	77	V _{DDX1}	–	–	–	–

Table 4. Table Pin-Out Summary¹ (Sheet 5 of 5)

LQFP 144	LQFP 112	QFP 80	Pin	2nd Function	3rd Function	4th Function	5th Function
140	108	–	PK7	ROMCTL	$\overline{\text{EWAIT}}$	–	–
141	109	78	PP7	KWP7	PWM7	SCK2	–
142	110	–	PP6	KWP6	PWM6	$\overline{\text{SS2}}$	–
143	111	79	PP5	KWP5	PWM5	MOSI2	–
144	112	80	PP4	KWP4	PWM4	MISO2	–

¹ Table shows a superset of pin functions. Not all functions are available on all derivatives.

² $\overline{\text{CS3}}$ is not accessible on 112-pin package.

5 Module Summary

This section describes the compatibility considerations for HCS12XD family members with module differences. [Table 5](#) shows the register memory map differences across the family. Three different dies (MC9S12XDP512, MC9S12XDQ256, and MC9S12XDG128) with a super set of features support all the HCS12XD family members as shown in [Table 1](#).

The unimplemented register space shown in [Table 5](#) is not allocated to any module. Therefore, writing to these locations has no effect and read access to these locations returns 0. Accessing a reserved location can have unpredictable effects on MCU operation. Do not access any of these unimplemented locations.

NOTE

The part names in [Table 5](#) correspond with the assigned part ID numbers shown in [Table 2](#).

Table 5. HCS12XD Family Register Memory Map Differences¹

Address	Module	9S12XDP512	9S12XDQ256	9S12XDG128
0x00B0-0x00B7	IIC1 (inter IC bus)	X	–	–
0x00B8-0x00BF	SCI2 (serial communications interface)	X	X	–
0x00C0-0x00C7	SCI3 (serial communications interface)	X	–	–
0x00F8-0x00FF	SPI2 (serial peripheral interface)	X	X	–
0x0130-0x0137	SCI4 (serial communications interface)	X	X	–
0x0138-0x013F	SCI5 (serial communications interface)	X	–	–
0x0180-0x01BF	CAN1 (scalable CAN)	X	X	–
0x01C0-0x01FF	CAN2 (scalable CAN)	X	X	–
0x0200-0x023F	CAN3 (scalable CAN)	X	–	–
0x0240-0x027F	PIM (port integration module) ²	X	X	X
0x02C0-0x02DF	ATD0 (analog-to-digital-converter)	X	X	–

¹ Not all features are available in some of the 112- and 80-pin packages.

² The port integration modules differ from each other, but they are upwards compatible.

5.1 Analog-to-Digital Converter

This section describes the different ATD configurations and pin assignments across the HCS12XD family. Any existing ATD software driver code may require modification when migrating between different packages or family members with different minor family identifiers in the part ID, as shown in [Table 2](#).

Devices with part ID 0xC410/0xC411 or 0xC000 have up to two ATD modules (ATD0 and ATD1) with up to 24 ATD signals routed to pins PAD[7:0] on ATD0 and PAD[23:8] on ATD1.

Devices with part ID 0xC100/0xC101 have one ATD block (ATD1) with up to 16 ATD signals routed to pins PAD[15:0].

Reading the part ID value from the two 8-bit read-only registers (PARTIDH – 0x001A and PARTIDL – 0x001B) indicates which ATD configuration is accessible as shown in [Table 6](#). The wrap bits in ATD1CTL0 can configure the 16-channel ATD1 to look like an 8-channel ATD for conversion sequences that wrap around at channel seven.

Table 6. ATD Configuration and Pin Assignments

Part ID	Package	ATD0	Pin Name	ATD1	Pin Name
0xC410/0xC411 0xC000	144 LQFP	8ch	PAD[7:0]	16ch	PAD[23:8]
	112 LQFP	8ch	PAD[7:0]	8ch	PAD[15:8]
	80 QFP	8ch	PAD[7:0]		
0xC100/0xC101	112 LQFP			16ch	PAD[15:0]
	80 QFP			8ch	PAD[7:0]

NOTE

For compatibility across the HCS12XD family, consider developing software driver code with at least two different ATD routines that decode the part ID value and use the value to point to the appropriate ATD routine. Memory availability should also be considered for the increased code size from the additional ATD routine.

5.2 Inter IC Interface (IIC)

The IIC module is compatible across the HCS12XD family. All members and packages of the HCS12XD family have at least one IIC module (IIC0). For compatibility, use only IIC0 and the module routing register should remain with default values.

5.3 Serial Communication Interface (SCI)

The SCI modules are compatible across the HCS12XD family. All members and packages of the HCS12XD family have at least two SCI modules (SCI0 and SCI1). For compatibility, use only SCI0 and SCI1 and the module routing register should remain with default values.

5.4 Serial Peripheral Interface (SPI)

The SPI modules are compatible across the HCS12XD family. All members and packages of the HCS12XD family have at least two SPI modules (SPI0 and SPI1). For compatibility, use only SPI0 and SPI1 and the module routing register should remain with default values.

5.5 Controller Area Network (CAN)

The CAN modules are compatible across the HCS12XD family. All members and packages of the HCS12XD family have at least one CAN module (CAN0). For compatibility, use only CAN0 and the module routing register should remain with default values.

5.6 XGATE

The XGATE is compatible across the HCS12XD family. All members and packages of the HCS12XD family have an XGATE. For compatibility, do not use the XGATE to access flash.

6 Memory Configuration and Access

The HCS12XD family devices have compatible local and global memory maps. The global memory spaces reserved for the internal resources (RAM, EEPROM, and FLASH) are predetermined in the MMC module. You cannot change the size of individual internal resources fixed in the design of each device. Refer to the reference manual for further details. [Table 7](#) shows the memory spaces occupied by the on-chip resources with the top addresses fixed. [Table 8](#), [Table 9](#), and [Table 10](#) show the memory sizes for each HCS12XD family device.

NOTE

The part names in this section correspond with the assigned part ID numbers shown in [Table 2](#).

Retaining code compatibility across the HCS12XD family requires accessing only the memory locations implemented on the smallest device, allowing portability from larger devices.

Table 7. Global Implemented Memory Space

Internal Resource	Bottom (Low) Address	Top (High) Address
Registers	0x00_0000	0x00_07FF
RAM	RAM_LOW = 0x10_0000 minus size of RAM	0x0F_FFFF
EEPROM	EEPROM_LOW = 0x14_0000 minus size of EEPROM	0x13_FFFF
Flash	FLASH_LOW = 0x80_0000 minus size of flash	0x7F_FFFF

6.1 RAM Memory

The HCS12XD family offers up to 32 Kbytes of RAM. Do not access areas of RAM unimplemented on devices with lower RAM sizes to maintain compatibility. The RAM memory sizes implement from the higher order address to the lower order address. Out of reset, the RPAGE register has equivalent values for HCS12XD family devices. The RPAGE register should be left with the reset value, 0xFD, for code compatibility and portability. [Table 8](#) summarizes the RAM size and address location for each device.

Table 8. Available RAM Pages on HCS12XD Family

RAM Page RP[7:0]	Global Address	DP512	DT512 DT384	DQ256 DT256 DG256	D256	DG128	D128	D64
0xF8	0x0F_8000 - 0x0F_8FFF	32K Byte						
0xF9	0x0F_9000 - 0x0F_9FFF							
0xFA	0x0F_A000 - 0x0F_AFFF							
0xFB	0x0F_B000 - 0x0F_BFFF							
0xFC	0x0F_C000 - 0x0F_CFFF		20K Byte	16K Byte	14K Byte	12K Byte	8K Byte	4K Byte
0xFD	0x0F_D000 - 0x0F_DFFF							
0xFE	0x0F_E000 - 0x0F_EFFF							
0xFF	0x0F_F000 - 0x0F_FFFF							

6.2 EEPROM Memory

The HCS12XD family offers up to 4 Kbytes of EEPROM. To maintain compatibility, do not access areas of EEPROM unimplemented on devices with lower EEPROM sizes. [Table](#) summarizes the EEPROM size and address location for each device.

Table 9. Available EEPROM Pages on HCS12XD Family

EEPROM Page EP[7:0]	Global Address	DP512 DT512 DT384 DQ256 DT256 D256	DG128 D128	D64
0xFC	0x13_F000 – 0x13_F3FF	4K Byte		
0xFD	0x13_F400 – 0x13_F7FF			
0xFE	0x13_F800 – 0x13_FBFF		2K Byte	
0xFF	0x13_FC00 – 0x13_FFFF			1K Byte

6.3 Flash Memory

The HCS12XD family offers up to 512 Kbytes of flash. To maintain compatibility, do not use the XGATE to access flash and do not access any unimplemented areas of flash on devices with smaller flash sizes.

Table 10 summarizes the flash size and configuration for each device.

Table 10. MC9S12XD Family Flash Configuration

Global Address	Dx512/ D512	Dx384	Dx256/ D256	Dx128/ D128	D64
0x78_0000 (PPAGE 0xE0)	128K	128K	128K		
0x7A_0000 (PPAGE 0xE8)	128K				
0x7C_0000 (PPAGE 0xF0)	128K	128K			
0x7E_0000 (PPAGE 0xF8)	128K	128K	128K	128K	64K

Shared XGATE/CPU area
 Not implemented

XGATE read access to flash is not possible on Dx128/D128 and D64 with part ID 0xC100/0xC101. Program pages available on Dx384 are 0xE0–0xE7 and 0xF0–0xFF. Program pages available on Dx256/D256 are 0xE0–0xE7 and 0xF8–0xFF. Shared XGATE/CPU area is on Dx512/Dx384 at global address 0x78_0800 to 0x78_FFFF (30Kbyte). Shared XGATE/CPU are on Dx256/D256 at global address 0x78_0800 to 0x79_3FFF (46Kbyte).

7 Modes of Operations

This section describes the available user modes for the HCS12XD family. BDM is available in all operating modes but must be enabled before firmware commands are executed. Some systems may have a control bit that allows suspending the function during background debug mode.

When the device operates in expanded modes (except emulation single-chip mode) on 144-pin packages, accesses to the global addresses not occupied by the on-chip resources (unimplemented areas or external space) result in accesses to the external bus.

7.1 Normal Expanded Mode

Ports K, A, and B are configured as a 23-bit address bus, ports C and D are configured as a 16-bit data bus, and port E provides bus control and status signals. See Table 3 for specific availability of GPIO pins on each package. This mode allows 16-bit external memory and peripheral devices to be interfaced to the system. The fastest external bus rate is divided by 2 from the internal bus rate.

7.2 Normal Single-Chip Mode

There is no external bus in this mode. The processor program is executed from internal memory. Ports A, B, C, D, K, and most pins of port E are available as general-purpose I/O. See Table 3 for specific availability of GPIO pins on each package.

7.3 Special Single-Chip Mode

This mode is for debugging single-chip operation, boot-strapping, or security related operations. The background debug module BDM is active in this mode. The CPU executes a monitor program located in an on-chip ROM. BDM firmware is waiting for additional serial commands through the BKGD pin. There is no external bus after reset in this mode.

7.4 Emulation of Expanded Mode

This mode is for emulation systems where the target application is normal expanded mode. Code executes from external memory or internal memory depending on the state of ROMON and EROMON bit. In this mode, internal operation is visible on external bus interface.

7.5 Emulation of Single-Chip Mode

This mode is for emulation systems where the target application is normal single-chip mode. Code executes from external memory or internal memory depending on the state of ROMON and EROMON bit. In this mode, internal operation is visible on external bus interface.

In emulation single-chip mode on 144-pin packages, accesses to the global addresses not occupied by the on-chip resources (unimplemented areas or external space) also result in accesses to the external bus. CPU accesses to the global addresses occupied by the external space result in an illegal access reset (system reset). The BDM accesses to the external space are performed, but data is undefined.

NOTE

The 80-pin and 112-pin packages do not have expanded bus available. For compatibility, the MMC control register (MMCCTL1) should be left with default values ROMHM=RAMHM=0 and expanded, and emulation modes should not be used on the 144-pin packages.

8 Resets and Interrupts

All HCS12XD family devices have the same vector locations. The inputs for peripheral modules not on the device are tied to ground so no interrupts for those vectors can occur. [Table 11](#) shows the differences in the allocation of peripheral interrupts.

Table 11. Interrupt Vector Location Differences^{1 2}

Vector Address	Interrupt Source	9S12XDP512	9S12XDQ256	9S12XDG128
Vector base + \$D2	ATD0 (analog-to-digital-converter)	X	X	–
Vector base + \$BC	SPI2 (serial peripheral interface)	X	X	–
Vector base + \$AE	CAN1 wake-up	X	X	–
Vector base + \$AC	CAN1 errors	X	X	–
Vector base + \$AA	CAN1 receive	X	X	–
Vector base + \$A8	CAN1 transmit	X	X	–
Vector base + \$A6	CAN2 wake-up	X	X	–
Vector base + \$A4	CAN2 errors	X	X	–
Vector base + \$A2	CAN2 receive	X	X	–
Vector base + \$A0	CAN2 transmit	X	X	–
Vector base + \$9E	CAN3 wake-up	X	–	–
Vector base + \$9C	CAN3 errors	X	–	–
Vector base + \$9A	CAN3 receive	X	–	–
Vector base + \$98	CAN3 transmit	X	–	–
Vector base + \$8A	SCI2 (serial communications interface)	X	X	–
Vector base + \$88	SCI3 (serial communications interface)	X	–	–
Vector base + \$86	SCI4 (serial communications interface)	X	X	–
Vector base + \$84	SCI5 (serial communications interface)	X	–	–
Vector base + \$82	IIC1 (inter IC bus)	X	–	–

¹ Not all features are available in some of the 112- and 80-pin packages.

² The part names used in [Table 11](#) correspond with the assigned part ID numbers shown in [Table 2](#).

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