



Considerations for Migrating Existing DSP563xx Designs to Symphony™ DSPs

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1 Introduction

The DSP56301 and DSP56303 were introduced in the early 1990s and were the very first two-derivative devices in the DSP56300 family of general-purpose, 24-bit, fixed-point, digital signal processors. Since those first two devices, the DSP56307, DSP56L307, DSP56309, DSP56311, and DSP56321 devices have also been introduced. Each new device typically brought an increase in performance and larger internal memory spaces. The similarity of the peripherals, the similar register addresses, and the pin compatibility of all these general-purpose DSPs allowed for relatively easy migration of designs between the various devices in the family with little modification required to hardware and software.

With the passage of time and given the normal life cycle of products, only the DSP56311 and DSP56321 remain active products, the rest having been fully retired or classified as not recommended for new designs. As a result, existing product designs based on any of these latter DSPs will need to be migrated to the DSP56311 or DSP56321 or retired. This guide is intended for users that are familiar with the general-purpose DSP563xx devices.

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The Symphony series of digital signal processors are based on the same DSP56300 core as the general-purpose devices but with a slightly different complement of peripherals specifically intended for digital audio signal processing. The design philosophy of the Symphony DSPs was slightly different than their general-purpose cousins; the Symphony DSPs were designed with a variety of different packages and have various different peripheral complements. This document describes considerations for migrating an existing DSP563xx-based design to a Symphony DSP. Currently, the following devices in the Symphony DSP family should be considered when evaluating the future of an existing DSP563xx design: DSP56371, DSP56374, DSP56720, DSP56721, DSP56724, and DSP56725.

The DSP5672x devices are the newest members of the Symphony branch of the DSP family. They are dual DSP56300-core devices where each core has a combination of dedicated and shared peripherals along with a bank of shared memory between the two cores.

2 Considerations

Because the general-purpose DSP563xx family and the Symphony family devices share the same core, porting existing algorithms is typically straight forward. Differences in the peripherals between the two families require special attention be paid to the peripherals and the code that handles I/O. Porting the I/O code requires analysis and effort. This section gives a brief overview of the major differences that need to be considered when migrating an existing application to a Symphony DSP.

2.1 Pin Compatibility

Unlike the pin-compatibility afforded by the general-purpose DSP563xx DSPs, there are only two pairs of fully pin-compatible Symphony DSPs, as follows:

- DSP56720 and DSP56724 in the 144-pin QFP package
- DSP56721 and DSP56725 in the 80-pin QFP package

The rest of the Symphony DSPs are not pin-compatible with each other. The general-purpose DSP563xx DSPs are not pin-compatible with any of the Symphony DSPs.

2.2 Power Supply

The earlier DSP devices are single voltage devices. All pins are powered from the same 3.3-V voltage supply. To reduce power consumption, later DSP devices were designed as dual-voltage devices. The core and the PLL operate from a lower power supply voltage than the I/O. All the DSPs' I/O power supply voltage is 3.3 V. [Table 1](#) shows the core and I/O power supply voltages for the Symphony DSPs. In an existing application with a signal voltage DSP, an additional voltage regulator needs to be provided to supply the lower voltage for the DSP core.

Table 1. Symphony DSPs Power Supply Voltages

Device	Core (V)	I/O (V)
56371	1.25	3.3
56374	1.25	3.3
56720/56721	1.0	3.3

Table 1. Symphony DSPs Power Supply Voltages (continued)

Device	Core (V)	I/O (V)
56724/56725	1.0 or 1.2 ¹	3.3

Note:

1. Depends on core speed

Even though the Symphony DSPs are operated from a 3.3-V I/O voltage supply, most of the device functional inputs can tolerate 5.0 V. All of the DSP56374 and DSP56371 I/O pins are 5-V tolerant, except the DSP56374 EXTAL pin is not 5-V tolerant. All of the DSP56720 and DSP56721 I/O pins can tolerate 5 V as well. Refer to the Data Sheet for each DSP for the specific details of the 5-V tolerance.

2.3 Clock Generation

Like the general-purpose DSP563xx DSPs, the Symphony DSPs have an internal phase lock loop (PLL) for clock generation. The maximum core frequency for each Symphony DSP is listed in [Table 2](#).

The PLLs in the Symphony DSPs do not require the external PCAP capacitors that are needed for the general-purpose DSP563xx DSPs. In addition, the Symphony DSP PLLs are all programmed slightly different from each other. Consult the User's Guide for a particular DSP for the specific programming sequence for each device's PLL.

Table 2. Maximum Operating Frequency for Symphony DSPs

Device	Frequency
56371	180 MHz
56374	150 MHz
56720/56721	200 MHz
56724/56725	200 MHz at core = 1.00 V 250 MHz at core = 1.20 V

2.4 Internal Memory

The Symphony DSPs, like their general-purpose relatives, come with a variety of internal RAM capacities. [Table 3](#) details the size of the internal RAM in each memory space for the default memory configuration (for example, when memory switch bit OMR:MS = 0). Although not listed in the table, four additional memory configurations are available for each device when OMR:MS = 1, where the total memory in each memory space is shifted about based on the memory switch mode bits OMR:MSW[1:0]. Refer to the DSPs' User's Guide for the specifics of the alternate memory configurations.

Table 3. Default Internal RAM Configuration of Symphony DSPs in 24-Bit Words

Device	Total RAM	P	X	Y	Shared
56371	88 Kwords	4 Kwords	36 Kwords	48 Kwords	—
56374	18 Kwords	6 Kwords	6 Kwords	6 Kwords	—

Table 3. Default Internal RAM Configuration of Symphony DSPs in 24-Bit Words (continued)

Device	Total RAM	P		X		Y		Shared
56720/56721	248 Kwords	8 Kwords (core 0)	8 Kwords (core1)	36 Kwords (core0)	36 Kwords (core1)	48 Kwords (core0)	48 Kwords (core1)	64 Kwords
56724/56725	112 Kwords	4 Kwords (core 0)	2 Kwords (core1)	28 Kwords (core0)	12 Kwords (core1)	24 Kwords (core0)	10 Kwords (core1)	32 Kwords

Additionally, the dual-core DSP5672x devices contain shared memory. This unified region of internal RAM is shared between the two cores and may be accessed with zero wait states as X or Y memory and one wait state as P memory. Instructions may be executed from shared memory but the hardware has not been optimized for doing so. Each core may access separate blocks within shared memory without contention.

2.5 External Memory

All of the general-purpose DSP563xx DSPs have an external memory interface (usually referred to as Port A or EMI). In contrast, only the DSP56720 and DSP56724 have an external memory controller (EMC). The Port A and EMC external memory interfaces are completely different and support different memory types. Additionally, there is no instruction cache support in the Symphony DSP5672x EMC.

The EMC of the DSP56720 and DSP56724 supports SDRAM, SRAM, EPROM, flash EPROM, burstable RAM, regular DRAM, and EDO DRAM devices. It should also be noted that the EMC, unlike Port A, is a multiplexed address and data bus, which requires external latches to be used in a system that includes external memory.

2.6 DMA Controller

The DSP56371 and DSP56374 each have a 6-channel DMA controller like the general-purpose DSP563xx DSPs. The dual-core Symphony DSP5672x devices have extended the DMA controller of each core to eight channels per core. The additional two DMA channels in the dual-core devices have the restrictions that they cannot serve as triggers for any of the first six DMA channels and that they cannot themselves be triggered by any of the IRQx signals. In all other respects, the DMA controller and registers are the same as those of the general-purpose DSPs.

2.7 Serial Communication

This section outlines the differences between the ESSI and ESAI interfaces and between the SCI and SHI interfaces.

2.7.1 ESSI vs. ESAI

The general-purpose DSP563xx DSPs each have two enhanced synchronous serial interfaces (ESSI) typically used for communicating with ADCs, DACs, and codecs. Each ESSI has one receiver and up to three transmitters. The ESSI can be operated in synchronous mode where the receiver and transmitter(s) have the same bit clock and frame sync, generated internally or supplied externally. Alternatively, the

receiver and transmitter(s) may be clocked asynchronously but in this case, one set of clocks must be generated internally while the other set of clocks is supplied externally.

The Symphony DSPs have an analogous port, the enhanced serial audio interface (ESAI). The DSP56371 and DSP56374 each have two ESAIs, while the DSP5672x devices have four ESAIs, two for each core. The ESAI module provides a much more flexible superset of functionality than the ESSI.

The capabilities of the ESAI is wholly a superset of all those of the ESSI. The two most notable differences between the ESAI and the ESSI are related to the number of transmit and receive pins and clocking schemes. The ESAI can be configured to have up to six transmitters and no receivers or two transmitters and up to four receivers. The transmit and receive sections may be clocked completely independently from each other, unlike the ESSI. Further, both sets of clocks may be simultaneously generated internally or simultaneously supplied externally allowing for full asynchronous operation.

2.7.2 SCI vs. SHI

The general-purpose DSP563xx DSPs have a serial communication interface (SCI) that allows (RS-232-like) asynchronous serial communication as well as limited synchronous communication. The Symphony DSP56371 and DSP56374 each have one serial host interface (SHI) while the DSP5672x devices have two SHIs, one for each core. Unfortunately, because the SHI only supports I²C and SPI protocols, the SHI is unable to directly support asynchronous SCI operation often used in existing applications built around one of the general-purpose DSP563xx DSPs. In this case, a different communication mechanism/protocol will need to replace the original.

2.8 Host Port

All the general-purpose DSP563xx DSPs have an 8-bit-wide parallel communication interface, the host interface (HI08), which allows an external controller to communicate with the DSP using various protocols. Of all the Symphony DSPs, only the DSP56721 144-pin package has a 24-bit-wide host data interface (HDI24). Although only 16 of the internal 24 data signals are available for use externally, the HDI24 can be used in the same manner as the HI08 on the general-purpose DSP563xx DSPs, including booting either one or both cores from the host port.

Internally, each core of the DSP56721 has its own HDI24 interface. Externally, the host port of one core is selected through the use of the HDI_SEL pin; only one port may be selected at any given time. There is also no mechanism internal to the DSP56721 for selecting which host port is active externally because the HDI24 is a slave-only peripheral.

2.9 Triple Timer Mode

The triple timer module is exactly the same between all of the general-purpose DSP563xx DSPs and Symphony DSPs. Each single core device has a single triple timer module and the dual core devices have two triple timers, one for each core. The most significant difference between the general-purpose DSP563xx DSPs and the Symphony DSPs is that in some Symphony DSPs, all three of the timer pins are not brought out of the device. [Table 4](#) shows the number of timer pins, if any, that are brought out for each of the Symphony DSPs.

Table 4. Number of Triple Timers and Pinned out TIO pins for Symphony

Device	Timers	TIO Pins
DSP56371	1	2 (TIO0 and TIO1 only)
DSP56374 (52-pin and 80-pin)	1	3 (TIO0, TIO1, and TIO2)
DSP56720/DSP56724	2	0
DSP56721/DSP56725 (80-pin)	2	0
DSP56721 (144-pin)	2	1 (TIO0 only) for each timer

2.10 EFCOP

The DSP56L307, DSP56311, and DSP56321 contain a programmable enhanced filter co-processor (EFCOP) module that may be used to reduce the CPU load on the DSP core for filtering operations. The DSP56371 is the only Symphony DSP to contain the EFCOP module. For any existing application that takes advantage of the EFCOP hardware module, the DSP56371 must be used unless the EFCOP code is converted to a software-only implementation.

2.11 GPIO

Like the general-purpose DSP563xx DSPs, nearly all of the peripheral pins of the Symphony DSPs can also be used as GPIO. Many of the Symphony DSP pins are 5-V tolerant as well. It should be noted that the register bit settings for placing pins in GPIO mode differ slightly between the general-purpose DSP563xx and the Symphony DSPs. Consult the General Purpose Input/Output section of your particular Symphony DSP User's Guide for details.

3 Migration Example 1—MIDI Synthesizer

3.1 System Overview

Figure 1 details the block diagram of the first migration example case study, a MIDI synthesizer. The system is controlled by the ColdFire device, which handles all the front panel controls and MIDI input and output. The flash contains the system software as well as the DSP application code. The DSP56303 boots through the HI08 host port. Once the application is up and running, the DSP application parameters may be modified through the HI08 by the ColdFire system controller. Audio data is input and output through the AD/DA, which is connected to the DSP56303 via the ESSIO port. Delays and echoes are possible through the use of the external EDO DRAM connected to the DSP56303.

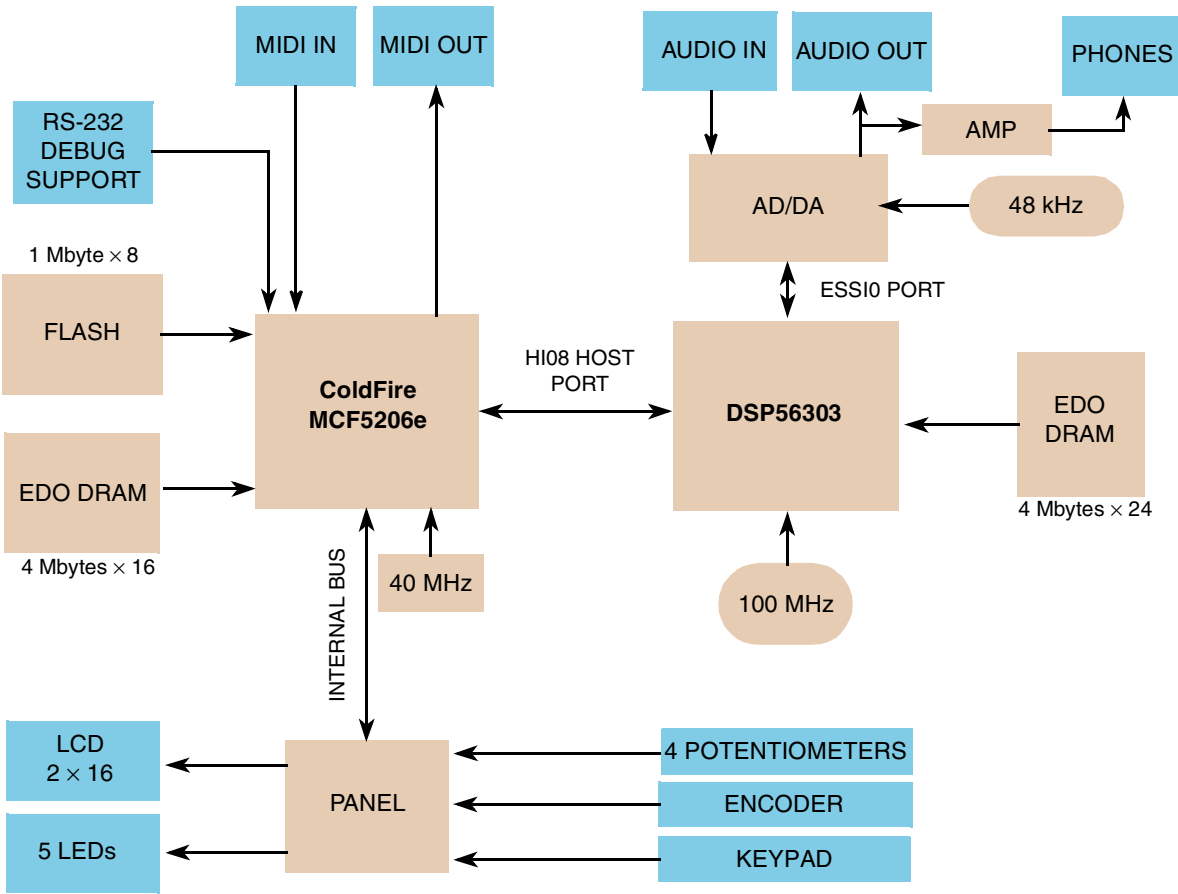


Figure 1. MIDI Synthesizer Block Diagram

3.2 Considerations for Migration

To migrate the DSP56303 in this system to a Symphony DSP, the following should be considered:

- Core supply voltage
- Maximum operating frequency
- Internal memory size

- Synchronous serial interface for AD/DA
- External memory interface
- Host port

The core supply voltage of the DSP56303 is 3.3 V, while the Symphony DSPs' core supply ranges from 1.00 to 1.25 V. In an existing application, an additional voltage regulator needs to be provided to supply the lower voltage for the DSP core. As the maximum operating frequency of the Symphony DSPs range from 150 to 200 MHz, any one of them is capable of taking the place of the DSP56303 (a 100-MHz device) in this synthesizer system. As far as internal memory is concerned, any one of the Symphony DSPs has more internal memory than the DSP56303, so again, any of the Symphony DSPs are potential replacements in this application. The ESAI, with functionality that is a superset of that of the ESSI, can be configured to connect to the AD/DA in this application, allowing any one of the Symphony DSPs to be a candidate for replacement.

The two considerations in this application that become critical when narrowing down of the choice of which, if any, Symphony DSP can replace the DSP56303 comes down to the HI08 host port and the external memory interface (EMI) because none of the Symphony DSPs have both of these peripherals on a single device. Although no direct replacement is possible in this application, there are two options that could fit the bill as will be discussed in the following sections. A third option is also discussed that does not work for this particular case, but could work for different applications.

In all cases, the DSP application code would need to be modified to support the Symphony DSP's differing peripheral set. In this application, it would be the PLL and the ESAI, the host port and the EMC. The particulars of the latter two depend on which particular Symphony DSP is chosen, as will be noted below.

3.3 Option 1—DSP56724 with Emulated Host Port

Using the DSP56724 to replace the DSP56303 in this application would allow the external DRAM memory to be retained but at the expense of the host port. Note that the host port is used to boot the DSP as well as for inter-processor communication during normal operation.

The host port of the DSP56303 could be emulated on the second core of the DSP56724 in software using GPIO and IRQ pins. In this case, no software on the ColdFire side would need to be changed unless the access transactions needed to be slowed down. Only software emulating the host port in the second core would need to be developed. The emulated host port would certainly be much slower than the hardware host port but in this application, the bulk of the transfer occurs when the DSP is booted up and the application code is downloaded or when a whole new DSP application is subsequently downloaded. During normal operation, smaller packets of information are transferred between the ColdFire and DSP.

The speed of the emulated host port running on the second core could be optimized by using the shared memory between the cores and the ability of one core to interrupt the other. It should also be noted that DSP requires an external serial EEPROM to boot the second core with the emulation software because there is no native "boot from host port mode." In this scenario, one core should be booted from a serial EEPROM (either I²C or SPI) and the other core should be booted from the first core.

3.4 Option 2—DSP56721 with No External Memory

If a DSP56721 in the 144-pin package were to replace the DSP56303, then the parallel host port connection between the ColdFire and the DSP could be retained. Going this route keeps the ability for the ColdFire to directly boot the DSP via the host port and retains the high throughput the parallel bus allows.

The obstacle to going this route is the lack of an external memory interface which eliminates the possibility of using the EDO RAM to implement the long delays and echoes. However, a single core of the DSP56721 has more than enough horsepower to replace the DSP56303. Using the shared memory and inter-core communication, the second core's RAM (in all three memory spaces) could be used as additional memory in which to store data. The challenge in using the second core in this way is efficiently shuttling the data between the two cores and only about 1/10th of the memory would be available compared to the original application.

3.5 Option 3—DSP56724 with SPI Replacement of Host Port

While this possibility will not work for this particular application, if a serial port were free on the ColdFire, the parallel host port connection between the DSP and the ColdFire could be replaced with an SPI serial connection. In this scenario, there is some software work that needs to be done on both sides since the low level drivers need to be changed to support the replacement serial connection. As with option 1, the transfers are much slower due to the serial nature but depending on the particular application, the data rate afforded by a serial connection may be adequate. Additionally, because the DSP56724 can boot from the SHI in SPI mode, no external serial EEPROM is required because the ColdFire can boot the DSP directly over the serial connection. Note that the I²C could be used instead, but the maximum bus speed in that case is even slower than SPI.

4 Migration Example 2—DSP Farm

4.1 System Overview

Figure 2 details a simplified block diagram of a DSP farm such as might be seen in a telecom switch or cell phone base station. In this system, the main CPU boots up each DSP56303 individually through the host port, each DSP having its own chip select. Each DSP56303 is connected to its own codec through one ESSIO. The other ESSIO of each DSP is on the same bus where each DSP transmits and receives data from a TDM network.

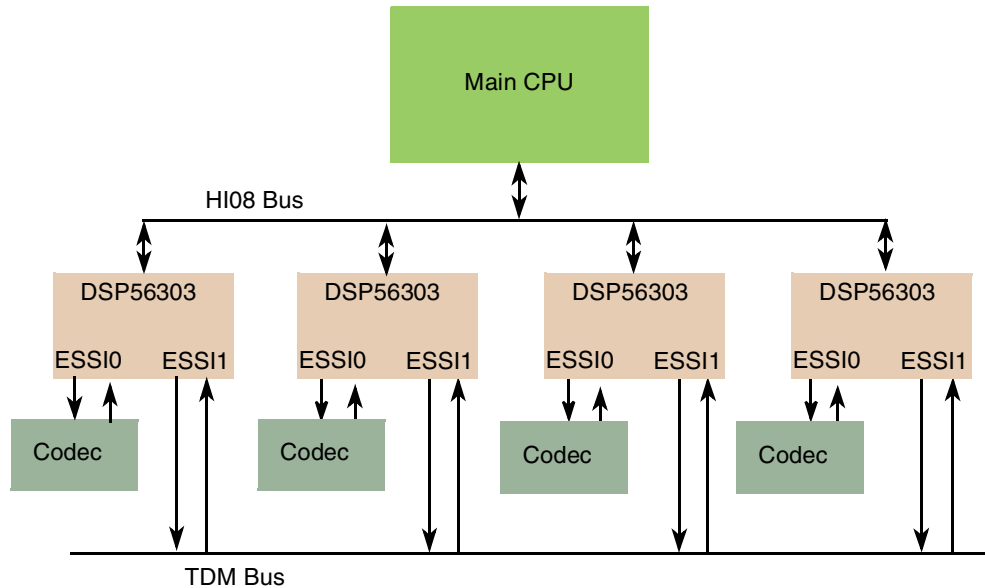


Figure 2. DSP Farm Block Diagram

4.2 Considerations for Migration

In this case, the choice of a replacement device becomes almost trivial. Because an HI08 bus interconnects the main CPU to all the DSPs, the best choice is to use the Symphony DSP with a host port (HDI24), the DSP56721 in the 144-pin package. All of the other considerations regarding core voltage and maximum operating frequency apply as in Section 3, “Migration Example 1—MIDI Synthesizer,” but there is an additional advantage in this application. Because there are two cores within the DSP56721 and a total of four ESAIs, two dual-core DSP56721s can replace the four DSP56303s shown in the diagram. The total system parts count is reduced as a result. It should be noted that in a migrated system using the DSP56721 that the main CPU can only communicate with one core’s host port at a time, selected by the HDI_SEL pin. Figure 3 shows the simplified block diagram of the DSP farm migrated to the DSP56721.

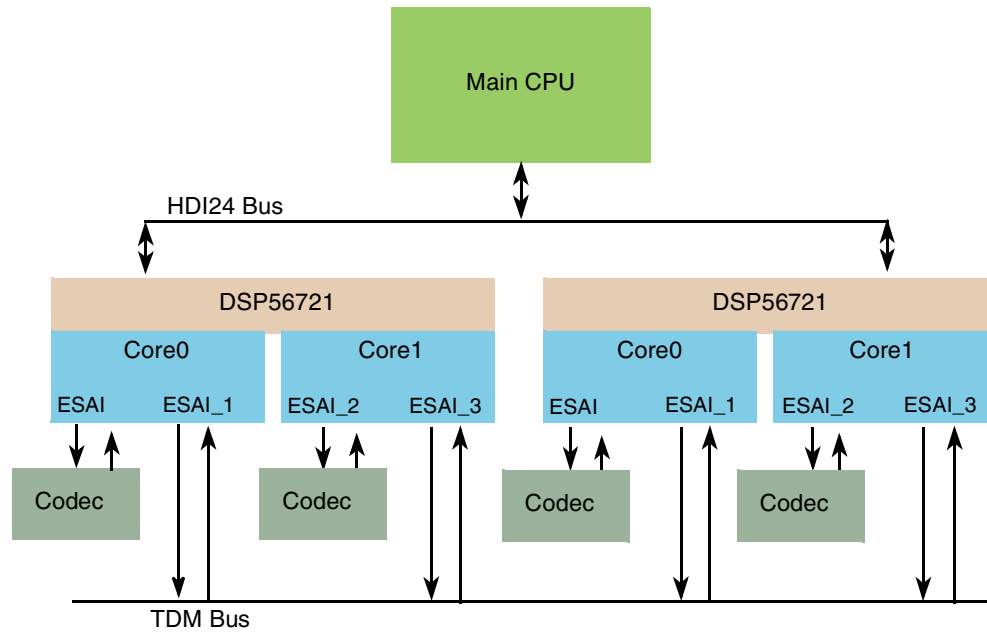


Figure 3. Migrated DSP Farm Block Diagram

5 References

Other useful references are as follows:

- DSP56300 Family Manual
- DSP56371 User’s Guide
- DSP56371 Data Sheet
- DSP56374 User’s Guide
- DSP56374 Data Sheet
- DSP56720/DSP56721 Reference Manual
- DSP56720/DSP56721 Data Sheet
- DSP56724/DSP56725 Reference Manual
- DSP56724/DSP56725 Data Sheet

6 Revision History

Table 5 provides a revision history for this application note.

Table 5. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	12/2008	Initial public release.

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