

# MC9S08DZ60 Migrating from the 3M05C to M74K Mask Set

by: D. Scott Brown  
Applications Engineering  
Microcontrollers Solutions Group  
Austin, TX, USA

Gordon Borland  
Applications Engineering  
Microcontrollers Solutions Group  
East Kilbride, Scotland

## 1 Introduction

Freescale provides the M74K mask sets of the 9S08DZ60 to address a number of errata found on previous mask sets, including errata associated with the timer PWM module (TPM) module.

Both the 0M74K and 1M74K mask sets may be offered to customers. There are no functional differences between the 0M74K and 1M74K. The remainder of the document will refer to the M74K to denote both.

This document addresses the differences between the two mask sets, 3M05C and M74K. This application note does not describe in detail how to use the DZ60 in a particular system. It highlights the differences from the earlier mask set versions and provides guidance in migrating code. Programmers and designers must consult the specific HCS08 MCU data sheet for further information on using and programming the device. This application note also refers to errata data *PWM Boundary Case Issues in HCS08 Timer PWM Module (TPM)*

## Contents

1	Introduction	1
2	Introducing the DZ60 and the M74K Mask set	2
2.1	M74K 9S08DZ60 Enhanced Features Over the 3M05C Version	2
3	Multi-Purpose Clock Generator (MCG)	3
4	Timer PWM Module v3	3
5	TPMxCnVH:TPMxCnVL Latching	3
5.1	Input Capture Mode	3
5.2	Output Compare Mode	4
5.3	Edge Aligned PWM Mode	4
5.4	Center Aligned PWM Mode	4
5.5	Resetting the Latching Mechanism	5
6	Coherency Mechanism in Background Debug Mode (BDM)	5
7	Inter-Integrated Circuit (IIC)	6
8	IIC Control Register 2 (IICC2)	6
9	10-Bit Address Extension	6
10	EEPROM Blank Check	7
11	PTA7/ADP7	7
12	Controller Area Network (MSCAN)	8
13	Conclusion	8

## Introducing the DZ60 and the M74K Mask set.

*SE110-TPM*. To download this document go to [freescale.com](http://freescale.com)

Device mask sets can be identified by the part markings that include the mask set on the device package.

### NOTE

With the exception of mask set errata documents, if any other Freescale document contains information that conflicts with the information in the device data sheet, the data sheet must be considered to have the most current and correct data.

The major differences between the 3M05C and M74K mask sets are within the following modules:

- Multi-purpose clock generator (MCG)
- Timer / pulse width modulation (TPM)
- Inter-integrated circuit (IIC) serial peripheral
- EEPROM
- Port pin, PTA7
- MSCAN

## 2 Introducing the DZ60 and the M74K Mask set.

Further expanding the core's offerings in the automotive and industrial spaces by adding CAN and EEPROM, the DZ60 represents an evolutionary step for Freescale's S08 family.

The M74K mask set addresses errata and CAN bus conformance issues can seen in the 3M05C mask set DZ60 to better support those application spaces.

### 2.1 M74K 9S08DZ60 Enhanced Features Over the 3M05C Version

Multi-purpose clock generator (MCG)

- Addressed narrow clock pulse errata, sometimes encountered in FEI/FEE mode

Timer/pulse width modulation (TPMv3)

- Addressed errata. See *PWM Boundary Case Issues in HCS08 Timer PWM Module (TPM) SE110-TPM* found in TPM v2

Inter-integrated circuit (IIC) serial peripheral

- 10-bit operation is now available

### NOTE

High drive strength setting on ports still prohibits IIC functionality.

EEPROM — Blank check correctly shows state of EEPROM locations

PTA7/ADP7 — Able to use the ADC channel AD7

MSCAN — Conformance robustness issue fixed

Of the above enhancements, the TPMv3 (M74K mask) is the only module that might require code changes from software previously written and tested on a mask set with TPMv2 (3M05C mask).

#### NOTE

If using IIC in a 7-bit addressing mode as a workaround for 10-bit addressing mode errata. The code will also need conversion.

### 3 Multi-Purpose Clock Generator (MCG)

The M74K addresses an errata sometimes observed when the FLL is enabled where the output of the MCG has short clock pulses that potentially lead to runaway code. There are no functional differences between the 3M05C and M74K other than eliminating the errata behavior. No code considerations are necessary.

### 4 Timer PWM Module v3

The M74K timer module is essentially the same on the 3M05C. The way the timer modules have been integrated into the MCU is slightly different. These differences can be summarized as:

- TPMxCnVH:TPMxCnVL latching
- Coherency mechanism in background debug mode

In the process of addressing some errata associated with the TPMv2, necessary design changes were made that have impacted behavior in a few modes. These module changes were implemented to address TPM functional shortcomings for using in a number of targeted applications. These changes also maintain compatibility with newer S08 devices.

As a result, the order that registers are written to configure the TPM modules may vary from TPMv2 to TPMv3.

### 5 TPMxCnVH:TPMxCnVL Latching

On the M74K the latching mechanism for registers TPMxCnVH:TPMxCnVL is different from the 3M05C.

#### 5.1 Input Capture Mode

In the input capture mode, reading either byte (TPMxCnVH or TPMxCnVL) latches the contents of both bytes into a buffer where they remain until the other byte is read. This is true for both the M74K and 3M05C.

On the M74K writes to TPMxCnVH:TPMxCnVL are ignored in input capture mode. On the 3M05C it is possible to write to TPMxCnVH:TPMxCnVL in input capture mode.

## 5.2 Output Compare Mode

In output compare mode, writing to either byte (TPMxCnVH or TPMxCnVL) latches the value into a buffer.

For the 3M05C, the TPMxCnVH:L registers are updated from the buffer as a coherent 16-bit value after the second byte has been written.

In the case of the M74K, the TPMxCnVH:L registers are updated from the buffer, as a coherent 16-bit value according to the value of CLKS bits.

If (CLKS[1:0] = 00), the registers are then updated when the second byte is written.

If (CLKS[1:0] 00), the registers are then updated at the next TPM counter change (end of the prescaler counting) after the second byte is written.

## 5.3 Edge Aligned PWM Mode

In the edge aligned PWM mode, writing to either byte (TPMxCnVH or TPMxCnVL) latches the value into a buffer.

For the 3M05C, the TPMxCnVH:L registers are updated from the buffer as a coherent 16-bit value when the TPM counter changes from TPMxMODH:L to \$0000 after the second byte has been written.

In the case of the M74K, the TPMxCnVH:L registers are updated from the buffer as a coherent 16-bit value according to the value of CLKS bits.

If (CLKS[1:0] = 00), the registers are then updated when the second byte is written.

If (CLKS[1:0] 00), the registers are then updated after the second byte has been written when the TPM counter changes from (TPMxMODH:L - 1) to (TPMxMODH:L). If the TPM counter is a free-running counter, the TPMxCnVH:L registers are then updated when the TPM counter changes from \$FFFE to \$FFFF.

## 5.4 Center Aligned PWM Mode

In center aligned PWM mode, writing to either byte (TPMxCnVH or TPMxCnVL) latches the value into a buffer.

For the 3M05C, the TPMxCnVH:L registers are updated from the buffer as a coherent 16-bit value when the TPM counter changes from TPMxMODH:L to (TPMxMODH:L - 1) after the second byte has been written.

In the case of the M74K, the TPMxCnVH:L registers are updated from the buffer as a coherent 16-bit value according to the value of CLKS bits.

If (CLKS[1:0] = 00), the registers are then updated when the second byte is written.

If (CLKS[1:0] 00), the registers are then updated after the second byte has been written when the TPM counter changes from (TPMxMODH:L - 1) to (TPMxMODH:L). If the TPM counter is a free-running counter, then the TPMxCnVH:L registers are updated when the TPM counter changes from \$FFFE to \$FFFF.

## 5.5 Resetting the Latching Mechanism

Writing to TPMxCnSC resets the latching mechanism for TPMxCnVH:L on both the 3M05C and M74K. In input capture mode writing to TPMxCnSC after reading one channel value register but before reading the other resets the latching mechanism and may result in the current channel value register data being overwritten if a new input capture occurs.

In output compare or PWM modes writing to TPMxCnSC, after writing to the channel value registers TPMxCnVH:L before they are updated, effectively cancels the write to TPMxCnVH:L leaving the register values unchanged.

This is particularly relevant for the M74K, depending upon the configuration of CLKS and the selected mode there could be a considerable time before registers TPMxCnVH:TPMxCnVL are updated. It is therefore important to ensure that TPMxCnSC is not written during this time unless the user wishes to cancel a previous write to the channel value registers.

As a result of these differences in the latching mechanism, users may have to initialize their timer registers in a different order than before to allow this.

## 6 Coherency Mechanism in Background Debug Mode (BDM)

Registers TPMxCNTH:L, TPMxMODH:L, and TPMxCnVH:L have a coherency mechanism that latches both bytes of the register into a buffer where they remain latched until both bytes have been accessed. This allows coherent 16-bit reads or writes in either big-endian or little-endian order for easier implementation.

On the M74K this coherency mechanism behaves differently from the 3M05C in background debug mode.

**TPMxCNTH:L** — On the M74K any read of TPMxCNTH:L registers in background debug mode returns the value of the TPM counter which is frozen.

For the 3M05C, if only one byte of the TPMxCNTH:L registers was read before entering BDM, then any subsequent read of TPMxCNTH:L registers during BDM returns the latched value of TPMxCNTH:L from the read buffer instead of the frozen TPM counter value.

On the M74K the read coherency mechanism can be reset in BDM if there is a write to TPMxSC, TPMxCNTH, or TPMxCNTL. These conditions do not reset the read coherency mechanism on the 3M05C.

**TPMxCnVH:L** — On the M74K any read of TPMxCnVH:L registers in background debug mode returns the value of these registers.

For the 3M05C, if only one byte of the TPMxCnVH:L registers was read before entering BDM, then any subsequent read of TPMxCnVH:L registers during BDM returns the latched value of TPMxCnVH:L from the read buffer instead of the value from the registers.

On the M74K the read coherency mechanism can be reset in BDM if there is a write to TPMxCnSC. This condition does not reset the read coherency mechanism on the 3M05C.

TPMxMODH:L — On the M74K the write coherency mechanism of the TPMxMODH:L registers can be reset in BDM if there is a write to TPMxSC. This condition does not reset the read coherency mechanism on the 3M05C.

For more information on the TPM, please refer to the Freescale document MC9S08DZ60 Data Sheet.

## 7 Inter-Integrated Circuit (IIC)

The inter-integrated circuit (IIC) peripheral on the M74K offers all the functionality of the 3M05C IIC, while fixing the 10-bit addressing mode errata.

## 8 IIC Control Register 2 (IICC2)

This 10-bit addressing mode is enabled via the IICC2 register.

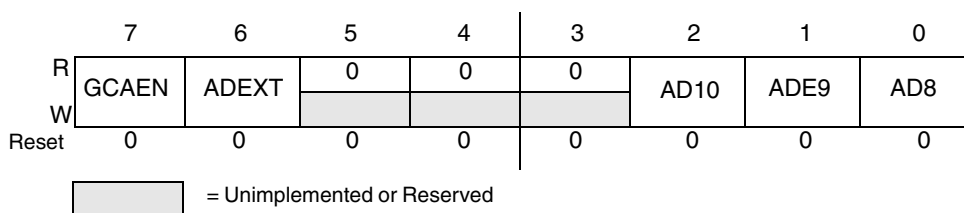


Figure 1. IIC Control Register (IICC2)

Table 1. IICC2 Field Descriptions

Field	Description
7 GCAEN	General Call Address Enable – The GCAEN bit enables or disables general call address. 0 General call address is disabled. 1 General call address is enabled.
6 ADEXT	Address extension – The ADEXT bit controls the number of bits used for the slave address. 0 7-bit address scheme. 1 10-bit address scheme.
2:0 AD[10:8]	Slave Address – The AD[10:8] field contains the upper three bits of the slave address in the 10-bit address scheme. This field is only valid when the ADEXTbit is set.

The IICC2 register controls the general call address function and the 10-bit address extension.

## 9 10-Bit Address Extension

Setting bit ADEXT allows the IIC to operate using an extended slave address of ten bits. The additional three address bits (AD10:8) are contained within IICC2.

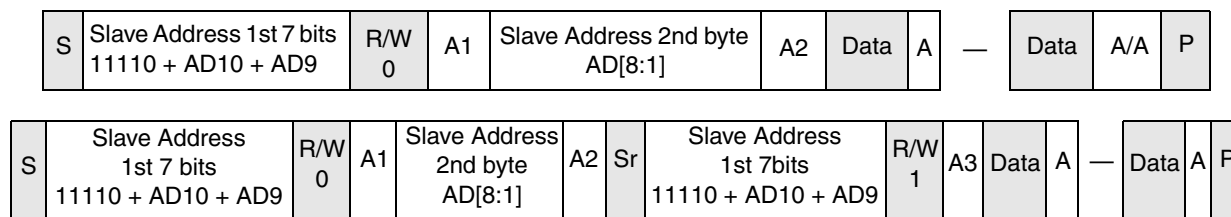
When conducting data transfers using 7-bit addressing, a single address byte is used to identify the slave and indicate the data direction. Therefore, the format was always a calling address byte followed by data bytes for both master transmitter and master receiver communications.

When the 10-bit extended address is enabled, the protocol for initiating data transfers via the IIC is slightly changed.

In the case of a master transmitter data transfer of two address bytes are required to address the slave. The first address byte always has 0x11110 as its first 5 bits, followed by address bits AD10 and AD9 then the data direction bit. The second address byte consists of the remaining address bits (AD8:1). Once both address bytes have been successfully acknowledged then the master can begin to transmit data to the slave.

For a master receiver data transfer the protocol is more complicated. In this case three address bytes are necessary to address the slave. The first two address bytes are configured exactly as the master transmit data transfer. After these two bytes have been successfully acknowledged, a repeated start signal is sent and the first address byte is resent, but this time with the data direction bit configured to indicate that the slave must transmit data to the master receiver.

A summary of the 10-bit extended address protocol is shown below for both a master transmitter and master receiver data transfers.



**Figure 2. Master–Transmitter Addresses Slave–Receiver with a 10-bit Address**

S = START signal

Ax = Acknowledge bit

Sr = repeated START signal

P = STOP signal

For more information on the IIC, please refer to Freescale document MC9S08AC60 Data Sheet.

## 10 EEPROM Blank Check

With the M74K mask sets, a blank check will display the correct contents of the EEPROM.

Other than eliminating the errata behavior, there are no functional differences between 3M05C and M74K. No code considerations are necessary.

## 11 PTA7/ADP7

With the M74K mask sets, the customer is now able to use the port pin as an analog input. However, the pin can no longer be used to wake the part from stop.

If this pin was used to wake the part up from stop, then code must be modified.

## 12 Controller Area Network (MSCAN)

The MSCAN module on the M74K mask set received improvements to pass CAN conformance testing. Other than eliminating the errata behavior, there are no functional differences between 3M05C and M74K. No code considerations are necessary.

## 13 Conclusion

Freescale's M74K mask set of the 9S08DZ60 offers customers a robust solution, addressing the errata found on the 3M05C for automotive and industrial applications. The changes found in the latest mask set do not present any difficulties for programmers or designers familiar with previous versions that wish to migrate to the new version.

All of the new features and enhancements above must be taken into account when migrating from the 3M05C to the M74K.

Finally the user is advised to read the relevant chapters of the latest 9S08DZ60 specifications to ensure that all of the new features and any differences have been fully captured.



THIS PAGE IS INTENTIONALLY BLANK

## **How to Reach Us:**

### **Home Page:**

[www.freescale.com](http://www.freescale.com)

### **Web Support:**

<http://www.freescale.com/support>

### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor, Inc.  
Technical Information Center, EL516  
2100 East Elliot Road  
Tempe, Arizona 85284  
1-800-521-6274 or +1-480-768-2130  
[www.freescale.com/support](http://www.freescale.com/support)

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[www.freescale.com/support](http://www.freescale.com/support)

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor China Ltd.  
Exchange Building 23F  
No. 118 Jianguo Road  
Chaoyang District  
Beijing 100022  
China  
+86 10 5879 8000  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### **For Literature Requests Only:**

Freescale Semiconductor Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
1-800-441-2447 or +1-303-675-2140  
Fax: +1-303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.



Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2008. All rights reserved.

AN3776  
Rev. 0  
09/2008