IRTC Compensation and 1 Hz Clock Generation

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Contents

1   Introduction

The MC9S08GW64 provides a low-cost SOC (System-on-Chip) platform for e-meter applications. Its on-chip independent real-time clock (IRTC) module provides the functionality of a basic real-time clock, such as time-keeping and calendaring. The IRTC also provides functionality to compensate the 1 Hz clock for variations in crystal or in temperature.

This application note describes the compensation of the IRTC and how to generate a 1 Hz clock for calibration.

2   Compensation of IRTC

The IRTC uses the external 32768 Hz oscillator clock to generate the 1 Hz clock with a prescaler of 32768. The IRTC_COMPEN register is used to configure the compensation; it includes the compensation interval and compensation value. The compensation circuit adds or removes the number of oscillator cycles (compensation value) in a period (compensation interval) determined by the IRTC_COMPEN register.

The compensation interval is an unsigned number which can be set to 1–255 seconds; but the compensation value is a signed number which ranges from –128 to 127. Adding or removing one clock cycle generates about ±30.5 ppm

(1/32768) deviation, so the compensation capability is from 0.119 ppm (interval = 255, value = 1) to 3906 ppm (interval = 1, value = –128). The compensation is disabled when the compensation interval or value is set to zero.

The IRTC module performs the compensation in the first second of the compensation interval. Based on the compensation configuration, the first second is added or removed for the number of oscillator clock cycles (compensation value), but the other seconds keep no changes. So the time-length for each second is different, but the timing precision overall is high because of the compensation.

The IRTC module of the MC9S08GW64 can be configured to output the compensated 1 Hz clock via the RTCCLKOUT pin. Figure 1 illustrates the 1 Hz lock on the RTCCLKOUT pin. The time-length of the positive level is only one oscillator clock cycle (1/32768 second).
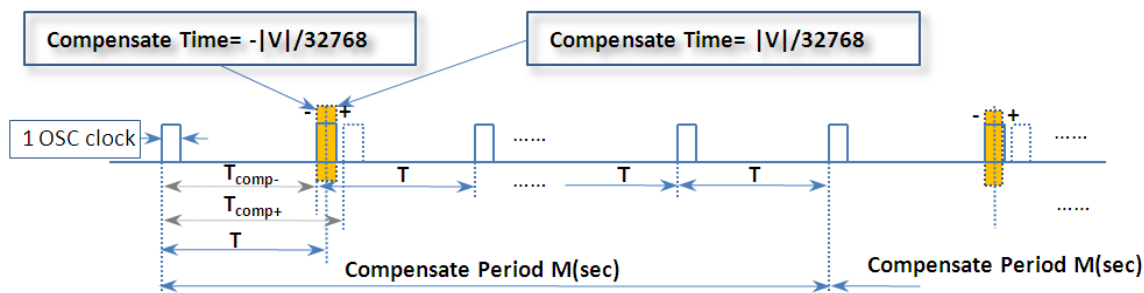
Figure 1. Compensation output of IRTC

In the figure, the compensation interval is M and the compensation value is V.

T= 32768 oscillator clock

$T_{comp+/-}$ = (32768 ± |V|) oscillator clock

The first second (T_{comp}) is shortened or prolonged for |V| oscillator clock cycles according to the compensation value. The time-length for the other seconds is still 32768 oscillator clock cycles (T).

The compensation interval and value can be selected according to the crystal error and the precision after compensation. Table 1 provides examples for calculating the compensation interval and value by using the minimum error after compensation.

Table 2 lists the compensation value and error after compensation for different compensation intervals when the crystal error is –2 ppm. The compensation values are calculated for different compensation intervals (using Equation 2); the errors after compensation are also calculated according to different compensation intervals and values (Equation 3). The best compensation interval (61) and value (4) are selected based on the minimum error after compensation.

Equation 1: $\mathrm{Dev}_{OneClock} = \dfrac{10^{12}}{32768 \times \left(10^6 - CrystalError\right)}$

Equation 1 calculates the deviation generated by a new crystal clock cycle.

Equation 2: $CompensationValue = \dfrac{CrystalError \times CompensationInterval}{Dev_{OneClock}}$

Equation 3:
$ErrorAfterCompensation = CrystalError \times CompensationInterval - CompensationValue \times Dev_{OneClock}$

In Table 1 the compensation value and the error after compensation are listed for different crystal error values. The compensation interval is limited to 127. After compensation, the error is decreased greatly if the measuring period is greater than the compensation interval.

Table 1. Compensation value depending on crystal error (compensation interval < 128)

Crystal error (frequency: ppm)	Compensation interval	Compensation number	Error after compensation (ppm)
0	0	0	0
−1	61	−2	0.035095215
−2	61	−4	0.07006836
−3	61	−6	0.104919435
−4	61	−8	0.139648441
−5	116	−19	−0.16891478
−6	117	−23	−0.099914526
−7	109	−25	−0.065887414
−8	103	−27	−0.031982369
−9	78	−23	−0.102020207
−10	58	−19	−0.171813907
−11	86	−31	0.034515495
−12	89	−35	0.102417146
−13	54	−23	−0.104827762
−14	109	−50	−0.142455756
−15	59	−29	−0.003509322
−16	103	−54	−0.077148016
−17	79	−44	0.165314065
−18	39	−23	−0.108337175
−19	53	−33	0.060943967
−20	29	−19	−0.177612073
−21	93	−64	0.083985236
−22	43	−31	0.024109345
−23	69	−52	−0.122435684
−24	103	−81	−0.135496623
−25	83	−68	0.143433914
−26	27	−23	−0.113952162
−27	26	−23	−0.114654029
−28	97	−89	−0.01159455
−29	20	−19	−0.182830323
−30	59	−58	−0.033567743
…	…	…	…

Table 2. Compensation value and error after compensation for different compensation intervals (crystal error = –2 ppm)

Compensation interval	Total error in compensation interval (ppm)	Compensation value	Round compensation value	Error after compensation (ppm)
1	–2	–0.065536131	0	–2
2	–4	–0.131072262	0	–4
3	–6	–0.196608393	0	–6
4	–8	–0.262144524	0	–8
5	–10	–0.327680655	0	–10
6	–12	–0.393216786	0	–12
7	–14	–0.458752918	0	–14
8	–16	–0.524289049	–1	14.517517
9	–18	–0.58982518	–1	12.517517
10	–20	–0.655361311	–1	10.517517
11	–22	–0.720897442	–1	8.5175171
12	–24	–0.786433573	–1	6.5175171
13	–26	–0.851969704	–1	4.5175171
14	–28	–0.917505835	–1	2.5175171
15	–30	–0.983041966	–1	0.5175171
16	–32	–1.048578097	–1	–1.4824829
17	–34	–1.048578097	–1	–3.4824829
18	–36	–1.179650359	–1	–5.4824829
19	–38	–1.24518649	–1	–7.4824829
20	–40	–1.310722621	–1	–9.4824829
21	–42	–1.376258753	–1	–11.482483
22	–44	–1.441794884	–1	–13.482483
23	–46	–1.507331015	–2	15.035034
24	–48	–1.572867146	–2	13.035034
25	–50	–1.638403277	–2	11.035034
26	–52	–1.703939408	–2	9.0350342
27	–54	–1.769475539	–2	7.0350342
28	–56	–1.83501167	–2	5.0350342
29	–58	–1.900547801	–2	3.0350342
30	–60	–1.966083932	–2	1.0350342
31	–62	–2.031620063	–2	–0.9649658
32	–64	–2.097156194	–2	–2.9649658
33	–66	–2.162692325	–2	–4.9649658

Table continues on the next page...

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Table 2. Compensation value and error after compensation for different compensation intervals (crystal error = –2 ppm) (continued)

Compensation interval	Total error in compensation interval (ppm)	Compensation value	Round compensation value	Error after compensation (ppm)
34	–68	–2.228228456	–2	–6.9649658
35	–70	–2.293764588	–2	–8.9649658
36	–72	–2.359300719	–2	–10.964966
37	–74	–2.42483685	–2	–12.964966
38	–76	–2.490372981	–2	–14.964966
39	–78	–2.555909112	–3	13.552551
40	–80	–2.621445243	–3	11.552551
41	–82	–2.686981374	–3	9.5525513
42	–84	–2.752517505	–3	7.5525513
43	–86	–2.818053636	–3	5.5525513
44	–88	–2.883589767	–3	3.5525513
45	–90	–2.949125898	–3	1.5525513
46	–92	–3.014662029	–3	–0.4474487
47	–94	–3.08019816	–3	–2.4474487
48	–96	–3.145734291	–3	–4.4474487
49	–98	–3.211270423	–3	–6.4474487
50	–100	–3.276806554	–3	–8.4474487
51	–102	–3.342342685	–3	–10.447449
52	–104	–3.407878816	–3	–12.447449
53	–106	–3.473414947	–3	–14.447449
54	–108	–3.538951078	–4	14.070068
55	–110	–3.604487209	–4	12.070068
56	–112	–3.67002334	–4	10.070068
57	–114	–3.735559471	–4	8.0700684
58	–116	–3.801095602	–4	6.0700684
59	–118	–3.866631733	–4	4.0700684
60	–120	–3.932167864	–4	2.0700684
61	–122	–3.997703995	–4	0.0700684
62	–124	–4.063240126	–4	–1.9299316
63	–126	–4.128776258	–4	–3.9299316
64	–128	–4.194312389	–4	–5.9299316
…	…	…	…	…

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In a real application, we can calculate and select the suitable compensation interval and value according to the precision after compensation. The maximum compensation interval can also be set according to the requirement for different applications. For example, the maximum compensation interval must be set to 60 if your application needs high precision timing for every minute.

The crystal error can be calculated according to the environment temperature and the crystal life. The firmware can use a look-up table to get the compensation value and update the IRTC_COMPEN register when the crystal error changes. The procedure for doing this will not be described in this application note.

3 Using FTM to generate 1 Hz clock

In this section, one solution for using the FTM to correct the 1 Hz clock output by IRTC will be described. The 1Hz clock

- Has higher precision (cycle by cycle)
- Has about 50% duty cycle

3.1 1 Hz clock generation based on RTCCLKOUT

With the IRTC compensation scheme, the precision of RTCCLKOUT clock output in the long term is ensured. Provided that the compensation interval is M (M > 1) seconds in figure 1, "Compensation output of IRTC," the first second in the compensation interval is different from the other seconds because it includes the compensation time. If we can average the compensation time-length in a compensation interval to make every second in this interval have the same length (each second can be compensated), we will get a high-precision clock output.

The firmware calculates the compensation time for every second, and applies this compensation time to each second in the compensation interval. If the compensation interval is M and the compensation value is N, the compensation time for each second is $N / (32768 \times M)$ second. The time-length of $N / (32768 \times M)$ may be a very small number, so a high frequency clock is necessary for getting higher resolution (precision).

In this solution we use the bus clock, which is generated by the FLL with an external 32768 Hz crystal (XOSC1) engaged. The FLL and IRTC share the same external oscillator. The FLL multiplier of the ICS module is set to 512, so the bus clock frequency is 512×32768 Hz. The compensation time for each second is $(512 \times N) / M$ bus clock, so it cancels the impact of the variance or changes caused by temperature or the age of the crystal.

Looking at figure 1, "Compensation output of IRTC," we can see that the last clock edge in the current compensation period is also the first clock edge of the next compensation period. By taking the first clock edge in each compensation period as the alignment, the IRTC compensation precision is inherited (either the rising or falling edge can be used for the alignment; this is controlled by the firmware setting).

The MC9S08GW64 provides an FTM module with 2 channels. One channel is used to capture the pulse output by IRTC module in this solution, and the other channel is used to output the 1 Hz clock.

The FTM is set to use the bus clock when channel 1 captures the rising (or falling) edge of the IRTCCLKOUT output. The FTMCH1 interrupt is triggered and the FTM counter value is saved to the FTMCH1V register when the edge is captured. In the FTMCH1 interrupt service routine, the FTMCH0 is set to out-compare mode, the compare value is set to the sum of FTMCH0V and a shift value Φ. The value Φ is the sum of a constant σ and the adjust value for each clock cycle. Table 3 lists the rising time of the IRTCCLKOUT and FTM output, the time-width of IRTCCLKOUT and FTM output.

Table 3. 1Hz timing of IRTCCLKOUT and FTM output

Rising edge number	0	1	2	3	…	M
IRTCCLCKOUT time	0	32768 + V	2 × 32768 + V	3 × 32768 + V	—	M × 32768 + V

Table continues on the next page...

Table 3.   1Hz timing of IRTCCLKOUT and FTM output (continued)

| Rising edge number	0	1	2	3	…	M
FTM CH0 ouput time	σ	$32768 + V + \sigma - (M - 1) \times T_{AVG}$	$2 \times 32768 + V + \sigma - (M - 2) \times T_{AVG}$	$3 \times 32768 + V + \sigma - (M - 3) \times T_{AVG}$	…	$M \times 32768 + V + \sigma - (M - 3) \times T_{AVG}$
IRTCCLKOUT clock width	N/A	$32768 + V$	32768	32768	32768	32768
FTM CH0 ouput clock width	N/A	$32768 + T_{AVG}$	$32768 + T_{AVG}$	$32768 + T_{AVG}$	$32768 + T_{AVG}$	$32768 + T_{AVG}$

$T_{AVG} = V \div M$ (Oscillator clock)

$\qquad = 512 \times V \div M$ (Bus clock)

According to the timing in Table 3, we can see that the phase of the RTCCLKOUT output is shifted to the right with a value of σ at first. Each second is compensated with the average compensation value.

The diagrams in Figure 2 and Figure 3 describe the implementation of this solution in detail. Figure 2 illustrates the case when some oscillator clock cycles are added.
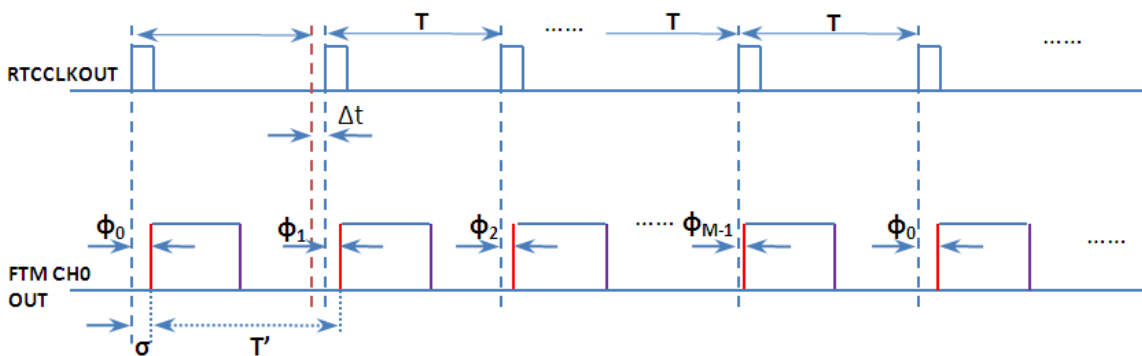
Figure 2. FTM output if compensation value > 0

In Figure 2 :
- Compensate period: M
- Compensate value: V (> 0)
- $\Delta t = V \times 10^{12} \div (32768 \times (10^6 - CrystalError))$
- $\Phi_0 = \sigma$
- $\Phi_1 = \sigma - (M - 1) \times T_{AVG}$
- $\Phi_2 = \sigma - (M - 2) \times T_{AVG}$
- …
- $\Phi_{M - 1} = \sigma - T_{AVG}$
- $T' = T + \Delta t = T + V \times 10^{12} \div (32768 \times (10^6 - CrystalError))$

Figure 3 illustrates the case when some oscillator clocks are removed.
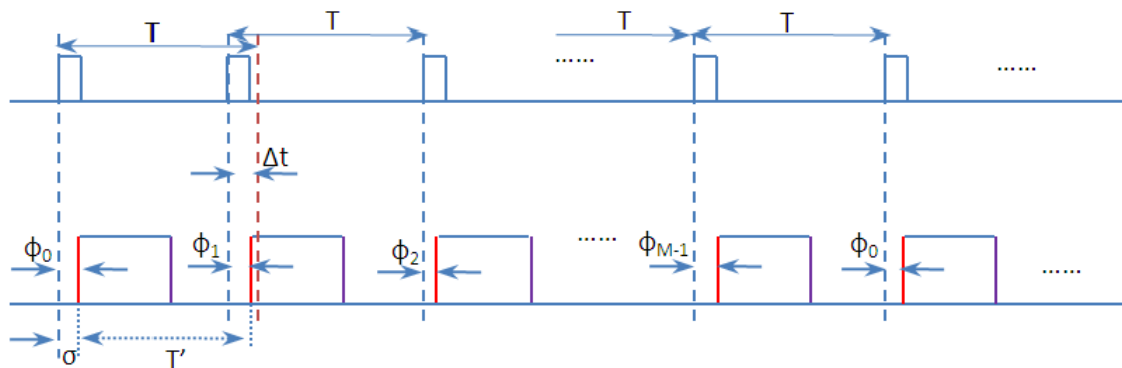
Figure 3. FTM output if compensation value < 0

In Figure 3:

- Compensate period: M
- Compensate value: V (< 0)
- $\Delta t = V \times 10^{12} \div (32768 \times (10^6 - CrystalError))$
- $\Phi_0 = \sigma$
- $\Phi_1 = \sigma + (M-1) \times T_{AVG}$
- $\Phi_2 = \sigma + (M-2) \times T_{AVG}$
- …
- $\Phi_{M-1} = \sigma + T_{AVG}$
- T' = T – Δt = T – |V| × 10^{12} ÷ (32768 × (10^6 – CrystalError))

The shift value σ (delay) is used for two purposes:

1. Shift the phase of IRTC clock output — the compensation time for each second is based on this value.
2. The FTMCH1 interrupt is given enough time to be serviced.

The compensation time for each second will be increased by the value of σ. In the attached example code, the σ value is set to 0x8000, which is about 1.9 ms when the bus clock is 32768 × 512 Hz. The σ value is determined by the compensation period and the maximum compensation value.

$0 < \sigma - (M - 1)(512 \times V/M) < 0xFFFF$

–128 < V < 127

Basically, the crystal error is minus over the temperature changes, so the σ value can be set to a small value (for example, 0x2000 or 0x1000). The compensation range will be expanded.

FTMCH0 is set to out compare mode (set output on match), the FTMCH0 pin is set to high state once the FTM counter matches the value in the FTMCH0V register, and the FTMCH0 interrupt is triggered. The FTM clock divider is set to 128, and FTMCH0 is configured to clear output on match after 0.5 second. When the FTMCH0 output is cleared, the FTM clock divider is changed to 1.

3.2 Code example

One CodeWarrior project is included with this application note. The code is developed in CodeWarrior 6.3 IDE. It can run on the MC9S08GW64 tower board (TWR-S08GW64) with a small re-work (Figure 4). The RTCCLKOUT (pin 20) must be connected to FTMCH1 (pin 38). The 1 Hz clock can be measured on FTMCH0 (pin 37).
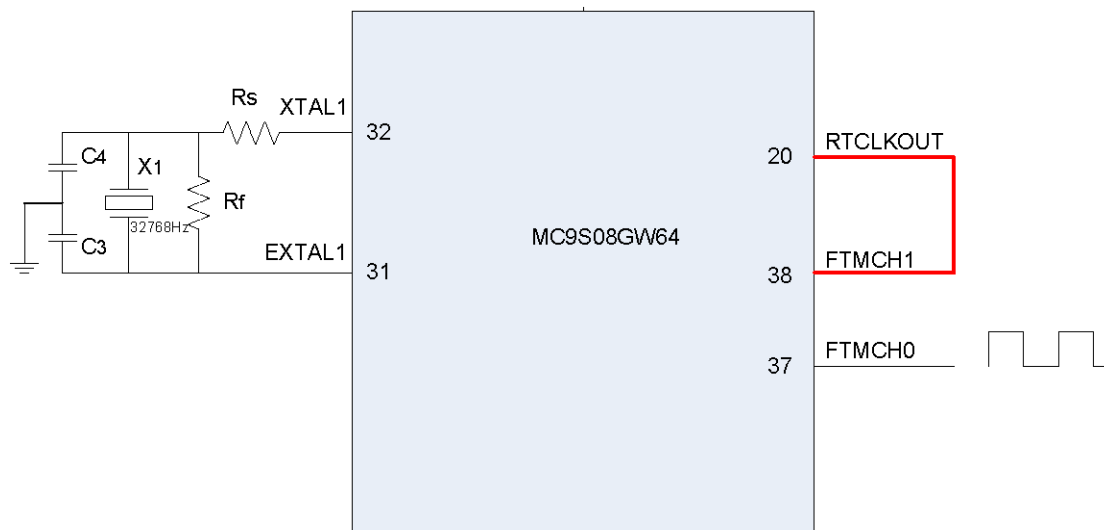
Figure 4. TWR-S08W64 after being reworked

In the interrupt service routine of FTMCH1:

```
void interrupt VectorNumber_Vftmch1 FTMCH1_Isr(void)
{
  long tmp;

  (void)FTMC1SC;
  FTMC1SC_CH1F = 0;

  if(IRTC_STATUS_L_C_DON || Comp_Start_Flag )
  {
................
```

The C_DON bit (IRTC_STATUS_L_C_DON) of the IRTC_STATUS register will be set before the compensation period is completed. This bit is used to align the compensation period.

IRTC compensation is used to output a 1 Hz clock with high precision for a long period (> compensation interval). The FTM is used to ensure the same clock period cycle by cycle in a compensation interval.

The external crystal error can be calculated according to the temperature and the life of the crystal. The calculation method is not mentioned in this document.

NOTE

When you develop the MC9S08GW64 project, the IRTC initialization or IRTC interrupt service routine is recommended to disable the IRTC interrupt or service the IRTC interrupt events. This is because the IRTC module keeps the previous configuration even when new firmware is downloaded. The IRTC interrupt must be serviced or disabled in the initialization routine; otherwise, it may result in an unpredicted problem.

4 Summary

This application note introduces compensation of the IRTC, and a solution for generating a 1 Hz clock with the same clock width cycle by cycle.

The IRTC can output a clock with high precision for a long period (greater than the compensation period). The FTM is used to ensure the precision cycle by cycle in the compensation period. According to the bench test result, the 1 Hz clock can achieve up to ±2 ppm precision.

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