Freescale Semiconductor
Application Note

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Migration and Device Emulation within the MPC560xB/C/D Family

The 32-bit MPC560xB/C/D automotive microcontrollers are a family of System-on-Chip (SoC) devices designed to be central to the development of the next generation of central vehicle body controller, smart junction box, front module, peripheral body, door control, and seat control applications.

Jointly developed by Freescale Semiconductor and STMicroelectronics™, the MPC560xB/C/D car body family is a series of automotive microcontrollers based on the Power Architecture™ Book E, and are designed specifically for embedded automotive applications.

The MPC560xB/C/D family is a highly scalable and compatible family of devices. However, designing an application that can be easily ported across different members of this family requires knowledge of their specific features and of any significant differences between them.

This document focuses specifically on migrating applications between two sets of products among the family:

Contents

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- MPC5604B: For sales type MPC5604B/C, MPC5603B/C, and MPC5062B/C
- MPC5607B: For sales type MPC5607B, MPC5606B, and MPC5605B

The set namings refer to the most featured sale type in each set.

The following use cases will be addressed:

- Migrating from MPC5604B to MPC5607B
- Migrating from MPC5607B to the MPC5604B

1 MPC5607B and MPC5604B comparison overview

Features of the MPC5604B are, in general, a subset of ones available on the MPC5607B.

However, in some cases additional features have been added or enhancements have been made. Thus when designing an application that may be ported between the MPC5607B and the MPC5604B, it is imperative to understand clearly the differences between them.

The diagrams in Figure 1 highlight at a high level the key differences between these devices.

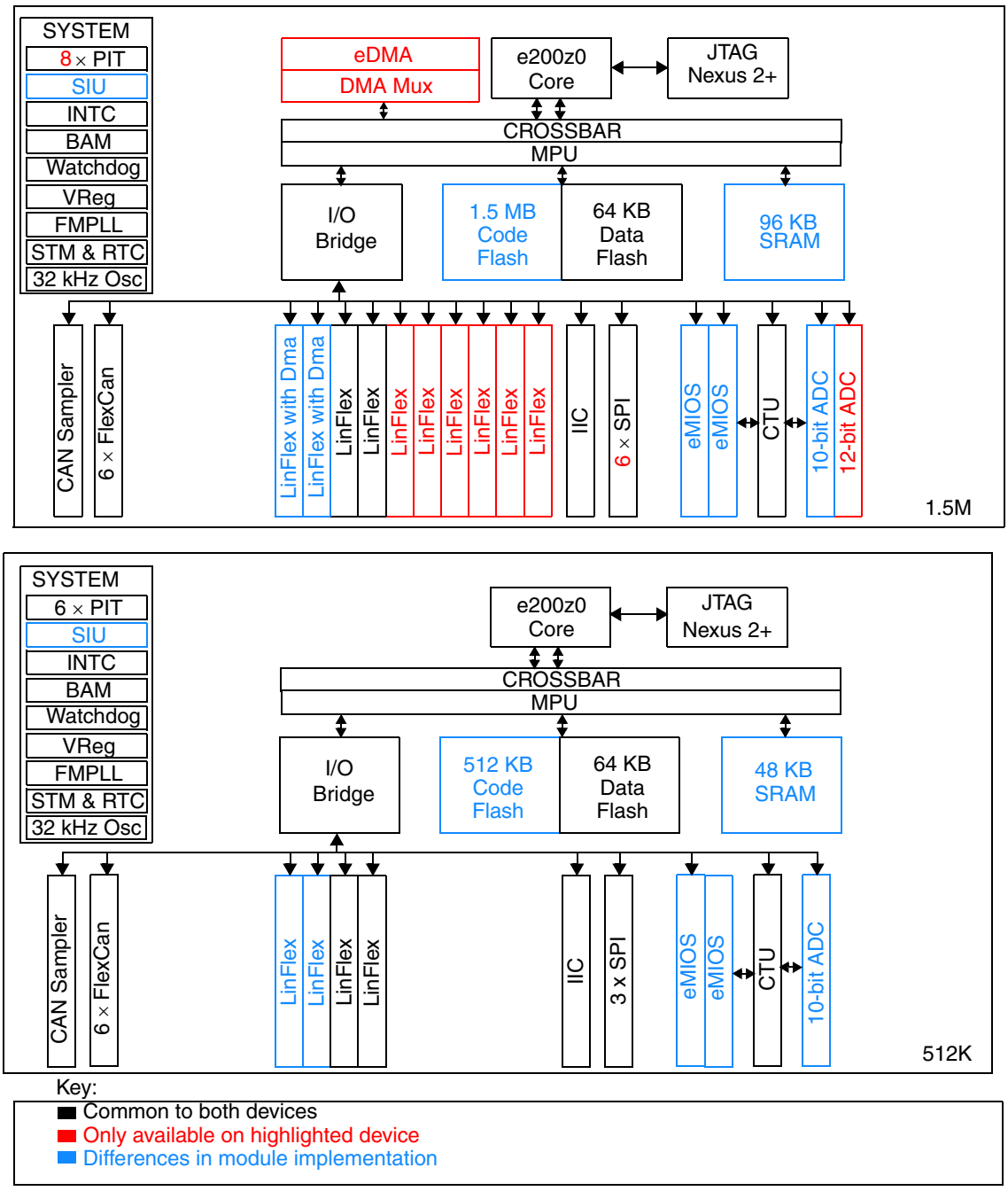

Figure 1. MPC5607B and MPC5604B comparison overview

2 List of differences between MPC5607B and MPC5604B

2.1 Introduction

For an overview of general differences between member of the MPC560xB/C/D Car Body device family, please refer to “MPC560xB/C/D family — Product Differences”.

The sections hereafter describe in more detail the specific differences between MPC5607B and MPC5604B that the user must be aware of when porting applications between these devices.

2.2 ADC

MPC5607B implementation of ADC is the following:

- One 12-bit ADC with:
  - Sixteen high-precision “ADC1_P” channels; pins shared with ADC 10-bit
  - Eight normal “ADC1_S” channels; three pins shared with ADC 10-bit
  - PIT6 injection trigger
  - Three analog thresholds
- One 10-bit ADC with:
  - Sixteen high precision “ADC0_P” channels; pins shared with ADC 12-bit
  - Twenty-eight normal “ADC0_S” channels; three pins shared with ADC 12-bit
  - Four normal “ADC0_X”channels that can be entries for external multiplexing for up to thirty-two external channels
  - PIT2 injection trigger
  - Six analog thresholds

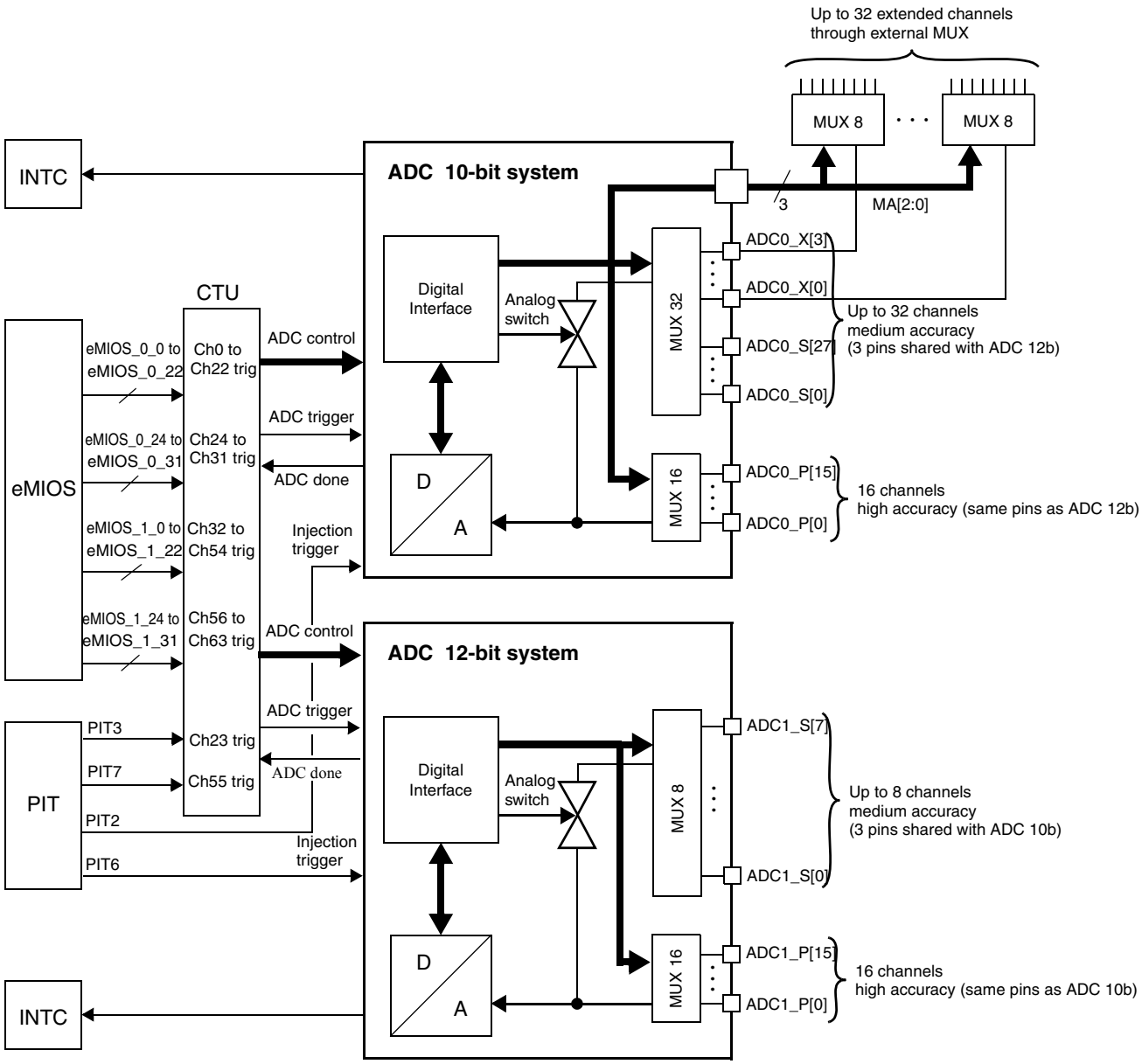

Figure 2. ADC implementation of MPC5607B

MPC5604B implementation of ADC is the following:

- One 10-bit ADC with:
  - — Sixteen high precision “ADC0_P”channels
  - — Sixteen normal “ADC0_S” channels
  - — Four normal “ADC0_X” channels can be entries for external multiplexing for up to thirty-two external channels
  - — PIT2 injection trigger
  - — Four analog thresholds

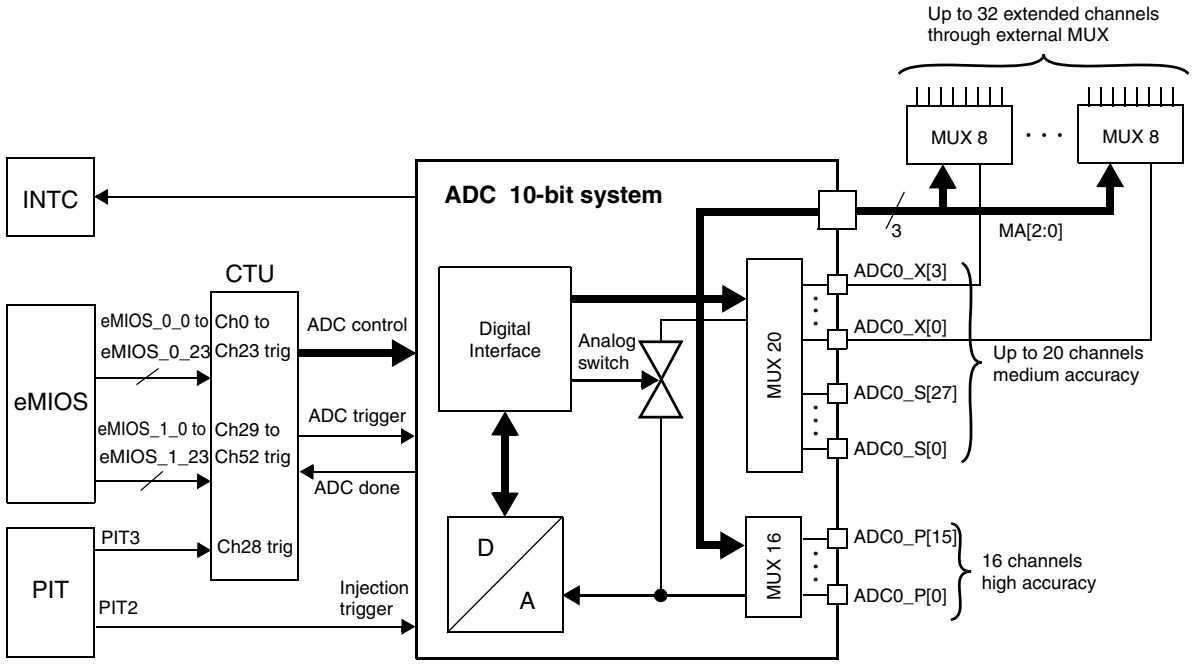

Figure 3. ADC implementation of MPC5604B

The results of a conversion are stored in the appropriate result register. Software should account for the effective 2-bit offset of the MSB of the result between 10-bit ADC results and 12-bit ADC results.

In addition, analog threshold handling is different between MPC5607B and MPC5604B:

- MPC5604B uses four possible analog threshold ranges. Each single range can be allocated to one single channel.
- MPC5607B uses six possible analog threshold ranges (on its 10-bit ADC). A single range can be shared between several ADC channels. The 12-bit ADC follows the same rules with three analog thresholds.

The respective sets of registers to handle analog thresholds are different. This is therefore important from a migration perspective (see later in this document).

2.3 eMIOS

The eMIOS modules can have channel types shown in Table 1.

Table 1. eMIOS channel types

Description	Name	Channel type				
		Type X	Type Y	Type F	Type G	Type H
General purpose input/output	GPIO	x	x	x	x	x
Single action input capture	SAIC	x	x	x	x	x
Single action output compare	SAOC	x	x	x	x	x
Modulus counter	MC	x	—	—	—	—
Modulus counter buffered (up/down)	MCB	x	—	—	x	—
Input pulse width measurement	IPWM	—	—	—	x	x
Input period measurement	IPM	—	—	—	x	x
Double action output compare	DAOC	—	—	—	x	x
Output pulse width and frequency modulation buffered	OPWFMB	x	—	—	x	—
Center-aligned output PWM buffered with dead time	OPWMCB	—	—	—	x	—
Output pulse width modulation buffered	OPWMB	x	x	—	x	x
Output pulse width modulation trigger	OPWMT	x	x	—	x	x

MPC5607B contains two eMIOS modules (eMIOS_0 and eMIOS_1) organized as shown in Figure 4.

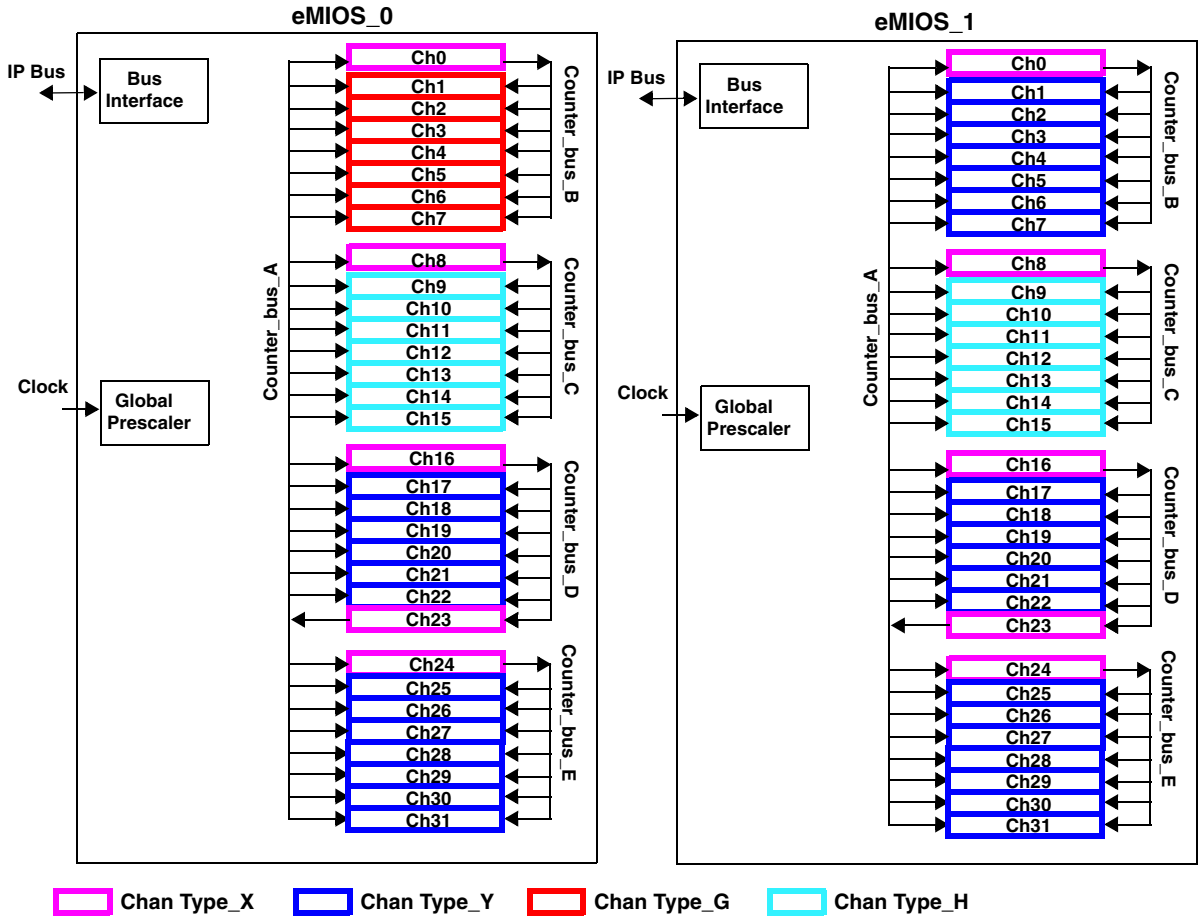

Figure 4. eMIOS Implementation of MPC5607B

MPC5604B contains two eMIOS modules (eMIOS_0 and eMIOS_1) organized as shown in Figure 5.

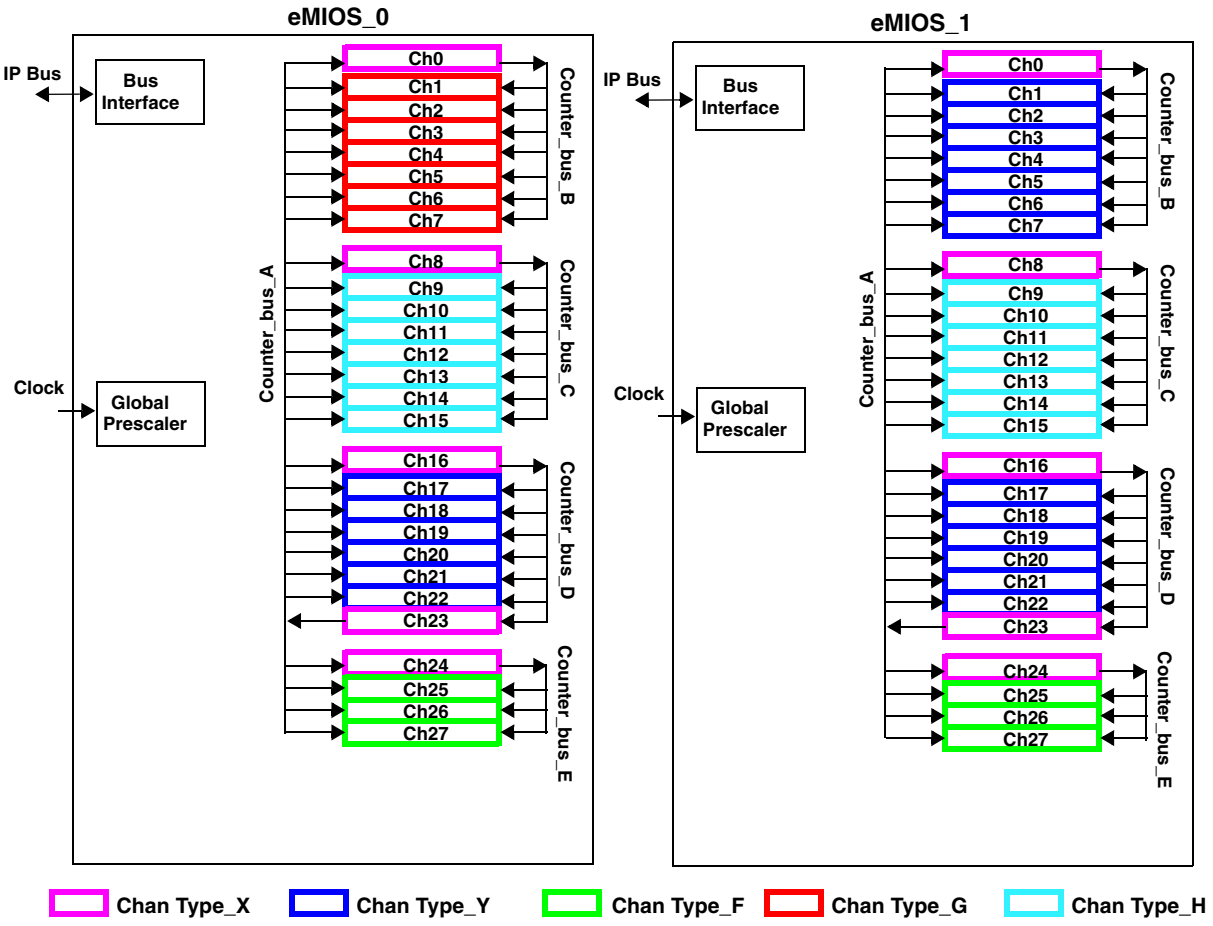

Figure 5. eMIOS implementation of MPC5604B

2.4 LinFlex

MPC5607B contains ten LinFlex modules. Two of them are enabled to issue DMA requests:

- LinFlex 0 and 1 can issue DMA requests
- LinFlex 2 to 9 are not DMA enabled

MPC5604B contains four LinFlex modules. None of them are enabled to issue DMA requests.

3 Packages and pinout

The differences between the analog and digital functionality multiplexed on the pins of the MPC5607B and MPC5604B devices are summarized in the next tables. Only the 100LQFP and 144LQFP packages have been described since these are the only packages common to both of these devices.

Key

Function unique to MPC5604B
Function unique to MPC5607B
Function Common to MPC5604B and MPC5607B

Table 2. 100LQFP MPC5604B to MPC5607B comparison

Pin	Pad	Alternate input functions			Alternate I/O functions			
					ALT0	ALT1	ALT2	ALT3
1	PB[3]	WKPU[11]	LIN0RX		GPIO[19]	E0UC[31]	SCL	
2	PC[9]	WKPU[13]	LIN2RX		GPIO[41]		E0UC[7]	
3	PC[14]	EIRQ[8]			GPIO[46]	E0UC[14]	SCK_2	
4	PC[15]	EIRQ[20]			GPIO[47]	E0UC[15]	CS0_2	
5	PA[2]	WKPU[3]			GPIO[2]	E0UC[2]		MA[2]
6	PE[0]	WKPU[6]	CAN5RX		GPIO[64]	E0UC[16]	CAN_samp1_RX	
7	PA[1]	WKPU[2]			GPIO[1]	E0UC[1]	NMI[0]	
8	PE[1]				GPIO[65]	E0UC[17]	CAN5TX	
9	PE[8]				GPIO[72]	CAN2TX	E0UC[22]	CAN3TX
10	PE[9]	WKPU[7]	CAN2RX	CAN3RX	GPIO[73]	CAN_samp2_RX	E0UC[23]	CAN_samp3_RX
11	PE[10]	EIRQ[10]			GPIO[74]	LIN3TX	CS3_1	E1UC[30]
12	PA[0]	WKPU[19]			GPIO[0]	E0UC[0]	CLKOUT	E0UC[13]
13	PE[11]	WKPU[14]	LIN3RX		GPIO[75]	E0UC[24]	CS4_1	
14	Vpp							
15	VDD_HV							
16	VSS_HV							
17	RESET							
18	VSS_LV							
19	VDD_LV							
20	VDD_BV							
21	PC[11]	WKPU[5]	CAN1RX	CAN4RX	GPIO[43]	CAN_samp1_RX	CAN_samp4_RX	MA[2]
22	PC[10]				GPIO[42]	CAN1TX	CAN4TX	MA[1]
23	PB[0]				GPIO[16]	CAN0TX	E0UC[30]	LIN0TX
24	PB[1]	WKPU[4]	CAN0RX	LIN0RX	GPIO[17]	CAN_samp0_RX	E0UC[31]	
25	PC[6]				GPIO[38]	LIN1TX	E1UC[28]	
26	PC[7]	WKPU[12]	LIN1RX		GPIO[39]		E1UC[29]	

Table 2. 100LQFP MPC5604B to MPC5607B comparison (continued)

Pin	Pad	Alternate input functions			Alternate I/O functions			
					ALT0	ALT1	ALT2	ALT3
27	PA[15]	WKPU[10]			GPIO[15]	CS0_0	SCK_0	E0UC[1]
28	PA[14]	EIRQ[4]			GPIO[14]	SCK_0	CS0_0	E0UC[0]
29	PA[4]	WKPU[9]		LIN5RX	GPIO[4]	E0UC[4]		CS0_1
30	PA[13]				GPIO[13]	SOUT_0	E0UC[29]	
31	PA[12]	EIRQ[17]	SIN_0		GPIO[12]		E0UC[28]	CS3_1
32	VDD_LV							
33	VSS_LV							
34	XTAL							
35	VSS_HV							
36	EXTAL							
37	VDD_HV							
38	PB[9]	WKPU[26]	ADC1_S[5]	ADC0_S[1]	GPIO[25]			
39	PB[8]	WKPU[25]	ADC1_S[4]	ADC0_S[0]	GPIO[24]			
40	PB[10]	WKPU[8]	ADC1_S[6]	ADC0_S[2]	GPIO[26]			
41	PD[0]	WKPU[27]	ADC1_P[4]	ADC0_P[4]	GPIO[48]			
42	PD[1]	WKPU[28]	ADC1_P[5]	ADC0_P[5]	GPIO[49]			
43	PD[2]		ADC1_P[6]	ADC0_P[6]	GPIO[50]			
44	PD[3]		ADC1_P[7]	ADC0_P[7]	GPIO[51]			
45	PD[4]		ADC1_P[8]	ADC0_P[8]	GPIO[52]			
46	PD[5]		ADC1_P[9]	ADC0_P[9]	GPIO[53]			
47	PD[6]		ADC1_P[10]	ADC0_P[10]	GPIO[54]			
48	PD[7]		ADC1_P[11]	ADC0_P[11]	GPIO[55]			
49	PD[8]		ADC1_P[12]	ADC0_P[12]	GPIO[56]			
50	PB[4]		ADC1_P[0]	ADC0_P[0]	GPIO[20]			
51	VSS_HV_ADC0							
52	VDD_HV_ADC0							
53	PB[5]		ADC1_P[1]	ADC0_P[1]	GPIO[21]			
54	PB[6]		ADC1_P[2]	ADC0_P[2]	GPIO[22]			
55	PB[7]		ADC1_P[3]	ADC0_P[3]	GPIO[23]			
56	PD[9]		ADC1_P[13]	ADC0_P[13]	GPIO[57]			
57	PD[10]		ADC1_P[14]	ADC0_P[14]	GPIO[58]			
58	PD[11]		ADC1_P[15]	ADC0_P[15]	GPIO[59]			
*59	PB[11]		Vss_HV_ADC1	ADC0_S[3]	GPIO[27]	E0UC[3]		CS0_0

Table 2. 100LQFP MPC5604B to MPC5607B comparison (continued)

Pin	Pad	Alternate input functions			Alternate I/O functions			
					ALT0	ALT1	ALT2	ALT3
*60	PD[12]		Vdd_HV_ADC1	ADC0_S[4]	GPIO[60]	CS5_0	E0UC[24]	
61	PB[12]			ADC0_X[0]	GPIO[28]	E0UC[4]		CS1_0
62	PD[13]			ADC0_S[5]	GPIO[61]	CS0_1	E0UC[25]	
63	PB[13]			ADC0_X[1]	GPIO[29]	E0UC[5]		CS2_0
64	PD[14]			ADC0_S[6]	GPIO[62]	CS1_1	E0UC[26]	
65	PB[14]			ADC0_X[2]	GPIO[30]	E0UC[6]		CS3_0
66	PD[15]			ADC0_S[7]	GPIO[63]	CS2_1	E0UC[27]	
67	PB[15]			ADC0_X[3]	GPIO[31]	E0UC[7]		CS4_0
68	PA[3]	EIRQ[0]	ADC1_S[0]		GPIO[3]	E0UC[3]	LIN5TX	CS4_1
69	VSS_HV							
70	VDD_HV							
71	PA[7]	EIRQ[2]	ADC1_S[1]		GPIO[7]	E0UC[7]	LIN3TX	
72	PA[8]	EIRQ[3]	ABS[0]	LIN3RX	GPIO[8]	E0UC[8]	E0UC[14]	
73	PA[9]		FAB		GPIO[9]	E0UC[9]		CS2_1
74	PA[10]		ADC1_S[2]		GPIO[10]	E0UC[10]	SDA	LIN2TX
75	PA[11]	EIRQ[16]	ADC1_S[3]	LIN2RX	GPIO[11]	E0UC[11]	SCL	
76	PE[12]	EIRQ[11]	ADC1_S[7]	SIN_2	GPIO[76]		E1UC[19]	
77	PC[3]	EIRQ[6]	CAN4RX	CAN1RX	GPIO[35]	CS0_1	MA[0]	
78	PC[2]	EIRQ[5]			GPIO[34]	SCK_1	CAN4TX	
79	PA[5]				GPIO[5]	E0UC[5]	LIN4TX	
80	PA[6]	EIRQ[1]		LIN4RX	GPIO[6]	E0UC[6]		CS1_1
81	PH[10]				GPIO[122]		TMS	
82	PC[1]				GPIO[33]		TDO	
83	VSS_HV							
84	VDD_HV							
85	VDD_LV							
86	VSS_LV							
87	PC[0]				GPIO[32]		TDI	
88	PH[9]				GPIO[121]		TCK	
89	PE[2]	EIRQ[21]	SIN_1		GPIO[66]	E0UC[18]		
90	PE[3]				GPIO[67]	E0UC[19]	SOUT_1	
91	PC[5]	EIRQ[7]			GPIO[37]	SOUT_1	CAN3TX	
92	PC[4]	EIRQ[18]	SIN_1	CAN3RX	GPIO[36]	E1UC[31]		

Table 2. 100LQFP MPC5604B to MPC5607B comparison (continued)

Pin	Pad	Alternate input functions			Alternate I/O functions			
					ALT0	ALT1	ALT2	ALT3
93	PE[4]	EIRQ[9]			GPIO[68]	E0UC[20]	SCK_1	
94	PE[5]				GPIO[69]	E0UC[21]	CS0_1	MA[2]
95	PE[6]	EIRQ[22]			GPIO[70]	E0UC[22]	CS3_0	MA[1]
96	PE[7]	EIRQ[23]			GPIO[71]	E0UC[23]	CS2_0	MA[0]
97	PC[12]	EIRQ[19]	SIN_2		GPIO[44]	E0UC[12]		
98	PC[13]				GPIO[45]	E0UC[13]	SOUT_2	
99	PC[8]				GPIO[40]	LIN2TX	E0UC[3]	
100	PB[2]				GPIO[18]	LIN0TX	SDA	E0UC[30]

NOTE

Pins 59 and 60 are implemented as ADC_1 power supplies pins VSS and VDD respectively on the MPC5607B in the 100LQFP package. Refer to section 5.1 and 6.1 for further details.

Here is a package-oriented view:

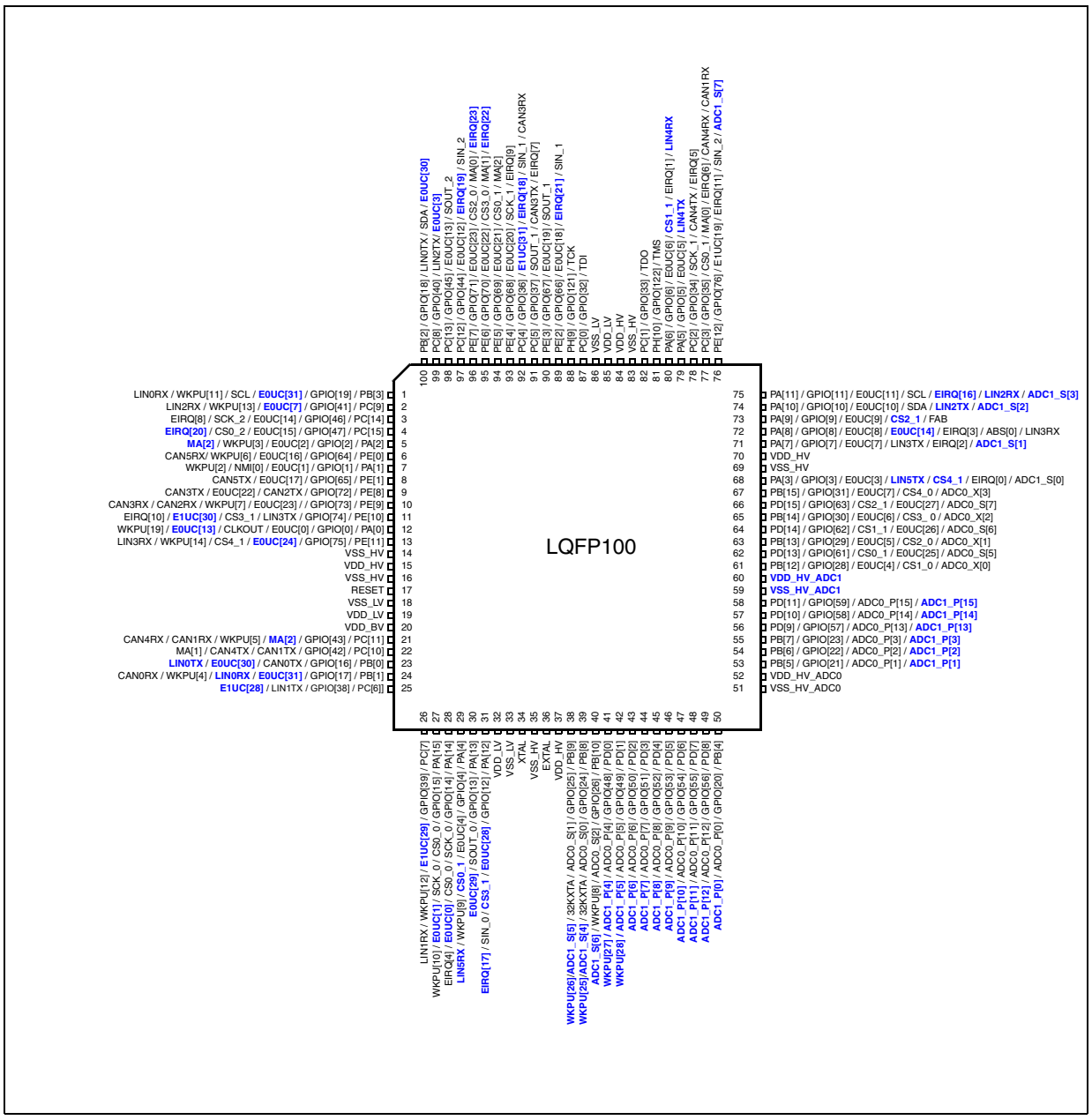

Figure 6. MPC5607B LQFP100 package

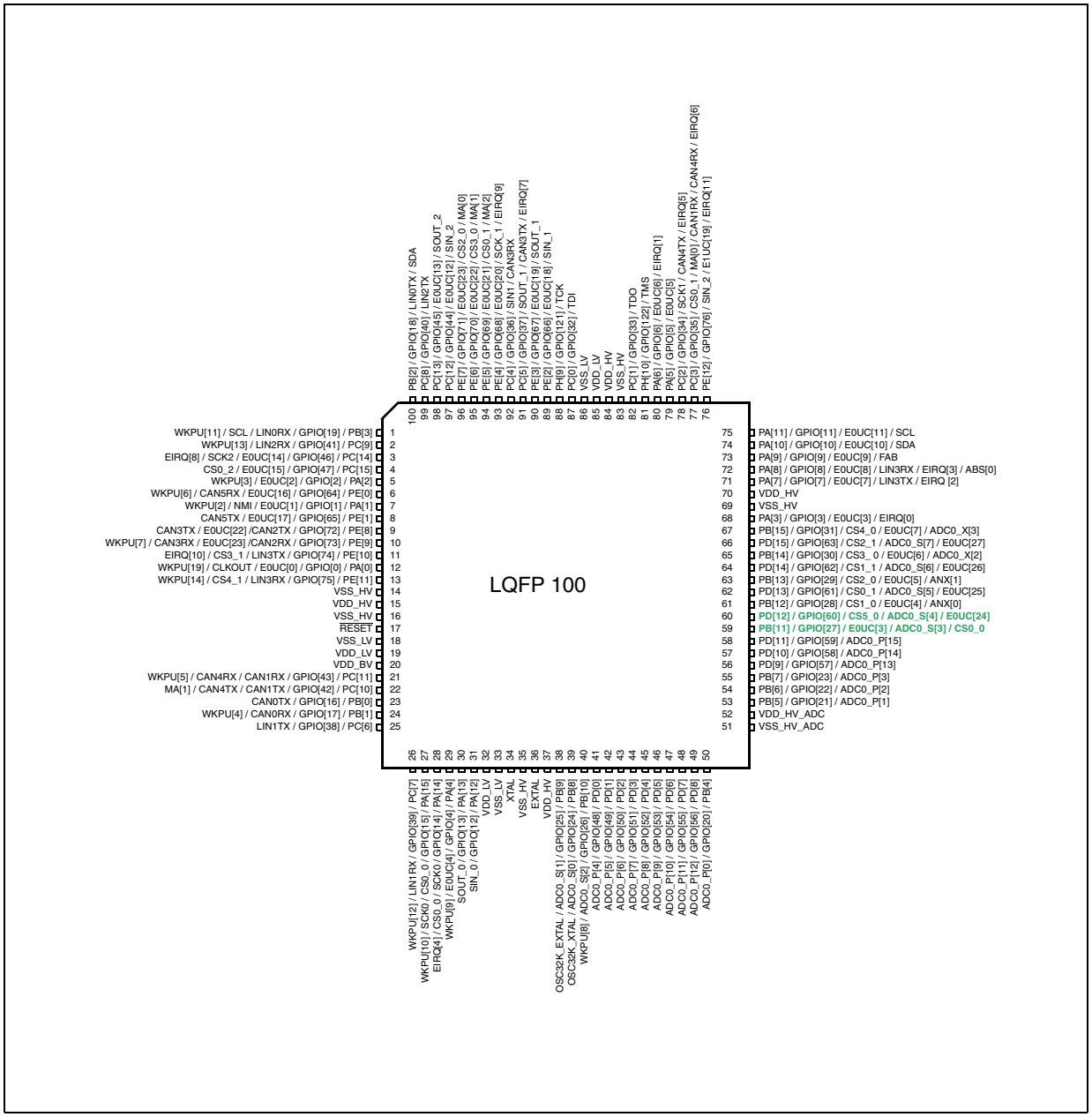

Figure 7. MPC5604B LQFP100 package

This is the description of the LQFP 144 packages:

Table 3. 144 LQFP MPC5604B to MPC5607B comparison

Pin	Pad	Alternate input functions			Alternate I/O functions			
					ALT0	ALT1	ALT2	ALT3
1	PB[3]	WKPU[11]	LIN0RX		GPIO[19]	E0UC[31]	SCL	
2	PC[9]	WKPU[13]	LIN2RX		GPIO[41]		E0UC[7]	
3	PC[14]	EIRQ[8]			GPIO[46]	E0UC[14]	SCK_2	
4	PC[15]	EIRQ[20]			GPIO[47]	E0UC[15]	CS0_2	
5	PG[5]	WKPU[18]	SIN_3		GPIO[101]	E1UC[14]		
6	PG[4]				GPIO[100]	E1UC[13]	SCK_3	
7	PG[3]	WKPU[17]			GPIO[99]	E1UC[12]	CS0_3	
8	PG[2]				GPIO[98]	E1UC[11]	SOUT_3	
9	PA[2]	WKPU[3]			GPIO[2]	E0UC[2]		MA[2]
10	PE[0]	WKPU[6]	CAN5RX		GPIO[64]	E0UC[16]	CAN_samp1_RX	
11	PA[1]	WKPU[2]			GPIO[1]	E0UC[1]	NMI[0]	
12	PE[1]				GPIO[65]	E0UC[17]	CAN5TX	
13	PE[8]				GPIO[72]	CAN2TX	E0UC[22]	CAN3TX
14	PE[9]	WKPU[7]	CAN2RX	CAN3RX	GPIO[73]	CAN_samp2_RX	E0UC[23]	CAN_samp3_RX
15	PE[10]	EIRQ[10]			GPIO[74]	LIN3TX	CS3_1	E1UC[30]
16	PA[0]	WKPU[19]			GPIO[0]	E0UC[0]	CLKOUT	E0UC[13]
17	PE[11]	WKPU[14]	LIN3RX		GPIO[75]	E0UC[24]	CS4_1	
18	Vpp							
19	VDD_HV							
20	VSS_HV							
21	RESET							
22	VSS_LV							
23	VDD_LV							
24	VDD_BV							
25	PG[9]	EIRQ[21]	LIN7RX		GPIO[105]	E1UC[18]		SCK_2
26	PG[8]	EIRQ[15]			GPIO[104]	E1UC[17]	LIN7TX	CS0_2
27	PC[11]	WKPU[5]	CAN1RX	CAN4RX	GPIO[43]	CAN_samp1_RX	CAN_samp4_RX	MA[2]
28	PC[10]				GPIO[42]	CAN1TX	CAN4TX	MA[1]
29	PG[7]	WKPU[20]	LIN6RX		GPIO[103]	E1UC[16]	E1UC[30]	
30	PG[6]				GPIO[102]	E1UC[15]	LIN6TX	

Table 3. 144 LQFP MPC5604B to MPC5607B comparison (continued)

Pin	Pad	Alternate input functions			Alternate I/O functions			
					ALT0	ALT1	ALT2	ALT3
31	PB[0]				GPIO[16]	CAN0TX	E0UC[30]	LIN0TX
32	PB[1]	WKPU[4]	CAN0RX	LIN0RX	GPIO[17]	CAN_samp0_RX	E0UC[31]	
33	PF[9]	WKPU[22]	CAN2RX	CAN3RX	GPIO[89]	E1UC[1]	CS5_0	
34	PF[8]				GPIO[88]	CAN3TX	CS4_0	CAN2TX
35	PF[12]				GPIO[92]	E1UC[25]	LIN5TX	
36	PC[6]				GPIO[38]	LIN1TX	E1UC[28]	
37	PC[7]	WKPU[12]	LIN1RX		GPIO[39]		E1UC[29]	
38	PF[10]				GPIO[90]	CS1_0	LIN4TX	E1UC[2]
39	PF[11]	WKPU[15]	LIN4RX		GPIO[91]	CS2_0	E1UC[3]	
40	PA[15]	WKPU[10]			GPIO[15]	CS0_0	SCK_0	E0UC[1]
41	PF[13]	WKPU[16]	LIN5RX		GPIO[93]	E1UC[26]		
42	PA[14]	EIRQ[4]			GPIO[14]	SCK_0	CS0_0	E0UC[0]
43	PA[4]	WKPU[9]		LIN5RX	GPIO[4]	E0UC[4]		CS0_1
44	PA[13]				GPIO[13]	SOUT_0	E0UC[29]	
45	PA[12]	EIRQ[17]	SIN_0		GPIO[12]		E0UC[28]	CS3_1
46	VDD_LV							
47	VSS_LV							
48	XTAL							
49	VSS_HV							
50	EXTAL							
51	VDD_HV							
52	PB[9]	WKPU[26]	ADC1_S[5]	ADC0_S[1]	GPIO[25]			
53	PB[8]	WKPU[25]	ADC1_S[4]	ADC0_S[0]	GPIO[24]			
54	PB[10]	WKPU[8]	ADC1_S[6]	ADC0_S[2]	GPIO[26]			
55	PF[0]			ADC0_S[8]	GPIO[80]	E0UC[10]	CS3_1	
56	PF[1]			ADC0_S[9]	GPIO[81]	E0UC[11]	CS4_1	
57	PF[2]			ADC0_S[10]	GPIO[82]	E0UC[12]	CS0_2	
58	PF[3]			ADC0_S[11]	GPIO[83]	E0UC[13]	CS1_2	
59	PF[4]			ADC0_S[12]	GPIO[84]	E0UC[14]	CS2_2	
60	PF[5]			ADC0_S[13]	GPIO[85]	E0UC[22]	CS3_2	
61	PF[6]			ADC0_S[14]	GPIO[86]	E0UC[23]	CS1_1	
62	PF[7]			ADC0_S[15]	GPIO[87]		CS2_1	
63	PD[0]	WKPU[27]	ADC1_P[4]	ADC0_P[4]	GPIO[48]			

Table 3. 144 LQFP MPC5604B to MPC5607B comparison (continued)

Pin	Pad	Alternate input functions			Alternate I/O functions			
					ALT0	ALT1	ALT2	ALT3
64	PD[1]	WKPU[28]	ADC1_P[5]	ADC0_P[5]	GPIO[49]			
65	PD[2]		ADC1_P[6]	ADC0_P[6]	GPIO[50]			
66	PD[3]		ADC1_P[7]	ADC0_P[7]	GPIO[51]			
67	PD[4]		ADC1_P[8]	ADC0_P[8]	GPIO[52]			
68	PD[5]		ADC1_P[9]	ADC0_P[9]	GPIO[53]			
69	PD[6]		ADC1_P[10]	ADC0_P[10]	GPIO[54]			
70	PD[7]		ADC1_P[11]	ADC0_P[11]	GPIO[55]			
71	PD[8]		ADC1_P[12]	ADC0_P[12]	GPIO[56]			
72	PB[4]		ADC1_P[0]	ADC0_P[0]	GPIO[20]			
73	VSS_HV_ADC0							
74	VDD_HV_ADC0							
75	PB[5]		ADC1_P[1]	ADC0_P[1]	GPIO[21]			
76	PB[6]		ADC1_P[2]	ADC0_P[2]	GPIO[22]			
77	PB[7]		ADC1_P[3]	ADC0_P[3]	GPIO[23]			
78	PD[9]		ADC1_P[13]	ADC0_P[13]	GPIO[57]			
79	PD[10]		ADC1_P[14]	ADC0_P[14]	GPIO[58]			
80	PD[11]		ADC1_P[15]	ADC0_P[15]	GPIO[59]			
81	PB[11]		Vss_HV_ADC1	ADC0_S[3]	GPIO[27]	E0UC[3]		CS0_0
82	PD[12]		Vdd_HV_ADC1	ADC0_S[4]	GPIO[60]	CS5_0	E0UC[24]	
83	PB[12]			ADC0_X[0]	GPIO[28]	E0UC[4]		CS1_0
84	PD[13]			ADC0_S[5]	GPIO[61]	CS0_1	E0UC[25]	
85	PB[13]			ADC0_X[1]	GPIO[29]	E0UC[5]		CS2_0
86	PD[14]			ADC0_S[6]	GPIO[62]	CS1_1	E0UC[26]	
87	PB[14]			ADC0_X[2]	GPIO[30]	E0UC[6]		CS3_0
88	PD[15]			ADC0_S[7]	GPIO[63]	CS2_1	E0UC[27]	
89	PB[15]			ADC0_X[3]	GPIO[31]	E0UC[7]		CS4_0
90	PA[3]	EIRQ[0]	ADC1_S[0]		GPIO[3]	E0UC[3]	LIN5TX	CS4_1
91	PG[13]				GPIO[109]	E0UC[27]	SCK_4	
92	PG[12]				GPIO[108]	E0UC[26]	SOUT_4	
93	PH[0]		SIN_1		GPIO[112]	E1UC[2]		
94	PH[1]				GPIO[113]	E1UC[3]	SOUT_1	
95	PH[2]				GPIO[114]	E1UC[4]	SCK_1	
96	PH[3]				GPIO[115]	E1UC[5]	CS0_1	

Table 3. 144 LQFP MPC5604B to MPC5607B comparison (continued)

Pin	Pad	Alternate input functions			Alternate I/O functions			
					ALT0	ALT1	ALT2	ALT3
97	PG[1]	EIRQ[14]	CAN5RX		GPIO[97]		E1UC[24]	
98	PG[0]				GPIO[96]	CAN5TX	E1UC[23]	
99	VSS_HV							
100	VDD_HV							
101	PF[15]	EIRQ[13]	CAN1RX	CAN4RX	GPIO[95]	E1UC[4]		
102	PF[14]				GPIO[94]	CAN4TX	E1UC[27]	CAN1TX
103	PE[13]				GPIO[77]	SOUT_2	E1UC[20]	
104	PA[7]	EIRQ[2]	ADC1_S[1]		GPIO[7]	E0UC[7]	LIN3TX	
105	PA[8]	EIRQ[3]	ABS[0]	LIN3RX	GPIO[8]	E0UC[8]	E0UC[14]	
106	PA[9]		FAB		GPIO[9]	E0UC[9]		CS2_1
107	PA[10]		ADC1_S[2]		GPIO[10]	E0UC[10]	SDA	LIN2TX
108	PA[11]	EIRQ[16]	ADC1_S[3]	LIN2RX	GPIO[11]	E0UC[11]	SCL	
109	PE[12]	EIRQ[11]	ADC1_S[7]	SIN_2	GPIO[76]		E1UC[19]	
110	PG[14]				GPIO[110]	E1UC[0]	LIN8TX	
111	PG[15]		LIN8RX		GPIO[111]	E1UC[1]		
112	PE[14]	EIRQ[12]			GPIO[78]	SCK_2	E1UC[21]	
113	PE[15]				GPIO[79]	CS0_2	E1UC[22]	
114	PG[10]		SIN_4		GPIO[106]	E0UC[24]	E1UC[31]	
115	PG[11]				GPIO[107]	E0UC[25]	CS0_4	
116	PC[3]	EIRQ[6]	CAN4RX	CAN1RX	GPIO[35]	CS0_1	MA[0]	
117	PC[2]	EIRQ[5]			GPIO[34]	SCK_1	CAN4TX	
118	PA[5]				GPIO[5]	E0UC[5]	LIN4TX	
119	PA[6]	EIRQ[1]		LIN4RX	GPIO[6]	E0UC[6]		CS1_1
120	PH[10]				GPIO[122]		TMS	
121	PC[1]				GPIO[33]		TDO	
122	VSS_HV							
123	VDD_HV							
124	VDD_LV							
125	VSS_LV							
126	PC[0]				GPIO[32]		TDI	
127	PH[9]				GPIO[121]		TCK	
128	PE[2]	EIRQ[21]	SIN_1		GPIO[66]	E0UC[18]		
129	PE[3]				GPIO[67]	E0UC[19]	SOUT_1	

Table 3. 144 LQFP MPC5604B to MPC5607B comparison (continued)

Pin	Pad	Alternate input functions			Alternate I/O functions			
					ALT0	ALT1	ALT2	ALT3
130	PC[5]	EIRQ[7]			GPIO[37]	SOUT_1	CAN3TX	
131	PC[4]	EIRQ[18]	SIN_1	CAN3RX	GPIO[36]	E1UC[31]		
132	PE[4]	EIRQ[9]			GPIO[68]	E0UC[20]	SCK_1	
133	PE[5]				GPIO[69]	E0UC[21]	CS0_1	MA[2]
134	PH[4]				GPIO[116]	E1UC[6]		
135	PH[5]				GPIO[117]	E1UC[7]		
136	PH[6]				GPIO[118]	E1UC[8]		MA[2]
137	PH[7]				GPIO[119]	E1UC[9]	CS3_2	MA[1]
138	PH[8]				GPIO[120]	E1UC[10]	CS2_2	MA[0]
139	PE[6]	EIRQ[22]			GPIO[70]	E0UC[22]	CS3_0	MA[1]
140	PE[7]	EIRQ[23]			GPIO[71]	E0UC[23]	CS2_0	MA[0]
141	PC[12]	EIRQ[19]	SIN_2		GPIO[44]	E0UC[12]		
142	PC[13]				GPIO[45]	E0UC[13]	SOUT_2	
143	PC[8]				GPIO[40]	LIN2TX	E0UC[3]	
144	PB[2]				GPIO[18]	LIN0TX	SDA	E0UC[30]

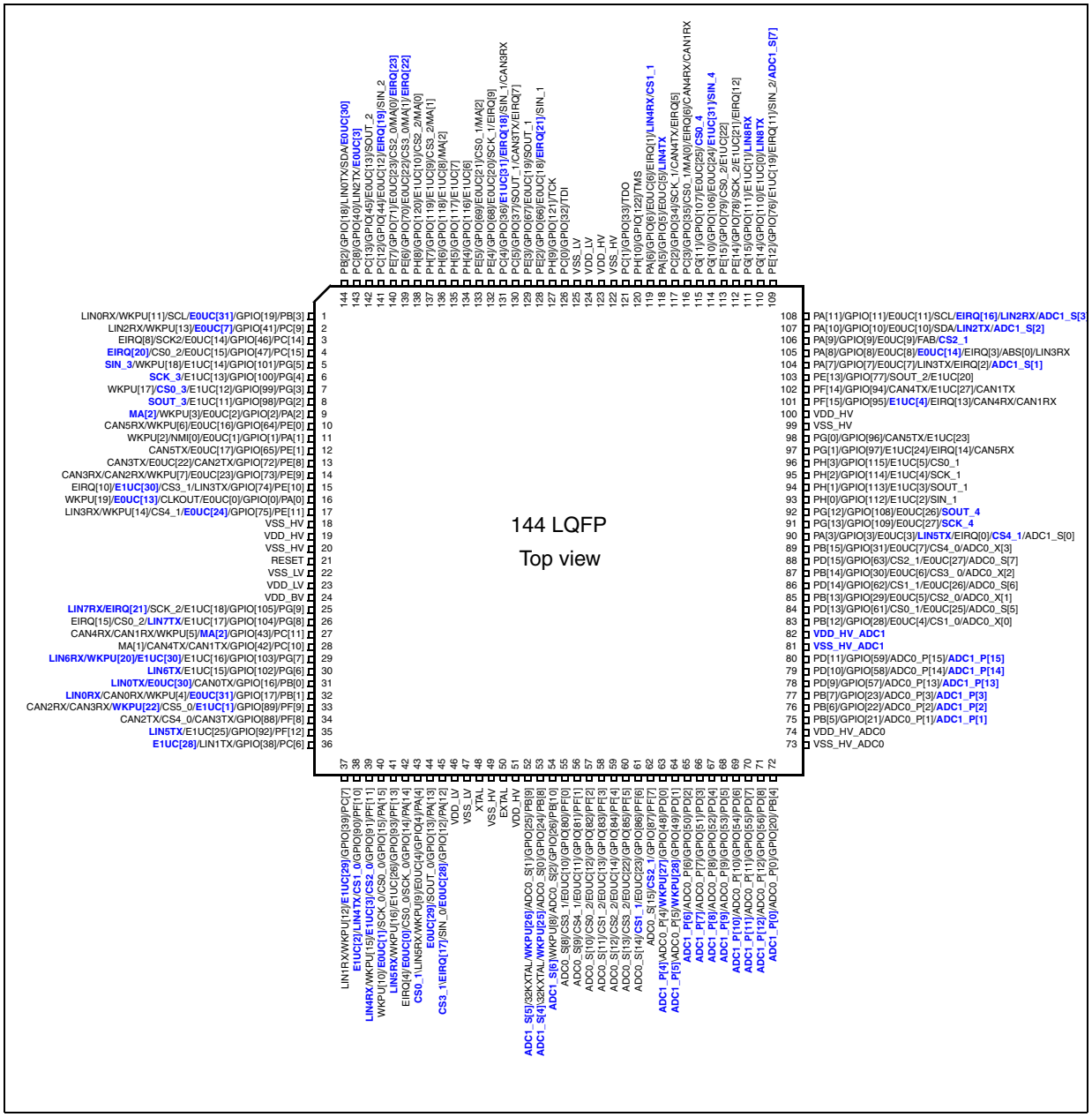

Figure 8. MPC5607B LQFP144 package

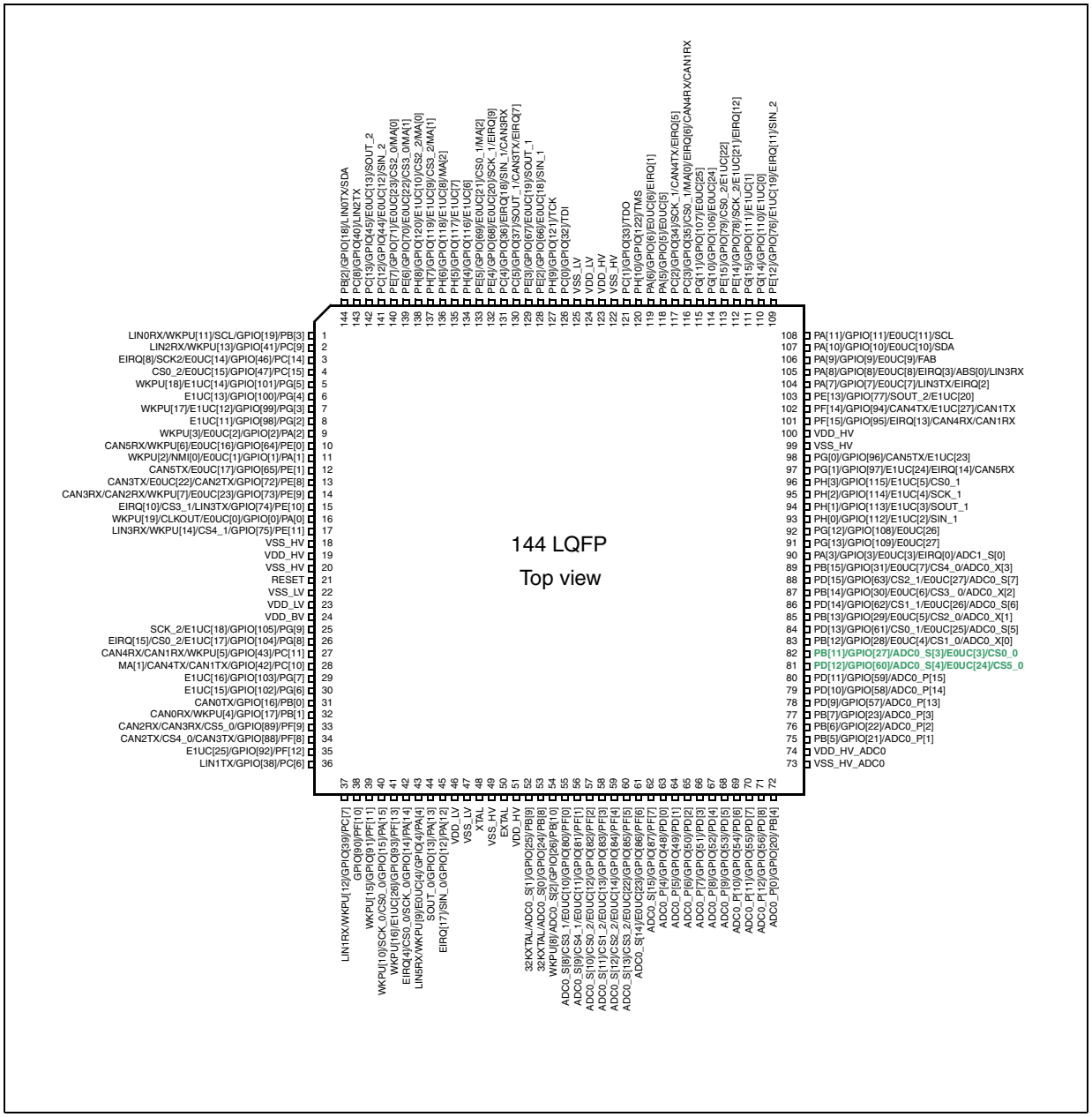

Figure 9. MPC5604B LQFP144 package

4 Device ID

The MCU ID registers MIDR1 and MIDR2 contain information pertaining to the device including part number, package type, mask set information, and parametric data such as flash size and inclusion of data flash.

The device identification register within the JTAG controller is read by debuggers to identify the device under test.

Table 4 details the register contents for each device and package option. Software that depends on the contents of this register should be modified. Refer to the respective device reference manuals for full bit level descriptions of these registers.

Table 4. Device ID Registers (table to be updated)

Device	Package	Flash size	MIDR1	MIDR2	JTAGC ID
MPC5604C	100LQFP	512 KB	0x5604_34XX	0x2800_4310	TBD
MPC5604B	144LQPF	512 KB	0x5604_34XX	0x2800_4210	TBD
MPC5604B	100LQFP	512 KB	0x5604_24XX	0x2800_4210	TBD
MPC5603C	100LQPF	384 KB	0x5603_24XX	0x2200_4310	TBD
MPC5603B	144LQPF	384 KB	0x5603_34XX	0x2200_4210	TBD
MPC5603B	100LQPF	384 KB	0x5603_24XX	0x2200_4210	TBD
MPC5602C	100LQPF	256 KB	0x5602_24XX	0x2000_4310	TBD
MPC5602B	144LQPF	256 KB	0x5602_34XX	0x2000_4210	TBD
MPC5602B	100LQPF	256 KB	0x5602_24XX	0x2000_4210	TBD
MPC5601D	100LQPF	128 KB	0x5601_24XX	0x1800_4410	0x0AE4401D
MPC5601D	64LQPF	128 KB	0x5601_04XX	0x1800_4410	0x0AE4401D
MPC5602D	100LQPF	256 KB	0x5602_24XX	0x2000_4410	0x0AE4401D
MPC5602D	64LQPF	256 KB	0x5602_04XX	0x2000_4410	0x0AE4401D

NOTE

0xXX denote mask set and revision number.

5 Migrating from MPC5604B to MPC5607B

While migrating an application from MPC5604B to MPC5607B, the user should pay attention to:

- Pins
- ADC
- LinFlex
- eMIOS

5.1 Pins

PB11 and PD12 are available on MPC5604B on all packages. PB11 and PD12 are not available on MPC5607B on the LQFP100 and LQFP144 packages. If an application on the MPC5604B uses these pins then a modification will be mandatory to route these features to other IOs.

5.2 ADC

MPC5607B and MPC5604B have the same number of ADC0 10-bit channels (sixteen precise, twenty-eight standard, and four extended). However, threshold implementation is different. An application using them on MPC5604B should be modified as follows to migrate to MPC5607B:

- Do not use Threshold Control Registers (TRC[0..3]) since they are unavailable on MPC5607B.
  - Instead use Channel Watchdog Enable Register (CWEN0), with Channel Watchdog Selection Registers (CWSEL[0..1]).
- Rewrite usage of Watchdog Threshold Interrupt Mask Register (WTIMR) and Watchdog Threshold Interrupt Status Register (WTISR).
  - MPC5604B low and high threshold bits are grouped in the registers.
  - MPC5607B low and high threshold bits are grouped two by two. Therefore usage of these registers must be rewritten.
  - In addition, MPC5607B Analog Watchdog Out of Range Register (AWORR0) gives information about channel numbers that were out of analog range.

5.3 LinFlex

The two first LinFlex modules of the MPC5607B are actually LinFlexD modules, which can handle DMA requests and FIFO for UART mode. Since this module is a superset of the standard LinFlex module present on MPC5604B, there will be no issue in migration, due to this upward compatibility.

5.4 eMIOS

Implementation of MPC5607B is a superset of the one present on MPC5604B. Therefore, there will be no issue in migration, due to this upward compatibility.

6 Migrating from MPC5607B to MPC5604B

While migrating an application from MPC5607B to MPC5604B, the user should pay attention to:

- Pins
- Regulator
- Clocks
- RAM
- Flash
- DMA
- PIT
- eMIOS
- ADC
- CTU
- LINFlex

- DSPI

6.1 Pins

On their common set of features, there will be no issue on pin mapping while migrating. Refer to the pin mapping differences for further details.

6.2 Regulator

MPC5607B ballast feature is not available on MPC5604B.

6.3 Clocks

MPC5607B ability to have system or RTC clock on the CLKOUT is not available with MPC5604B. Any application relying on this feature will not work.

6.4 RAM

MPC5604B has less available RAM in Power Domain 2 than MPC5607B. An application will have to be recoded to fit the smaller RAM size.

6.5 Flash

MPC5604B has less available code flash than MPC5607B. An application will have to be recoded to fit the smaller code flash size.

Data flash is the same in both cases.

6.6 DMA

MPC5607B has a DMA with DMAMUX — MPC5604B does not. Therefore, any code or usage of registers or interrupts related to DMA will not work. An application will need to be recoded without DMA usage.

6.7 PIT

MPC5607B has eight PITs. MPC5604B has six. Table 5 and Table 6 show respective implementation details regarding internal connections.

Table 5. MPC5607B PIT details

PIT	Interrupt	Peripheral trigger	DMA trigger
0	YES	NO	YES
1	YES	NO	YES
2	YES	10-bit ADC	NO
3	YES	CTU ch28	NO

Table 5. MPC5607B PIT details (continued)

PIT	Interrupt	Peripheral trigger	DMA trigger
4	YES	NO	YES
5	YES	NO	YES
6	YES	12-bit ADC	NO
7	YES	CTU ch51	NO

Table 6. MPC5604B PIT details

PIT	Interrupt	Peripheral trigger	DMA trigger
0	YES	NO	Not applicable
1	YES	NO	Not applicable
2	YES	10-bit ADC	Not applicable
3	YES	CTU ch28	Not applicable
4	YES	NO	Not applicable
5	YES	NO	Not applicable

Therefore, an application using PIT6 and PIT7 will not work with MPC5604B and must be reworked.

6.8 eMIOS

MPC5604B has fewer channels on each eMIOS, and its channels have a different feature set than MPC5607B. Refer to eMIOS comparison to see how to adapt an application for migration.

6.9 ADC

MPC5607B has two ADCs, one with 10-bit resolution (ADC0 10-bit) and one with 12-bit resolution (ADC1 12-bit). MPC5604B has only one ADC 10 bit. Any application using ADC1 on MPC5607B will have to be modified to use the ADC0 of MPC5604B.

In addition, an application that uses the analog threshold feature will have to be recoded with scheme and quantities of thresholds available on MPC5604B.

6.10 CTU

All CTU channels above 31 in MPC5607B do not exist on MPC5604B.

6.11 LINFlex

MPC5607B LinFlex 4 to 9 can’t be used on MPC5604B. In addition, LinFlex 0 and 1 lose their DMA ability, FIFO on UART mode, and byte length in UART mode, on MPC5604B.

6.12 DSPI

MPC5607B DSPI 3 to 5 cannot be used on MPC5604B.

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