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Application Note

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Recovering MC56F8300 Family Devices from Extreme RFI

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Contents

1 Introduction

Some DSC's are subjected to extreme Radio Frequency Interference (RFI) during end customer product testing. During this extreme RFI, it is expected that the product will stop functioning. In some very extreme cases the RFI induces a state in the DSC that will not clear itself when the RFI is removed. In this case, the DSC reset pin may be used to restore DSC operation. For the extremely rare case where the reset pin does not clear the condition, the device is cleared with a power cycle. For those customers who do not wish to use a power cycle to restore operation under these extreme conditions, two alternatives to a power cycle are discussed in this application note. Sufficient detail is provided to implement one or the other solution, if needed.

This application note details two alternative methods for reseting a Freescale MC56F8300 family device besides the nominal reset pin function, the nominal JTAG sequences, and the nomincal power on reset. The nominal methods are not treated in this document. Information about them is available in:

- Reference manual titled *DSP56800E and DSP56800EX* revision 3, (document number DSP56800ERM)
- The data sheet for your particular device
- User manual titled *56F800 Peripheral User Manual Also Supports 56F8100 Device Family*, revision 10 (document number MC56F8300UM)

Two special methods covered in this application note are:

- Use of a special JTAG sequence to force a power on reset rather than a pin reset — This approach works on all 56F8300 devices, in all configurations as long as there is access to the JTAG pins and they are configured for use as JTAG pins at the time of the extreme RFI event.
- Use of the OCR_DIS pin in a special manner contraindicated by the data sheet— if available in the package and the design— to force the core voltage level below the reset threshold thereby effecting a true power on reset. This approach works as long as the voltage regulators are used to build up the 2.5 volts needed by the core on the VCAP pins. This is normally the case if capacitors are installed on the VCAP pins rather than a 2.5 volt power source.

2 Special JTAG sequence to force a logical power on reset

It is beyond the scope of this application note to cover all the topics required to use JTAG. However, further information on JTAG and the TAP is available in the documents cited above, as well as the industry standard IEEE1149. This section focuses on the actual JTAG command sequence developed using HBUG, a software tool available from Freescale under NDA. The data on the JTAG interface was captured and recorded using a logic analyzer attached to an MC56F8355 device controlled by HBUG.

The details of the TAP command are proprietary to Freescale, but many of them are documented in the HBUG Perl program and its associated documentation. There is no charge for HBUG, but the execution of an NDA is mandatory to obtain HBUG. HBUG comes with training and documentation materials, but is not supported by Freescale after its delivery.

NOTE

To request HBUG under NDA, please contact your Freescale sales representative or your distributor.

Some Perl scripts for HBUG offer an explanation as a starting point to understand the actual JTAG sequence HBUG produced to effect the power on reset of the 8300 family devices. Then, the actual data capture from the resulting JTAG sequence is shown. Both the rising and falling edges of TCK is used to trigger the state style logic analyzer data capture of the JTAG interface.

2.1 HBUG script used to generate the JTAG signal traffic

The RFI results in a condition where the device does not respond to the reset pin. However, the JTAG tap is working normally. This makes it possible to command the device to effect a power on reset.

The HBUG session log used to generate the power on reset is shown below. The lines that begin with ‘#’ indicate a response from the HBUG program. Lines ending in ‘;’ are a command to HBUG from the HBUG console. HBUG was connected from the PC via the parallel port through a parallel port to the JTAG converter to the JTAG port of the device that was not responding to the reset pin.

The following HBUG commands restore the device to running condition:

```
reset_to_rti();
# Negative transition on RESETB
# Negative transition on TRSTB
# Positive transition on TRSTB
# => 1
check_chip_id(1);
# Found DSP56F8345 (Monza C) chip TAP IDCODE = 11F4401D.
# => 0
shift_instruction(CHIP_LOCKOUT_RECOVERY, X);
# => 01
shift_data("8000",X);
# => 0000
shift_instruction(CHIP_KTR_EN,X);
# => 01
shift_data("0420",X);
# => 0000
```

```
# Negative transition on TRSTB
# Positive transition on TRSTB
# Found DSP56F8345 (Monza C) chip TAP IDCODE = 11F4401D.
# Switching to Hawk V2 TAP controller...
# Found expected Hawk V2 TAP IDCODE value = 02211004.
# Postive transition on RESETB
# D=>Debug: DSP core halted and in Debug Mode
# Negative transition on RESETB
# Negative transition on TRSTB
# Postive transition on RESETB
# Positive transition on TRSTB
```

Subsequent to this, the device operates normally. The JTAG signals were recorded and are included in section 2.2

The key to this script working is the setting of bit 10 of the KTR (kernel test register). This is done with the shift_data HBUG command, shift_data(“0420”,X).

2.2 Data capture from logic analyzer

The data captured from the logic analyzer is recorded in the table below. The data is available in simple text format as captured on the logic analyzer from Freescale with this application note.

State Counts	TRST_B	RESET_B	TDI	TDO	TMS	TCK
0	0	0	0	0	0	1
1	0	0	0	0	1	0
2	0	0	0	0	1	1
3	0	0	0	0	1	0
4	0	0	0	0	1	1
5	0	0	0	0	1	0
6	0	0	0	0	1	1
7	0	0	0	0	1	0
8	0	0	0	0	1	1
9	0	0	0	0	1	0
10	0	0	0	0	1	1
11	0	0	0	0	1	0
12	1	0	0	0	0	1
13	1	0	0	0	0	0
14	1	0	0	0	0	1
15	1	0	0	0	0	0
16	1	0	0	0	0	1
17	1	0	0	0	0	0
18	1	0	0	0	1	1
19	0	0	0	0	1	0
20	1	0	0	0	1	1
21	1	0	0	0	1	0

Table continues on the next page...

Special JTAG sequence to force a logical power on reset

State Counts	TRST_B	RESET_B	TDI	TDO	TMS	TCK
22	1	0	0	0	0	1
23	1	0	0	0	0	0
24	1	0	0	0	0	1
25	1	0	0	0	0	0
26	1	0	0	0	0	1
27	1	0	0	1	0	0
28	1	0	1	1	0	1
29	1	0	1	0	0	0
30	1	0	0	0	0	1
31	1	0	0	0	0	0
32	1	0	0	0	0	1
33	1	0	0	0	0	0
34	1	0	0	0	0	1
35	1	0	0	0	0	0
36	1	0	0	0	0	1
37	1	0	0	0	0	0
38	1	0	0	0	0	1
39	1	0	0	0	0	0
40	1	0	0	0	1	1
41	1	0	0	0	1	0
42	1	0	0	0	1	1
43	1	0	0	0	1	0
44	1	0	0	0	0	1
45	1	0	0	0	0	0
46	1	0	0	0	1	1
47	1	0	0	0	1	0
48	1	0	0	0	0	1
49	1	0	0	0	0	0
50	1	0	0	0	0	1
51	1	0	0	0	0	0
52	1	0	0	0	0	1
53	1	0	0	1	0	0
54	1	0	0	1	0	1
55	1	0	0	0	0	0
56	1	0	0	0	0	1
57	1	0	0	1	0	0

Table continues on the next page...

State Counts	TRST_B	RESET_B	TDI	TDO	TMS	TCK
58	1	0	0	1	0	1
59	1	0	0	1	0	0
60	1	0	0	1	0	1
61	1	0	0	1	0	0
62	1	0	0	1	0	1
63	1	0	0	0	0	0
64	1	0	0	0	0	1
65	1	0	0	0	0	0
66	1	0	0	0	0	1
67	1	0	0	0	0	0
68	1	0	0	0	0	1
69	1	0	0	0	0	0
70	1	0	0	0	0	1
71	1	0	0	0	0	0
72		0	0	0	0	1
73	1	0	0	0	0	0
74	1	0	0	0	0	1
75	1	0	0	0	0	0
76	1	0	0	0	0	1
77	1	0	0	0	0	0
78	1	0	0	0	0	1
79	1	0	0	0	0	0
80	1	0	0	0	0	1
81	1	0	0	1	0	0
82	1	0	0	1	0	1
83	1	0	0	0	0	0
84	1	0	0	0	0	1
85	1	0	0	0	0	0
86	1	0	0	0	0	1
87	1	0	0	0	0	0
88	1	0	0	0	0	1
89	1	0	0	1	0	0
90	1	0	0	1	0	1
91	1	0	0	0	0	0
92	1	0	0	0	0	1
93	1	0	0	1	0	0

Table continues on the next page...

Special JTAG sequence to force a logical power on reset

State Counts	TRST_B	RESET_B	TDI	TDO	TMS	TCK
94	1	0	0	1	0	1
95	1	0	0	1	0	0
96	1	0	0	1	0	1
97	1	0	0	1	0	0
98	1	0	0	1	0	1
99	1	0	0	1	0	0
100	1	0	0	1	0	1
101	1	0	0	1	0	0
102	1	0	0	1	0	1
103	1	0	0	0	0	0
104	1	0	0	0	0	1
105	1	0	0	0	0	0
106	1	0	0	0	0	1
107	1	0	0	0	0	0
108	1	0	0	0	0	1
109	1	0	0	1	0	0
110	1	0	0	1	0	1
111	1	0	0	0	0	0
112	1	0	0	0	0	1
113	1	0	0	0	0	0
114	1	0	0	0	0	1
115	1	0	0	0	1	0
116	1	0	0	0	1	1
117	1	0	0	0	1	0
118	1	0	0	0	0	1
119	1	0	0	0	0	0
120	1	0	0	0	1	1
121	1	0	0	0	1	0
122	1	0	0	0	1	1
123	1	0	0	0	1	0
124	1	0	0	0	0	1
125	1	0	0	0	0	0
126	1	0	0	0	0	1
127	1	0	0	0	0	0
128	1	0	0	0	0	1
129	1	0	0	1	0	0

Table continues on the next page...

State Counts	TRST_B	RESET_B	TDI	TDO	TMS	TCK
130	1	0	0	1	0	1
131	1	0	0	0	0	0
132	1	0	0	0	0	1
133	1	0	0	0	0	0
134	1	0	1	0	0	1
135	1	0	1	0	0	0
136	1	0	0	0	0	1
137	1	0	0	0	0	0
138	1	0	0	0	0	1
139	1	0	0	0	0	0
140	1	0	0	0	0	1
141	1	0	0	0	0	0
142	1	0	0	0	1	1
143	1	0	0	0	1	0
144	1	0	0	0	1	1
145	1	0	0	0	1	0
146	1	0	0	0	0	1
147	1	0	0	0	0	0
148	1	0	0	0	1	1
149	1	0	0	0	1	0
150	1	0	0	0	0	1
151	1	0	0	0	0	0
152	1	0	0	0	0	1
153	1	0	0	0	0	0
154	1	0	0	0	0	1
155	1	0	0	0	0	0
156	1	0	0	0	0	1
157	1	0	0	0	0	0
158	1	0	0	0	0	1
159	1	0	0	0	0	0
160	1	0	0	0	0	1
161	1	0	0	0	0	0
162	1	0	0	0	0	1
163	1	0	0	0	0	0
164	1	0	0	0	0	1
165	1	0	0	0	0	0

Table continues on the next page...

Special JTAG sequence to force a logical power on reset

State Counts	TRST_B	RESET_B	TDI	TDO	TMS	TCK
166	1	0	0	0	0	1
167	1	0	0	0	0	0
168	1	0	0	0	0	1
169	1	0	0	0	0	0
170	1	0	0	0	0	1
171	1	0	0	0	0	0
172	1	0	0	0	0	1
173	1	0	0	0	0	0
174	1	0	0	0	0	1
175	1	0	0	0	0	0
176	1	0	0	0	0	1
177	1	0	0	0	0	0
178	1	0	0	0	0	1
179	1	0	0	0	0	0
180	1	0	0	0	0	1
181	1	0	0	0	0	0
182	1	0	0	0	0	1
183	1	0	0	0	0	0
184	1	0	1	0	1	1
185	1	0	1	0	1	0
186	1	0	0	0	1	1
187	1	0	0	0	1	0
188	1	0	0	0	0	1
189	1	0	0	0	0	0
190	1	0	0	0	1	1
191	1	0	0	0	1	0
192	1	0	0	0	1	1
193	1	0	0	0	1	0
194	1	0	0	0	0	1
195	1	0	0	0	0	0
196	1	0	0	0	0	1
197	1	0	0	0	0	0
198	1	0	0	0	0	1
199	1	0	0	1	0	0
200	1	0	0	1	0	1
201	1	0	0	0	0	0

Table continues on the next page...

State Counts	TRST_B	RESET_B	TDI	TDO	TMS	TCK
202	1	0	1	0	0	1
203	1	0	1	0	0	0
204	1	0	0	0	0	1
205	1	0	0	0	0	0
206	1	0	0	0	0	1
207	1	0	0	0	0	0
208	1	0	0	0	0	1
209	1	0	0	0	0	0
210	1	0	0	0	0	1
211	1	0	0	0	0	0
212	1	0	0	0	1	1
213	1	0	0	0	1	0
214	1	0	0	0	1	1
215	1	0	0	0	1	0
216	1	0	0	0	0	1
217	1	0	0	0	0	0
218	1	0	0	0	1	1
219	1	0	0	0	1	0
220	1	0	0	0	0	1
221	1	0	0	0	0	0
222	1	0	0	0	0	1
223	1	0	0	0	0	0
224	1	0	0	0	0	1
225	1	0	0	0	0	0
226	1	0	0	0	0	1
227	1	0	0	0	0	0
228	1	0	0	0	0	1
229	1	0	0	0	0	0
230	1	0	0	0	0	1
231	1	0	0	0	0	0
232	1	0	0	0	0	1
233	1	0	0	0	0	0
234	1	0	1	0	0	1
235	1	0	1	0	0	0
236	1	0	0	0	0	1
237	1	0	0	0	0	0

Table continues on the next page...

Special JTAG sequence to force a logical power on reset

State Counts	TRST_B	RESET_B	TDI	TDO	TMS	TCK
238	1	0	0	0	0	1
239	1	0	0	0	0	0
240	1	0	0	0	0	1
241	1	0	0	0	0	0
242	1	0	0	0	0	1
243	1	0	0	0	0	0
244	1	0	1	0	0	1
245	1	0	1	0	0	0
246	1	0	0	0	0	1
247	1	0	0	0	0	0
248	1	0	0	0	0	1
249	1	0	0	0	0	0
250	1	0	0	0	0	1
251	1	0	0	0	0	0
252	1	0	0	0	0	1
253	1	0	0	0	0	0
254	1	0	0	0	1	1
255	1	0	0	0	1	0
256	1	0	0	0	1	1
257	1	0	0	0	1	0
258	1	0	0	0	0	1
259	1	0	0	0	0	0
260	0	0	0	0	0	1
261	0	0	0	0	1	0
262	0	0	0	0	1	1
263	0	0	0	0	1	0
264	0	0	0	0	1	1
265	0	0	0	0	1	0
266	0	0	0	0	1	1
267	0	0	0	0	1	0
268	0	0	0	0	1	1
269	0	0	0	0	1	0
270	0	0	0	0	1	1
271	1	1	0	0	0	0
272	1	1	0	0	0	1
273	1	1	0	0	0	0

Table continues on the next page...

State Counts	TRST_B	RESET_B	TDI	TDO	TMS	TCK
274	1	1	0	0	0	1
275	1	1	0	0	0	0

3 Using the OCR_DIS pin to effect a power on reset

In cases where the OCR_DIS pin is available, and the VCAP pins are attached to capacitors and not to an external voltage source (of 2.5 Volts), the OCR_DIS pin may be used to cause power distribution inside the device to cease. This results in a power on reset.

To use this method, use OCR_DIS to disable the voltage regulator until the voltage on VCAP falls low enough to trigger a power on reset. The time this needs to be held (pulse width on OCR_DIS) depends on the capacitance available and the current draw of the device after being disabled by the extreme RFI.

4 Conclusion

This application note details two alternative methods for resetting a Freescale MC56F8300 family device besides the nominal reset pin function, the nominal JTAG sequences, and the nominal power on reset:

- JTAG pins
- OCR_DIS pin

These methods need to be considered only if the application involves extreme RFI, such as can be achieved with difficultly even in a laboratory environment. Which, if any, of the options to implement would depend on the available resources..

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