ale Semiconductor, Inc.
tion Note

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Compact Thermal Model for Dual 24 V High-side Switch Family

1 Introduction

This application note describes the R/C thermal models of the MC06XS4200, MC10XS4200, and MC20XS4200 devices. This application note includes the thermal data for the aforementioned SMARTMOS devices and for the MC22XS4200 and MC50XS4200 devices.

These intelligent high-side switches are designed to be used in 24 V systems such as trucks, busses, and special engines. The low $R_{DS(on)}$ channels can control incandescent lamps, LEDs, solenoids or DC motors. Control, device configuration, and diagnostics are performed through a 16-bit SPI interface, allowing easy integration into existing applications. For a complete feature description, refer to the individual data sheets.

Contents

2 Thermal Model Extraction Details

3D transient thermal simulations were conducted to determine the thermal impedance of 06XS4200, 10XS4200, and 20XS4200 devices in combination with the short-circuit test board (by printed circuit board (PCB)) under natural convection conditions with an ambient temperature of 25 °C.

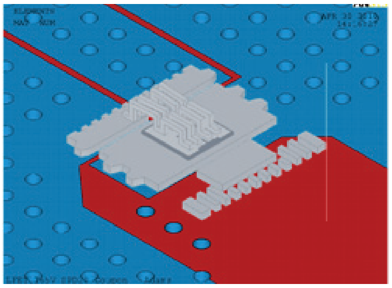

Figure 1. ANSYS 3D Model of the Device Mounted on Test Board

Methodology involved the separation of the thermal impedance model to a short-circuit test board thermal impedance, coupled to the packaged die thermal impedance. 3D transient thermal simulations were performed for each dual 24 V high-side switch component separately, to deduce the impedance models.

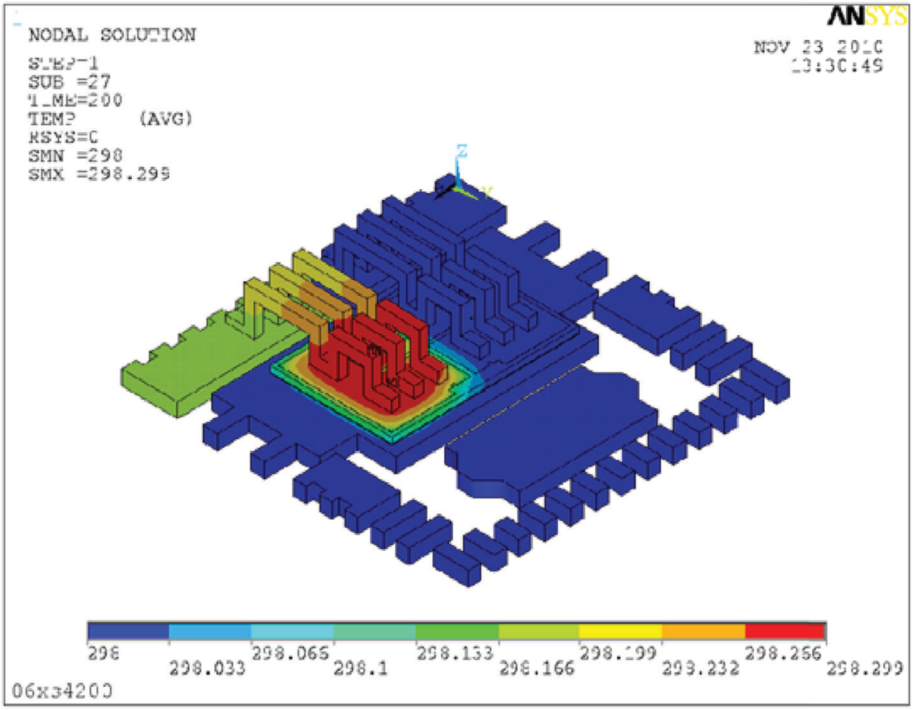

Figure 2. Example of Temperature Distribution (in Kelvin) in Die/Package When Only One MC06XS4200 Channel is Active

3 R/C Thermal Model

3.1 Model Description

The models described in Figure 3 and Figure 4 provide excellent accuracy over a wide dynamic range, without burdensome simulation times or model complexity. The foundation of each of the R/C models is an empirically calibrated ANSYS Finite Element Model. The first step in creating the R/C model is to exercise an ANSYS thermal model to create the device's transient thermal response. Next, the model's R/C network is selected so that its response matches that of the ANSYS simulation. A series of 5 or 6 RC pairs provides a usable simulation range from 10 μs to steady state. The R/C models are based on the peak temperatures predicted in the ANSYS simulations, so the R/C models predict peak, not averaged, die temperature during transient.

The models describe only the device's junction-to-case thermal response. They do not predict the thermal response of the PCB on which it is to be mounted. The two common types of R/C network models are Foster and Coyer. They differ in how their thermal capacitances are represented and managed. Foster models use paralleled R/C pairs connected in a series string. They are mathematically representative of the response, but their resistors and capacitors cannot be related to the physical capacitances and resistances in the device's thermal path. The output node of a Foster model must be connected to a fixed temperature source and not another thermal model. Foster models are mathematically easier to derive, and that is why they are sometimes preferred. The thermal capacitors in Cauer models are connected to thermal "ground". This topology allows the model to store heat energy within the device. Unlike Foster models, Cauer models yield accurate simulations when connected in series to other thermal models, such as that of a PCB.

The model's thermal grounds can be connected to Node 0 or to a fixed temperature source in the simulation, such as an ambient temperature source.

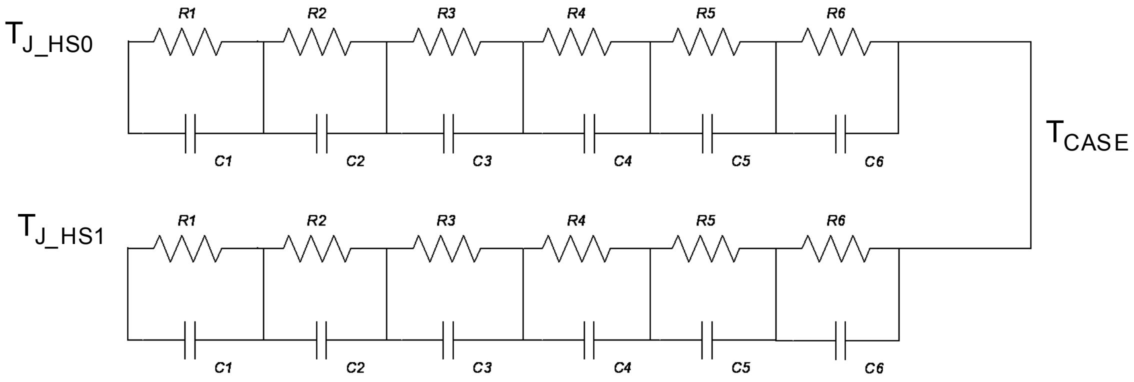

Figure 3. R/C Foster Thermal Model Description

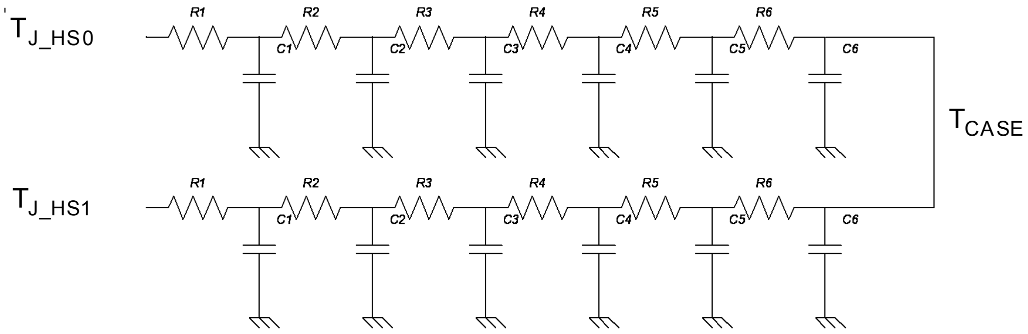

Figure 4. R/C Cauer Thermal Model Description

3.2 Model Parameters per Device

The R/C values are presented in the following tables.

Table 1. 06XS4200 R/C Parameters

Foster Resistance (°C/W)	Foster Capacitance (J/°C)	Cauer Resistance (°C/W)	Cauer Resistance (°C/W)
R1 = 0.001	C1 = 0.0006	R1 = 0.00178	C1 = 0.0004477
R2 = 0.0045	C2 = 0.0044	R2 = 0.02459	C2 = 0.001365
R3 = 0.01	C3 = 0.009	R3 = 0.0704	C3 = 0.001753
R4 = 0.145	C4 = 0.0048	R4 = 0.0946	C4 = 0.002642
R5 = 0.095	C5 = 0.0526	R5 = 0.07656	C5 = 0.062315
R6 = 0.028	C6 = 0.8051	R6 = 0.01548	C6 = 1.36646

Table 2. 10XS4200 R/C Parameters

Foster Resistance (°C/W)	Foster Capacitance (J/°C)	Cauer Resistance (°C/W)	Cauer Resistance (°C/W)
R1 = 0.002	C1 = 0.0003	R1 = 0.00324	C1 = 0.0002352
R2 = 0.0071	C2 = 0.0028	R2 = 0.04066	C2 = 0.000884
R3 = 0.018	C3 = 0.005	R3 = 0.1067	C3 = 0.00107
R4 = 0.235	C4 = 0.003	R4 = 0.1541	C4 = 0.001719
R5 = 0.15	C5 = 0.0367	R5 = 0.11189	C5 = 0.04552
R6 = 0.03	C6 = 2.6667	R6 = 0.02545	C6 = 3.08981

Table 3. 20XS4200 R/C Parameters

Foster Resistance (°C/W)	Foster Capacitance (J/°C)	Cauer Resistance (°C/W)	Cauer Resistance (°C/W)
R1 = 0.004	C1 = 0.00015	R1 = 0.0064	C1 = 0.000118
R2 = 0.0011	C2 = 0.0018	R2 = 0.0872	C2 = 0.0004561
R3 = 0.08	C3 = 0.00125	R3 = 0.12486	C3 = 0.0005482
R4 = 0.47	C4 = 0.00245	R4 = 0.3931	C4 = 0.001767
R5 = 0.12	C5 = 0.05	R5 = 0.07859	C5 = 0.07477
R6 = 0.028	C6 = 2.6786	R6 = 0.02285	C6 = 3.1976

4 Thermal Data

4.1 MC06XS4200

Table 4. MC06XS4200 Specifications

Device	23 ld PQFN-EP MC06XS4200
Package	23 ld PQFN-EP
Pitch	0.9
Flag Size	7.6 mm x 4.7 mm
Flag Style	Solid Pad

Table 5. Thermal Resistance Data

Rating	Description	Symbol	Value	Unit	Notes
Junction to Ambient Natural Convection (Power Die)	Thermally enhanced four layer board (HPRA coupon)	$R_{\theta JA}$	12.0	°C/W	(1)
Junction to Ambient Natural Convection (Power Die)	Four layer board (JEDEC 2s2p)	$R_{\theta JA}$	24.3	°C/W	(1),(2)
Junction to Board (Power Die)	Thermally enhanced four layer board (HPRA coupon)	$R_{\theta JB}$	1.3	°C/W	(3)
Junction to Board (Power Die)	Four layer board (JEDEC 2s2p)	$R_{\theta JB}$	3.5	°C/W	(3)
Junction to Case (bottom/flag) (Power Die)	Flag bottom side is fixed to ambient temperature	$R_{\theta JC}$ (bottom)	0.144	°C/W	(6)
Junction to Case (top) (Power Die)	Heat is forced through package top side	$R_{\theta JC}$ (top)	12.7	°C/W	(4)
Junction to Package Top	Natural Convection (thermally enhanced board)	ΨJT	0.3	°C/W	(5)
Junction to Package Top	Natural Convection (2s2p)	ΨJT	0.65	°C/W	(5)

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
6. Thermal resistance between the die and the case bottom/flag surface (simulated) (flag bottom side fixed to ambient temperature).

The finite element model included the following package parameters:

- Lead frame material: copper C194
- Lead frame overall thickness: 0.5 mm
- Power Die Attach: 92.5Pb5Sn2.5Ag solder die attach, k = 46 W/mK
- Mold Compound: k = 0.92 W/mK

- Ambient temperature: 25 °C
- Thermally enhanced board (HPRA coupon) 1.8 mm thick 4 copper layer each 95% coverage and 76 µm thick

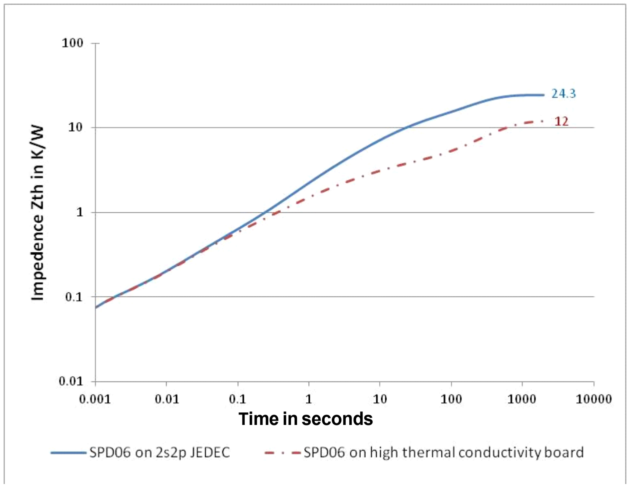

Figure 5. Impedance Curves of MC06XS4200 on JEDEC 2s2p and Thermally Enhanced HPRA Board

4.2 MC10XS4200

Table 6. MC10XS4200 Specifications

Device	23 ld PQFN-EP MC10XS4200
Package	23 ld PQFN-EP
Pitch	0.9
Flag Size	5.1 mm x 4.7 mm
Flag Style	Solid Pad

Table 7. Thermal Resistance Data

Rating	Description	Symbol	Value	Unit	Notes
Junction to Ambient Natural Convection (Power Die)	Thermally enhanced four layer board (HPRA coupon)	$R_{\theta JA}$	12.2	°C/W	(1)
Junction to Ambient Natural Convection (Power Die)	Four layer board (JEDEC 2s2p)	$R_{\theta JA}$	24.1	°C/W	(1),(2)
Junction to Board (Power Die)	Thermally enhanced four layer board (HPRA coupon)	$R_{\theta JB}$	1.5	°C/W	(3)
Junction to Board (Power Die)	Four layer board (JEDEC 2s2p)	$R_{\theta JB}$	5.0	°C/W	(3)
Junction to Case (bottom/flag) (Power Die)	Flag bottom side is fixed to ambient temperature	$R_{\theta JC}$ (bottom)	0.22	°C/W	(6)
Junction to Case (top) (Power Die)	Heat is forced through package top side	$R_{\theta JC}$ (top)	13.2	°C/W	(4)
Junction to Package Top	Natural Convection (thermally enhanced board)	Ψ_{JT}	0.35	°C/W	(5)
Junction to Package Top	Natural Convection (2s2p)	Ψ_{JT}	0.8	°C/W	(5)

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
6. Thermal resistance between the die and the case bottom/flag surface (simulated) (flag bottom side fixed to ambient temperature).

The finite element model included the following package parameters:

- Lead frame material: copper C194
- Lead frame overall thickness: 0.5 mm
- Power Die Attach: 92.5Pb5Sn2.5Ag solder die attach, k = 46 W/mK
- Mold Compound: k = 1.0 W/mK
- Ambient temperature: 25 °C
- Thermally enhanced board (HPRA coupon) 1.8 mm thick 4 copper layer each 95% coverage and 76 µm thick

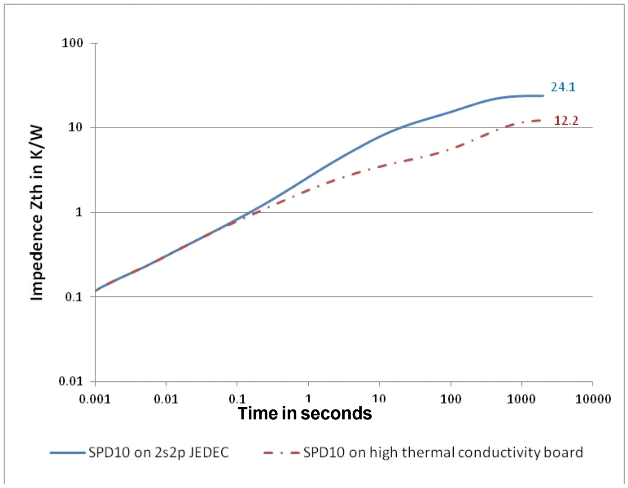

Figure 6. Impedance Curves of MC10XS4200 on JEDEC 2s2p and Thermally Enhanced HPRA Board

4.3 MC20XS4200

Table 8. MC20XS4200 Specifications

Device	23 ld PQFN-EP MC20XS4200
Package	23 ld PQFN-EP
Pitch	0.9
Flag Size	3.4 mm x 4.7 mm
Flag Style	Solid Pad

Table 9. Thermal Resistance Data

Rating	Description	Symbol	Value	Unit	Notes
Junction to Ambient Natural Convection (Power Die)	Thermally enhanced four layer board (HPRA coupon)	$R_{\theta JA}$	12.4	°C/W	(1)
Junction to Ambient Natural Convection (Power Die)	Four layer board (JEDEC 2s2p)	$R_{\theta JA}$	24.6	°C/W	(1),(2)
Junction to Board (Power Die)	Thermally enhanced four layer board (HPRA coupon)	$R_{\theta JB}$	1.9	°C/W	(3)
Junction to Board (Power Die)	Four layer board (JEDEC 2s2p)	$R_{\theta JB}$	5.3	°C/W	(3)
Junction to Case (bottom/flag) (Power Die)	Flag bottom side is fixed to ambient temperature	$R_{\theta JC}$ (bottom)	0.32	°C/W	(6)
Junction to Case (top) (Power Die)	Heat is forced through package top side	$R_{\theta JC}$ (top)	14.5	°C/W	(4)
Junction to Package Top	Natural Convection (thermally enhanced board)	Ψ_{JT}	0.5	°C/W	(5)
Junction to Package Top	Natural Convection (2s2p)	Ψ_{JT}	1.2	°C/W	(5)

Notes
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
6. Thermal resistance between the die and the case bottom/flag surface (simulated) (flag bottom side fixed to ambient temperature).

The finite element model included the following package parameters:

- Lead frame material: copper C194
- Lead frame overall thickness: 0.5 mm
- Power Die Attach: 92.5Pb5Sn2.5Ag solder die attach, k = 46 W/mK
- Mold Compound: k = 1.0 W/mK
- Ambient temperature: 25 °C
- Thermally enhanced board (HPRA coupon) 1.8 mm thick 4 copper layer each 95% coverage and 76 μm thick

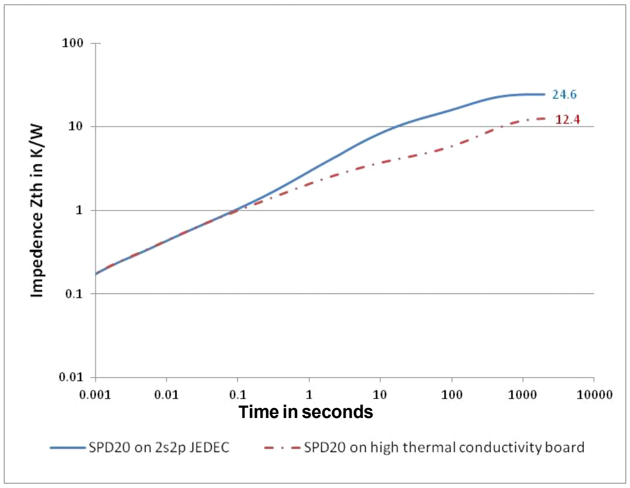

Figure 7. Impedance Curves of MC20XS4200 on JEDEC 2s2p and Thermally Enhanced HPRA Board

4.4 MC22XS4200

Table 10. MC22XS4200 Specifications

Package	32ld SOIC-W 7.5x11x2.4 EP 0.65p
Pitch	0.65 mm
Flag Size	7.485 mm x 5.1 mm
Flag Style	Exposed Pad

Table 11. Thermal Resistance Data

Rating	Description	Symbol	Value	Unit	Notes
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	81.0	°C/W	(1),(2)
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	22.0	°C/W	(1),(3)
Junction to Board	Four layer board (JEDEC 2s2p)	$R_{\theta JB}$	8.0	°C/W	(4)
Junction to Case (top)	Heat is forced through package top side	$R_{\theta JCTop}$	24.0	°C/W	(5)
Junction to Case (bottom)	Flag bottom side is fixed to ambient temperature	$R_{\theta JCBottom}$	1.4	°C/W	(6)
Junction to Package Top	Natural Convection	Ψ_{JT}	8.0	°C/W	(7)

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Simulation Details

All thermal ratings are determined at 125 °C operating temperature. The model included the following package parameters:

- Lead frame material: Copper
- Lead frame overall thickness: 0.2 mm
- Lead width: 0.29 mm
- Flag to bond finger gap: 0.2 mm, Angle: 0 degrees
- Die Attach: k = 0.4 W/mK (Control) and 10 W/mK (Power)
- Mold Compound: k = 0.96 W/mK

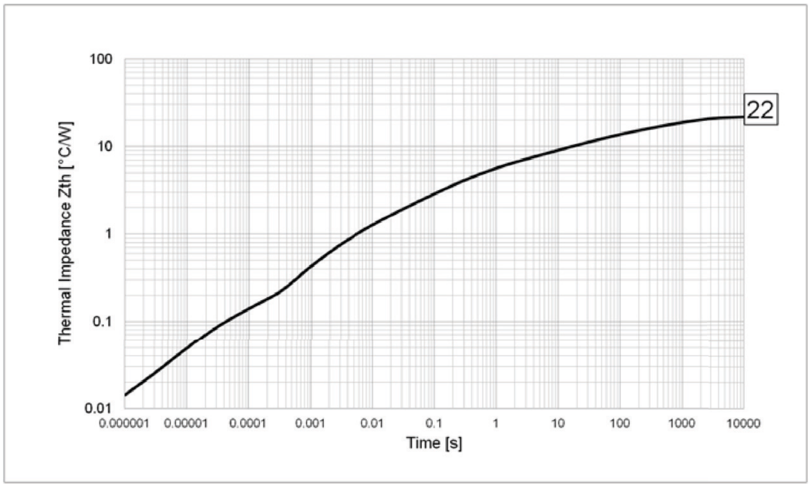

Figure 8. Impedance Curve for MC22XS4200 on JEDEC 2s2p

4.5 MC50XS4200

Table 12. MC50XS4200 Specifications

Package	32 ld SOIC-W 7.5x11x2.4 EP 0.65p
Pitch	0.65 mm
Flag Size	7.485 mm x 5.1 mm
Flag Style	Exposed Pad

Table 13. Thermal Resistance Data

Rating	Description	Symbol	Value	Unit	Notes
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	82.0	°C/W	(1),(2)
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	24.0	°C/W	(1),(3)
Junction to Board	Four layer board (JEDEC 2s2p)	$R_{\theta JB}$	9.0	°C/W	(4)
Junction to Case (top)	Heat is forced through package top side	$R_{\theta JCTop}$	26.0	°C/W	(5)
Junction to Case (bottom)	Flag bottom side is fixed to ambient temperature	$R_{\theta JCBottom}$	2.7	°C/W	(6)
Junction to Package Top	Natural Convection	Ψ_{JT}	9.0	°C/W	(7)

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Simulation Details

All thermal ratings are determined at 125 °C operating temperature. The model included the following package parameters:

- Lead frame material: Copper
- Lead frame overall thickness: 0.2 mm
- Lead width: 0.29 mm
- Flag to bond finger gap: 0.2 mm, Angle: 0 degrees
- Die Attach: k = 0.4 W/mK (Control) and 10 W/mK (Power)
- Mold Compound: k = 0.96 W/mK

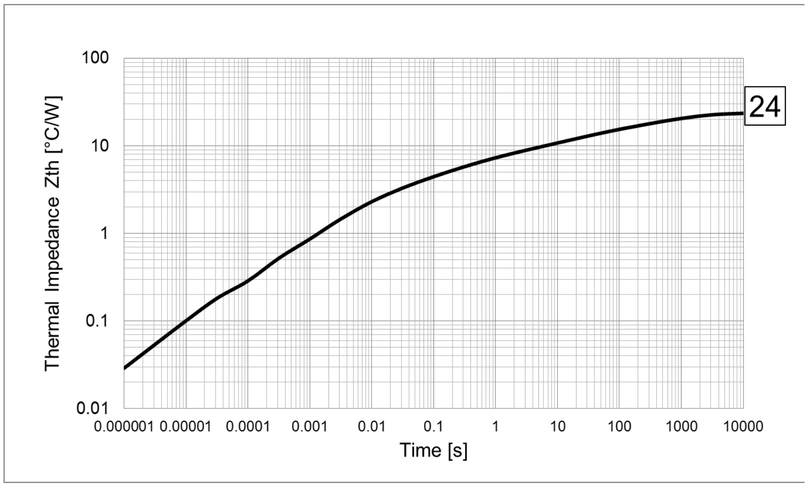

Figure 9. Impedance Curves for MC50XS4200 on JEDEC 2s2p

5 References

Following are URLs where you can obtain information on related Freescale products and application solutions:

Freescale.com Support Pages	Description	URL
MC06XS4200	Data Sheet	http://cache.freescale.com/files/analog/doc/data_sheet/MC06XS4200.pdf
MC10XS4200	Data Sheet	http://cache.freescale.com/files/analog/doc/data_sheet/MC10XS4200.pdf
MC20XS4200	Data Sheet	http://cache.freescale.com/files/analog/doc/data_sheet/MC20XS4200.pdf
MC22XS4200	Data Sheet	http://cache.freescale.com/files/analog/doc/data_sheet/MC22XS4200.pdf
MC50XS4200	Data Sheet	http://cache.freescale.com/files/analog/doc/data_sheet/MC50XS4200.pdf
KT06XS4200UG	Evaluation Board User Guide	http://cache.freescale.com/files/analog/doc/user_guide/KT06XS4200UG.pdf
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KT20XS4200UG	Evaluation Board User Guide	http://cache.freescale.com/files/analog/doc/user_guide/KT20XS4200UG.pdf
KT22XS4200UG	Evaluation Board User Guide	http://cache.freescale.com/files/analog/doc/user_guide/KT22XS4200UG.pdf
KT50XS4200UG	Evaluation Board User Guide	http://cache.freescale.com/files/analog/doc/user_guide/KT50XS4200UG.pdf
KITUSBSPIEVME	Interface Dongle	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=KITUSB-SPIEVME
	White Paper	http://www.ansys.com

6 Revision History

Revision	Date	Description
1.0	9/2012	• Initial release
2.0	12/2014	• Thermal data added for MC06XS4200, MC10XS4200, MC20XS4200, MC22XS4200, MC50XS4200

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