

MPC5674F ECC Initialization and Application Information

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1 Overview

This application note describes the Error Correction Code (ECC) and its behavior within an application for the MPC5674F automotive microcontroller.

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2 Introduction

ECC is a mechanism used to detect and, potentially, correct memory errors in both SRAM and Flash for the MPC5674F. This is done by generating ECC syndrome bits. There are eight ECC syndrome bits for each 64-bit data for both SRAM and Flash. ECC syndrome bits are calculated on write accesses and then used on read accesses to detect and correct errors. ECC hardware on the MPC5674F will automatically correct single-bit errors when reading from a memory location corrupted with a single-bit error. Multi-bit errors are not correctable.

The Error Correction Status Module (ECSM) allows the application to collect information on memory errors reported by the ECC. ECSM registers store detailed information about address, attributes, and data of the error.

To ensure correct behavior of the ECC and ECSM, the user should consider the following:

- Initialization of SRAM and Flash to ensure correct ECC behavior

Initialization

- Configuration of the ECSM for error reporting
- ECC reporting behavior

3 Initialization

3.1 Initialization of memories

After Power on Reset (POR), the contents of internal SRAM, including the ECC syndrome bits, are random. Therefore the corresponding ECC syndrome bits are unknown, and may not match the corresponding data, resulting in ECC errors. To prevent generating ECC errors during a read access of uninitialized SRAM, an initialization routine must perform 64-bit writes to all SRAM locations. This will initialize the ECC syndrome bits, to match the corresponding data.

The Flash module is nonvolatile and the syndrome bits are calculated and stored when the Flash is programmed.

The ECC mechanism does not need any further initialization.

3.2 ECSM setup

The ECSM has to be initialized to report ECC errors to the ECSM. The ECSM can provide address, data, and further attributes associated with an ECC error. Error reporting can be enabled individually for single-bit errors and multi-bit, noncorrectable, errors, and independently for SRAM and Flash.

To enable single-bit error reporting and capture the error details for:

- SRAM, set the ER1BR bit in the ECSM Error Configuration Register (ECSM_ECR).
- Flash, set the EF1BR bit in ECSM_ECR.

To enable noncorrectable error reporting and capture the error details for:

- SRAM, set the ERNCR bit in the ECSM Error Configuration Register (ECSM_ECR).
- Flash, set the EFNCR bit in ECSM_ECR.

Upon the detection of an ECC error the ECSM can be used to request interrupts to the INTC, additional to the interrupts requested by a master, the core will also generate exceptions on the detection of an ECC error. It is possible to use the ECSM reporting without an interrupt being requested. To use ECSM error reporting without generating an ECSM interrupt:

- Enable noncorrectable reporting in the ECSM.
- Ensure the external interrupt is disabled.
- Ensure that the INTC_PSR[PRI] value for the ECC error interrupt request is 0.

4 ECC reporting behavior

On the detection of an ECC error different behaviors for the error reporting will be observed, depending on several factors.

4.1 Single-bit error detection and correction

Single-bit errors will be corrected automatically by the ECC.

If ECSM single-bit error reporting is enabled the R1BC bit is set if the error was detected in SRAM, and the F1BR bit if the error was detected in the Flash. If either of these bits is set, it will result in an ECC interrupt request to the interrupt controller. Address, data, and other attributes related to the error are also captured in the associated ECSM registers.

4.2 Multi-bit error detection

If the ECC detects a multi-bit error, a core exception is generated:

- When the ECC error is a result of a CPU data access or a CPU instruction fetch, the exception raised will be an IVOR1, regardless of the settings of the EE and the ME bits in the Machine State Register (MSR), and also regardless of whether error reporting is enabled in the ECSM.
- ECC errors generated by other masters like eDMA and so on do not generate machine check exceptions, as these accesses are not visible to the core. In this case, the ECC error will be captured within the respective master's own registers and this master will, if configured accordingly, request an interrupt.

In addition to the above ECC error reporting for a noncorrectable ECC error, the ECSM can report errors and, if configured, request interrupts to the INTC.

If error reporting is enabled and a noncorrectable ECC error occurs, error information is recorded in other ECSM registers and an interrupt request is generated on vector 9 of the interrupt controller (INTC). If vector 9 of INTC is enabled, an external exception (IVOR4) is generated.

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