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Application Note

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Demodulating Communication Signals of Qi-Compliant Low-Power Wireless Charger Using MC56F8006 DSC

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Contents

1 Introduction

Wireless power is becoming more and more popular today, through which a number of electronic items like mobiles, laptops, media players, can be charged without cords or wires. It is beginning to show great potential in the consumer market.

Wireless Power Consortium (WPC) has developed a standard called Qi, which defines the types of inductive coupling and the communications protocol to be used for low-power wireless devices. Qi creates interoperability between the Power Transmitter and the Power Receiver. As a regular member of WPC, Freescale has its own Qi-compliant low-power wireless charger reference design for the customers now.

Qi-compliant wireless devices use amplitude-shift keying (ASK) modulation to communicate

between Power Receiver and Power Transmitter. This application note aims to describe the Qi communication data demodulation design for wireless charger transmitter with MC56F8006 digital signal controller (DSC) including Qi communication interface, demodulation circuits design, and demodulation software design.

2 Qi communication interface

Amplitude shift keying (ASK) is a relatively simple modulation scheme. ASK is equivalent to the amplitude modulation of the analog signal, and the carrier frequency signal is multiplied by a binary digital. The frequency and phase of the carrier are kept constant, and the amplitude is variable. Information bits are passed through the carrier's amplitude. It is called binary amplitude shift keying (2ASK) because the modulation signal can take only two binary levels, 0 or 1. The multiplication result of this binary digit with the carrier frequency is equivalent to the carrier frequency on or off. It means that the modulated digital signal is 1 when carrier transmission takes place and 0 when there is no carrier transmission.

The Power Receiver communicates to the Power Transmitter using backscatter modulation. For this purpose, the Power Receiver modulates the amount of power drawn from the Power Signal. The Power Transmitter detects this as a modulation of the current through and/or voltage across the Primary Cell. In other words, the Power Receiver and Power Transmitter use amplitude modulated Power Signal to provide a Power Receiver to Power Transmitter communications channel.

2.1 Modulation scheme

The Power Receiver shall modulate the amount of power drawn from the Power Signal, such that the Primary Cell current or Primary Cell voltage assumes two states, namely a HI state and a LO state. A state is characterized in that the amplitude is constant within a certain variation Δ for at least t_s ms. The difference of the amplitude of the Primary Cell current in the HI and LO state is at least 15 mA. The difference of the amplitude of the Primary Cell voltage in the HI and LO state is at least 200 mV. Figure 1 and Table 1 show the details.

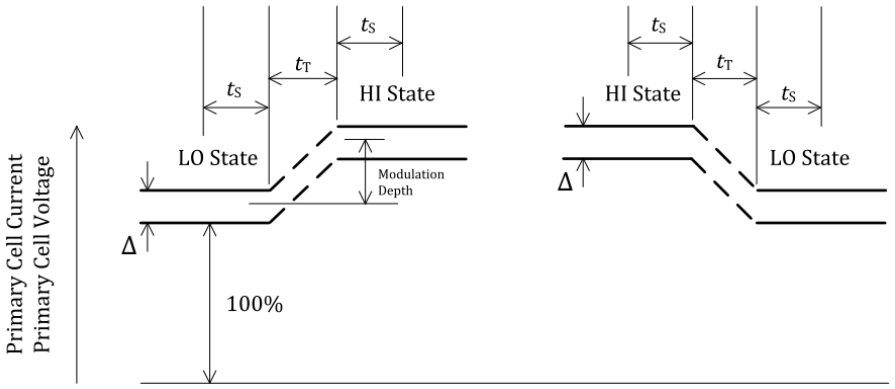

Figure 1. Modulation scheme

Parameter	Symbol	Value	Unit
Maximum transition time	t_T	100	us
Minimum stable time	t_s	150	us
Current amplitude variation	Δ	8	mA
Voltage amplitude variation	Δ	110	mV

Table 1. Modulation timing definition

2.2 Bit encoding scheme

The Power Receiver shall use a differential bi-phase encoding scheme to modulate data bits onto the Power Signal. For this purpose, the Power Receiver shall align each data bit to a full period t_{CLK} of an internal clock signal, such that the start of a data bit coincides with the rising edge of the clock signal. This internal clock signal shall have a frequency $f_{CLK} = 2^{\pm 4\%}$ kHz.

The Receiver shall encode a ONE bit using two transitions in the Power Signal, such that the first transition coincides with the rising-edge of the clock signal, and the second transition coincides with the falling-edge of the clock signal. The Receiver shall encode a ZERO bit using a single transition in the Power Signal, which coincides with the rising-edge of the clock signal. The following figure shows an example.

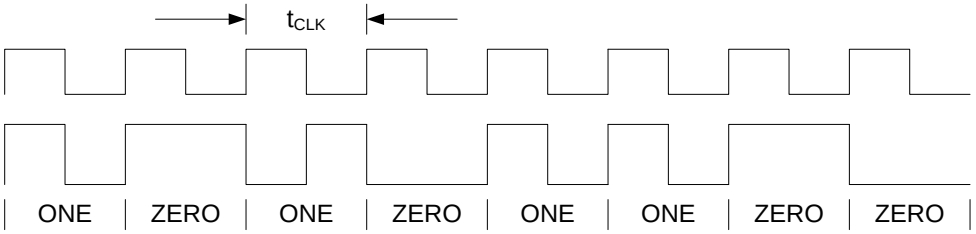

Figure 2. Bit encoding scheme

2.3 Byte encoding scheme

The Power Receiver shall use an 11-bit asynchronous serial format to transmit a data byte. This format consists of a start bit, the 8 data bits of the byte, a parity bit, and a single stop bit. The start bit is a ZERO. The order of the data bits is LSB first and the parity bit is odd. This means that the Power Receiver shall set the parity bit to ONE if the data byte contains an even number of ONE bits. Otherwise, the Power Receiver shall set the parity bit to ZERO. The stop bit is a ONE.

The following figure shows the data byte format including the differential bi-phase encoding of each individual bit, using the value 0x35 as an example.

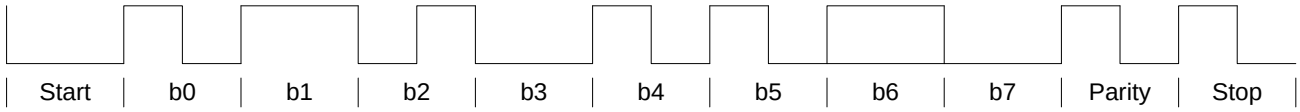

Figure 3. Byte encoding scheme

2.4 Packet structure

The Power Receiver shall communicate to the Power Transmitter using data packets. As shown in Figure 4, a packet consists of four parts, namely a preamble, a header, a message, and a checksum. The preamble consists of a minimum of 11 and a maximum of 25 bits, all set to ONE, and encoded as defined in Bit encoding scheme. The preamble enables the Power Transmitter to synchronize with the incoming data and accurately detect the start bit of the header.

The header, message, and checksum consist of a sequence of three or more bytes encoded as defined in Header, Message, and Checksum.

Figure 4. Packet structure

The Power Transmitter shall consider a data packet as received correctly if:

- The Power Transmitter has detected at least four preamble bits that are followed by a start bit.
- The Power Transmitter has not detected a parity error in any of the bytes that comprise the packet. This includes the header byte, the message bytes, and the checksum byte.
- The Power Transmitter has detected the stop bit of the checksum byte.
- The Power Transmitter has determined that the checksum byte is consistent. (see Checksum)

If the Power Transmitter does not receive a packet correctly, the Power Transmitter shall discard the packet, and not use any of the information contained therein. In the ping phase as well as in the identification and configuration phase, this typically leads to a timeout, which causes the Power Transmitter to remove the Power Signal.

2.4.1 Header

The header consists of a single byte that indicates the packet type. In addition, the header implicitly provides the size of the message contained in the packet.

2.4.2 Message

The Power Receiver shall ensure that the message contained in the packet is consistent with the packet type indicated in the header. See Qi Specification, Part1 Section 6 for a detailed definition of the possible messages. The first byte of the message, byte B0, directly follows the header.

2.4.3 Checksum

The checksum consists of a single byte, which enables the Power Transmitter to check for transmission errors. The Power Transmitter shall calculate the checksum as follows:

$$C := H \oplus B_0 \oplus B_1 \oplus ... \oplus B_{last}$$

Where C represents the calculated checksum, H represents the header byte, and B_0, B_1,…, B_{last} represent the message bytes.

If the calculated checksum and the checksum byte contained in the packet are not equal, the Power Transmitter shall determine that the checksum is inconsistent.

3 Demodulation circuit design

The Power Receiver communicates to the Power Transmitter using backscatter modulation as defined in Modulation scheme. The function of communication demodulation circuit is to detect the 2 kHz Communication Signal from the 110 kHz Power Signal.

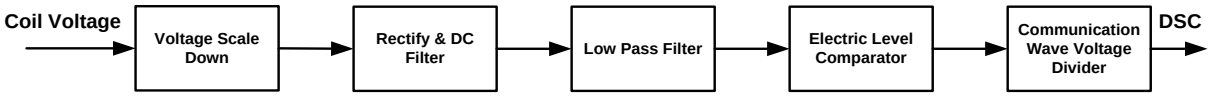

Figure 5. Block diagram of communication demodulation circuit

Figure 5 shows the block diagram of communication demodulation circuit. The input of the circuit is coil voltage with communication signals, and the output is communication data following bit encoding scheme. The circuit can be divided into the following five parts:

- Voltage scale down part
- Rectifier and DC filter
- Low-pass filter
- Electric level comparator
- Communication wave voltage divider

Each of these components is described in the following subsections.

Figure 6 shows the input of the demodulation circuit. The fundamental waves are the primary voltage and the carrier waves are communication signals.

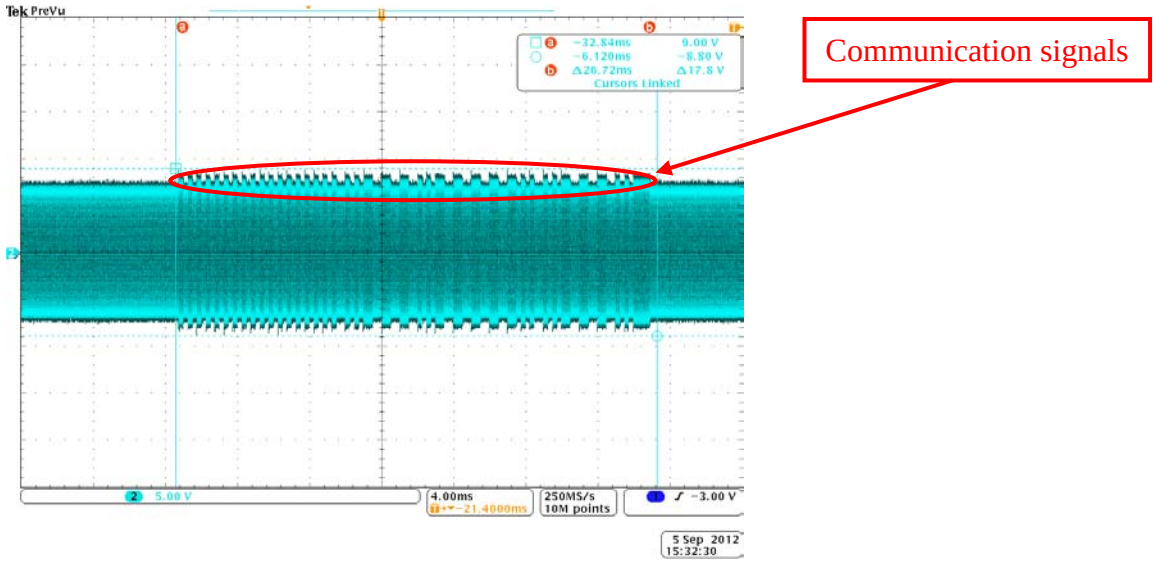

Figure 6. Waveform of primary coil voltage

3.1 Voltage scale down circuit

The range of coil voltage is from 16-32 V pk-pk, and can reach levels exceeding 40 V pk-pk. As shown in Figure 7, the function of a voltage scale down circuit is to scale down the voltage Coil_IN to GNDA and Coil_OUT to GNDA. Differential circuit is used to adjust the midpoint of the wave to 2.5 V and the amplitude of the wave between 0–5 V.

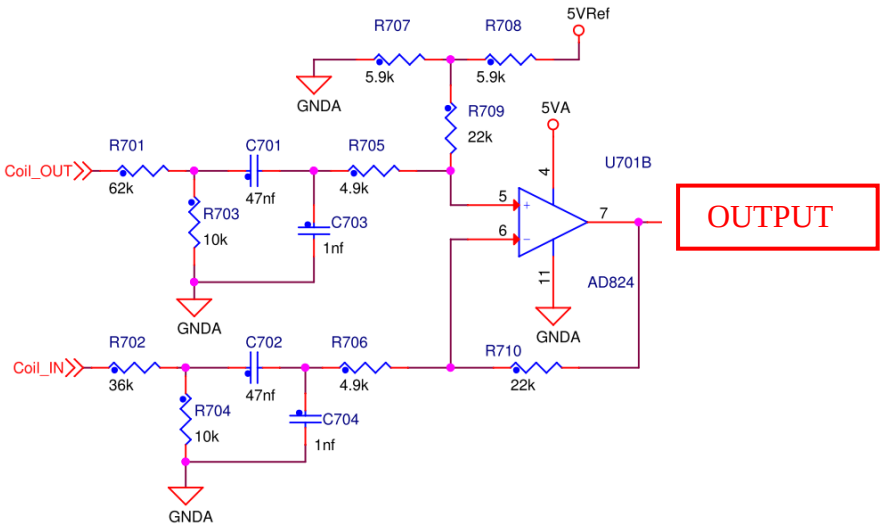

Figure 7. Voltage scale down circuit

Figure 8 shows the communication wave after the voltage scale down circuit.

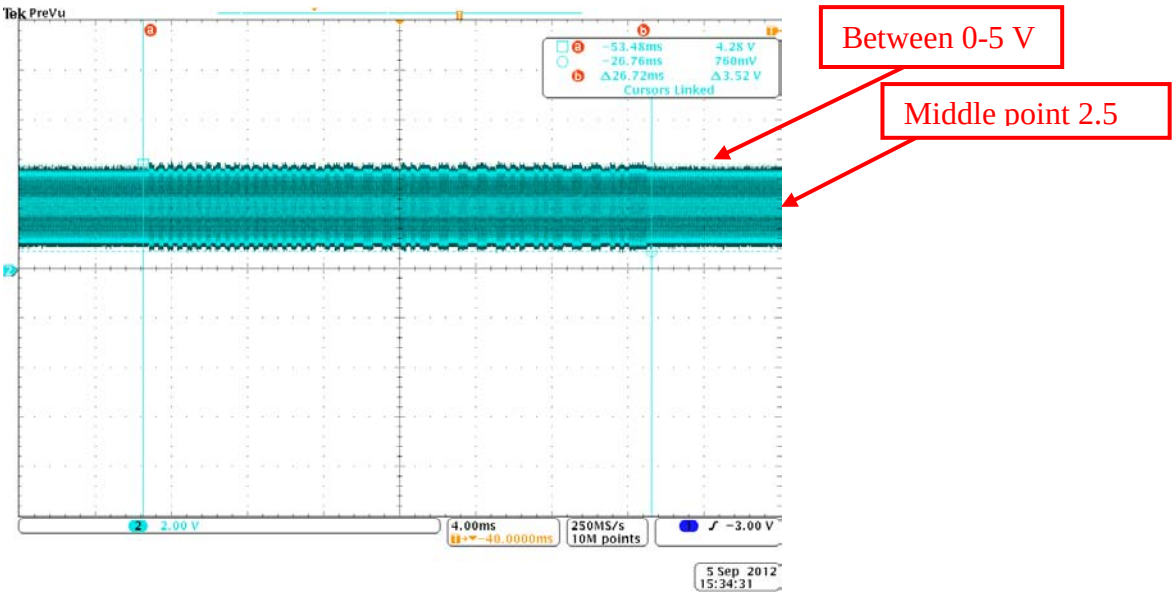

Figure 8. Communication wave after the voltage scale down circuit

3.2 Rectify and DC filter circuit

As shown in Figure 9, the functions of rectify and DC filter circuit are as follows.

1. Rectify the wave to get the first half cycle, transfer the sinusoidal wave to saw tooth wave.
2. Filter the DC part of the wave to make 2.5 V the middle point of the sawtooth wave.

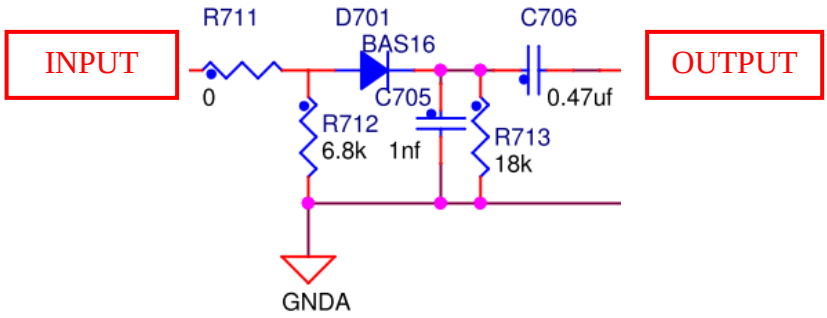

Figure 9. Rectifier and DC filter circuit

Figure 10 shows the communication wave after rectify and DC filter circuit.

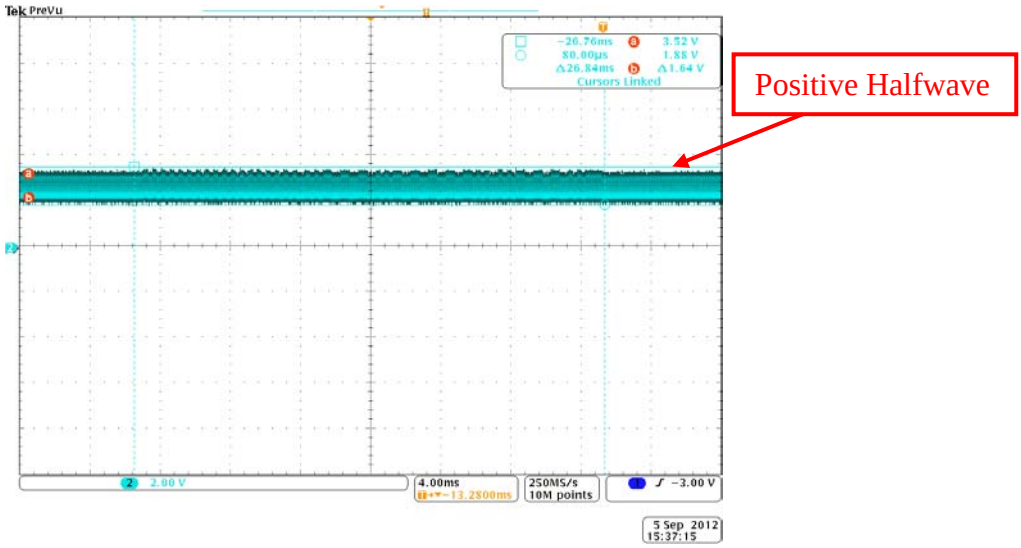

Figure 10. Communication wave after the rectify and DC filter circuits

3.3 Low-pass filter design

Figure 11 shows the low-pass filter circuit. Improved second-order low pass filter is used. The function is to filter the 107 kHz high-frequency power wave to get the 2 kHz low-speed communication data.

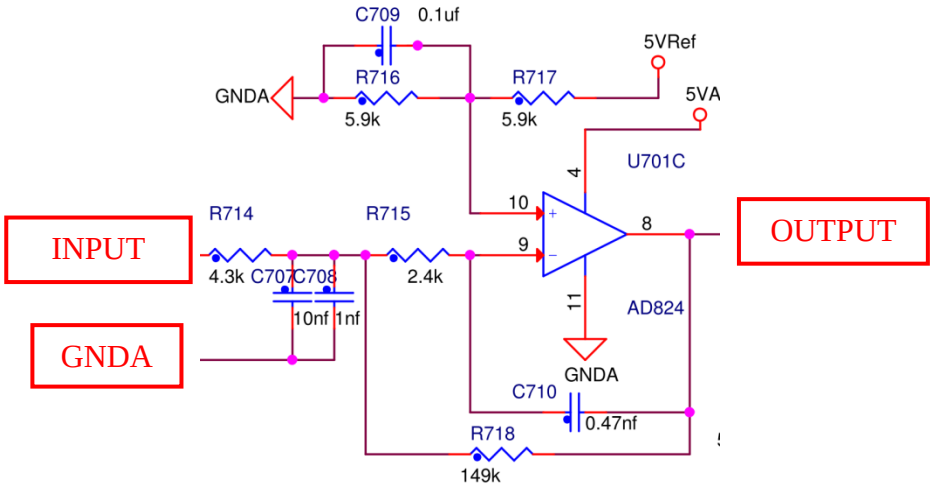

Figure 11. Low-pass filter

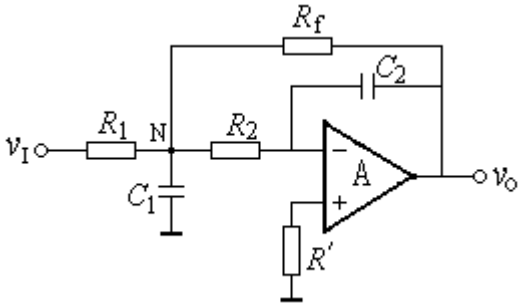

Figure 12. Improved second-order low-pass filter

Figure 12 shows the schematic of improved second-order low-pass filter selected in the design.

The following equations can be used to determine several parameters of the low-pass filter.

$$V_o(s) = \frac{-1}{sC_2R_2}V_N(s)$$

Where $V_o(s)$ is the output of the second-order low pass filter, and $V_N(s)$ is the voltage at point N.

The current to point N is 0. See the following equation.

$$\frac{V_i(s)-V_N(s)}{R_1} - V_N(s)sC_1 - \frac{V_N(s)}{R_2} - \frac{V_N(s)-V_o(s)}{R_f} = 0$$

$V_i(s)$ is the input of the second-order low-pass filter. Resistors R_1, R_2, R_f and capacitors C_1 and C_2 determine the parameters of low-pass filters.

Transfer function can be calculated using the following equation.

$$A_v(s) = \frac{-R_f/R_1}{1+sC_2R_2R_f(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_f})+s^2C_1C_2R_2R_f}$$

Set $s = j\omega$, then the frequency response can be calculated as:

$$\dot{A}_v = \frac{A_{vp}}{1-(\frac{f}{f_0})^2 + j\frac{1}{Q}\frac{f}{f_0}}$$

$$(f_0 = \frac{1}{2\pi\sqrt{C_1C_2R_2R_f}},\ A_{vp} = -\frac{R_f}{R_1},\ Q = (R_1 \parallel R_2 \parallel R_f)\sqrt{\frac{C_1}{R_2R_fC_2}})$$

(f_0: Pass band Cut off frequency, A_{vp}: Pass band gain, Q: $|\dot{A}_v|_{(f=f_0)} = QA_{vp}$)

Set R_1 = 4.3 kΩ, R_2= 2.4 kΩ, R_f =149 kΩ, C_1 =11 nF and C_2= 0.47 nF.

$$f_0 = \frac{1}{2\pi\sqrt{C_1 C_2 R_2 R_f}}$$

$$= \frac{1}{2\pi\sqrt{11*10^{-9}*0.47*10^{-9}*2.4*10^{3}*149*10^{3}}}$$

$$= 3.7kHz$$

$$A_{vp} = -\frac{R_f}{R_1} = 34.65$$

$$Q = (R_1 \parallel R_2 \parallel R_f)\sqrt{\frac{C_1}{R_2 R_f C_2}} = 1.13$$

$$|1-(\frac{f_c}{f_0})^2 + j\frac{1}{Q}\frac{f_c}{f_0}| = \sqrt{2}$$

$$f_c = 1.33 f_0 = 4.9kHz$$

(f_c : -3 db cut-off frequency)

The following figure shows the communication wave after the second-order LPF.

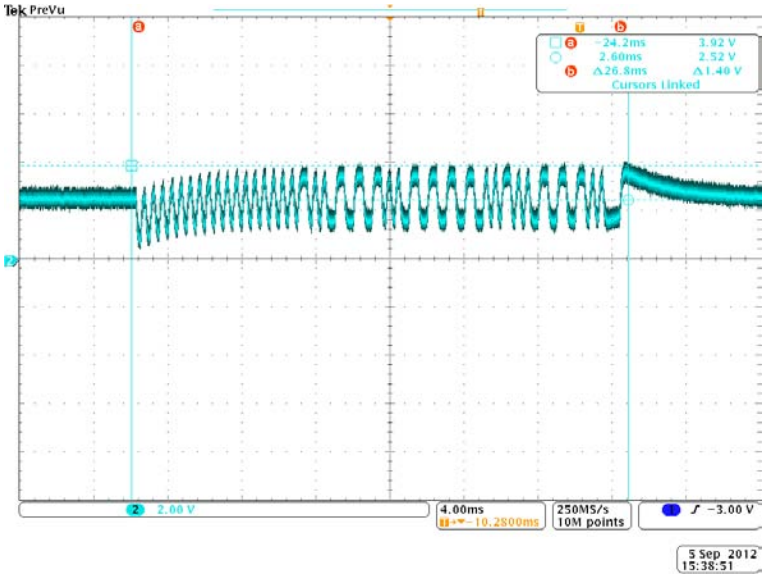

Figure 13. Communication wave after the second-order low-pass filter

3.4 Comparator

The function of comparator is to compare the input signal value with reference (2.5 V) to get a square wave. A comparator circuit is shown in the following figure.

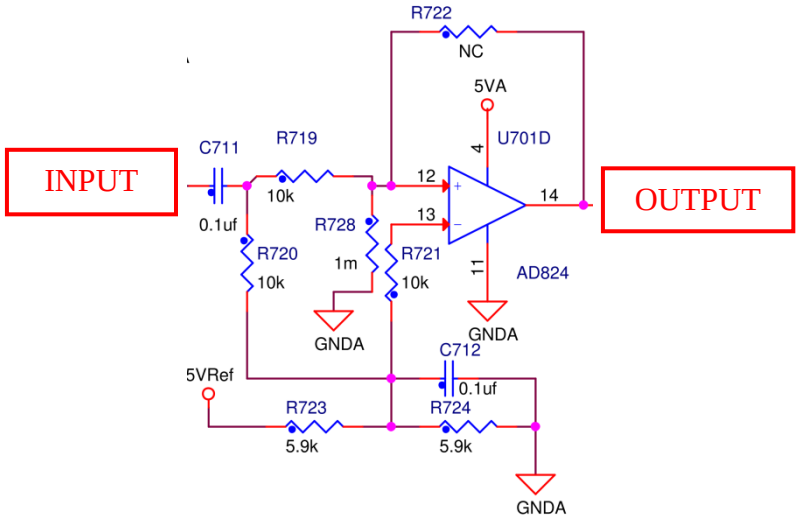

Figure 14. Comparator circuits

The following figure shows the communication wave after comparator circuit.

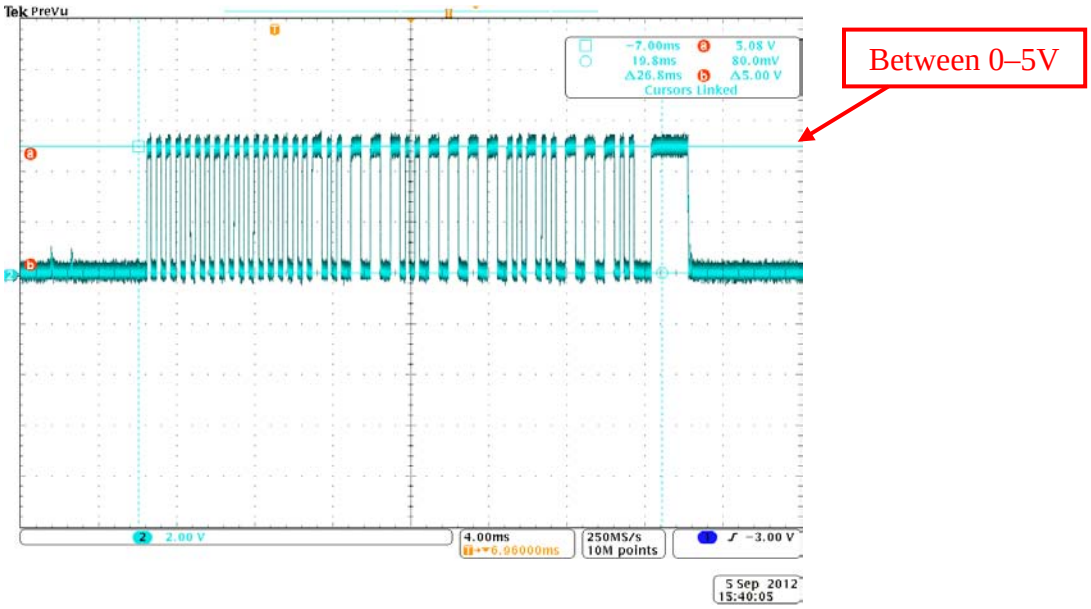

Figure 15. Communication wave after the comparator circuit

3.5 Voltage divider

The voltage divider circuit is shown in Figure 16. The function of this circuit is to make the amplitude of square wave to be 3.3 V for the DSC to detect.

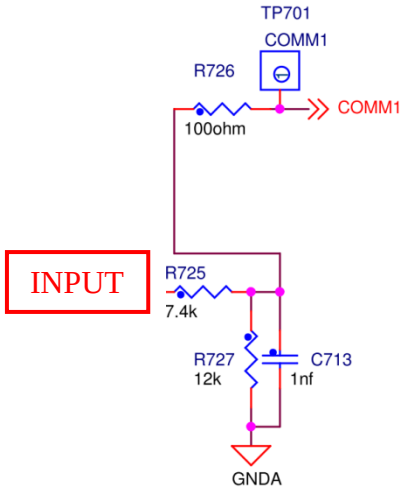

Figure 16. Voltage divider circuit

Figure 17 shows the communication wave after the voltage divider circuit. The output of the circuit is connected to DSC capture input channel.

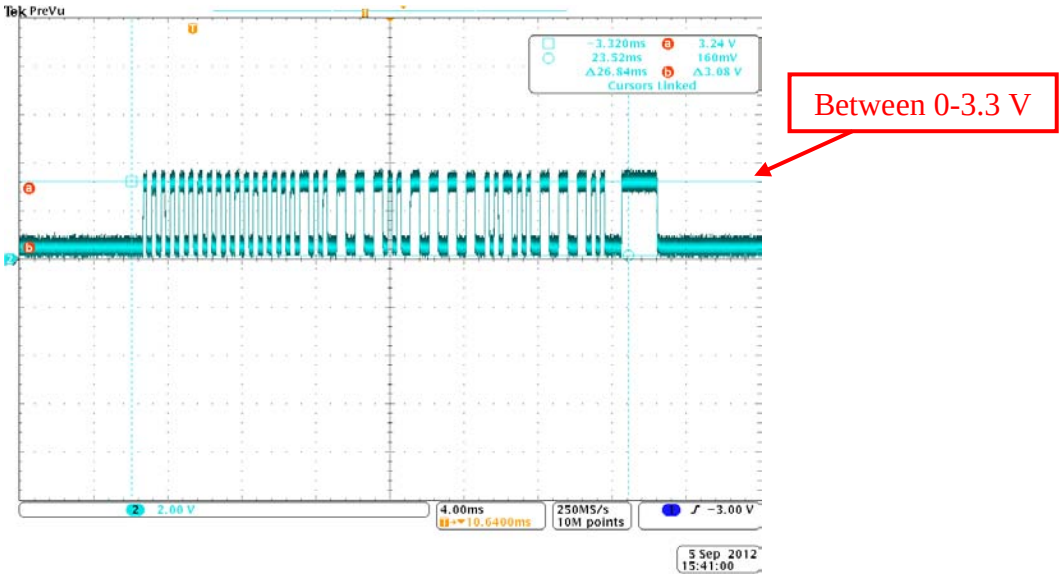

Figure 17. Communication wave after the voltage divider circuit

4 Demodulation software design

The timer module (TMR) of MC56F8006 DSC contains two identical counter/timer groups. Both counters have capture and compare capability. The capture register enables an external signal to take a “snapshot” of the counter’s current value.

Freescale’s Wireless Charger Transmitter uses the capture function of MC568006 DSC DTMR1 to realize the demodulation. The capture register will enable both the rising- and falling-edge trigger mode. When rising or falling edge occurs, the current counter value is triggered to be captured. By calculating the high-level and low-level signal lasting time, the data received can be demodulated.

4.1 Preamble decoding scheme

In the beginning stages of a data packet, there may be some electric level transition lost, so it is critical to find the starting point of a header received. The preamble enables the Power Transmitter to synchronize with the incoming data and accurately detect the start bit of the header. The preamble consists of a minimum of 11 and a maximum of 25 bits, all set to ONE. A ZERO bit received means the end of preamble and the starting bit of the next byte.

Figure 18 shows the preamble decoding flowchart. When the Capture ISR occurs, it will record the capture value and check the receiving mode first. Considering the communication speed to be 2 Kbit/s, the period of a bit is 500 µs; a minimum of 11 and a maximum of 25 bits set to ONE means a minimum of 22 and maximum 50 of 250 µs pulses are captured.

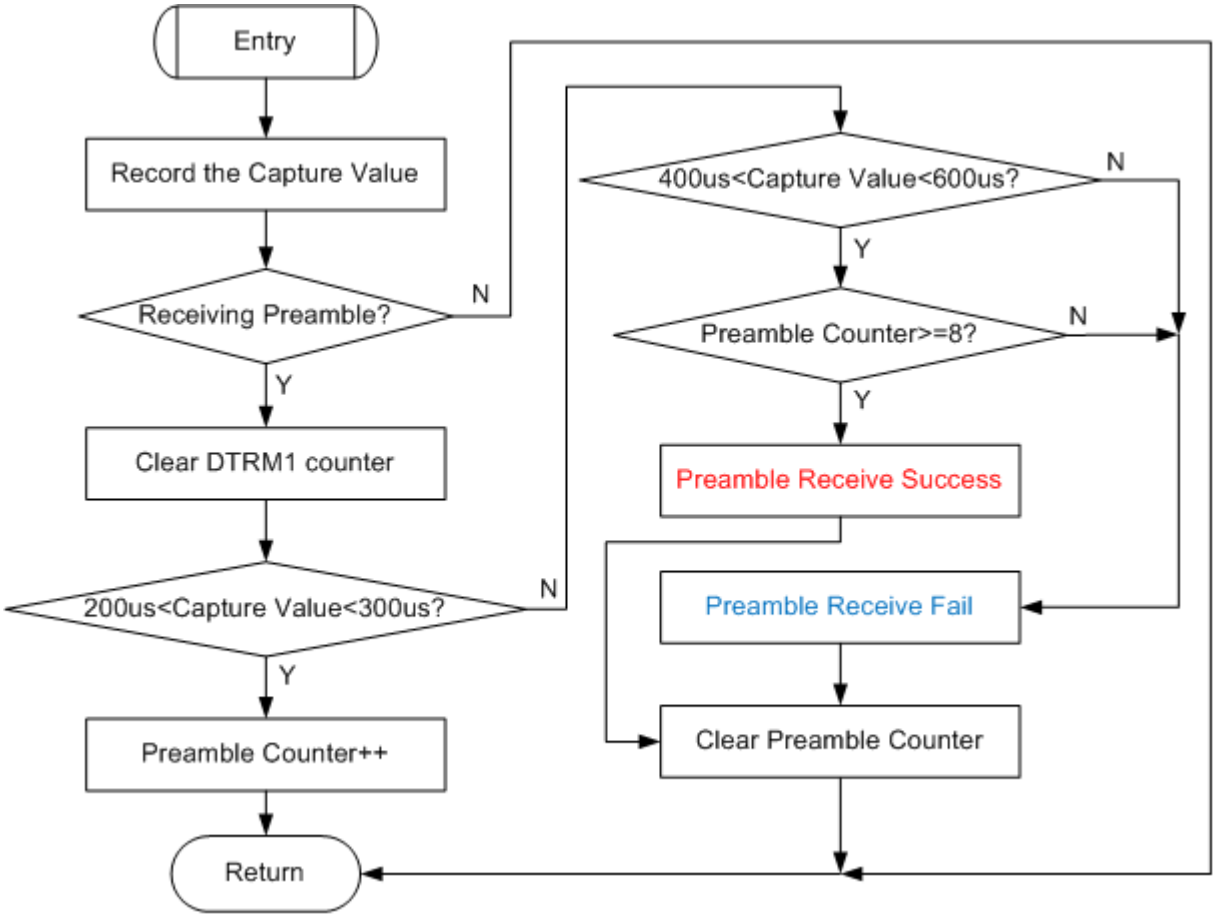

Figure 18. Preamble decoding flowchart

According to the Qi Protocol definition in Byte encoding scheme, the Power Transmitter has detected at least four preamble bits that are followed by a start bit, which means at least eight 250 µs pulses are captured. In order to increase redundancy and reliability, set the half cycle time to be 200–300 µs, and full cycle time to be 400–600 µs.

4.2 Bit decoding scheme

4.2.1 Method 1: Traditional method

After the preamble is successfully received, bit receiving of the following header and data begins. One electrical level transition at half cycle during full cycle means a bit ONE received, or a bit ZERO received. If the electrical level transition is not at half cycle point or full cycle point, the bit receive fails and returns to the initial preamble receiving mode. The following figure shows the bit decoding flowchart of method 1.

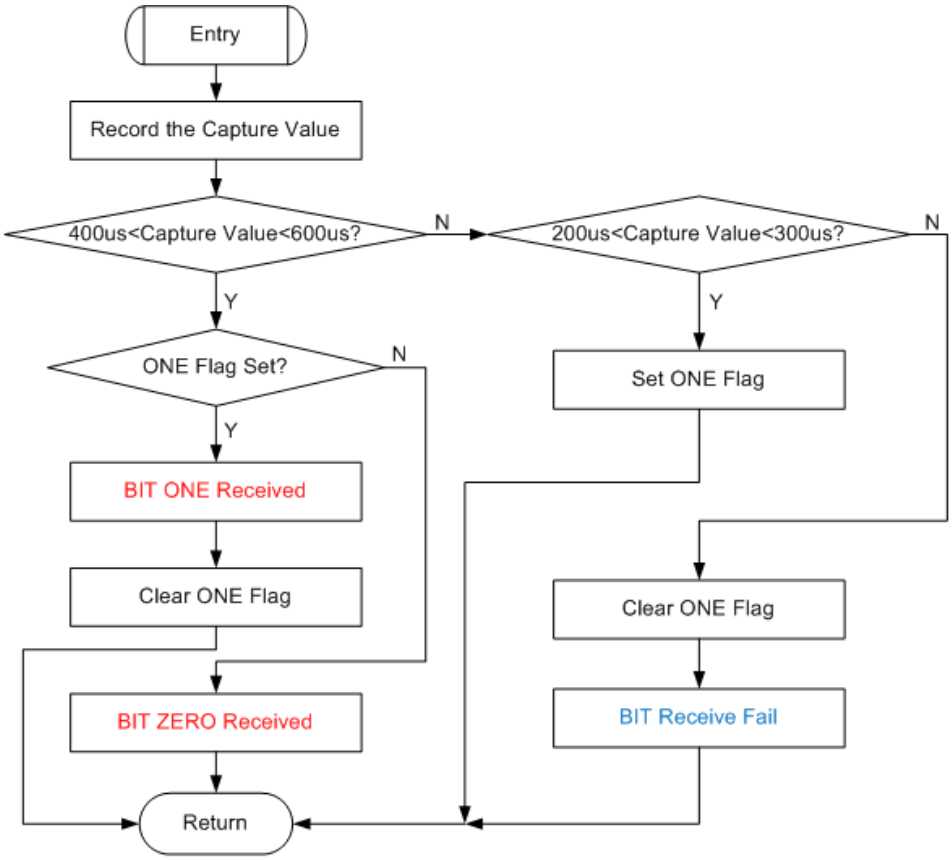

Figure 19. BIT decoding flowchart of method 1

4.2.2 Method 2: Optimized anti-jamming algorithm

In order to improve the communication reliability between the Power Receiver and Transmitter, a new method with optimized anti-jamming algorithm is developed to filter the glitch on the communication wave. The flowchart is shown in the following figure.

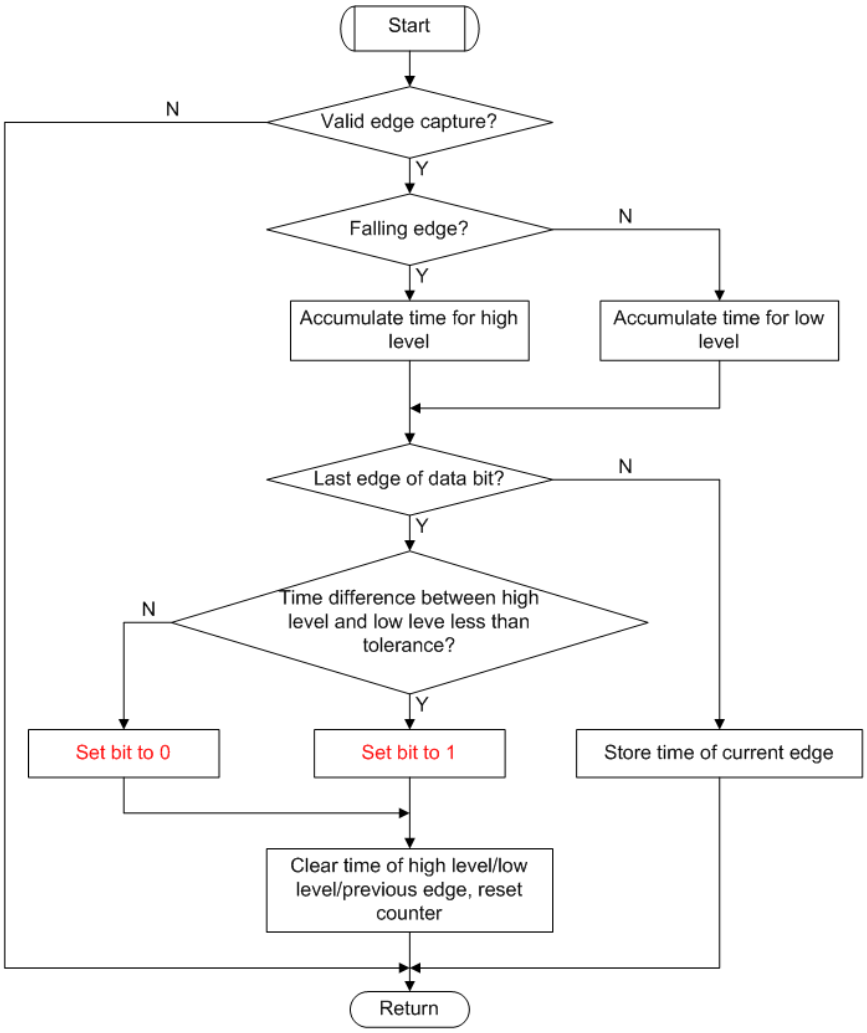

Figure 20. Optimized anti-jamming algorithm flowchart

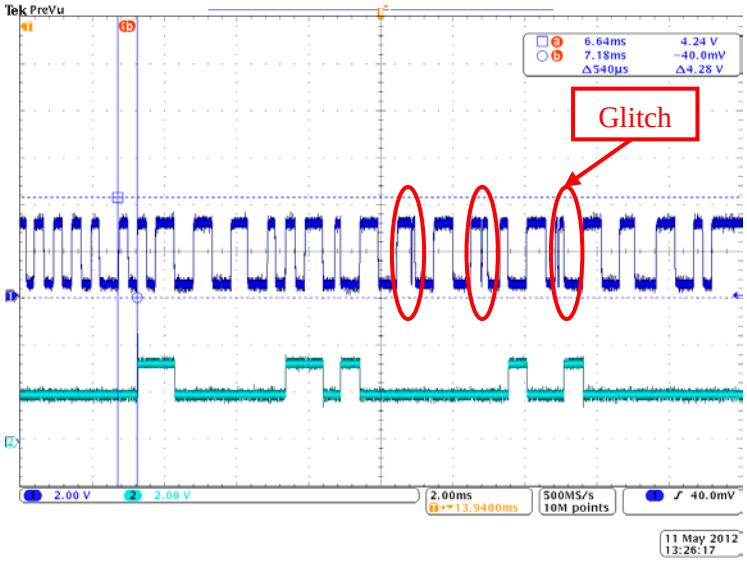

Figure 21. Bit receiving wave with anti-jamming algorithm

As shown in Figure 21, Channel 1 indicates communication wave, and Channel 2 indicates the data bit received by DSC. By using the optimized anti-jamming algorithm in software, the glitch on the communication wave is filtered and the DSC receives the correct data. Thus, the communication system becomes more reliable.

4.3 Byte decoding scheme

Figure 22 shows the byte decoding flowchart. An 11-bit asynchronous serial format is used to transmit a data byte. Each time a bit received success will be stored. After 11 bits received, even check will determine whether the byte received is correct or incorrect. An incorrect byte received will make the state return to initial preamble receiving mode.

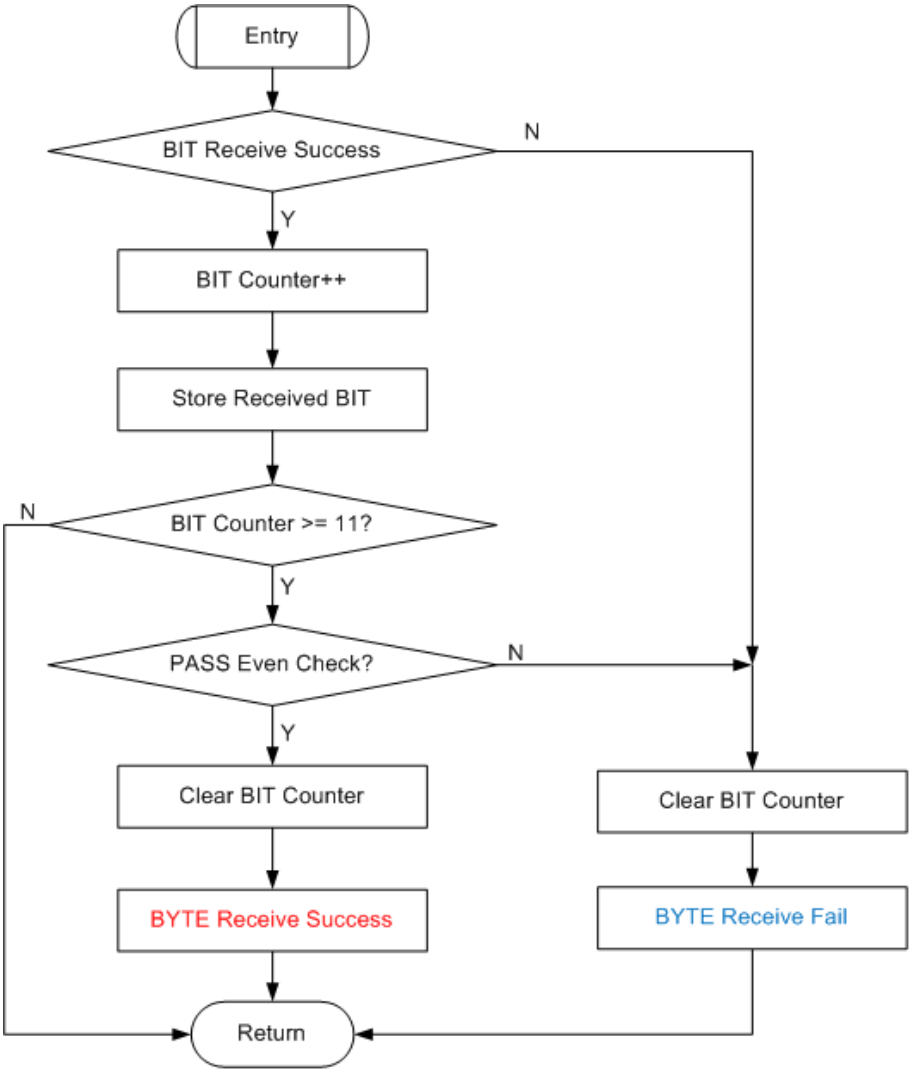

Figure 22. Byte decoding flowchart

4.4 Packet decoding scheme

The header consists of a single byte that indicates the packet type. In addition, the header implicitly provides the size of the message contained in the packet. After the first byte (Header) is successfully received, the length of the packet can be determined.

Figure 23 shows the packet decoding flowchart. When all bytes of the packet have been received, checksum will be calculated to judge whether the packet received is correct or not. If a correct packet is received, packet analysis will start, or the packet will be discarded.

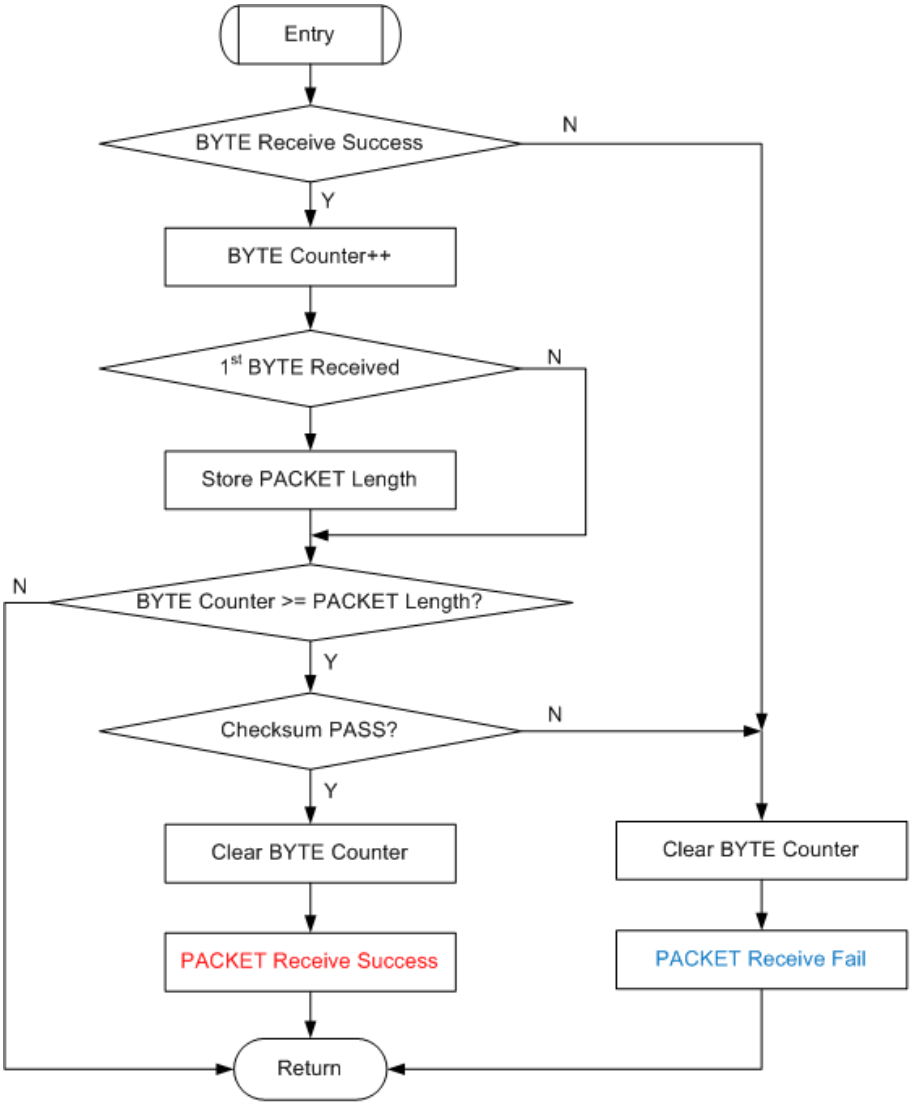

Figure 23. Packet decoding flowchart

4.5 Overtime detection

Overtime detection helps to make the state return to preamble receiving mode when the DTMR1 counter exceeds 800 µs. The compare ISR of DTMR1 is used to realize this function. If the overtime compare event occurs, all the related registers and variables will be cleared. The following figure shows the overtime detection flowchart.

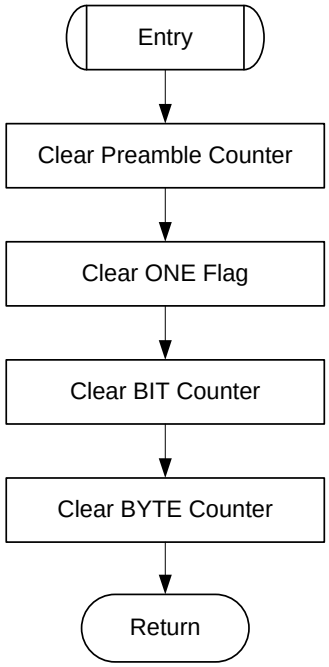

Figure 24. Overtime detection flowchart

5 Test results and conclusion

5.1 Test result

As shown in Figure 25, demodulation circuits correctly demodulate the communication data from the input coil voltage as channel 3. DTM1 module of MC56F8006 DSC analyses the input wave as channel 2, and the correct ONE or ZERO bit information as channel 1.

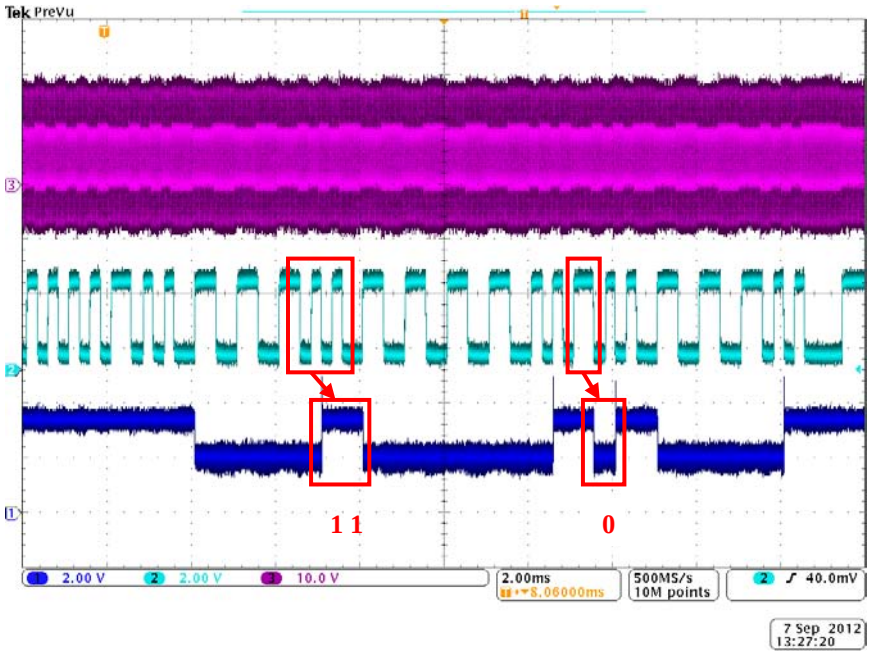

Figure 25. Communication demodulation test wave

The complete packet demodulated by MC56F8006 DSC is shown in Figure 26. This data is obtained from FreeMASTER debugging tools when the system is operating. All the starting packets including Signal Strength Packet, Identification Packet, and Configuration Packet are received correctly according to the Qi protocol.

wRec_byte[3]	0x3	HEX	1000	Current Receive Control Error Packet
wRec_byte[4]	0x0	HEX	1000	
wRec_byte[5]	0x3	HEX	1000	
bStart_Ping_byte[0]	0x1	HEX	1000	
bStart_Ping_byte[1]	0x7c	HEX	1000	Signal Strength Packet
bStart_Ping_byte[2]	0x7d	HEX	1000	
bStart_Ping_byte[3]	0x71	HEX	1000	
bStart_Ping_byte[4]	0x10	HEX	1000	
bStart_Ping_byte[5]	0x0	HEX	1000	
bStart_Ping_byte[6]	0xff	HEX	1000	Identification Packet
bStart_Ping_byte[7]	0x76	HEX	1000	
bStart_Ping_byte[8]	0x54	HEX	1000	
bStart_Ping_byte[9]	0x32	HEX	1000	
bStart_Ping_byte[10]	0x10	HEX	1000	
bStart_Ping_byte[11]	0x9e	HEX	1000	
bStart_Ping_byte[12]	0x51	HEX	1000	
bStart_Ping_byte[13]	0xa	HEX	1000	
bStart_Ping_byte[14]	0x0	HEX	1000	
bStart_Ping_byte[15]	0x0	HEX	1000	Configuration Packet
bStart_Ping_byte[16]	0x0	HEX	1000	
bStart_Ping_byte[17]	0x0	HEX	1000	
bStart_Ping_byte[18]	0x5b	HEX	1000	

Figure 26. Packet demodulation by MC56F8006 DSC

5.2 Conclusion

The low-power wireless charger compliant to the Qi protocol is becoming more common today. Communication signal demodulation strategy is the most critical technology to the charging performance. In this application note, a complete solution to demodulating communication signals from power wave with MC56F8006 DSC is provided, which has high reliability and very low cost. It can be easily used in all Qi-compliant A types and B types low-power wireless chargers with wide input voltage from 5–19 V. The solution could also be easily used for other parts of Freescale DSC family.

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