NXP Semiconductors
Application Note

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Clock calibration

for the dual SOIC 24 V high-side switch family

1 Introduction

This application note describes the clock calibration and how to use a reference time slot of the MC06XS4200, MC10XS4200, MC20XS4200, MC22XS4200, and MC50XS4200 devices. These intelligent high-side switches are designed to be used in 24 V systems such as trucks, busses, and special engines. They can be used in some industrial and 12 V applications as well. The low $R_{DS(on)}$ channels can control incandescent lamps, LEDs, solenoids, or DC motors. Control, device configuration, and diagnostics are performed through a 16-bit SPI interface, allowing easy integration into existing applications. For a complete feature description, refer to the individual data sheets.

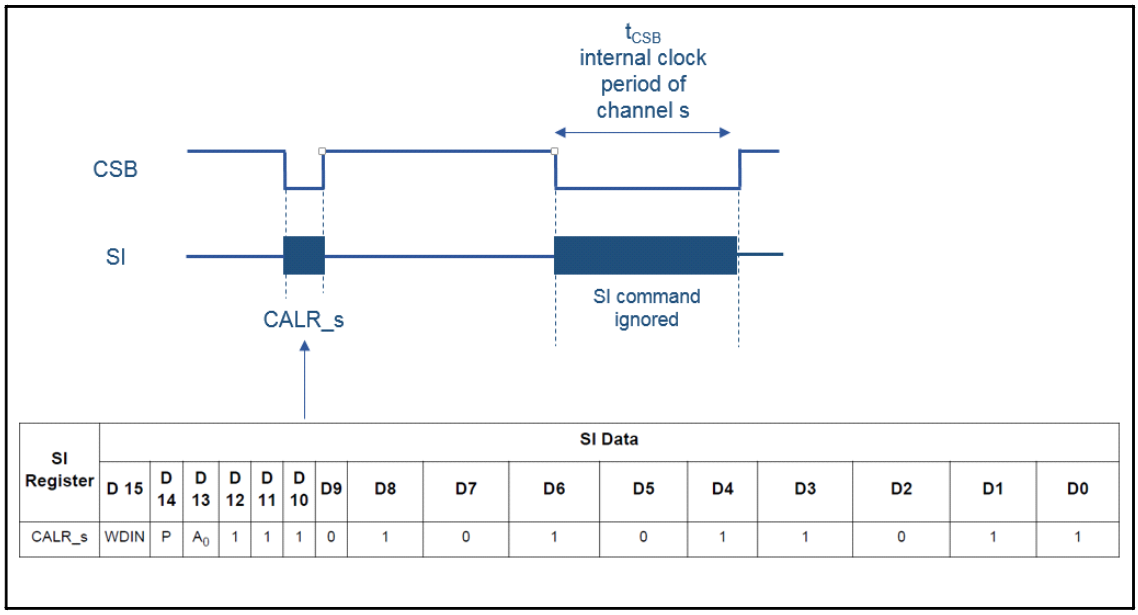
Contents

2 Internal clock calibration

Each channel has a fully independent PWM module activated by setting PWM_en_s. It modulates an internal or external clock signal. Setting Clock_int_s = 1 (bit D6 of the OCR_s register) activates the internal clock, and setting Clock_int_s = 0 activates the external clock. By using a reference time slot (usually available from an external microcontroller), the period of each of the internal PWM clocks can be changed or calibrated.

Calibration of the default period = $1/f_{PWM(0)}$ reduces its maximum variation from about ±30% to ±10%. The programming procedure is as follows:

- Initialization by sending a dedicated word to the SI-CALR register.
- Next, the device sets the new value of the switching period in two steps. First it measures the time elapsed between the first falling edge on the CSB pin and the next rising edge on the CSB pin (t_{CSB}). Then it changes the value of the internal clock period accordingly. The actual value of the channel's switching period is obtained by multiplying the internal clock period by 256.



SI Register	SI Data															
	D 15	D 14	D 13	D 12	D 11	D 10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CALR_s	WDIN	P	A_0	1	1	1	0	1	0	1	0	1	1	0	1	1

Figure 1. Clock calibration sequence

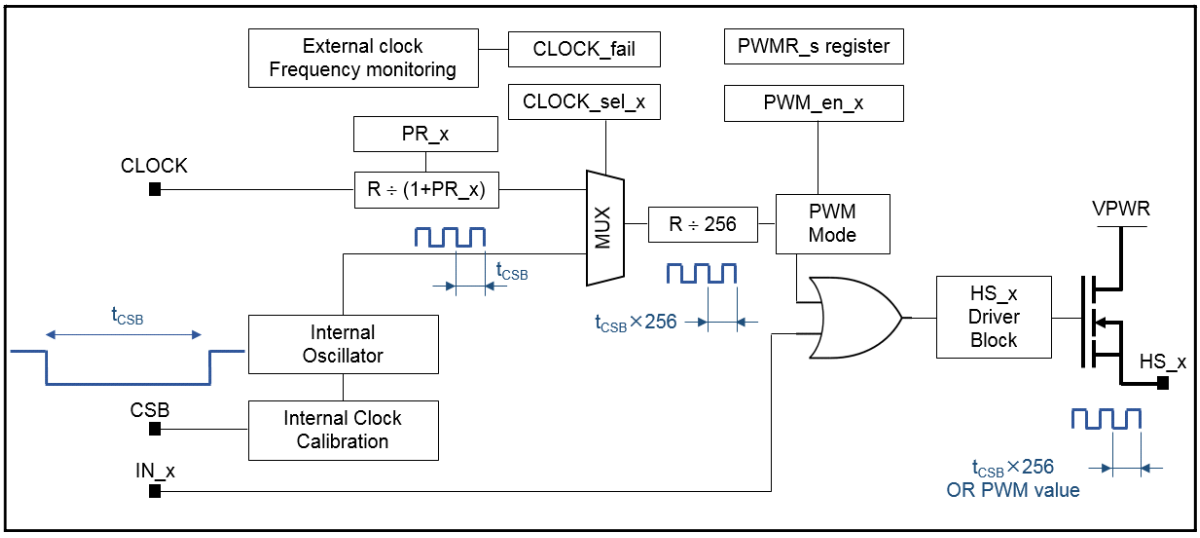


Figure 2. Internal and external clock operation

3 Timing specification

The timing specification related to clock calibration is detailed in Table 5. of each device datasheet. See Reference documents.

Table 1. Calibration timing specification

Minimum required low time during calibration of the internal clock through CSB	$t_{CSB(MIN)}$	1.0	1.5	2.0	µs
Maximum allowed low time during calibration of the internal clock through CSB	$t_{CSB(MAX)}$	70	100	130	µs

Figure 3 provides a description of specified timings converted to frequencies, as well as frequency ranges where the frequency target is preferred.

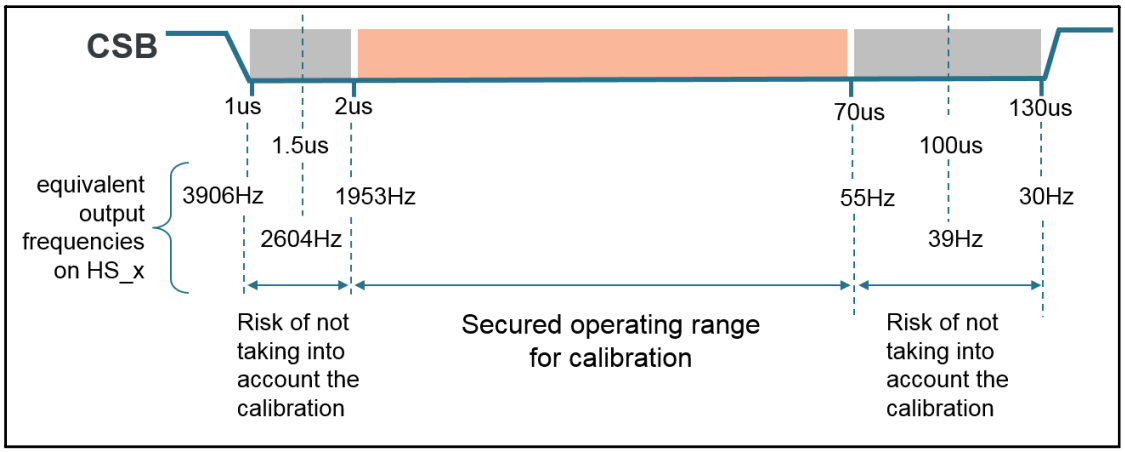


Figure 3. Calibration timing specification

When the duration of the negative CSB pulse is outside a predefined time slot (from $t_{CSB(MIN)}$ to $t_{CSB(MAX)}$), the calibration event is ignored and the internal clock frequency remains unchanged. If the value ($f_{PWM(0)}$) has not been previously calibrated, it remains at its default level.

4 Reference documents

Table 2. AN5108 reference documents

Description	URL
MC06XS4200 Data Sheet	http://www.nxp.com/files/analog/doc/data_sheet/MC06XS4200.pdf
MC10XS4200 Data Sheet	http://www.nxp.com/files/analog/doc/data_sheet/MC10XS4200.pdf
MC20XS4200 Data Sheet	http://www.nxp.com/files/analog/doc/data_sheet/MC20XS4200.pdf
MC22XS4200 Data Sheet	http://www.nxp.com/files/analog/doc/data_sheet/MC22XS4200.pdf
MC50XS4200 Data Sheet	http://www.nxp.com/files/analog/doc/data_sheet/MC50XS4200.pdf

5 Revision history

Revision	Date	Description of changes
1.0	4/2015	Initial release
	7/2016	Updated to NXP document form and style

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