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Application Note

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MPC5777M Hardware Design Guide

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Contents

1 Introduction

The MPC5777M is a multi-core 32-bit microcontroller initially intended for automotive powertrain applications. It contains two e200z7 and one e200z4 Power Architecture® cores running at up to 300 MHz.

This application note details the options of the MPC5777M power supplies and the correct external circuitry required for all of the power supplies, including digital, analog, and SRAM standby. It also discusses configuration options for clock, reset, and ADCs, as well as recommended debug and peripheral communication connections, and other major external hardware required for the device.

The MPC5777M requires multiple external power supply voltages to operate. The main power supplies required are1.3 V for the internal logic and 5 V for the internal regulator and on-chip analog to digital converters. The 5 V supply can also be used to supply pin input and output voltages. The internal regulator generates the 3.3 V required to power the on-chip flash memory. Optionally, 3.3 V can be supplied for the External Bus Interface (EBI), FlexRay, and the JTAG interface input and output voltages. The SRAM has a separate supply input for keep-alive features, if they are required.

2 Overview of MPC5777M package options

The MPC5777M is available in six different package options; three of these are intended for production and three are intended to provide additional features to support debug and calibration.

Table 1. MPC5777M package options

Package	Description
416 BGA PD	Production: Provides access to the primary features of the device, does not include EBI (External Bus Interface)
416 BGA ED	Development: Footprint compatible with the 416 BGA ED package with additional Nexus High Speed Aurora Trace interface and calibration device
512 BGA PD	Production: Superset of 416 BGA PD, with more I/O ports available and EBI
512 BGA ED	Development: Footprint compatible with the 512 BGA ED package with additional Nexus High Speed Aurora Trace interface and calibration device

The decision of which package to use should be based on the number of input/output pins required for the application and the area available for the target system. The following table shows the size differences of the packages. See the device data sheet for complete package dimensions and ball placement. Drawings are also available on the Freescale web site; search for the case outline number shown in Table 2.

Table 2. Package sizes

Package Type	Device Type	Physical Size	Case Outline Number
416TEPBGA	Production	27 x 27 mm	98ARE10523D
416TEPBGA	Emulation	27 x 27mm	98ASA00493D
512TEPBGA	Production & Emulation	25 x 25 mm	98ASA00262D

3 Power supply

MPC5777M microcontrollers include a robust power management infrastructure that enables applications to select among various user modes and to monitor internal voltages for high- and low-voltage conditions. The monitoring capability is also used to ensure supply voltages and internal voltages are within the required ranges before the microcontroller can exit reset.

The MPC5777M MCU supports three different input voltages:

- 1.3V (required) for the internal logic
- 5V (required) for the Power Management controller, I/O, Debug, ADCs and external communication interfaces.It is essential that 5v is applied to the VDD_HV_IO_MAIN supply for the device to exit Reset.
- 3.3V (optional) for FlexRay, I/O, Debug and external communication interfaces

The 3.3 V required for the flash memory is generated by an on-chip regulator. This regulator requires an external decoupling capacitor on VDD_HV_FLA.

3.1 Power supply signals and pins

Table 3 lists all power domains with corresponding pin names.

Table 3. MCU supply pins

Domain name	Supply Voltage	Description
VDD_HV_IO_JTAG	3.3V or 5V	JTAG I/O and oscillator supply
VDD_HV_ADV	5V	High voltage supply for the ADC modules
VDD_HV_ADR_S	5V	Voltage reference of ADC SAR module
VDD_HV_ADR_D	5V	Voltage reference of ADC Σ/Δ module
VDD_HV_PMC	5V	High voltage Power supply for internal power management unit
VDD_HV_IO_MAIN	5V	High voltage Power supply for the I/Os
VDD_HV_FLA[1]	3.3V - Internal Regulator	Decoupling supply pin for Flash voltage regulator
VDD_HV_IO_FLEX	3.3V or 5V	FlexRay & Ethernet 3.3V I/O Supply
VDD_HV_IO_FLEXE	3.3V or 5V	FlexRay & Ethernet &EBI 3.3V I/O Supply
VDD_HV_IO_EBI	3.3V or 5V	
VDD_LV_STBY	1.3V	Buddy device core power supply
VDD_LV	1.3V	Low voltage power supply for the core area
VDD_HV_IO_BD[2]	3.3V or 5V	High voltage Power supply for Buddy device I/O

1. No connection to external supply needed.
2. Only present on the 416ED and 512ED emulation devices

Some of the supplies can be powered with different supply voltages. In particular, the MCU allows flexibility in the supply of voltages that power selected input and output pins (VDD_HV_IO_JTAG). These supplies are "high" supplies and can be connected to either a nominal 3.3 V or 5.0 V supply. See the data sheet for each specific device to learn what voltages can be connected to the power pins, but the generally used voltage is shown in Table 3 and in the figure below.

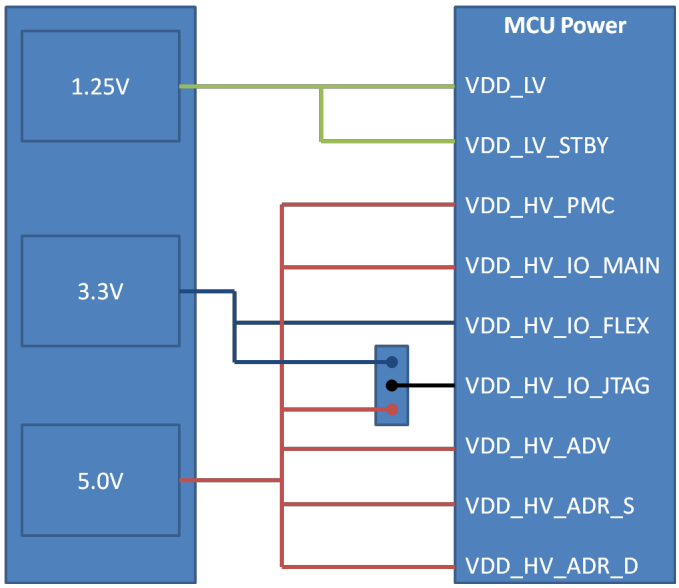

Figure 1. Supply connections overview

The different package options mean that there are a different number of pins/balls available for the power supply, depending on the package. It also means that in some cases, some supplies might not be available. All supply pins/balls that are available on the package should be connected to a supply voltage.

Table 4 shows all power domains and the suggested decoupling and/or filter capacitors for their corresponding pins. These values are provided as a guideline and will vary depending on the application and capability of the power supplies used.

Table 4. Supply pin decoupling caps

Domain name	Supply Voltage	Bulk	Bypass
VDD_HV_IO_JTAG	3.3 V or 5 V	100 nF	1 nF
VDD_HV_IO_BD	3.3 V or 5 V	100 nF	1 nF
VDD_HV_ADV	3.3 V or 5 V	4.7 µF	0.1 µF
VDD_HV_ADR_S	3.3 V or 5 V	100 nF	
VDD_HV_ADR_D	3.3 V or 5 V	100 nF	
VDD_HV_IO_MAIN	5 V	4.7 µF	10 nF[1]
VDD_HV_PMC	5 V	4.7 µF[2]	0.1 µF
VDD_HV_FLA	3.3 V	1.5 µF	
VDD_HV_IO_EBI	3.3 V or 5 V	100 nF	
VDD_HV_IO_FLEX	3.3 V or 5 V	100 nF	
VDD_HV_IO_FLEXE	3.3 V or 5 V	100 nF	
VDD_LV_STBY	1.3 V	100 nF	
VDD_LV	1.3 V	10 µF	47 nF

1. External capacitors for the IO pins are dependent on the application.
2. VDD_HV_PMC pin only present on 416BGA package. On the 512BGA package VDD_HV_PMC is connected to VDD_HV_IO_MAIN. No additional capcitance is required for the 512BGA

3.2 Input and output pins - power supply segmentation

The input and out pins are powered from three domains: VDD_HV_IO_MAIN, VDD_HV_IO_FLEX, and VDD_HV_IO_JTAG. Each I/O pin is associated with one of these three domains. The majority of I/O pins are powered by VDD_HV_IO_MAIN. The VDD_HV_IO_FLEX and VDD_HV_IO_JTAG domains are primarily intended to allow the FlexRay and JTAG interfaces to be operated at a voltage level different from the VDD_HV_IO_MAIN domain. However, they can also be used to provided a limited amount of I/O pins at an alternative voltage level to the main domain.

The voltage level supplied on the I/O domains determins the output voltage level and input transition levels for the I/O pins associated with that domain. The pins that are powered from VDD_HV_IO_JTAG and VDD_HV_IO_FLEX are shown in Table 5. All other I/O pins are supplied from VDD_HV_IO_MAIN.

Table 5. I/O pin power domain association

I/O power domain	I/O pins
VDD_HV_IO_FLEX	PC[10:15] PE[12] PK[14:15] PM[0:8] PM[11]
VDD_HV_IO_FLEXE	PS[0:15] PT[0:15] PY[4]
VDD_HV_IO_EBI	PV[1:15] PW[0:15]
VDD_HV_IO_EBI_CLKOUT	PV[0]
VDD_HV_IO_JTAG	PA[5:9] PA[14] PI[15] PD[6:7] PF[13] PI[14:15]

3.3 Decoupling capacitors layout priorities

When trade offs must be made in the layout, it is important to ensure that the highest priority decoupling capacitors are placed as closely as possible to the MCU. The list below orders the supplies from highest to lowest priority in terms of decoupling capacitor placement.

1. VDD_HV_ADR_S & VDD_HV_ADR_D
2. VDD_HV_ADV
3. VDD_HV_IO_JTAG
4. VDD_LV
5. VDD_HV_IO_BD
6. VDD_HV_PMC
7. VDD_HV_FLA
8. VDD_HV_IO_MAIN
9. VDD_HV_EBI
10. VDD_HV_IO_FLEX
11. VDD_HV_IO_FLEXE
12. VDD_LV_STBY

Highest priority is given to the analog-to-digital converters reference and power supply decoupling: VDD_HV_ADR_S, VDD_HV_ADR_D, and VDD_HV_ADV. Clean supplies are vital to ensure that the highest accuracy is achieved with the ADCs. Next, the supply for the oscillator is prioritized as this helps to ensure reliable and stable operation from the external oscillator.

Medium priority is given to VDD_LV, VDD_HV_IO_BD, VDD_HV_PMC, and VDD_HV_FLA. VDD_LV is the main supply for the on-chip digital logic and this is prioritized as it affects the largest amount of logic on the device. VDD_HV_IO_BD powers the high speed Nexus Aurora pins and noise on this domain would affect the quality of the output. VDD_HV_PMC powers the flash regulator and VDD_HV_FLA is the output of this this regulator. A good supply to the flash memory ensures reliable flash programming and erasing.

VDD_HV_IO_MAIN, VDD_HV_IO_EBI, VDD_IO_FLEX, VDD_IO_FLEXE, and VDD_LV_STBY are given lower priority. Although it is still important that these supplies have a clean power signal, the hardware they power is less affected by noise.

3.4 Supply monitoring

The MPC5777M monitors the voltage supply internally. The function of the power-on reset (POR) and low-voltage detect (LVD) circuits is to hold the device in reset. The device is held in reset regardless of how slow the supply voltage rise is, until the point at which the POR and LVDs are released.

The POR and LVD circuits function correctly even if the input voltage is non monotonic.

For detailed information on the low-voltage detect (LVD) and high-voltage detect (HVD) circuits please refer to the device reference manual.

3.4.1 Behavior of LVD / HVD

The internal LVD circuits monitor when the voltage on the corresponding supply is below defined values and either assert a reset or an interrupt. The LVDs also support hysteresis for the falling and rising trip points.

Although there is an option to disable the LVDs and HVDs following reset, they are capable of being used in a ‘monitor’ only mode and also capable of generating a safe/interrupt event. The LVDs/HVDs can also be configured after device initialization preventing reset to happen when supply crosses the LVD threshold, providing a higher voltage range. An application then verifies that the device remains in the functional range.

NOTE

LVD096 and LVD270 (low range LVDs) cannot be disabled. These modules are used during power-up phase and must ensure that an absolute lowest threshold of operation is never crossed. This is not a guarantee that the device will function down to this level. It is rather a guarantee that the device will recover if this level is crossed.

3.4.2 Power-on reset

The power management controller (PMC) controls the power-on reset ($\overline{\text{PORST}}$) for the MCU. When the critical power supplies are below minimum levels, the MCU is held in the POWER-UP phase of the reset state machine, until the power supplies have reached their specified levels. Power sequencing is not necessary. When the required voltage levels have been reached, the reset generation module (RGM) propagates the device through the next steps of the boot process.

The PMC has two internal power-on reset circuits:

- VPORUPLV monitors the voltage on the 1.3 V input supply. It is monitoring the VDD_LV_CORE pin. The VPORUPLV asserts a reset when the input supply is below defined values.
- VPORUPHV monitors the voltage on the 5.0 V input supply. It is monitoring the VDD_HV_PMC pin. The $\overline{\text{PORST}}$ trip point is high enough to make sure all the LVD circuits are functional.

See the Reset chapter in the reference manual for $\overline{\text{PORST}}$/$\overline{\text{ESR0}}$ pin functionality.

3.4.3 Low-Voltage (LVD) and High-Voltage Detection (HVD)

The internal LVD circuits monitor when the voltage on the corresponding supply is below defined values and either assert a reset or an interrupt. The LVDs also support hysteresis in the falling and rising trip points.

- All LVDs and HVDs are capable of generating either a reset or an interrupt, with the following exceptions:
  - It is not possible to disable the LVD270 and it always generates a reset when triggered (for example, LVD monitoring the high voltage supply input).
  - It is not possible to disable the LVD096 and it always generates a reset when triggered (for example, LVD monitoring the internal core voltage). The LVD096 is integral to the POR management.
- All LVDs and HVDs configured for reset generation cause functional or destructive reset. MC_RGM PHASE0 is not exited until all destructive reset conditions are cleared.
- The appropriate bits in the PMC registers are set by LVD and HVD events.
- LVD and HVD control is protected by the SoC-wide register protection scheme. Therefore, it is configurable as long as the scheme is followed.
- There are user option bits available to allow degrading of "configurable" LVDs/HVDs from destructive down to functional reset. This is a write once mechanism managed by SSCM during device initialization.
- When the LVD or the HVD is enabled for destructive reset generation, then when a trigger event is detected, the external $\overline{\text{PORST}}$ pin is driven low.

The table below lists the LVD and HVD monitors and their characteristics.

Table 6. Voltage monitor electrical characteristics

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
V_{PORUP_LV}[1]	CC	[DST_MEDC18_0291][Covers: ADD14.010]LV supply power on reset threshold[end]	Rising voltage (power up)	1111	-	1235	mV
			Falling voltage (power down)[2]	1015	-	1125	
			[DST_MEDC18_0074] [Covers: ADD14.073]Hysteresis on power-up[end]	50	-	-	
V_{LVD096}	CC	LV internal[3] supply low voltage monitoring	See note [4]	1015	-	1145	mV
V_{LVD108}	CC	Core LV internal[3] supply low voltage monitoring	See note[5]	1150	-	1220	mV
V_{LVD112}	CC	LV external[6] supply low voltage monitoring	See note [3]	1175	-	1235	mV
V_{HVD140}	CC	LV external[7] supply high voltage monitoring	See note [8]	1385	-	1475	mV
V_{HVD145}	CC	LV external[7] supply high voltage reset threshold	-	1430	-	1510	mV
V_{PORUP_HV}[1]	CC	HV supply power on reset threshold[9]	Rising voltage (power up) on PMC/IO Main supply	4040	-	4480[7]	mV
			Rising voltage (power up) on IO JTAG and Osc supply	2730	-	3030	
			Rising voltage (power up) on ADC supply	2870	-	3182	
			Falling voltage (power down)[10]	2850	-	3162	
			Hysteresis on power up[11]	878	-	1630	
V_{POR240}	CC	HV supply power-on reset voltage monitoring	Rising voltage	2420	-	2780	mV
			Falling voltage	2400	-	2760	
V_{LVD270}	CC	HV supply low voltage monitoring	Rising voltage	2750	-	3000	mV
			Falling voltage	2700	-	2950	

Table continues on the next page...

Table 6. Voltage monitor electrical characteristics (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
V_{LVD295}	CC	Flash supply low voltage monitoring	Rising voltage	-	-	3120	mV
			Falling voltage	2920	-	3100	
V_{HVD360}	CC	Flash supply high voltage monitoring	Rising voltage	3435	-	3650	mV
			Falling voltage	3415	-	-	
V_{LVD360}	CC	HV supply low voltage monitoring	Rising voltage	-	-	4000	mV
			Falling voltage	3600	-	3880	
V_{LVD400}	CC	HV supply low voltage monitoring	Rising voltage	4110	-	4410	mV
			Falling voltage	3970	-	4270	
V_{HVD600}	CC	HV supply high voltage monitoring	Rising voltage	5560	-	5960	mV
			Falling voltage	5500	-	5900	
$t_{VDASSERT}$	CC	Voltage detector threshold crossing assertion	-	0.1	-	2	µs
$t_{VDRELEASE}$	CC	Voltage detector threshold crossing de-assertion	-	5	-	20	µs

1. V_{PORUP_LV} and V_{PORUP_HV} threshold are untrimmed values before completion of the power-up sequence. All other LVD/HVD thresholds are provided after trimming.
2. Assume all of LVDs on LV supplies disabled.
3. LV internal supply levels are measured on device internal supply grid after internal voltage drop.
4. LVD is released after tVDRELEASE temporization when upper threshold is crossed, LVD is asserted tVDASSERT after detection when lower threshold is crossed.
5. This specification is driven by LVD108_C. There are additional LVDs on PLL and Flash VDD_LV supply nets which will assert at voltage below LVD108_C.
6. LV external supply levels are measured on the die side of the package bond wire after package voltage drop. This is monitoring external regulator supply voltage and board voltage drop. This does not guarantee device is working down to minimum threshold. For minimum supply, refer to operating condition table.
7. The PMC supply also needs to be below 5472 mV (untrimmed HVD600 mV).
8. HVD is released after tVDRELEASE temporization when lower threshold is crossed, HVD is asserted tVDASSERT after detection when upper threshold is crossed. HVD140 does not cause reset.
9. This supply also needs to be below 5472 mV (untrimmed HVD600 min)
10. Untrimmed LVD300_A will be asserted first on power down.
11. Hysteresis is implemented only between the VDD_HV_IO_MAIN High voltage Supplies and the ADC high voltage supply. When these two supplies are shorted together, the hysteresis is as is shown in Figure 1. If the supplies are not shorted (VDD_IO_MAIN and ADC high voltage supply), then there will be no hysteresis on the high voltage supplies.

NOTE

LVD levels are measured on the die side of the package bond wire. For V_{DD_LV} levels, a maximum of 30 mV IR drop is incurred from the pin to all sinks on the die. For other LVD, the IR drop is estimated by the multiplying the supply current by 0.5 Ω.

3.4.4 Analog module self-test and parameter monitoring

All of the internal Power Management system analog signals can be monitored by the main analog-to-digital converter (ADC): Successive-Approximation-Register ADC B (SARB). The power management reference module provides enough current to fill ADC capacitances without changing values. The minimum resistance for the switches is provided at regulator module.

Figure 2 shows the monitoring implementation. These signals are used for calibration, diagnostics during test or for the user to actively monitor the signal levels. There is a dedicated ADC channel for these monitoring purposes.

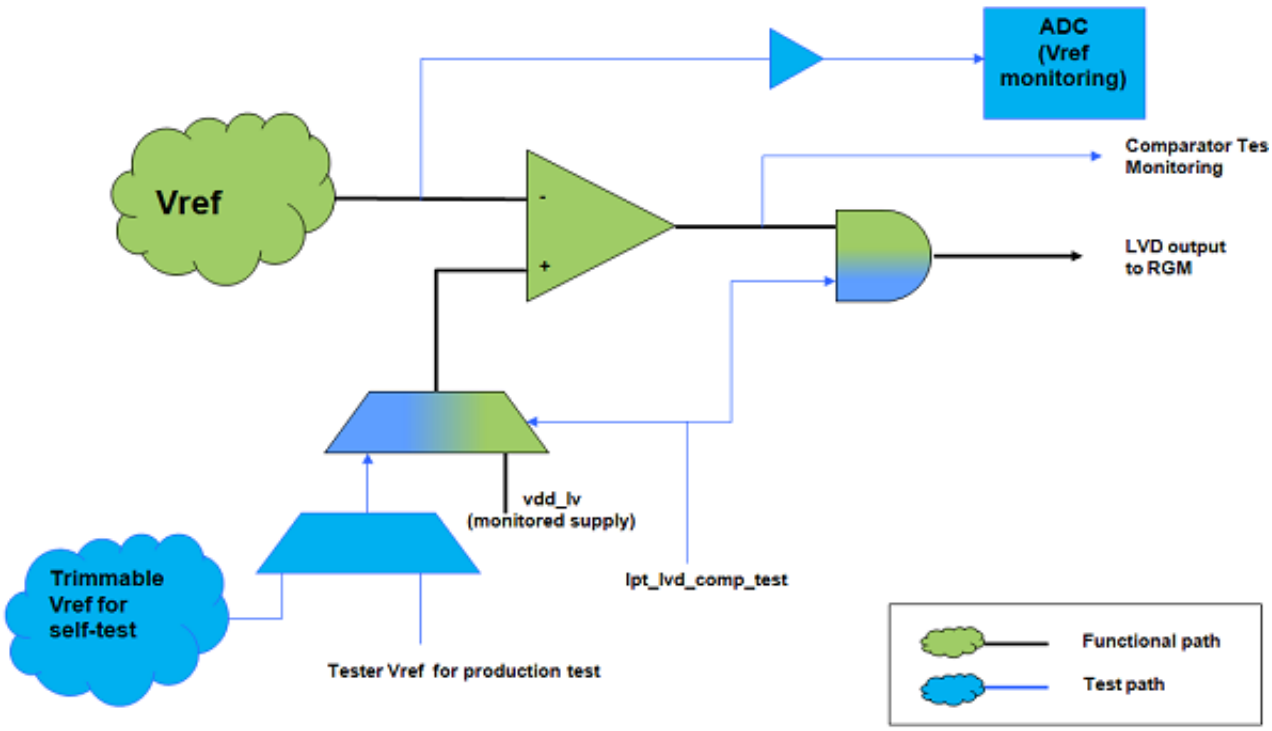

Figure 2. Analog module self-test

The table below lists all the internal test signals that can be monitored using ADC SARB.

Table 7. SARADC_B analog test channel assignment

SARADC_B input channel	Fast SAR	Fast SAR channel	Description
96	—	—	VDD_HV_PMC
97	—	—	VDD_HV_ADV_S
98	—	—	VDD_HV_JTAG_OSC
99	—	—	VDD_HV_FLA
100	—	—	VDD_HV_IO_MAIN
101	—	—	VDD_HV_IO_FLEX
102	—	—	Reserved
103	—	—	VDD_HV_IO_FLEXE
104	—	—	VDD_LV
105	—	—	VDD_HV_IO_EBI
106	—	—	Unbuffered PMC Trim Bandgap Reference (used in PMC)
107	—	—	2nd bandgap (Trimmed), (ADC mode=60, ADC register=35 from power management)
108	—	—	Buffered PMC Trim Bandgap Reference (used in Pad)
109	—	—	VSS_HV_ADV (Ground Supply for ADC)
110	—	—	PMC generic input 0

Table continues on the next page...

Table 7. SARADC_B analog test channel assignment (continued)

SARADC_B input channel	Fast SAR	Fast SAR channel	Description
111	—	—	2nd bandgap (Crude), (ADC mode=59, ADC register=36 from power management)
112	—	—	HV regulator supply LVD falling edge 280_C
113	—	—	HV regulator supply HVD rising edge 600_C
114	—	—	HV flash supply LVD falling edge 280_F
115	—	—	HV flash supply HVD rising edge 360_F
116	—	—	LV core supply LVD falling edge 114_C
117	—	—	LV core supply HVD falling edge 140_C
118	—	—	LV flash supply LVD falling edge 114_F
119	—	—	Reserved
120	—	—	Temperature sensor
121	—	—	ADC bandgap reference
122	—	—	Reserved[1]
123	—	—	Reserved[1]
124	—	—	SAR BIAS 0 — VSS_HV_ADR_S through 20 KΩ source impedance
125	—	—	SAR BIAS 1 — 1/3 (VDD_HV_ADR_S - VSS_HV_ADR_S) through 20 KΩ source impedance
126	—	—	SAR BIAS 2 — 2/3 (VDD_HV_ADR_S - VSS_HV_ADR_S) through 20 KΩ source impedance
127	—	—	SAR BIAS 3 — (VDD_HV_ADR_S - VSS_HV_ADR_S) through 20 KΩ source impedance

1. Channels 122 and 123 are reserved for factory use only.

Using the SARADCB PMC generic input channel 110 the following parameters can be measured.

Table 8. Parameter monitoring via ADC channel

PMC ADC Mode Signal Description	ADC Channel Select Register	ADC Mode Description	Nominal value expected
Internal Voltage	6b101000	Internal Voltage	0.855 V
POR for security	6b000001	Power-On-Reset on LV core supply for security	1.0 V
POR for security	6b011111	Power-On-Reset on LV flash supply for security	1.0 V
LVD096_C	6b011110	Power-On-Reset on LV core supply	See VLVD096 in DS
LVD096_F	6b011101	Power-On-Reset on LV flash supply	See VLVD096 in DS
LVD108_B	6b011100	LVD on Buddy device supply	1.0 V
LVD112_C	6b011011	LVD on Low voltage supply core (cold point)	See LVD112 in DS
LVD108_F	6b011010	LVD on Flash Low voltage supply (hot point)	See VLVD108 in DS

Table continues on the next page...

Table 8. Parameter monitoring via ADC channel (continued)

PMC ADC Mode Signal Description	ADC Channel Select Register	ADC Mode Description	Nominal value expected
LVD108_P	6b011001	LVD on PLL Low voltage supply (hot point)	See VLVD108 in DS
LVD108_C	6b011000	LVD on Low voltage internal supply (hot point)	See VLVD108 in DS
HVD140_C	6b010111	LV Core supply high voltage detector (cold point)	See VHVD140 in DS
HVD145_F	6b111001	Flash LV supply high voltage detector (cold point)	See VHVD145 in DS
HVD145_C	6b111000	LV Core supply 2nd high voltage detector (cold point)	See VHVD145 in DS
Internal POR on HV	6b010101	HV PMC supply power-On-Reset detector	~Supply*1.2/ POR240_Threshold (falling)(See DS VPOR240)
LVD270_C	6b010100	HV PMC supply low voltage detector	LVD270_Threshold (falling) (see VLVD270 in DS
HVD600_C	6b010011	HV PMC supply high voltage detector	~Supply*1.2/ HVD600_Threshold (rising) (See VHVD360 in DS)
LVD270_F	6b010010	HV flash supply low voltage detector	HVD_Threshold (rising)" to "LVD270_Threshold (falling)(see VLVD270 in DS
LVD295_F	6b010001	HV flash supply low voltage detector	HVD_Threshold (rising)" to "LVD295_Threshold (falling) (see VLVD295 in DS
HVD360_F	6b010000	HV flash supply high voltage detector	~Supply*1.2/ HVD360_Threshold (rising) (See VHVD360 in DS)
LVD295_A	6b001111	HV ADC supply low voltage detector	LVD295_Threshold (falling) (see VLVD295 in DS
LVD400_A	6b001110	HV ADC supply low voltage detector	HVD_Threshold (rising)" to LVD400_Threshold (falling)
HVD600_A	6b001101	HV ADC supply high voltage detector	~Supply*1.2/ HVD600_Threshold (rising)
LVD270_IM	6b001100	HV IO main supply low voltage detector	~Supply*1.2/ LVD270_Threshold (falling)
LVD360_IM	6b001011	HV IO main supply low voltage detector	~Supply*1.2/ LVD360_Threshold (falling)

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Table 8. Parameter monitoring via ADC channel (continued)

PMC ADC Mode Signal Description	ADC Channel Select Register	ADC Mode Description	Nominal value expected
LVD400_IM	6b001010	HV IO main supply low voltage detector	~Supply*1.2/ LVD_Threshold (falling)
Internal POR on flash HV	6b001001	HV flash supply power-On-Reset detector	~Supply*1.2/ LVD_Threshold (falling)
LVD270_IF	6b001000	FlexRay I/O supply low voltage detector	~Supply*1.2/ LVD270_Threshold (falling)
LVD270_IJ	6b000110	JTAG I/O supply low voltage detector	~Supply*1.2/ LVD270_Threshold (falling)
LVD270_O	6b000100	Oscillator supply low voltage detector	~Supply*1.2/ LVD270_Threshold (falling)
LVD270_EBI	6b000011	HV IE supply low voltage detector	~Supply*1.2/ LVD270_Threshold (falling)
LVD270_IF2	6b000010	Second FlexRay I/O supply low voltage detector	~Supply*1.2/ LVD270_Threshold (falling)
Normal Operation Mode	6b000000	ADC channel off	—
—	6b111111	Reserved / ADC channel off	—
VDDREG	6b110111	Scaled VDDREG supply	PMC supply x 1/5
VDD ADC	6b110110	Scaled ADC supply	ADC supply x 1/5
VDD Oscillator	6b110101	Scaled Oscillator supply	Oscillator supply x 17/60
VDD Flash	6b110100	Scaled Flash supply	Flash supply (x 17/60)
VDD main I/O	6b110011	Scaled 5V main I/O supply	5V main I/O supply (x 1/5)
VDD Flexray	6b110010	Scaled Flexray supply	Flexray supply x 17/60
VDD Core	6b110001	Core supply hot Sense	Core supply hot Point
VDD PLL	6b110000	PLL supply Sense	PLL supply Sense
VDD EBI	6b101111	Scaled EBI supply	EBI supply x 17/60
VDD Flexray2	6b101110	Scaled 2nd Flexray supply	2nd Flexray supply x 17/60
VDD LFAST PLL	6b101101	LFAST PLL supply	LFAST PLL supply,1.28 V
VDD IJ	6b101100	Scaled Jtag supply	Jtag supply X17/60
LV flash supply sense	6b101011	LV flash supply sense point	LV flash supply sense point
buddy device supply sense	6b101010	Buddy Device supply sense point	Buddy Device supply sense point
LV core supply sense	6b101001	LV core supply cold sense point	LV core supply
internal voltage	6b100000	—	—
Vref0p45	6b010110	LVD/HVD self test voltage	0.47 V
Vref0p75	6b100111	LVD selftest voltage	0.74 V
Vref1p0	6b100110	LVD selftest voltage	1.0 V

Table continues on the next page...

Table 8. Parameter monitoring via ADC channel (continued)

PMC ADC Mode Signal Description	ADC Channel Select Register	ADC Mode Description	Nominal value expected
Vref1p5	6b100101	HVD selftest voltage	1.6 V
VDDA22A	6b111100	pre-regulator output	2.5 V
REF_1P0A	6b111011	1.0 V	1.0 V
VBG_REF_1P22	6b111110	1.2 V crude band gap	1.2 V
BG1P20_REF	6b111010	bandgap trimmed reference voltage	1.2 V
VREF_SOFT	6b000111	reference to 3.3V flash supply regulator	1.2 V
Vbandgap buffered	6b000101	1.2 V	1.2 V
BIS_VBG_REF_1P 22	6b100100	2nd crude band gap	1.20 V
BIS_BG1P20_REF	6b100011	2nd bandgap trimmed reference for flash regulators	1.2 V
Aux Reg REF	6b100010	Reference for Aux regulator	—
REF for LFAST PLL REG	6b100001	Reference to LFAST PLL regulator	1.28 V
—	6b111101	internal voltage	Reserved

3.5 Power sequence

The following section describes the power sequence and the relation between the different supplies during power-up and power-down.

The device is considered to be in a power sequence (or POWERUP state) when the device is either not supplied or is partially supplied. An internal power-on signal is used to identify POWERUP state. This signal is released high on exit of the power sequence. The power-on signal is a combination of LVDs monitoring of supplies:

- VDD_LV
- VDD_HV_PMC
- VDD_HV_IO
- VDD_HV_FLA

The actual threshold use for each LVD depends on the configuration of the device. This is configurable by hardware (flash option bits content) or by software (LVD event configuration through register interface). Once the power-on signal has been asserted, the device configuration is reset to default power-up configuration: during the initialization phase, the device defaults to a pre-determined state for each of the LVDs, HVDs, and the internal regulators. As the flash memory becomes available, the differential read process allows the trimmed data to be available for trimming the internal LVDs, HVDs, and regulators.

3.5.1 Power-up sequence

In this section, the assumption is made that all supplies are low when entering the power-up sequence. Brown-out and power down sequences are specified in the following sections.

At beginning of power-up, the internal power-on signal remains low due to the parasitic diodes. As soon as the minimum threshold is reached on VDD_LV, the power-on signal is forced low. It remains low until the power-up LVDs reach their upper (not trimmed) threshold. During power-up, all functional pins are maintained in a known state as described in the table below.

Table 9. Functional terminals state during power-up and reset

TERMINAL TYPE[1]	POWERUP[2] pad state	RESET pad state	DEFAULT pad state[3]	Comments
PORST	Strong pull-down	Weak pull-down	Weak pull-down	Power-on reset pad
ESR0[5]	Strong pull-down	Strong pull-down	Weak pull-up	Functional reset pad.
ESR1	High impedance	Weak pull-up	Weak pull-up	-
TESTMODE	Weak pull-down	Weak pull-down[6]	Weak pull-down[6]	-
GPIO	Weak pull-up[4]	Weak pull-up	Weak pull-up	-
ANALOG	High impedance	High impedance	High impedance	-
ERROR0	High impedance	High impedance	High impedance	During functional reset, pad state can be overridden by FCCU
JCOMP	High impedance	Weak pull-down	Weak pull-down	-
TCK	High impedance	Weak pull-down	Weak pull-down	-
TMS	High impedance	Weak pull-up	Weak pull-up	-
TDI	High impedance	Weak pull-up	Weak pull-up	-
TDO	High impedance	Weak pull-up	High impedance	-

1. Refer to pinout information for terminal type
2. POWERUP state is guaranteed from VDD_HV_IO>1.1 V and maintained until supply cross the power-on reset threshold: VPORUP_LV for LV supply, VPORUP_HV for high voltage supply.
3. Before software configuration
4. Pull-down and pull-up strength are provided in the MPC5777M Datasheet Pull-up/Pull-down are activated within 2 µs after internal reset has been asserted. Actual pad transition will depend on external capacitance.
5. Unlike ESR0, ESR1 is provided as normal GPIO and implements weak pull-up during power-up.
6. An internal pull-down is implemented on the TESTMODE pin to prevent the device from entering test mode if the package TESTMODE pin is not connected. It is recommended to connect the TESTMODE pin to $V_{SS\_HV\_IO}$ on the board for maximum robustness, but not required. The value of TESTMODE is latched at the negation of reset and has no affect afterward. The device will not exit functional reset with the TESTMODE pin asserted during power-up. The TESTMODE pin can be connected externally directly to ground without any other components.

The power-up sequence is as follows:

1. Digital reset is asserted, ensuring that all modules registers are reset to power-on value.
2. The POWERUP state can be exited when both VDD_LV and VDD_HV are above threshold. The VDD_LV conditions to exit POWERUP is as follows:
   - LVD096_C, LVD096_F upper threshold is crossed
   - LVD112_C upper threshold is crossed
3. After both LV, HV and temperature POWERUP exit conditions have been verified, the internal power-on signal is released to all analog modules.
4. The internal RC oscillator module starts initialization and provides a clock to the system after $\overline{\text{TRCSTARTUP}}$. The PMC digital interface reset is released after two RC clock cycles and LVD400_IM is masked. All other HV LVDs remain active.
5. The device proceeds with the reset sequence through RGM phase PHASE0, PHASE1[DEST], PHASE2[DEST] and PHASE3[DEST].
6. Voltage detector (LVD/HVD) modules are trimmed at the beginning of PHASE3[DEST]. Trimming of LVDs/HVDs is done by the SSCM at low voltage. After trimming is completed, SSCM waits for PMC acknowledge to proceed with the reset sequence.
7. The configurable LVD/HVD modules are optionally enabled at the beginning of PHASE3[DEST]. After trimming, the PMC interface monitors all the HVD/LVD outputs that have been enabled by the flash user option bits. When all enabled LVDs/HVDs are released and the analog temporization period has elapsed, LVDs/HVDs are unmasked.

8. When LVD108_C and LVD360_C are masked, the device relies on the PORST signal to detect a voltage failure during power-up. The device must wait for PORST to be released high before proceeding with power-up sequence. This may increase the amount of time necessary to complete the reset sequence.
9. After all LVDs/HVDs are unmasked the SSCM proceeds with the reset sequence, eventually running full speed accesses to the extended flash option bits required to complete device configuration.
10. The VDD_HV conditions to exit POWERUP are as follows:
    - LVD400_IM upper threshold is crossed
    - LVD360_IM upper threshold is crossed
    - LVD300_F upper threshold is crossed
    - LVD270_xx upper threshold is crossed

3.5.2 Power-down sequence

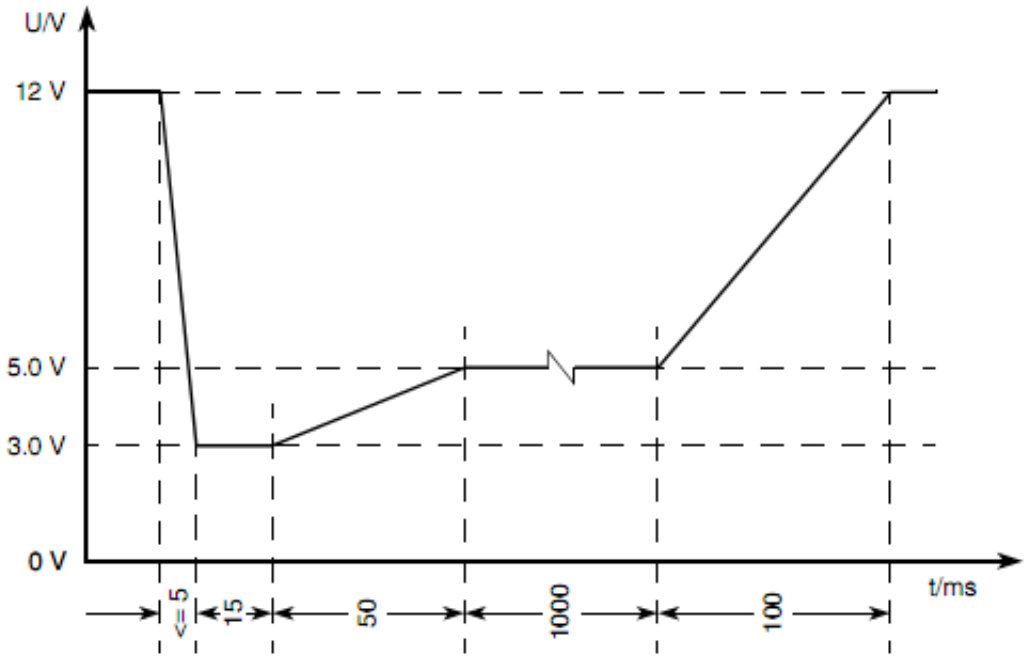
In case the threshold of the higher ranges, LVDs which are configured to generate a destructive reset is crossed, but neither LVD096 nor LVD270 threshold is crossed, device enters the PHASE0 phase. The power-down sequence is entered as soon as the threshold of one of the LVD096 or LVD270 is crossed. The device enters the POWERUP state. The device supplies may then proceed to drop down to ground either through device leakage or external pull-down.

3.5.3 Brown-out management

During brown-out, the MPC57xx devices re-enter the POWERUP phase as soon as the threshold of either LVD096 or LVD270 is crossed.

3.5.4 Low voltage during crank

The device is able to continue operation to the minimum input voltage during cranking. In order to proceed with execution during cranking and prevent device reset, it is important to correctly configure the high voltage LVDs. Figure 3 represents a typical customer application crank profile:



Note: This shows a typical customer crank voltage falling to 3.0 V. However, this is subject to change. See the data sheet for specifics.

Figure 3. Crank voltage application example

- Full parametric operation is a high voltage input between 4.5 V and 5.5 V
- Partial device operation is a voltage between 3.5 V and 4.0 V

4 Clock Circuitry

The MPC5777M devices can use either the on-chip oscillator with an external crystal or an external clock as the reference clock to the device. This reference is qualified in multiple manners before the PLL will begin lock operation. The “pre” FMPLL circuitry consists of an automatic level-controlled amplifier, a comparator, a loss of clock detector, and a predivider.

The most important aspects of an accurate clock source require that some care be taken in the layout and design of the circuitry around the crystal and FMPLL power supplies. Any noise in these circuits can affect the accuracy of the clock source to the FMPLL. The power supply for the PLLs is taken from VDD_LV. The oscillator is powered from VDD_HV_JTAG_OSC. Noise on these supplies can affect the accuracy and jitter performance of the oscillator and PLLs. In order to minimize any potential noise, it is recommended that the additional capacitors recommended in are fitted to the VDD_LV and VDD_HV_JTAG_OSC supplies.

The MPC5777M features configurable internal load capacitors for 20–40 MHz external oscillators (Cx and Cy). This feature is intended to simplify the design and reduce the overall system cost by eliminating external components and reducing the PCB footprint. If an 8–16 MHz oscillator is used, then external load capacitors must be used.

If the external oscillator is to be started by hardware during reset then this requirement, the crystal frequency and the capacitance must be specified in the UTEST Miscellaneous DCF Client records field; see the MPC5777M reference manual for details. An example schematic for the external oscillator connection is shown in the figure below.

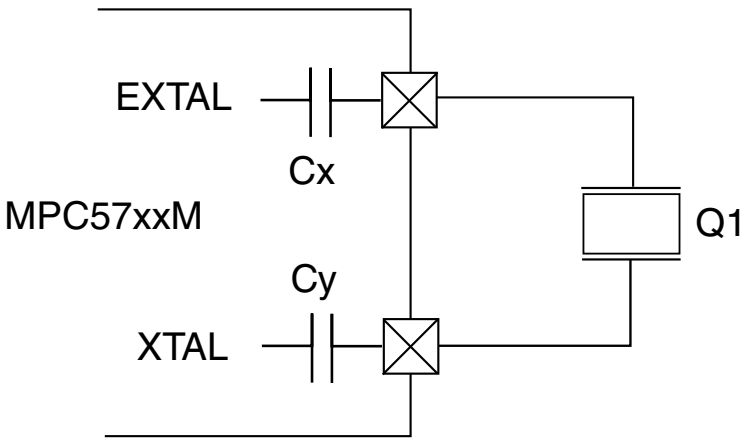


Figure 4. MPC5777M external oscillator connection

Since the layout of the module/board can affect the component values required, customers should have their board characterized by their crystal vendor to recommend values for Cx and Cy. The values shown in this document should be used as a starting point. These should be re-characterized for any change to the oscillator circuit layout, including routing changes of other circuitry near the crystal circuit.

In order to minimize signal degradation and improve Electro Magnetic Compatability (EMC), following guidelines should be followed:

- The oscillator should be placed as close as possible to the MCU.
- The trace lengths of the EXTAL and XTAL crystal connections should be as short as possible.
- The lengths of the EXTAL and XTAL traces should be matched as closely as possible.
- The EXTAL and XTAL traces must be on the same layer.
- Do not allow other signals to cross the Crystal connections.
- Keep high current and high speed signals away from the crystal components.
- The VSS_OSC connection should have its own individual isolated GND area. This can either be on a seperate layer, or as a seperate, segregated region of the GND Layer.
- The VSS_OSC region should be connected to system ground at the the VSS_OSC pin.
- Other than the connections shown in the above schematics, no other connections should be made to the crystal or EXTAL and XTAL device pins. Do not use XTAL to drive any other circuitry.

An example layout and accompanying schematic are shown in the figure below.

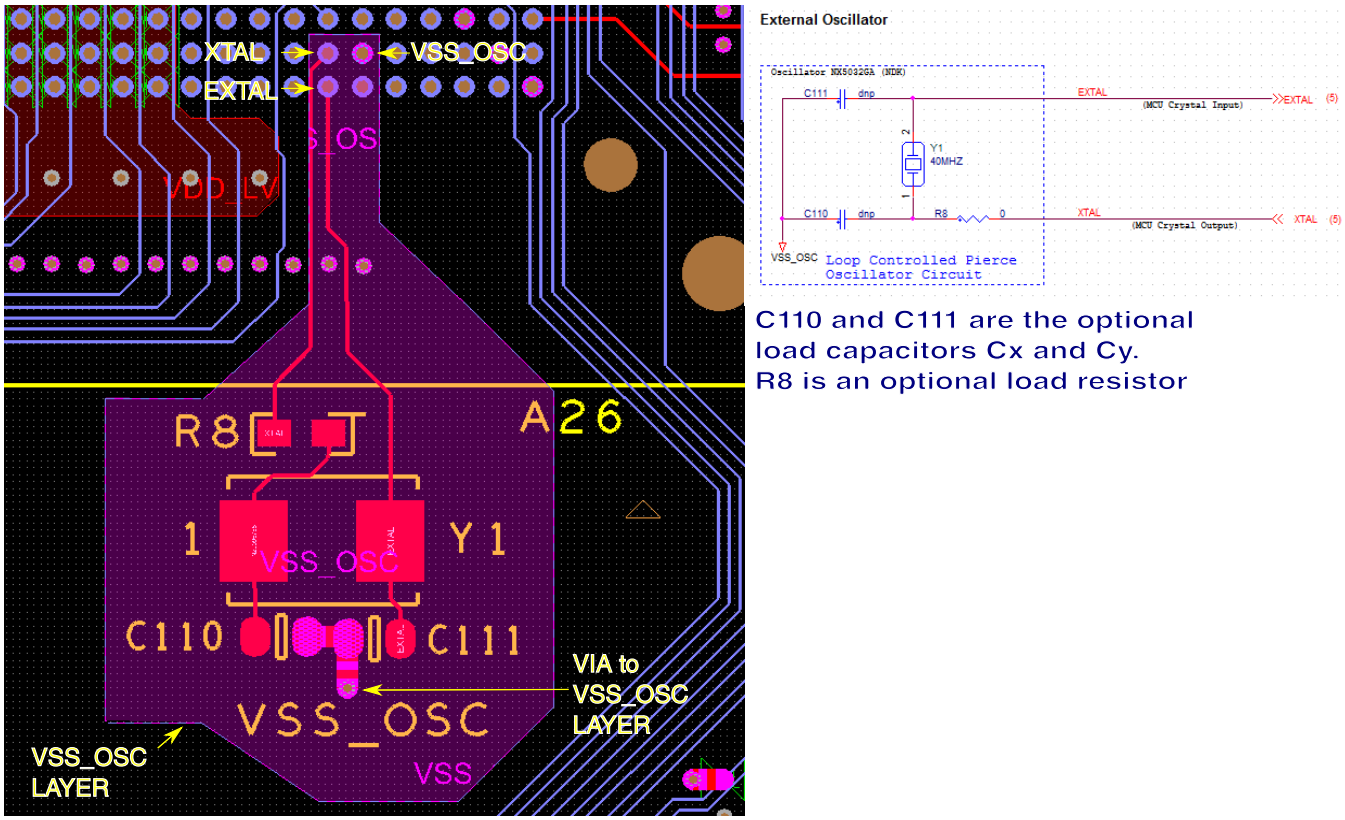


Figure 5. Example crystal layout

The recommendations from the crystal manufacturer will include not only a series resistor value but also the load capacitance required for the crystal (the total crystal load capacitance is usually specified in the crystal data sheet). Keep in mind that the load capacitance is the sum of the following:

- Physical capacitors (Cx and Cy)
- Capacitance of the MCU
- Capacitive loading of the board (CPCB)
- Pin capacitance (CMCU_PIN) of the MCU EXTAL and XTAL balls (BGA balls are specified as 7 pF maximum)

The requirement for the crystal vendor to measure the customer board is due to the board capacitance effect on the crystal load capacitors.

Generally, the method to calculate the capacitors values to use for Cx and Cy is given by the following:

CA = CB = 2 x CL

CA = Cx + Cs_xtal + CPCB

CB = Cy + Cs_xtal + CPCB

CL should come from the crystal specifications (requirements). CPCB should also include any socket capacitance if a socket is used. Cs_xtal is the total on chip stray capacitance on the XTAL/EXTAL pins and is listed in the device data sheet as 8 pF.

4.1 External clock connections

If an external clock is being used as clock reference to the MCU, then the XTAL pin should be connected to ground and the clock should be provided to EXTAL as shown in the figure below.

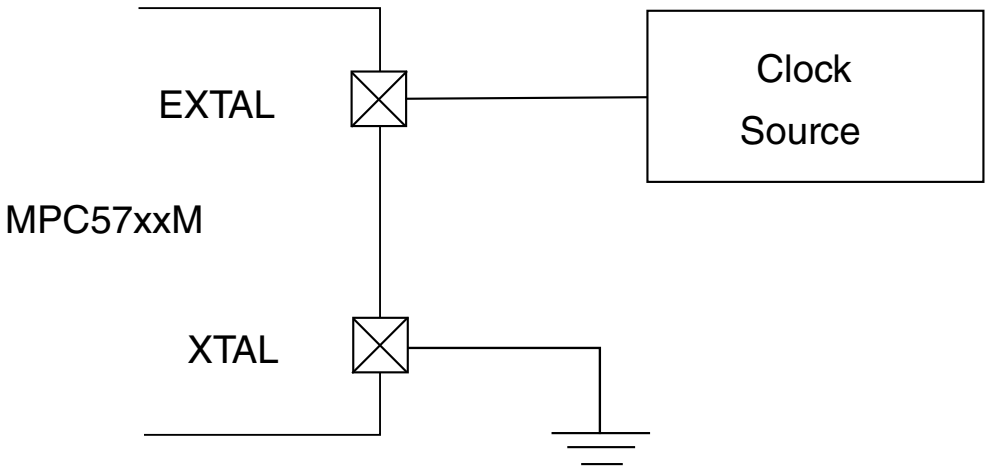


Figure 6. MPC5777M external clock connection

5 Device Reset Configuration

The MPC57xxM MCUs require only very basic external reset circuitry. External circuitry for device configuration is not required. The devices are configured during reset based on data in flash memory.

5.1 External reset signals

The MPC57xxM devices feature two external reset signals:

- Power-on reset (PORST)
- External signal reset (ESR0)

Both external reset signals are bidirectional and active-low. ESR0 indicates if the the device is active (high signal) or in reset. It is thus weak pullup after the reset sequence has completed. If not used, it can be left floating. A falling edge on this pin will trigger a functional reset to the Reset Generation Module. Forcing this pin low will keep the device in the last phase of the reset sequence (Phase3[Functional]).

After reset, PORST is configured as weak pulldown for safety reasons. In case PORST is disconnected the device will remain in reset. PORST is released when the device leaves the power-up state of the RGM. PORST has to be forced high externally so the device will leave the reset state. The internal weak pulldown of PORST is max 100 µA. It is recommended to use an external 4.7 kΩ pullup resistor to ensure remaining safely above the threshold.

6 Recommended debug connectors and connector pinout definitions

The MPC57xxM family implements the newly added (in the IEEE-ISTO 5001™-2011 version of the standard) high speed serial Nexus trace Auxiliary Port that uses the Xilinx™ Aurora physical interface. The Aurora interface allows the Nexus protocol information to be transmitted serially at a high date rate over one or more Aurora lanes. The Aurora protocol handles the encoding of the data and stripes the information across the number of lanes available on the device.

In addition to the high speed Nexus serial trace port, a new option is added in the MPC57xxM family devices to support a high speed calibration interface for run control and memory access: a High Speed Calibration interface based on JTAG and LFAST. The High Speed Calibration LFAST interface signals are alternate functions on the JTAG pins of the device. The device will start up in JTAG mode and the tool can request that the JTAG interface transitions to the High Speed Calibration LFAST interface.

This section gives recommendations for connections and pinouts of the available debug interfaces. For additional information on the MPC57xxM debug connector options and signal descriptions, see application note AN4225, "MPC57xxM C55 Family Debug Overview" available in freescale.com

Table 10 shows the recommended connectors for different applications for the MPC57xxM Family.

Table 10. Recommended connectors

Connector style	Target system part number	Connector type
14-pin BERG JTAG only	3M 2514-6002UB	JTAG-only configuration[1]
10-pin calibration connector	Samtec TFM-105	See separate High Speed Calibration LFAST interface custom connector documentation.
17-position (2 × 17, 34-pin) Samtec	Samtec ASP-137973-01	Serial Nexus configuration (supports up to 8 simplex lanes, less lanes are available if duplex support or High Speed Calibration LFAST interface support is required)

1. The existing MPC5500 and MPC5600 JTAG connector will be used on future MPC57xx devices.

NOTE

Whichever connector is chosen, "keep-out" areas may be required by some tools. Consult the preferred tool vendor to determine any area that must remain clear around the debug connector. Some tool vendors may include an extension cable to minimize "keep-out" areas, but use of an extension will degrade the signal. In many cases, this degradation will be insignificant, but it depends on many factors including clock frequency and target board layout.

6.1 MPC57xx JTAG connector

Table 11 shows the pinout of the recommended JTAG connector to support the MPC57xxM devices. This is an alternate JTAG only connector. It is not ideal for signal placement for ribbon cable used to support the High Speed Calibration LFAST interface.

The recommended connector for the target system is Tyco part number 2514-6002UB.

NOTE

This pinout is similar to the previous Freescale MPC5500/MPC5600 family of devices. The differences are noted below. The MPC5500/MPC5600 family did not have a calibration option.

Table 11. Recommended JTAG connector pinout

Description	Pin	Pin	Description
TDI	1	2	GND
TDO	3	4	GND
TCK	5	6	GND

Table continues on the next page...

Table 11. Recommended JTAG connector pinout (continued)

Description	Pin	Pin	Description
$\overline{\text{EVTI0}}$	7	8	$\overline{\text{PORST}}$[1]
$\overline{\text{ESR0}}$[2]	9	10	TMS
VREF	11	12	GND
$\overline{\text{EVTO0}}$	13	14	JCOMP

1. This pin was a no connect on the MPC55xx and MPC56xx devices.
2. Early versions of this document put the $\overline{\text{PORST}}$ signal on this pin. $\overline{\text{PORST}}$ and $\overline{\text{ESR0}}$ have been swapped to make it more backward compatible.

6.2 MPC5777M high-speed Nexus serial trace connector

For high speed Nexus Aurora trace applications, the Samtec™ ERF8 Series connector is recommended in the IEEE-ISTO 5001™-2011 standard. For the MPC57xx family, the 17 position (34 pins) connector is recommended. The part number of the Samtec connectors are shown in Table 12.

Table 12. Recommended high-speed serial trace connector part numbers

Connector	Part number (Samtec)	Style	Description
HS34	ASP-137973-01	Samtec ERF8 Series, 17 position by 2 row	Vertical mount for MCU module
HS34	TBD	Samtec ERF8 Series, 17 position by 2 row	Right Angle mount for MCU module

The Samtec ERF8 series of connectors is intended for high speed applications requiring a minimum footprint size with a reliable, latching connection. The recommended connector has two rows of seventeen contacts each with a spacing of 0.8 mm. The connector provides isolation between the high-speed trace signals and the low-speed JTAG and control signals. It also provides ample ground connections to ensure signal integrity. If at all possible, the connector should be placed onto the target system with the even numbered pins nearest the edge of the printed circuit board.

Figure 7 is courtesy of Samtec U.S.A (http://www.samtec.com/search/NEXUS.aspx).

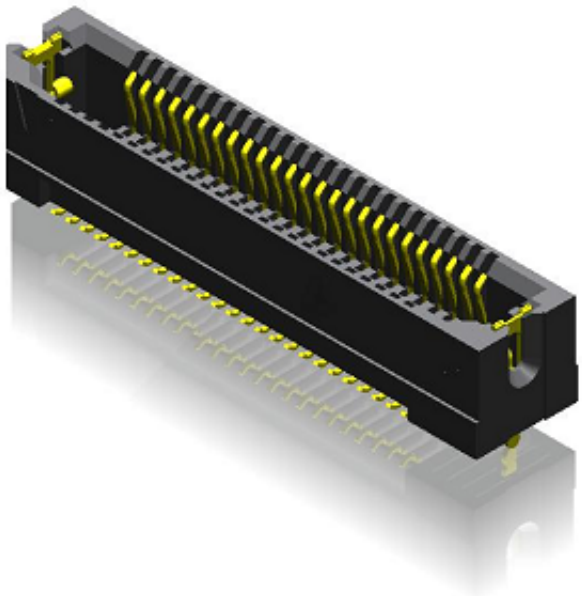


Figure 7. Recommended Nexus connector

The table below shows the recommended pinout for the Samtec connector.

Table 13. MPC5777M high-speed serial trace connector

Function	Pin No	Pin No	Function
TX0+	1	2	VREF
TX0-	3	4	TCK/TCKC/DRCLK
VSS	5	6	TMS/TMSC/TxDataP
TX1+	7	8	TDI/TxDataN
TX1-	9	10	TDO/RxDataP
VSS	11	12	JCOMP/RxDataN
TX2+	13	14	$\overline{\text{EVTI1}}$
TX2-	15	16	$\overline{\text{EVTI0}}$
VSS	17	18	$\overline{\text{EVTO0}}$
TX3+	19	20	$\overline{\text{PORST}}$
TX3-	21	22	$\overline{\text{ESR0}}$
VSS	23	24	VSS
(TX4+)	25	26	CLK+
(TX4-)[1]	27	28	CLK-
VSS	29	30	VSS
(TX5+)[1]	31	32	$\overline{\text{EVTO1}}$
(TX5-)[1]	33	34	N/C
VSS	GND	GND	VSS

1. Reserved for TXn signals, not currently used.

It is recommended that the "even" side of the connector be mounted closer to the edge of the printed circuit board to facilitate a direct connection to the tool.

6.3 Nexus Aurora target system requirements

The Nexus Aurora interface requires termination and AC coupling of the signals between the target system and the tool. The termination resistor for the Aurora clock is located inside the MCU. An external termination resistor is required. The transmit termination resistor must be implemented in the target system; however, it may be implemented internal to the FPGA of the tool.

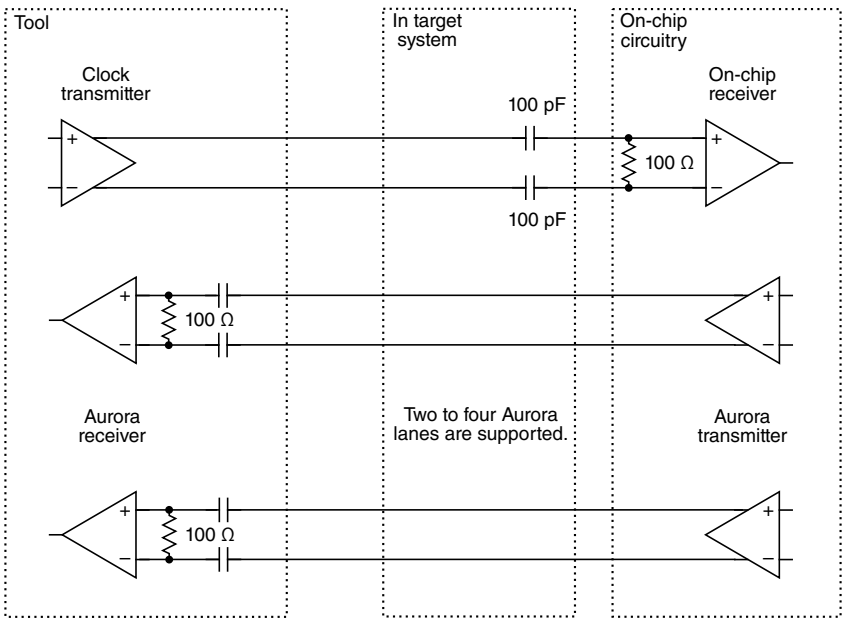


Figure 8. Nexus Aurora termination and coupling circuits

6.4 Minimum external circuitry

Next to the connector, additional circuitry is required for the Nexus/JTAG debug circuitry. The MPC57xx devices include internal pull devices that ensure the pins remain in a safe state; however, if there is additional circuitry connected to the Nexus/JTAG pins, or long traces that could be affected by other signals (due to crosstalk from high-current or high-speed signals), a minimum number of external pull resistors can be added to ensure proper operation under all conditions.

Table 14. Optional external pullups/downs

Nexus/JTAG signal	Resistor/capacitor direction and value	Description
JCOMP	10 kΩ pulldown	Holds debug port in reset and prevents any debug commands from interfering with the normal operation of the MCU
$\overline{\text{PORST}}$	4.7 kΩ pullup	The $\overline{\text{PORST}}$ input should be driven from an open collector output; therefore, it requires a pull-up resistor for the MCU
$\overline{\text{ESR0}}$	4.7 kΩ pullup	The $\overline{\text{ESR0}}$ input should be driven from an open collector output; therefore, it requires a pull-up resistor for the MCU

Table continues on the next page...

Table 14. Optional external pullups/downs (continued)

Nexus/JTAG signal	Resistor/capacitor direction and value	Description
Nexus CLKP & CLKN	100 nF on the signal lines	The LVDS Nexus clock signals require a capacitor for high speed functionality
$\overline{\text{EVTI}}$	10 kΩ pullup	A pullup resistor prevents debug mode from being forced after reset if debug mode is enabled (JCOMP = high). It also prevents breakpoints from being forced if debug mode is enabled. **NOTE:** In almost all situations, a resistor is not required on this signal.

In addition to the pullup and pulldown resistors, some systems may want to use buffers between the JTAG connector inputs (JCOMP, TDI, TDO, TMS, EVTI, EVTO, PORST, and ESR0) and the MCU. This will prevent over-voltage conditions from causing damage to the MCU signals. Normal systems should not require this circuitry, but it is helpful in systems that can be exposed to improper connections that provide voltages that are outside the operating conditions of the MCU. A common circuit to use is the Texas Instruments™ SN74CBTLV38615. This device is a bus switch that implements a bidirectional interface between two terminals with less than 5 Ω of resistance. It should be powered by the same supply that powers the debug port. The device enable should be connected to ground for the interface to be enabled whenever the debug port on the MCU is powered. This circuit provides a high impedance to the tool when the debug port is powered off.

7 External Bus Interface (EBI)

The External Bus Interface (EBI) handles the transfer of information between the internal busses and the memories or peripherals in the external address space. The EBI includes a memory controller that generates interface signals to support a variety of external memories. This includes Single Data Rate (SDR) synchronus burst mode flash and SRAM, and asynchronous/legacy memories FLASH and SRAM. It supports 3 regions (via chip selects), each with its own programmed attributes.

The EBI has the following features. For detailed information please see the MPC5777M reference manual.

- 32-Bit address bus with transfer size indication.
- 32-Bit Data bus (16-bit Data Bus Mode also supported)
- Memory controller with support for various memory types:
- synchronous burst SDR flash and SRAM
- asynchronous/legacy flash and SRAM
- Burst support (wrapped only)
- Port size configuration per chip select (16 or 32 bits)
- Support for Dynamic Calibration with up to 3 chip-selects
- Four Write/Byte Enable (WE[0:3]/BE [0:3]) signals
- Slower-speed clock modes
- Stop and Module Disable Modes for power savings
- Optional automatic CLKOUT gating to save power and reduce EMI
- Misaligned access support
- Compatible with MPC5xx
- Compatible with MPC5xx external bus (with some limitations)

The EBI signal properties are shown in Table 14. The assosciated pad configuration settings for MPC5777M are shown in the table below.

Table 15. Signal properties

Name	I/O Type	Function	Pull[1]
ADDR[8:31] ADDR[8:11]_WE[3:0]/BE[3:0]	I/O	Address bus	-
$\overline{\text{BDIP}}$	Output	Burst Data in Progress	Up
CLKOUT[2]	Output	Clockout	-
$\overline{\text{CS}}$[0:2]	Output	Chip Selects	-
DATA[0:31]	I/O	Data bus[3]	-
OE	Output	Output Enable	Up
RD_$\overline{\text{WR}}$	I/O	Read_Write	Up
TS	I/O	Transfer Start	Up

1. This column shows which signals require a weak pullup or pulldown. The EBI block does not contain these pullup/pulldown devices within the block. They are assumed to be in another module of the MCU (for example; pads module).
2. The CLKOUT signal is driven by the System Clock Block outside the EBI.
3. In Address/Data multiplexing modes, Data will also show the address during the address phase.

Table 16. EBI pads configuration

Pin	MSCR	Function	Description	BGA416	BGA512
PV[0]	289	CLKOUT	EBI Clock Output	AA26	AG30
PV[1]	290	/OE	EBI Output Enable Signal	AA24	AF30
PV[2]	291	RD_WR	EBI Read_Write Enable Output	AA23	AF29
PV[3]	292	/CS2	EBI Chip Select 2 Output	Y24	AE30
PV[4]	293	/CS1	EBI Chip Select 1 Output	Y25	AE29
PV[5]	294	/CS0	EBI Chip Select 0 Output	Y26	AD30
PV[7]	296	/TS	EBI Transfer Start Output	W24	AD29
PS[0]	257	D30	EBI Data[30] Signal	AD18	AJ12
PS[1]	258	D29	EBI Data[29] Signal	AE18	AK12
PS[2]	259	D28	EBI Data[28] Signal	AF18	AJ13
PS[3]	260	D26	EBI Data[26] Signal	AD19	AK13
PS[4]	261	D24	EBI Data[24] Signal	AE19	AJ14
PS[5]	262	D23	EBI Data[23] Signal	AF19	AK14
PS[6]	263	D20	EBI Data[20] Signal	AD20	AJ15
PS[7]	264	D16	EBI Data[16] Signal	AE20	AK15
PS[8]	265	D31	EBI Data[31] Signal (LSB)	AF20	AJ16
PS[9]	266	D27	EBI Data[27] Signal	AD21	AK16
PS[10]	267	D21	EBI Data[21] Signal	AE21	AJ17
PS[11]	268	D25	EBI Data[25] Signal	AF21	AK17
PS[12]	269	D19	EBI Data[19] Signal	AD22	AJ18
PS[13]	270	D22	EBI Data[22] Signal	AE22	AK18
PS[14]	271	D18	EBI Data[18] Signal	AD23	AJ19
PS[15]	272	D17	EBI Data[17] Signal	AE23	AK19

Table continues on the next page...

Table 16. EBI pads configuration (continued)

PT[0]	273	D14	EBI Data[14] Signal	AF22	AJ21
PT[1]	274	D11	EBI Data[11] Signal	AF23	AK21
PT[2]	275	D12	EBI Data[12] Signal	AB24	AJ22
PT[3]	276	D15	EBI Data[15] Signal	AC24	AK22
PT[4]	277	D8	EBI Data[8] Signal	AD24	AJ23
PT[5]	278	D13	EBI Data[13] Signal	AE24	AK23
PT[6]	279	D4	EBI Data[4] Signal	AF24	AJ24
PT[7]	280	D7	EBI Data[7] Signal	AB25	AK24
PT[8]	281	D3	EBI Data[3] Signal	AC25	AJ25
PT[9]	282	D0	EBI Data[0] Signal (MSB)	AD25	AK25
PT[10]	283	D5	EBI Data[5] Signal	AE25	AJ26
PT[11]	284	D10	EBI Data[10] Signal	AF25	AK26
PT[12]	285	D9	EBI Data[9] Signal	AB26	AJ27
PT[13]	286	D2	EBI Data[2] Signal	AC26	AK27
PT[14]	287	D1	EBI Data[1] Signal	AD26	AJ28
PT[15]	288	D6	EBI Data[6] Signal	AE26	AK28
PV[10]	299	A10_WE2	EBI Address 10 (MSB)	V24	AB29
PV[11]	300	A11_WE3	EBI Address 11	V25	AB30
PV[12]	301	A12	EBI Address 12 Output Signal	V26	AA29
PV[13]	302	A14	EBI Address 14 Output Signal	U24	AA30
PV[14]	303	A13	EBI Address 13 Output Signal	U25	Y29
PV[15]	304	A15	EBI Address 15 Output Signal	U26	Y30
PW[0]	305	A20	EBI Address 20 Output Signal	U23	U29
PW[1]	306	A16	EBI Address 16 Output Signal	T24	U30
PW[2]	307	A17	EBI Address 17 Output Signal	T25	T29
PW[3]	308	A18	EBI Address 18 Output Signal	T26	T30
PW[4]	309	A22	EBI Address 22 Output Signal	R24	R29
PW[5]	310	A19	EBI Address 19 Output Signal	R25	R30
PW[6]	311	A26	EBI Address 26 Output Signal	R26	P29
PW[7]	312	A23	EBI Address 23 Output Signal	P24	P30
PW[8]	313	A21	EBI Address 21 Output Signal	P25	N29
PW[9]	314	A25	EBI Address 25 Output Signal	P26	N30
PW[10]	315	A27	EBI Address 27 Output Signal	N23	M29
PW[11]	316	A28	EBI Address 28 Output Signal	N24	M30
PW[12]	317	A30	EBI Address 30 Output Signal	N25	L29
PW[13]	318	A29	EBI Address 29 Output Signal	N26	L30
PW[14]	319	A31	EBI Address 31 (LSB) Output	M24	K29
PW[15]	320	A24	EBI Address 24 Output Signal	M25	K30

8 Example of Communication Peripheral Connections

There are a wide range of peripheral pins available on the MCU. Many of these have fairly standard definitions for their use. This section provides example connections for some of the most commonly used communications peripherals, such as LIN, CAN, FlexRay, and RS-232 communication interfaces.

8.1 Example RS232 interface

The RS-232 (TIA/EIA-232-F) standard is a fairly common interface that was once available on nearly all computers. While this interface is disappearing, adapters are available to allow the use of RS-232 peripherals though other interfaces, such as USB. RS-232 was intended to be a very low-cost, low-performance interface. This interface was originally specified with signal voltages of +12 V and –12 V, typically. However, this has been lowered to a typical minimum voltage of +5 V and –5 V in recent years.

Figure 9 and Table 17 show the typical connections between the serial port of an MCU and the MAX3232-EP RS-232D transceiver from Texas Instruments (http://www.ti.com/). The transceiver operates from either a 3.3 V or a 5 V supply and includes two charge pumps to generate the output voltages that are required. This device contains two transmit drivers and two receivers. The charge pumps require four external capacitors.

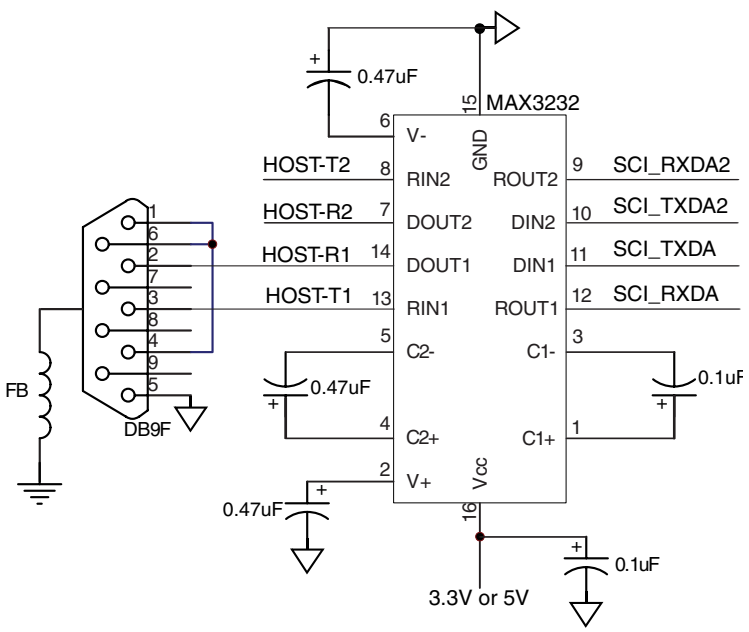


Figure 9. Typical SCI to RS232 circuit

NOTE

The commercial grade MAX3232 device is not rated for the full automotive temperature of –40 to +125° C and is not intended for automotive applications. This circuit should not be used or populated in a production module intended for automotive use. However, in many cases, the RS-232 interface is intended only as a development interface; therefore, the commercial device can be used for prototyping purposes. Texas Instruments does offer a device option with an operating temperature range of –40 to +85° C. Texas Instruments has an enhanced version of the device, MAX3232-EP, that is intended for

aerospace, medical, and defense applications. This version is available with an operating temperature range of –55 to +125° C.

Table 17. Typical RS-232D connector definition

Pin number	Description
1	Connect to pin 4 and 6
2	RS-232 TX (Transmit)
3	RS-232 RX (Receive)
4	Connect to pin 1 and 6
5	GND
6	Connect to pin 1 and 4
7	N/C
8	N/C
9	N/C

NOTE

N/C pins are not connected. The shell of the connector should be connected through a ferrite bead to ground.

8.2 Example LIN interface

Local Interconnect Network (LIN) is a commonly used low-speed network interface that consists of a master node communicating with multiple remote slave nodes. Only a single wire is required for communication and is commonly included in the vehicle wiring harness. Figure 10 shows a typical interface implemented using the Freescale MC33661 LIN transceiver.

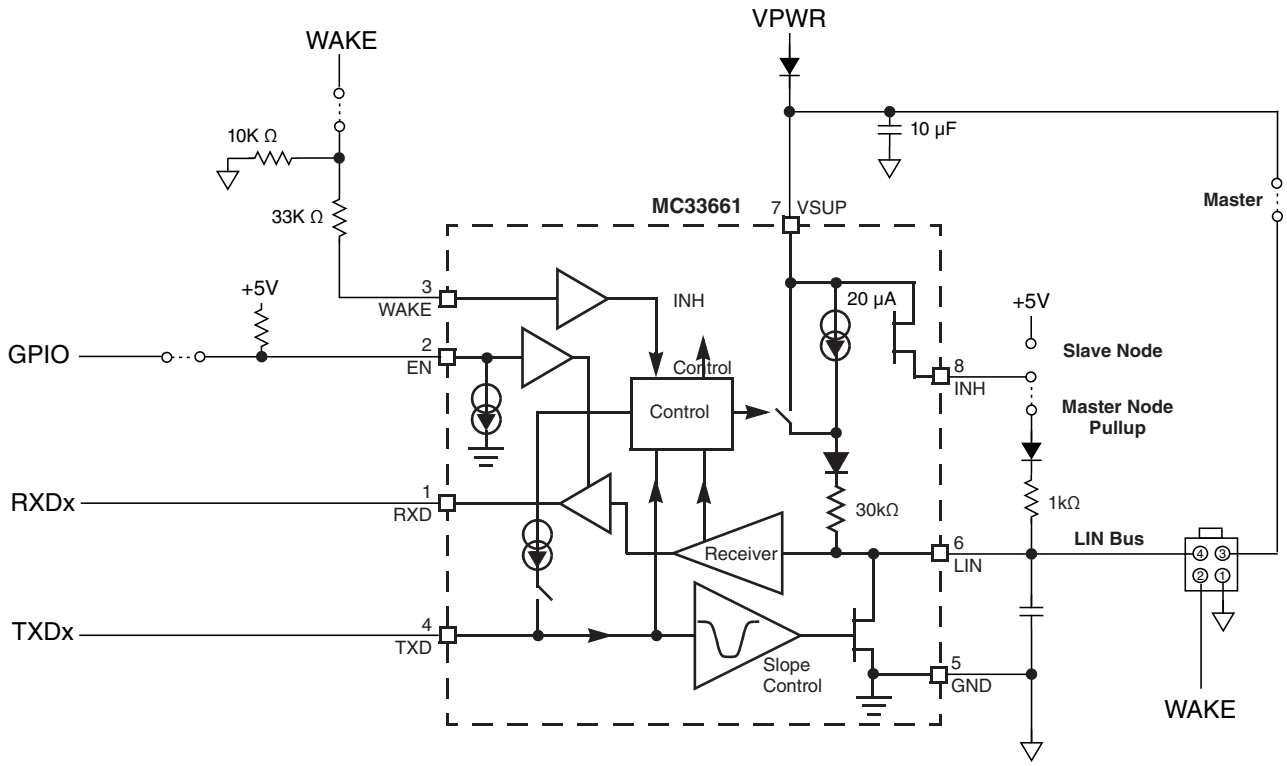


Figure 10. Typical LIN connections

Table 18 below shows the pins of the MC33661 and their typical connections to an MCU.

Table 18. MC33661 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	RXD	Output	Receive Data Output	MCU LIN RXD	LIN Receive Data Output to the MCU
2	EN	Input	Enable Control	MCU GPIO	Enables operation of the device
3	Wake	Input	Wake Input	LIN Bus Wake[1]	Wake enables the devices out of sleep mode
4	TXD	Input	Transmit Data Input	MCU LIN TXD	LIN Transmit Data Input from the MCU
5	GND	Input	Ground	System Ground Reference	Device ground reference
6	LIN	Input/Output	LIN Bus	LIN bus	Bidirectional pin that represents the single-wire transmit and receiver
7	VSUP	Input	Power Supply	Protected battery voltage	This is the power supply for the device and is typically connected to a nominal 12 V

Table continues on the next page...

Table 18. MC33661 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
8	INH	Output	Inhibit Output	LIN Bus (if master)	The Inhibit pin controls either an external regulator to turn on a slave node or is connected through a resistor to the LIN bus on master nodes

1. Wake is an optional signal on the LIN connector, but may come directly from a switch.

There is not a standard industry-defined LIN connector. Freescale uses a 4-pin Molex® connector that allows for the the LIN bus pin, a power supply source (VPWR), a wakeup signal, and a ground reference. Slave nodes will often implement two connectors to allow a daisy-chain of multiple nodes to be easily implemented. Table 19 shows the Freescale pinout.

Table 19. LIN connector pinout recommendation

Function	Pin number	Pin number	Function
LIN Bus	4	3	VPWR
Wake	2	1	Ground

In a typical system, these pins would be used as follows:

- LIN bus—This is the single-wire LIN bus that connects between the master LIN node and the slave LIN nodes.
- VPWR—This connector input can be used as the power input to a slave node. Care should be taken that sufficient current is available for the total number of LIN slaves that are powered through this connection. In some systems, this may come from the master LIN node.
- Wake—The Wake signal is typically used for each individual slave node to enable the LIN physical interface of that node and to consequently enable the power supply (using the INH output) to power up the MCU to perform some action. For example, when the handle on a car door is lifted, to turn on the MCU that controls a function inside the vehicle, such as powering a smart dome light or enabling the controls of a smart seat.
- Ground—Ground reference for the module.

Parts numbers for the 4-pin Molex Mini-Fit Jr.™ connector are shown in Table 20.

Table 20. Recommended connector part numbers

Description	Manufacturer part number (Molex)
4-pin right-angle connector with flange for target system, tin contacts, with latch	39-29-1048
4-pin right-angle connector with pegs for target system, tin contacts, with latch	39-30-1040
4-pin vertical connector with pegs for target system, tin contacts, with latch	39-29-9042
4-pin right-angle connector with flange for target system, gold contacts, latch	39-29-5043
Mating connector with latch for cable assemblies	39-01-2040
Female terminal for mating cable assembly	39-00-0077

8.3 FlexRay Interface Circuitry using TJA1080A

FlexRay is an automotive fault-tolerant 2-wire communications interface. FlexRay is generally used at 10,000 Kbit/s (10 Mbit/s).

Freescale FlexRay devices implement a bus driver interface compliant with Communications System Electrical Physical Layer Specification, Version 2.1 Rev A.

Typically, FlexRay bus data rates of 10 Mbit/s, 8 Mbit/s, 5 Mbit/s, and 2.5 Mbit/s are supported and although the logic portions of the interface are implemented in the device, an external physical interface device is required to allow multiple FlexRay modules to be connected together.

The NXP™ (http://www.nxp.com) TJA1080A device is typically used as the FlexRay transceiver, although others are available. One transceiver is required for each FlexRay channel. The figure below shows the typical connections using the TJA1080A.

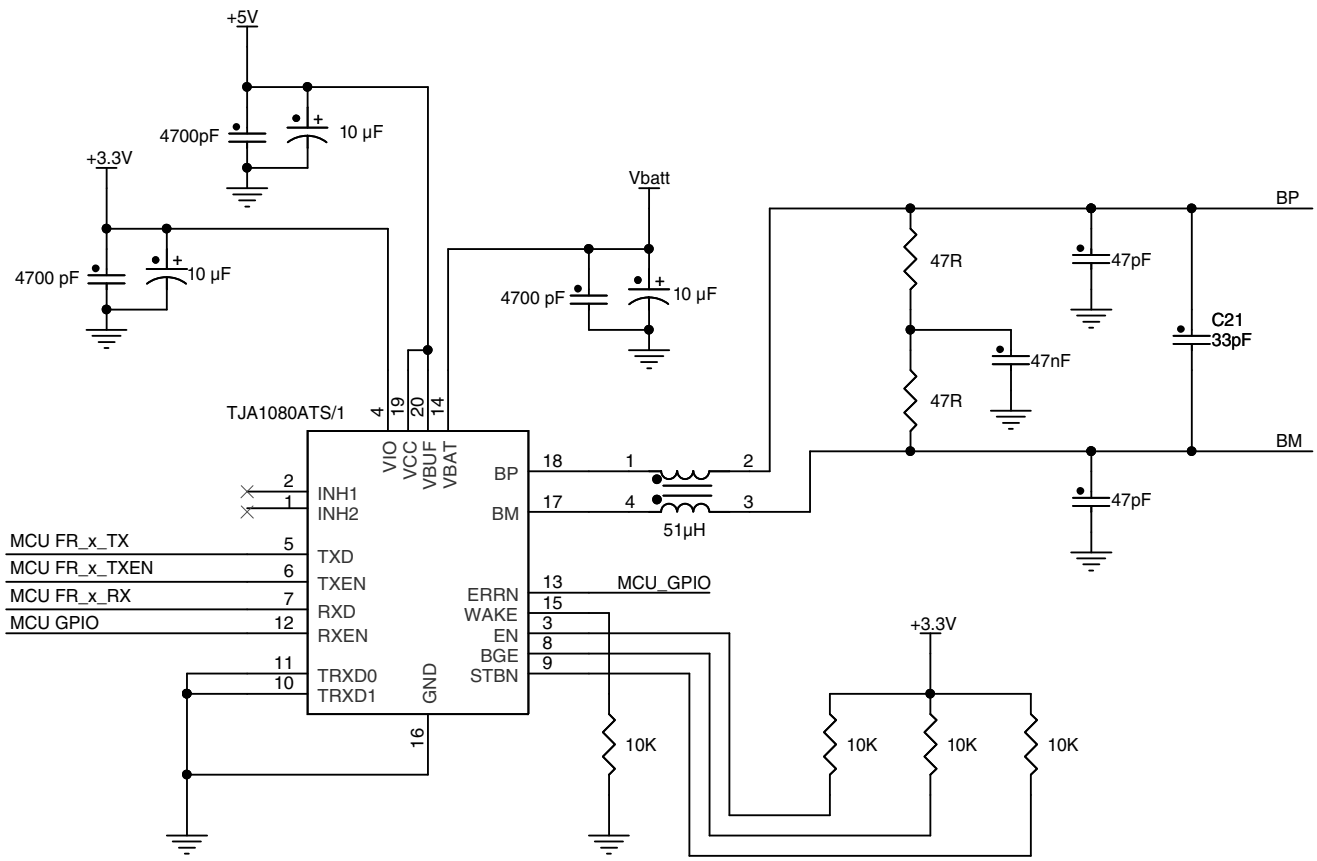


Figure 11. Typical FlexRay circuit

NOTE

- Decoupling shown as an example only
- TRXD0/TRXD1 is pulled to ground to enable the transceiver as a node device (not star configuration)
- In this configuration, only Normal mode is available. Further control is required to support low-power mode.

MCU and system connections to the TJA1080A are shown in the following table.

Table 21. TJA1080 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	INH2	Output	Inhibit 2 Output	None	Inhibit output to enable/disable external power supply
2	INH1	Output	Inhibit 1 Output	None	Inhibit output to enable/disable external power supply
3	EN	Input	Enable Input	Pull up to 3.3 V or connect to a spare MCU GPIO (output to MCU)	Enable input (for mode selection (along with the STBN pin). Internal pull-down (transmitter disabled, but allows reception, listen only mode)
4	V_{IO}	Input (power)	IO Power Supply	3.3 V	Power supply input for the MCU I/O signals
5	TXD	Input	Transmit Data	MCU FR_x_TX[1]	Transmit data from the MCU for transmitting on the FlexRay bus. Internal pullup
6	TXEN	Input	Transmit Enable	MCU FR_x_TXEN[1]	Transmit enable. A high level disables the transmitter. Internal pullup
7	RXD	Output	Receive Data	MCU FR_x_RX[1]	Receive data from the FlexRay bus to the MCU
8	BGE	Input	Bus Guardian Enable	Pull up to 3.3 V	The bus guardian input disables the transmitter. This feature is currently not supported
9	STBN	Input	Standby Input	Pull up to 3.3 V or connect to a spare MCU GPIO	Standby mode enable input (low to enter low power mode). Internal pull-down
10	TRXD1	Input/Output	Data Bus Line 1	Tie low	Data bus signal 1 for an inner star connection
11	TRXD0	Input/Output	Data Bus Line 0	Tie low	Data bus signal 0 for an inner star connection
12	RXEN	Output	Receive Enable	MCU GPIO (input to MCU)	Receive data enable indicates

Table continues on the next page...

Table 21. TJA1080 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
					data is available from the bus (low during activity)
13	ERRN	Output	Error Output	MCU GPIO (input to MCU)	The error diagnostic output drives low upon an error
14	V_{BAT}	Input (power)	Battery Supply Voltage	Protected battery voltage	Battery supply voltage
15	WAKE	Input	Local Wake Up Input	Tie low or connect to switch or MCU GPIO	The local wakeup input forces
16	GND	Input	Ground	Ground	Ground, power supply return reference
17	BM	Input/Output	Bus Line Minus	To FlexRay Connector	FlexRay bus minus signal
18	BP	Input/Output	Bus Line Plus	To FlexRay Connector	FlexRay bus plus signal
19	V_{CC}	Input (power)	Supply Voltage	5 V	Supply voltage for internal logic
20	V_{BUF}	Input (power)	Buffer Supply Voltage	5 V	Supply voltage for the FlexRay bus minus/plus signals

1. x can be A or B depending on the channel requirements in the system.

To support the requirements of different worldwide OEMs, two connector types for FlexRay are used on evaluation boards:

- One socket DB-9 for both FlexRay channels
- Two Molex (Mini Fit Jr.™) headers, one for each FlexRay channel

However, there are various connectors used for production hardware. Figure 12 and Table 22 show example pin-outs for both connector types. The DB-9 connector allows for two channels on a single connector. The dual channels allow for redundant wiring for increased reliability. The dual channel capability is built into the FlexRay standard.

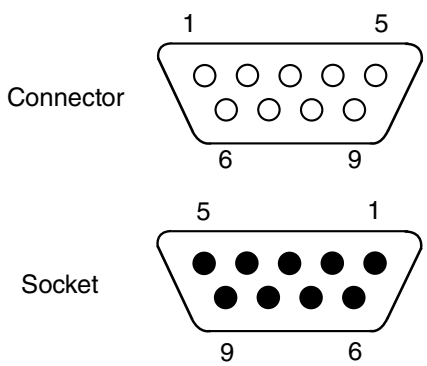


Figure 12. DB-9 connector and socket

Table 22. DB-9 pin-signal mapping

Pin Number	Signal Name	Full Name/Description
1	N/C	No connection
2	BM_A	Bus Minus Channel A
3	GND	No connection
4	BM_B	Bus Minus Channel B
5	SHIELD (OPTIONAL)	Optional Shield (if required)
6	N/C	No connection
7	BP_A	Bus Plus Channel A
8	BP_B	Bus Plus Channel B
9	N/C	No connection

NOTE

- A socket is used on the evaluation board and a cable with a connector connects with this.
- The metal shell of the socket should be connected through a ferrite bead to GND.

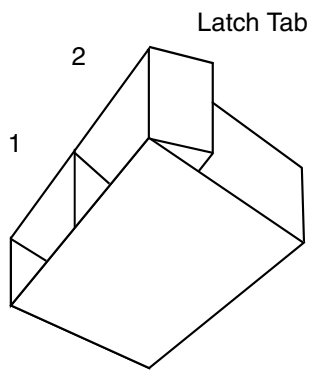


Figure 13. Molex connector picture

Table 23. Molex pin-signal mapping

Pin Number	Signal Name
1	BP
2	BM

NOTE

A connector is used on the evaluation board and a cable with a socket connects with this.

The Molex connectors are available in two types, one with pegs for mounting to the board and one without. The part numbers are shown in the following table.

Table 24. Recommended Molex Mini-Fit Jr. connector part numbers

Description	Manufacturer Part Number (Molex)
2-pin vertical connector with pegs for target system, tin contacts, latch	39-29-9022
2-pin vertical connector without pegs for target system, tin contacts, latch	39-28-8020
2-pin right-angle connector with pegs for target system, tin contacts, latch	39-30-0020
2-pin right-angle connector with flange for target system, tin contacts, latch	39-29-1028
Mating connector with latch for cable assemblies	39-01-2020
Socket terminal for mating cable assembly	39-00-0077

8.4 CAN Interface Circuitry

Controller Area Network (CAN) is commonly used in almost all automotive applications to allow communication between various microchips in the car.

The number of CAN modules on-chip varies from device to device. A separate CAN transceiver is required for each CAN module, although some CAN transceivers may have more than one transceiver on a single chip. It is possible to connect two CAN modules to a single transceiver if the transmit pins are put into open-collector mode with an external pullup resistor. However, the value of this resistor may limit the maximum speed of the CAN module if not sized properly for the speed.

Freescale CAN modules conform to CAN protocol specification version 2.0 B, and the transceivers shown in this application note comply with ISO 11898 physical layer standard.

Typically, CAN is used at either a low speed (5 Kbit/s to 125 Kbit/s) or a high speed (250 Kbit/s to 1 Mbit/s). Powertrain applications typically use a high speed (HS) CAN interface to communicate between the engine control unit and the transmission control unit. Body and chassis applications typically use a low speed (LS) CAN interface. In the dashboard of a vehicle, there is typically a gateway device that interfaces between HS and LS CAN networks.

Freescale has a high-speed standalone CAN physical interface device with built-in diagnostic capabilities (MC33902), as well as CAN transceivers integrated with other functions[1]. Other popular CAN transceivers include the NXP devices shown in the following table. Example TJA1050 HS and TJA1054 LS circuits are shown in this application note.

Table 25. NXP CAN transceiver comparison

	TJA1050	TJA1054	TJA1040	TJA1041
Bitrate (Kbit/s)	1000	125	1000	1000
Modes of operation	Normal, Listen-only	Normal, Standby, Sleep	Normal, Standby	Normal, Listen-only, Standby, Sleep

1. An example device is the MC33905 that includes a 5 V power supply controller, a CAN transceiver physical interface, and a LIN transceiver physical interface.

8.4.1 High-Speed CAN With Diagnostics: MC33902 Interface

For target systems that require full diagnostics of the CAN interface, the Freescale MC33902 high-speed CAN transceiver is available. Features of this device are:

- High-speed CAN interface for baud rates of 40 Kbit/s to 1.0 Mbit/s
- Compatible with ISO 11898 standard
- Single supply from battery
- I/O compatible from 2.75 V to 5.5 V via a dedicated input terminal (3.3 V or 5.0 V logic compatible)
- Low-power mode with remote CAN wakeup and local wake-up recognition and reporting
- CAN bus failure diagnostics and TXD/RXD pin monitoring, cold start detection, and wake-up sources reported through the ERR pin
- Enhanced diagnostics for bus, TXD, RXD, and supply pins available through pseudo-SPI via existing terminals EN, STBY, and ERR
- Split terminal for bus recessive level stabilization
- INH output to control external voltage regulator

A block diagram of this transceiver is shown below.

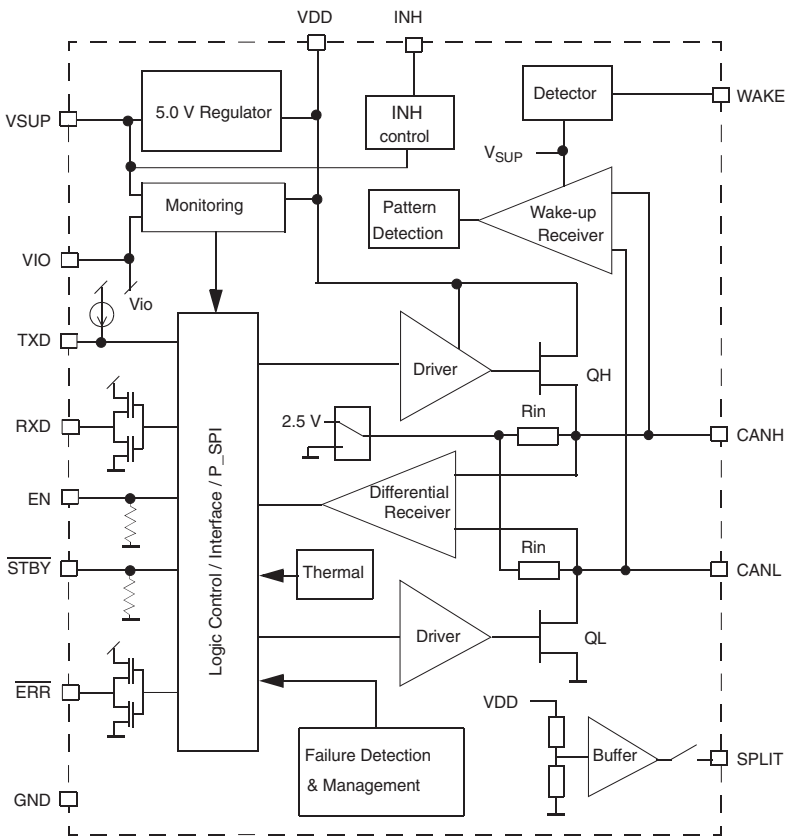


Figure 14. MC33902 block diagram

While a full SPI interface is not available for the diagnostic information, a quasi-SPI interface is available to communicate to the MCU. This interface is referred to as the P_SPI interface in the MC33902 data sheet.

The figure below shows an example schematic using the MC33902.

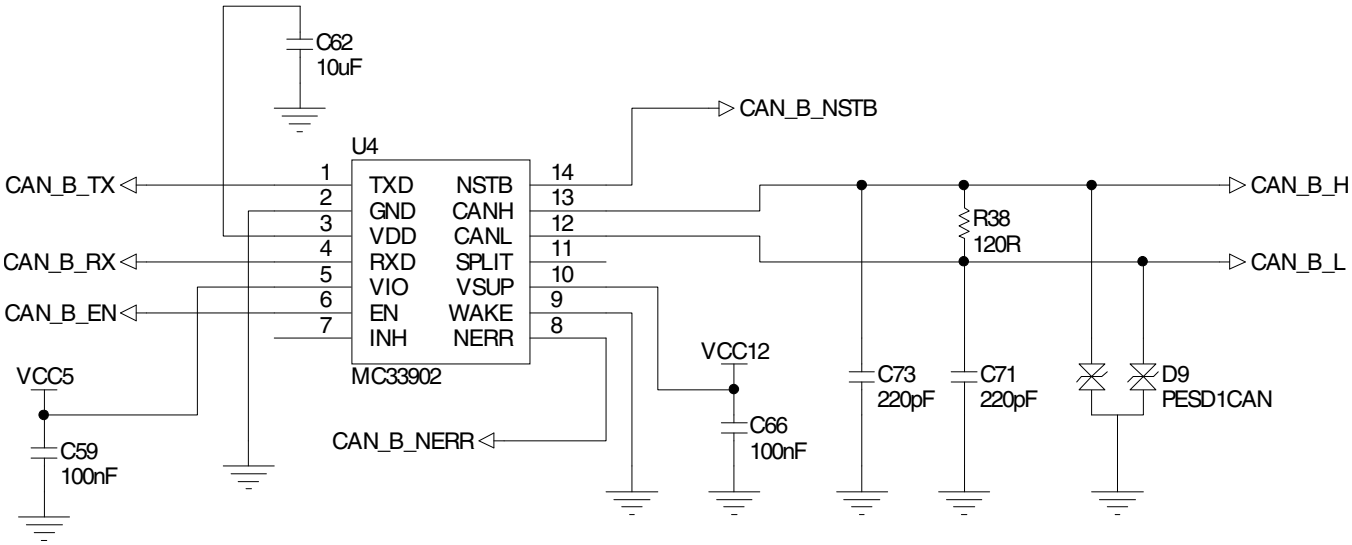


Figure 15. MC33902 high-speed CAN schematic

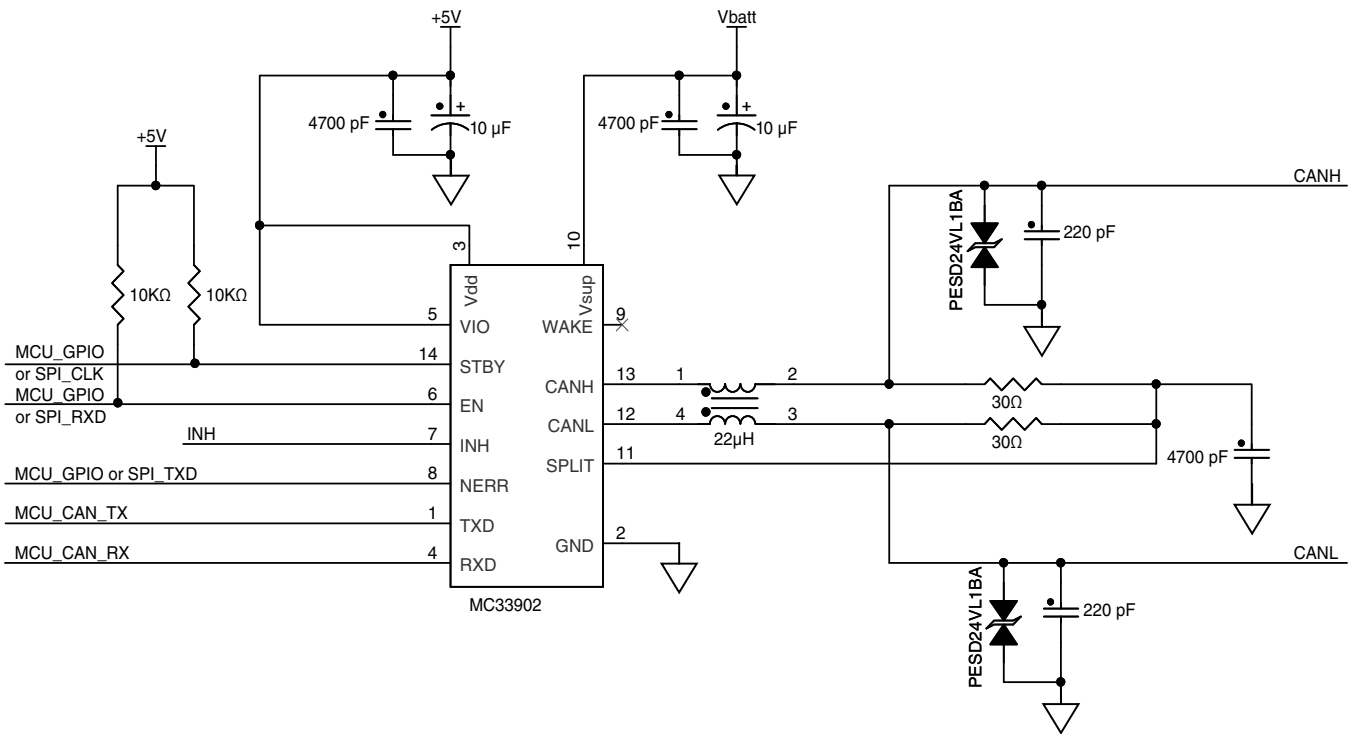


Figure 16. Typical high-speed CAN circuit using the MC33902

NOTE

- Decoupling and Bus protection shown as an example only.

The table below shows the pins of the MC33902 and the possible connections to a MCU and the target system.

Table 26. MC33902 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	TXD	Input	Transmit Data	MCU CAN TXDA	CAN transmit data input from the MCU
2	GND	Output	Ground	Ground	Ground termination
3	VDD	Output	VDD Internal Regulator Output	Bypass capacitors only	5 V power supply output. Requires external bypass capacitors.
4	RXD	Output	Receive Data	MCU CAN TXDA	CAN receive data output to the MCU
5	VIO	Input	Voltage Supply for IO	3.3 V or 5 V	Supply voltage input for the digital input and output pins. This should be matched to the IO voltage supply of the MCU. Most typically, this is 5 V, but could also be 3.3 V.
6	EN	Input	Enable	Main MCU GPIO or SPI transmit data outputeTPUA31 (GPIO)	This is the enable input for the device in static mode control. This is the master output/slave input when used in SPI mode, and the MOSI (master out, slave in) during SPI operation.
7	INH	Output	Inhibit	Use depends on intended operation (see text below)	Inhibit output for control of an external power supply regulator
8	$\overline{\text{ERR}}$	Output	Active Low Error	Main MCU GPIO or SPI receive data inputeTPUA26 (GPIO)	Pin for static error and wakeup flag reporting MISO (master in, slave out) during SPI operation
9	WAKE	Input	Wake	MCU GPIO (output)Tied to ground	Wake input
10	VSUP	Input	Voltage Supply	Battery voltage	Battery supply pin, nominally 12 V
11	SPLIT	Output	Split	CAN termination midpointNot Used	Output for connection of the CAN bus termination middle point
12	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
13	CANH	Input/Output	CAN Bus High	CAN Bus Connector	CAN bus high pin
14	$\overline{\text{NTSB}}$	Input	Standby	Main MCU GPIO or SPI Clock outputeTPUA28 (GPIO)	Standby input for device static mode control. CLK (Clock) during P_SPI operation

The use of the Inhibit pin (INH) is dependent on the selected target system operation. INH can turn an external power supply on and therefore wake a connected MCU for operation to save power when MCU operation is not required. In MPC5500 and MPC5600 automotive power train applications (engine control), INH is typically not used. However, in automotive body and chassis applications, it may be used.

8.4.2 High-Speed CAN TJA1050 Interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for high-speed applications using the NXP TJA1050 HS CAN transceiver.

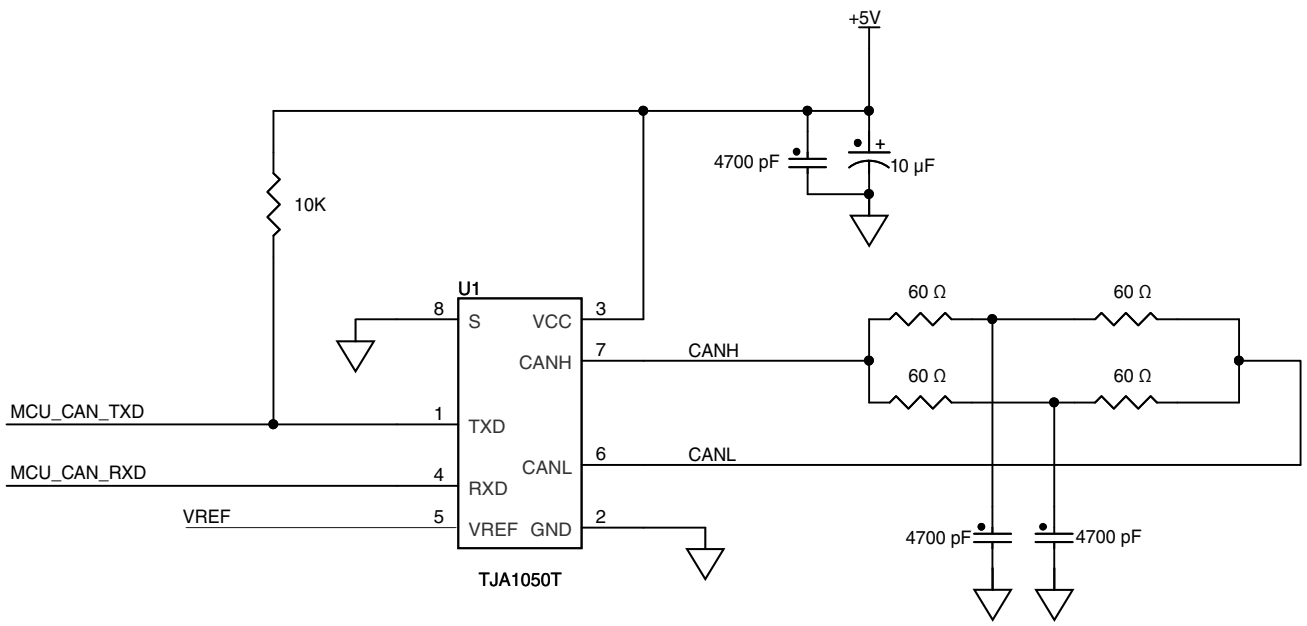


Figure 17. Typical high-speed CAN circuit using TJA1050

NOTE

- Decoupling shown as an example only.
- TXD/RXD pullup/pulldown may be required, depending on device implementation.

The table below describes the TJA1050 pin and system connections.

Table 27. TJA1050 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
2	GND	Output	Ground	Ground	Ground return termination
3	VCC	Input	—	5 V	Voltage supply input (5 V)
4	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU
5	VREF	Output	Reference voltage Output	Not used	Mid-supply output voltage. This is typically not used in many systems, but can be used if voltage translation needs to be done between the CAN transceiver and the MCU.
6	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
7	CANH	Input/Output	CAN Bus High	CAN Bus Connector	CAN bus high pin

Table continues on the next page...

Table 27. TJA1050 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
8	S	Input	Select	Grounded or MCU GPIO	Select for high-speed mode or silent mode. Silent mode disables the transmitter, but keeps the rest of the device active. This may be used in case of an error condition.

8.4.3 Low-Speed CAN TJA1054 Interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for low-speed applications using the NXP TJA1054 LS CAN transceiver. Optionally, the standby and enable pins can be connected to MCU GPIO pins for additional control of the physical interface.

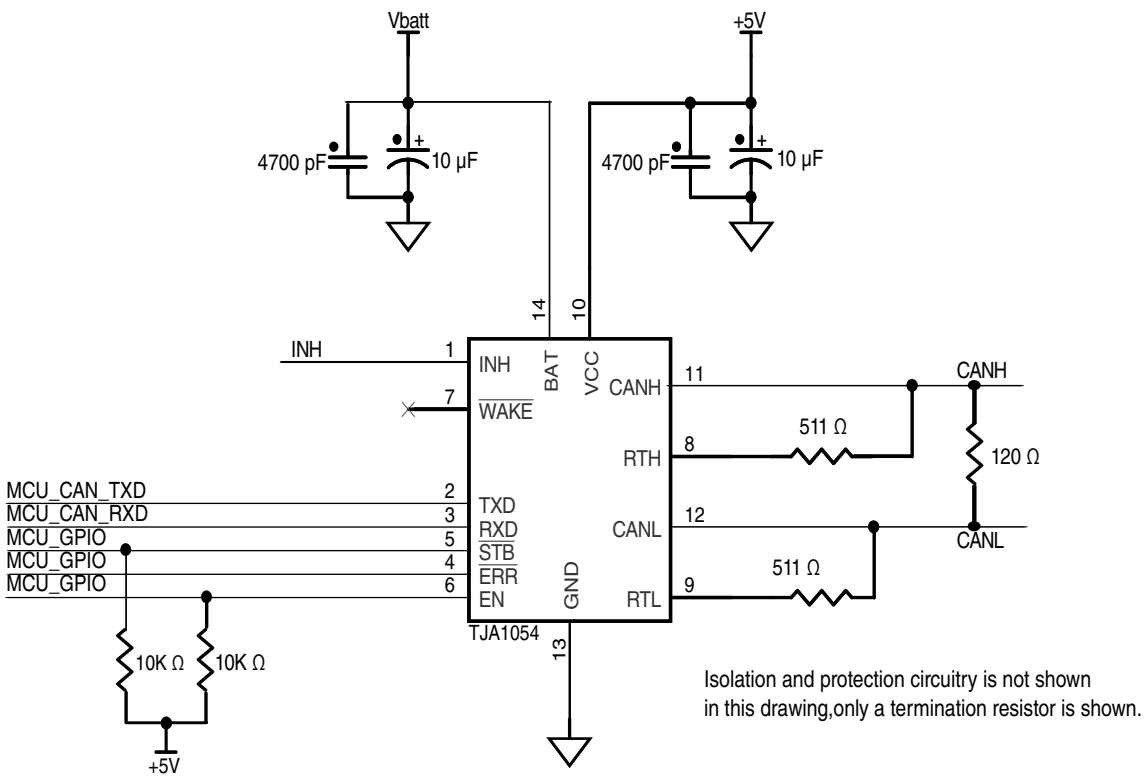


Figure 18. Typical low-speed CAN circuit using TJA1054

NOTE

- Decoupling shown as an example only.
- $\overline{\text{STB}}$ and EN should be pulled high for Normal mode. These signals can optionally be connected to MCU GPIO pins to allow MCU control of the physical interface.

The table below describes the TJA1054 pins and system connections.

Table 28. TJA1054 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	INH	Input	Inhibit	Typically not connected	Inhibit output for control of an external power supply regulator if a wake up occurs
2	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
3	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU
4	$\overline{\text{ERR}}$	Output	Error	MCU GPIO	The error signal indicates a bus failure in normal operating mode or a wake-up is detected in Standby or Sleep modes.
5	$\overline{\text{STB}}$	Input	Voltage Supply for IO	MCU GPIO	Standby input for device. It is also used in conjunction with the EN pin to determine the mode of the transceiver.
6	EN	Input	Enable	MCU GPIO	Enable input for the device. It is also used in conjunction with the STB pin to determine the mode of the transceiver.
7	$\overline{\text{WAKE}}$	Input	Wake	Typically not connected	Wake input (active low), both falling and rising edges are detected
8	RTH	Input	Termination Resistor High	Resistor to CANH	Termination resistor for the CAN bus high[1]
9	RTL	Input	Termination Resistor Low	Resistor to CANL	Termination resistor for the CAN bus low[1]
10	VCC	Input	Voltage Supply	5 V	Digital IO supply voltage, 5 V
11	CANH	Output	CAN Bus High	CAN Bus Connector	CAN bus high pin
12	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
13	Ground	Output	Ground	Ground	Ground return termination path
14	BAT	Input	Standby	Battery voltage	Battery supply pin, nominally 12 V

1. This allows the transceiver to control the CAN bus impedance under an error condition.

8.4.4 Recommended CAN Connector

Generally DB-9 connectors are used for evaluation boards to connect CAN modules together, whereas there are various connectors used for production hardware. The following figure shows the DB-9 connector and socket configuration of a typical evaluation board connector. A socket is used on the evaluation board and a cable with a connector connects with it.

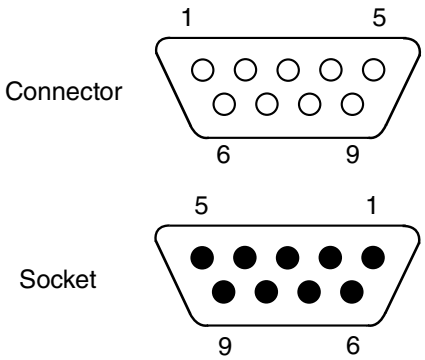


Figure 19. DB-9 connector and socket

The table below shows the typical connector pin-out definition.

Table 29. DB-9 pin signal mapping

Pin number	Signal name
1	N/C
2	CAN_L
3	GND
4	N/C
5	CAN_SHIELD (OPTIONAL)
6	GND
7	CAN_H
8	N/C
9	CAN_V+ (OPTIONAL)

NOTE

The metal shell of the socket should be connected through a ferrite bead to the chassis ground.

8.5 Ethernet interface examples

Ethernet is a communication technology that was originally developed for creating local area networks (LANs) between computers. Over time, it has become the standard wired communications network for the PC and is widely used within telecommunications and industrial applications. In recent years, Ethernet has found its way into automotive electronics with deployment in diagnostic and camera applications.

The Fast Ethernet Controller (FEC) implemented on the MPC57xxM devices is a communication controller that supports 10 and 100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The figure below shows a typical set up of the compete interface to the network. Here a DP83848VYB from Texas Instruments is used as the ethernet PHY. This will be used throughout this chapter to show an example interface.

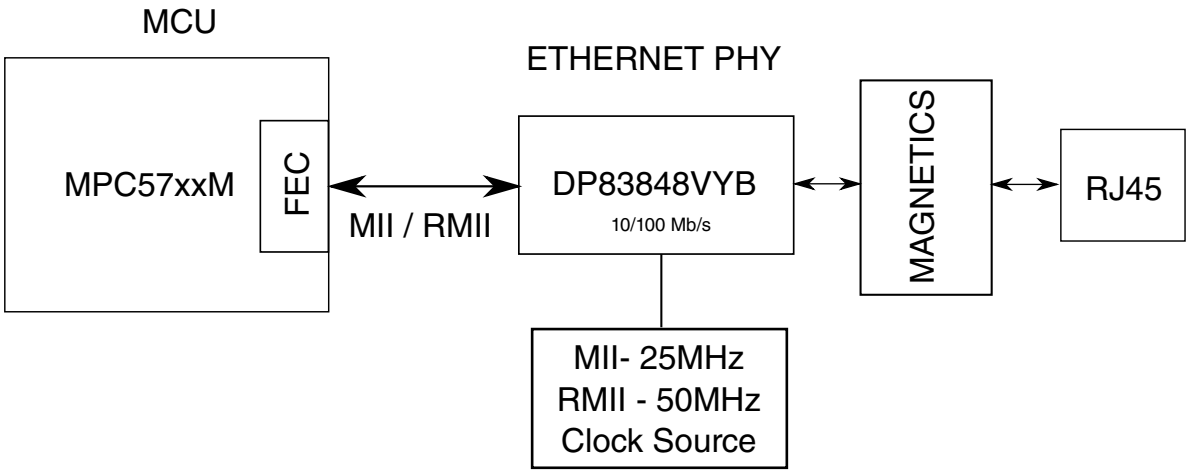


Figure 20. Ethernet application configuration example

As shown in Figure 20 the FEC can interface to a PHY using either the 10/100 Mbit/s MII or RMII or the 10 Mbit/s only 7-wire interface. Please note that the MII interface is only available on BGA devices. The FEC signals from the MCU take their voltage level from the VDD_HV_IO_FLEX supply domain. Most PHYs require signals in the 3.3 V range, so the VDD_HV_IO_FLEX should be set accordingly. Be aware that this domain is shared with the FlexRay I/O.

The FEC signals are summarised in Table 30 and their use in each interface type is highlighted as REQ = Required, N/A = Not applicable for this mode and OPN = Optional. Note that the signals required by different PHYs will vary in some cases for each interface option; see the data sheet of your selected PHY.

Table 30. MPC5777M FEC signal overview

Signal Name	Description	Direction	MII	RMII	7-Wire	Port Options
FEC_MDIO	Management Data Output	I/O	REQ	N/A	N/A	PC[2] / PC[11] / PI[15] / PM[7]
FEC_MDC	Management Data Clock	O	REQ	N/A	N/A	PC[3] / PI[14] / PM[8]
FEC_REF_CLK	RMII Reference Clock Output	O	N/A	REQ	N/A	PC[10]
FEC_TX_EN	Transmit Enable	O	REQ	REQ	REQ	PC[14]
FEC_TXD0	Transmit Data 0	O	REQ	REQ	REQ	PC[15]
FEC_TXD1	Transmit Data 1	O	REQ	REQ	N/A	PE[12]
FEC_TXD2	Transmit Data 2	O	REQ	N/A	N/A	PM[4]
FEC_TXD3	Transmit Data 3	O	REQ	N/A	N/A	PM[5]
FEC_TXER	Transmit Error	O	OPN	OPN	N/A	D[10]
FEC_RXCLK	Receive Clock	I	REQ	N/A	REQ	PC[10] / PM[8]
FEC_RXDV	Receive Data Valid	I	REQ	REQ[1]	N/A	PC[11] / PM[0]
FEC_RXD0	Receive Data 0	I	REQ	REQ	REQ	PC[12]
FEC_RXD1	Receive Data 1	I	REQ	REQ	N/A	PC[13]
FEC_RXD2	Receive Data 2	I	REQ	N/A	N/A	PM[1]
FEC_RXD3	Receive Data 3	I	REQ	N/A	N/A	PK[15]
FEC_TXCLK	Transmit Clock	I	REQ	N/A	REQ	PK[14]
FEC_RXER	Receive Error	I	OPN	OPN	N/A	PM[3]
FEC_CRS	Carrier Sense	I	REQ	N/A	REQ	PC[11] / PM[0]
FEC_COL	Collision Detection	I	REQ	OPN	REQ	PM[2]

1. FEC_RXDV in RMII mode generates RXDV and CRS

The following figure shows the typical connections for the physical interface between the MPC5777M MCU and the DP83848VYB PHY from Texas Instruments. The configuration has been set up to provide the option of using either MII or RMII interface from the MCU. A PulseJack™ J1011F21PNL RJ45 connector with integrated magnetics is also shown. When using RMII mode, the PHY must be clocked at 50 MHz. This can be done by supplying X1 with a clock output from the MCU in place of the 25 MHz crystal used in MII mode.

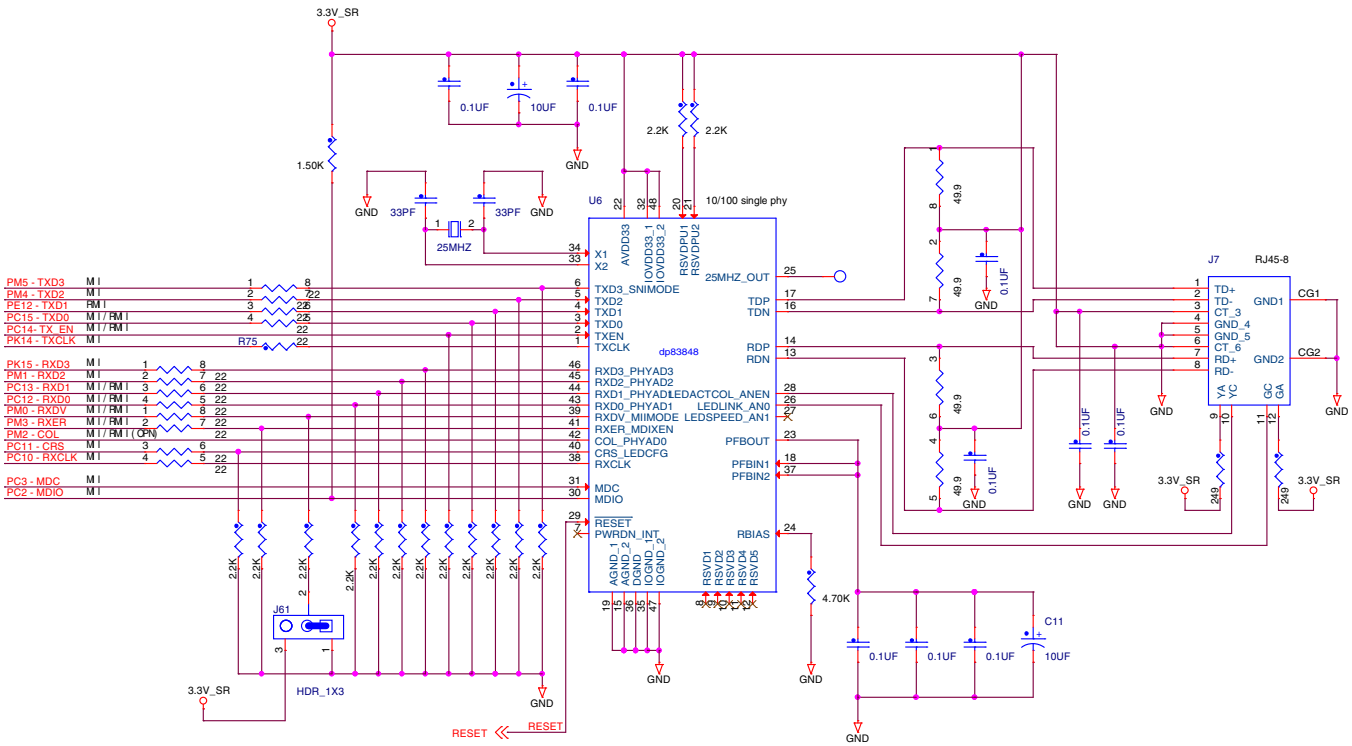


Figure 21. Ethernet example circuitry

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