Freescale Semiconductor
Application Note

Document Number: AN5181
Rev. 0, September 2015

Introduction to the MPC5746R Trace Adapter

Including an overview of the Emulation Device

by: Randy Dees

1 Introduction

The MPC5746R is a dual-core Power Architecture® based microcontroller (MCU) that includes an enhanced Timing Processor Unit 2. It is typically used in automotive powertrain or transmission applications. The MCU is available in three different production packages to handle a range of application requirements. A fourth package is available that is primarily used for development. This development package includes additional features that are not available in the production packages. The development device is called the Emulation Device or ED. The following table shows the different package options.

Table 1. MPC5746R Package options

Device	Package
MPC5646R Production Device	144 LQFP
MPC5646R Production Device	176 LQFP
MPC5646R Production Device	252 MAPBGA
MPC5646R Emulation Device	292 MAPBGA

Contents

To support development of new systems, the development or emulation device is available on a small board that can be used to adapt the Emulation Device into the footprint of the production packages. This is the Trace Adapter (TA).

This application note provides an overview of the MPC5746R TA boards, an overview of the features of the Emulation Device, and an introduction to use of the Emulation Device with the Lauterbach TRACE32® debugger and the PLS Universal Debug Engine debugger. While this application note is written about the MPC5746R TA, many of the concepts apply directly to the MPC5777M TA and may also apply to other development solutions available from Freescale for other MPC56xx and MPC57xx Microcontrollers (MCUs).

2 Trace Adapter overview

Freescale has created "Trace Adapters" (TA) to provide a full development environment that does not require that the customer include a full trace connector in their production module. The TA provides access to the full trace capabilities that are included in the emulation version of the device.

- 12 V power supply input
- Power supply for portions of the emulation device
- Full Nexus high-speed (Aurora) trace connector (17 position [34 pin] Samtec ASP–137973–01)
- Standard 14-pin Freescale Automotive Power Architecture JTAG connector
- User configurable options for some connections to the customer module

In cases where the emulation device has a different package than the production packages, TAs are available for the different production device footprints.

2.1 Trace Adapter hardware requirements

Use of the Trace Adapter (TA) allows access to all of the development features of the device without requiring a trace connector in the end-user's module. Modules should include a 14-pin JTAG connection, but a trace connector is not required.

The TA has options that allow the JTAG pins of the Emulation Device to be disconnected from the JTAG connector in the production module. This eliminates signal integrity issues with the multiple JTAG connectors and allows higher speed access of the JTAG port of the MCU. By default the TA JTAG signals are isolated from the production module signal traces, but can be connected if required.

The TA includes power regulators to power extra circuitry available in the Emulation Device. This allows the Buddy Die (BD) of the Emulation Device to be powered independently of the standard Production Die (PD), also located in the Emulation Device (see Emulation Device overview. These additional power supplies can be used to preload the calibration memory (overlay SRAM) prior to powering up the PD. This does require minimal power sequencing.

NOTE

The power supplies of the BD must be powered either prior to the power supplies of the PD or at the same time. The PD power supplies should never be powered prior to the BD.

The different power supplies of the MPC5746R are shown in the following table.

Table 2. MPC574xR power supplies

Supply name	Nominal Voltage	Description	Circuitry powered
Production die power supplies			
VDD_LV	1.25 V	Core Logic Low Voltage Supply	Most internal circuitry
VDD_HV_IO_MAIN	5.0 V	Main I/O Voltage Supply	Most device Input and output circuits

Table continues on the next page...

Table 2. MPC574xR power supplies (continued)

Supply name	Nominal Voltage	Description	Circuitry powered
VDD_HV_ADV_SAR	5.0 V	SAR ADC Voltage Supply	SAR ADC converter
VDD_HV_ADR_SAR	5.0 V	SAR ADC Voltage Reference	Reference for SAR_ADC
VDD_HV_ADV_SD	5.0 V	Sigma-Delta (SD) ADC Voltage Supply	SD ADC Converter
VDD_HV_ADR_SD	5.0 V	Sigma-Delta ADC Voltage Reference	Reference for SD ADC
VDD_HV_IO_JTAG	3.3 V or 5.0 V	Production Device JTAG I/O and External Oscillator Voltage Supply	JTAG pins[1] on production device and the crystal oscillator circuits
VDD_HV_IO_FEC	3.3 V or 5.0 V	Ethernet I/O Supply	Ethernet controller pins
VDD_HV_IO_MSC	3.3 V or 5.0 V	Microsecond Channel (MSC) I/O Supply	MSC pins
VDD_HV_PMC	5.0 V	Power Management Controller Supply	Internal regulators
VDD_HV_FLA[2]	3.3 V	PMC Flash Regulator Bypass Capacitor	Flash circuitry
VDDSTBY	1.3 V to 5.9 V	Standby RAM Supply Input	Standby SRAM
Buddy die power supplies			
VDD_LV_BD	1.25 V	Buddy Device Core Logic Low Voltage Supply	Internal BD circuitry
VDD_HV_IO_BD	3.3 or 5.0 V	Buddy Device Main I/O Voltage Supply	JTAG[3] and Nexus pins on the BD

1. In the emulation device, the JTAG pins of the production die are not connected in the package.
2. No connection to external supply required, but requires a bypass capacitor.
3. The JTAG pins of the Emulation device must be powered in the emulation device.

2.2 Trace Adapter connector locations

The Trace Adapter (TA) allows the use of either the Nexus Aurora connector or a JTAG only connection. The Nexus Aurora connector permits the full debugging capabilities to be accessible to the tool The JTAG only connector can be used for cases where features of the Emulation Device are needed, but Nexus trace is not required.

The TA requires a 12 V power supply for operation of the Emulation Device. A 2-pin connector is provided for this supply. The TA is shipped with a connector/wire assembly for power. The ends of the wires can be stripped and connected to the 2-terminal screw-connector on the Freescale MPC57xxMBB (Evaluation board[EVB]) motherboard to supply this power.

NOTE

The screw terminals are powered even when the ON/OFF switch on the motherboard is off.

The figure below shows the placement of components on the MPC5746R 252 BGA TA. It shows the external power connector and both the Nexus Aurora trace connector and the JTAG debug connector. The board dimensions are shown in the appendix MPC5746R Trace Adapter schematics and drawings.

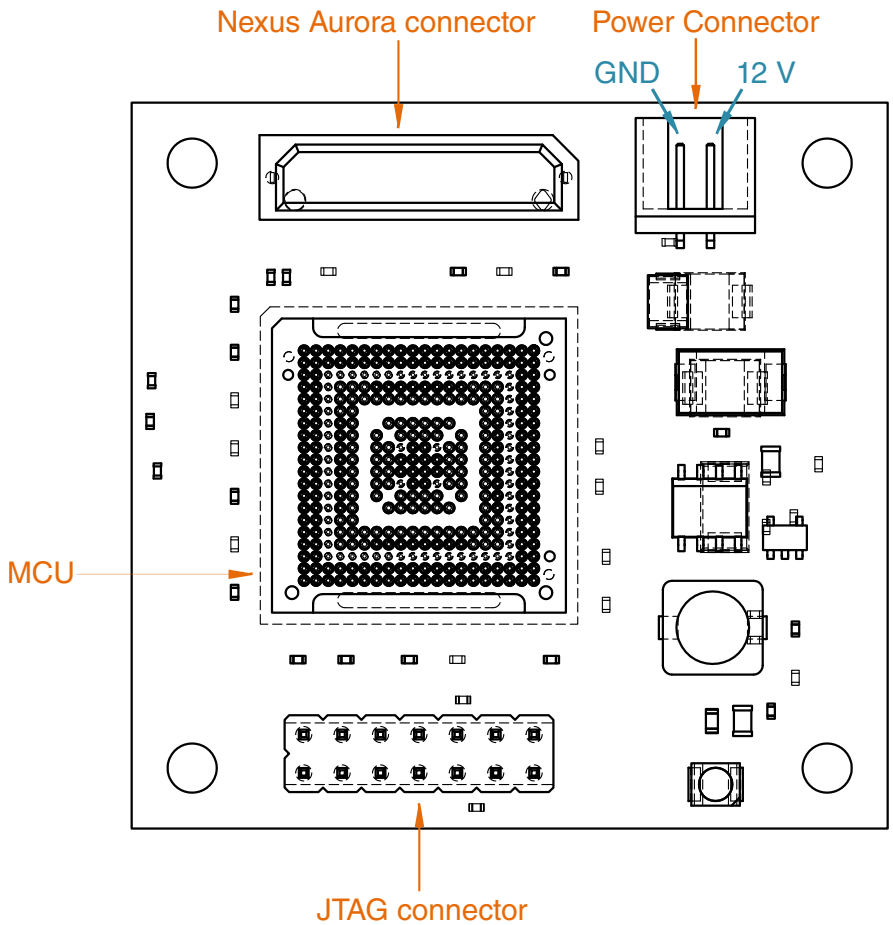

Figure 1. MPC5746R 252 BGA Trace Adapter parts placement

NOTE

The power connector on the first revision of the MPC5746R TA (REV 0) reversed the ground and 12V power connections.

2.3 MPC57xx standardized/legacy JTAG connector

The following table shows the pin out of the recommended JTAG connector to support the MPC57xxX devices.

This connector for the target system is the Tyco part number 2514-6002UB.

NOTE

This pin out is similar to the previous Freescale MPC5500/MPC5600 family of devices. The differences are shown below.

Table 3. JTAG only connector pin-out

Description	Pin	Pin	Description
TDI	1	2	GND
TDO	3	4	GND
TCK	5	6	GND
$\overline{\text{EVTI}}$/$\overline{\text{EVTO}}$[1]	7	8	$\overline{\text{PORST}}$[2, 3]

Table continues on the next page...

Table 3. JTAG only connector pin-out (continued)

Description	Pin	Pin	Description
RESET/ESR0	9	10	TMS
VREF	11	12	GND
RDY[4]	13	14	JCOMP

1. One set of EVTI and EVTO pins may be multiplexed together in the MCU package. (This pin was EVTI-only on the MPC5500/MPC5600 devices).
2. This pin was a no-connect on the MPC55xx and MPC56xx devices.
3. On some devices, this pin is named ext_POR.
4. The RDY signal is not available on the MPC57xxM devices. EVTO0 can be placed on this pin instead.

2.4 MPC57xx high-speed serial trace connector

For high speed Nexus Aurora trace applications, the Samtec ERF8 Series connector is recommended in the IEEE-ISTO 5001-2011 standard. For the MPC57xx family, the 17 position (34 pins) connector is recommended. The part numbers of the Samtec connectors are shown in the following table.

Table 4. Recommended high-speed serial trace connector part numbers

Connector	Part number (Samtec)	Style	Description
HS34	ASP-137973-01	Samtec ERF8 Series, 17 position by 2 row	Vertical mount for MCU module
HS34	ASP-177706-02	Samtec ERF8 Series, 17 position by 2 row	Right Angle mount for MCU module

The Samtec ERF8 series of connectors is intended for high speed applications requiring a minimum footprint size with a reliable, latching connection. The recommended connector has two rows of seventeen contacts each with a spacing of 0.8 mm. The connector provides isolation between the high-speed trace signals and the low-speed JTAG and control signals. It also provides ample ground connections to ensure signal integrity.

If at all possible, the connector should be placed onto the target system with the even numbered pins nearest the edge of the printed circuit board.

In addition, care should be taken in the layout of the high speed Aurora signals (TXn+, TXn-, CLK+, and CLK-) with a good return path (usually ground).

The following picture is courtesy of Samtec U.S.A (http://www.samtec.com/search/NEXUS.aspx).

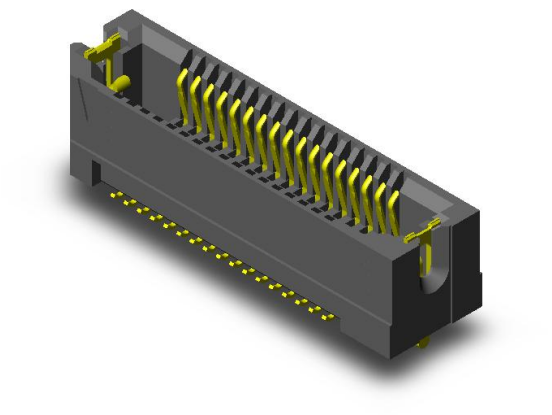

Figure 2. HS34 (ASP-137973-01) connector

The following table shows the recommended pin out for the Samtec connector.

Table 5. Generic MPC57xx high-speed serial trace connector

Position	MPC57xx Signal	Direction	Pin number	Pin number	Direction[1]	MPC57xx Signal	IEEE-5001-2012 GEN_IO signal name
	GND					GND[2]	
1	TX0+	Out	1	2	Out[3]	VREF	
2	TX0-	Out	3	4	In	TCK/TCKC	
3	GND		5	6	In/Out	TMS/TMSC[4]	
4	TX1+	Out	7	8	In	TDI	
5	TX1-	Out	9	10	Out	TDO	
6	GND		11	12	In	JCOMP	$\overline{\text{TRST}}$
7	TX2+	Out	13	14	Out	$\overline{\text{EVTI1}}$[5]	GEN_IO0
8	TX2-	Out	15	16	In	$\overline{\text{EVTI}}$(0)	
9	GND		17	18	Out	$\overline{\text{EVTO}}$(0)	
10	TX3+	Out	19	20	In/Out	$\overline{\text{RSTOUT}}$[6]	GEN_IO3
11	TX3-	Out	21	22	In/Out	$\overline{\text{RESET}}$[7]	$\overline{\text{RESET}}$
12	GND		23	24		GND	
13	TX4+	Out	25	26	In	CLK+	
14	TX4-	Out	27	28	In[8]	CLK-	
15	GND		29	30		GND	
16	TX5+	Out	31	32	Out	$\overline{\text{RDY}}$[9]	
17	TX5-	Out	33	34	In/Out	WDT[10]	GEN_IO5

Table continues on the next page...

Table 5. Generic MPC57xx high-speed serial trace connector (continued)

Position	MPC57xx Signal	Direction	Pin number	Pin number	Direction[1]	MPC57xx Signal	IEEE-5001-2012 GEN_IO signal name
	GND[2]				GND[2]		

1. Viewed from the MCU.
2. The connector locking mechanism provides additional ground connections on each end of the connector.
3. This is an output from the connector standpoint. It may or may not be from the MCU.
4. TCKC and TMSC are the IEEE 1149.7 signals on devices that support that interface.
5. Not available on all devices. No connect if the device does not support the signal.
6. $\overline{\text{PORST}}$ on the MPC57xxM and ext_POR on the MPC5744P.
7. $\overline{\text{ESR0}}$ on the some devices
8. Per the IEEE-ISTO 5001-2012, CLK+ and CLK- can either be outputs from the MCU or inputs to the MCU. For this family of devices, Freescale has defined this to be an input to the MCU. The tool must provide a LVDS clock at the desired Aurora transmission frequency from the MCU.
9. This pin can be used for $\overline{\text{EVTO1}}$ if $\overline{\text{RDY}}$ is not available.
10. WDT is an optional Watchdog Disable signal. It has no defined connection to the MCU. For systems that implement an external hardware watchdog circuit, this signal allows an external tool to disable that watchdog for debug purposes.

2.5 Nexus Auxiliary port and Aurora trace signals

The following table lists all of the Nexus serial trace signals.

NOTE

The Aurora signals require a 100 Ω termination resistor in the tool. The termination resistor should be located inside the tool near the receiver. In many cases, it may be located internal to the tool receiver.

NOTE

The MPC57xx devices incorporate an internal termination resistor in the Nexus Aurora Physical (NAP) block of the MCU for the LVDS clock (CLKP/CLKN).

Table 6. Nexus Auxiliary port and Aurora connector signals

Signal name	Full signal name	Description
TXnP (+)	Positive polarity transmit signal	The Nexus Aurora port uses one or more lanes of low voltage differential signals to transmit Nexus trace information. When multiple lanes are used, the data is striped between the different lanes. Zero to four lanes are currently projected on future devices. The connector supports up to six lanes.
TXnN (–)	Negative polarity transmit signal	
CLKP (+)	Positive polarity clock signal	The Nexus Aurora physical interface on the MCU requires a differential clock from the tool for formatting the Nexus trace information. The clock frequency should be the same as the transmit data speed.
CLKN (–)	Negative polarity clock signal	
$\overline{\text{EVTI}}$ ($\overline{\text{EVTI0}}$)	Nexus Event Input	After reset, the $\overline{\text{EVTI}}$[2] pin is used to initiate program and data trace synchronization messages or generate a

Table continues on the next page...

Table 6. Nexus Auxiliary port and Aurora connector signals (continued)

Signal name	Full signal name	Description
		breakpoint. If asserted during reset, upon negation of RESET, the device will enter debug mode and not begin code execution.
EVTI1[1,]	Nexus Event Input	Additional EVTI1 pin for additional synchronization or break functionality.
EVTO (EVTO0)[1]	Nexus Event Output	EVTO is an output that provides timing to a development tool for a single watchpoint or breakpoint occurrence. EVTI has multiple Nexus functions. In addition, the Development Semaphore Trigger module can also use the EVTO output pin.
EVTO1[1,3]	Nexus Event Output	EVTO1 is an additional event output signal.

1. Most of the pins on the device that support the Event signals can be defined to be either inputs (EVTIn) or outputs (EVTOn).
2. If no number is included, then 0 is assumed for both EVTI and EVTO.
3. Not all devices will support multiple EVTI and EVTO signals.

3 Emulation Device overview

The Emulation Device (ED) is a multi-chip device that includes additional features that are not available on the production die. These extra features are implemented on a second die ("buddy" die). The features that are available with the buddy die include the following:

- Separate power system
- 1 MB of overlay/trace SRAM
- Nexus high-speed (Aurora) Auxiliary trace port
- Separate System Integration Unit Lite (SIUL)
- Nexus Read/Write access client (NRWA)
- Independent Internal Resistor/Capacitor Oscillator (IRC)
- Control of JTAG pins of the device

The figure below shows the overall architecture of the PD and BD development resources.

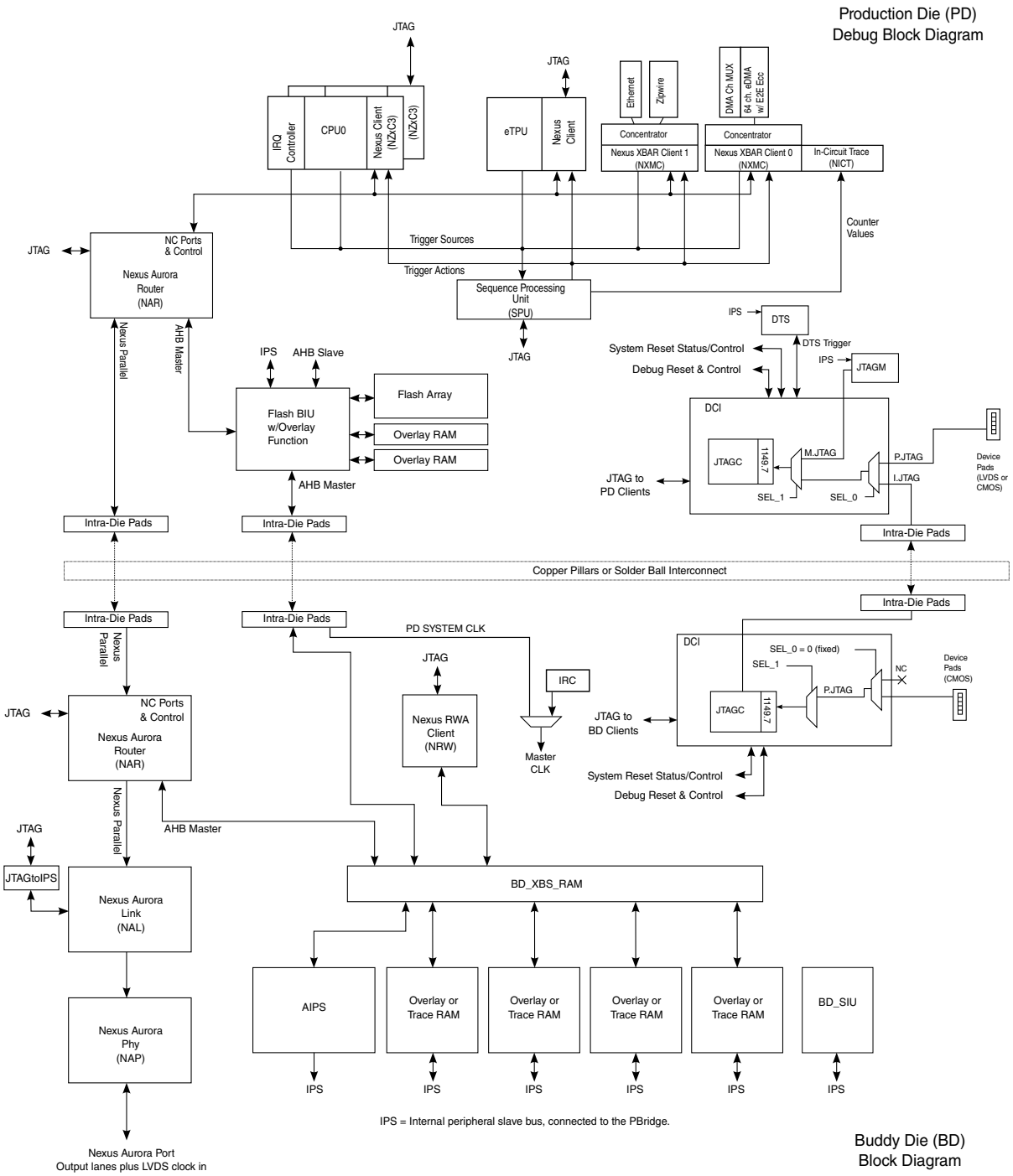

Figure 3. MPC5746R Emulation and Production Device debug architecture

3.1 Emulation Device internal physical construction

Internally, the Emulation Device consists of two die that are packaged in a single package. The first die in the package is the production die. This is the standard (same) die that is included in the production packaged device. The second die is a "buddy" die that includes additional functionality. This ensures that the functionality is the same during development as it is during production for the production features. The Emulation Device (for the MPC5746R) is packaged in a 292 Plastic over-molded Ball Grid Array (PBGA) package.

The figure below shows a cross-section of the construction of the emulation device. All balls are connected (through wire bonds) to bonding pads on the production die. The second die is mounted "flip-chip" on top of the production die.

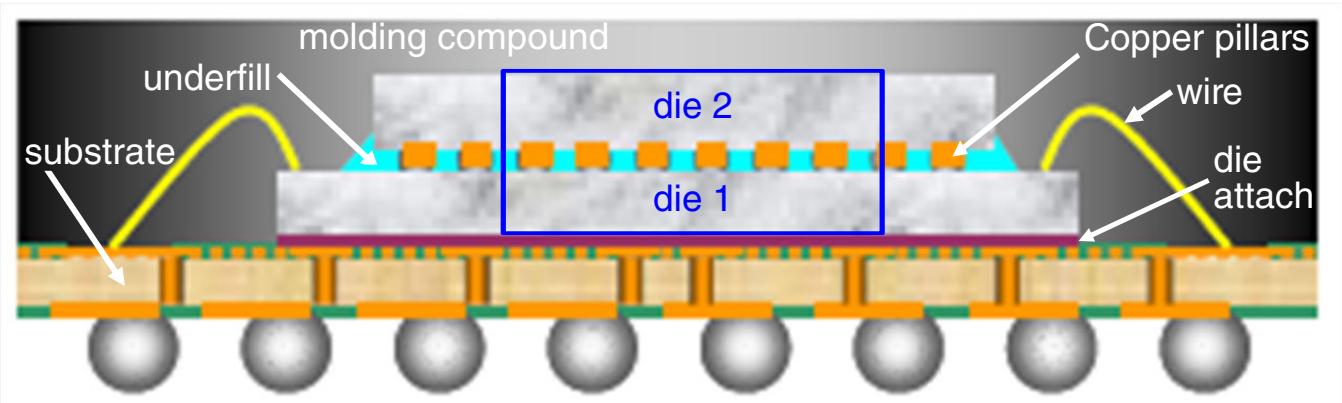

Figure 4. Emulation device physical construction cross-section

The two die are connected through copper pillars and the die are held in place with an under-fill. The figure below shows a magnified view of the die with the copper pillar construction.

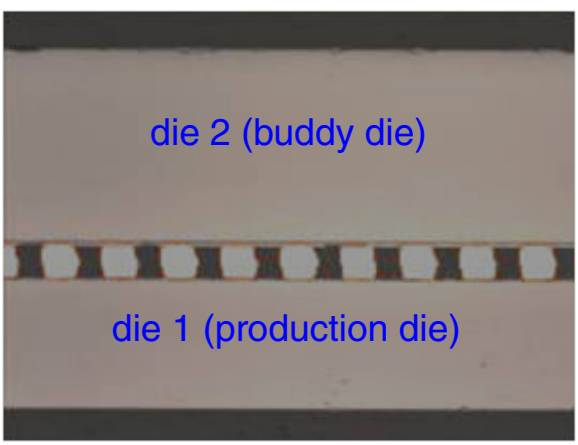

Figure 5. Die cross section

The following figure shows a larger view of the actual connections between the two die; a copper pillar on each die with solder making the connection between the pillars.

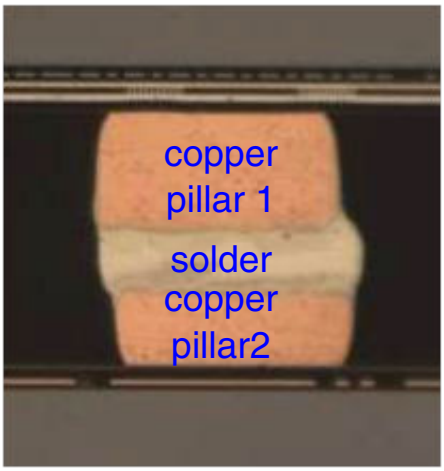

Figure 6. Copper pillar cross-section

3.2 MPC5746R Buddy Die architecture

The Buddy Die (BD) for the MPC5746R includes additional resources that can be used to supplement the development features that are available on the MPC5746R Production Device (PD). Functional block and descriptions of these blocks are:

- Debug and Calibration Interface (DCI) - The DCI includes the JTAG (IEEE 1149.1) controller and the IEEE 1149.7 interfaces and replaces the DCI/JTAG interface of the PD, but allows access to the PD JTAG interface by passing control from the BD JTAG interface to the PD JTAG interface. This requires the BD to be powered in the Emulation Device (ED) for debug operations of the Production Die (PD).
- Overlay/Trace SRAM - 1[1] MB of SRAM that can be split into four partitions allowing access by different masters and can be split between use as calibration overlay SRAM (for mapping over the internal PD FLASH) or as trace memory (holding trace information of the PD.
- Nexus Aurora Router (NAR) - The NAR receives trace information from the PD and allows it to either be sent to the Nexus Aurora Link (and ultimately out of the Nexus physical trace interface) or to the trace memory contained on the BD.
- Nexus Aurora Link (NAL) - The NAL takes the 30 Nexus Message Data Out parallel signals (MDO) and 2 Message Start/End Outputs ($\overline{\text{MSEO}}$) and splits the data into lanes and encodes it with an 8b10b format for transport over a multi-lane Aurora interface.
- Nexus Aurora Physical interface (NAP) - The NAP takes the parallel 8b10b data and serializes it for transmission out of the MCU.
- Nexus Read/Write Access client (NRWA) - The NRWA client provides an interface between the JTAG port of the BD to the BD resources (NAR and SRAM) to allow access from the JTAG port independent of the of PD.
- Crossbar (XBAR) slave interface - The XBAR allows parallel access between PD bus masters or access by the BD resources.
- Internal Resistor/Capacitor Oscillator (IRC) - The IRC provides a non-precise clock reference to the BD modules when the PD is not powered. It has a nominal frequency of 64 MHz, however, there is no trim capability and therefore, the accuracy of the frequency is ±30%.

The figure below shows the block diagram of the BD. This is a subset of the complete Emulation Device development resources (shown in Emulation Device overview).

1. The BD used on the MPC5777M includes 2 MB of SRAM.

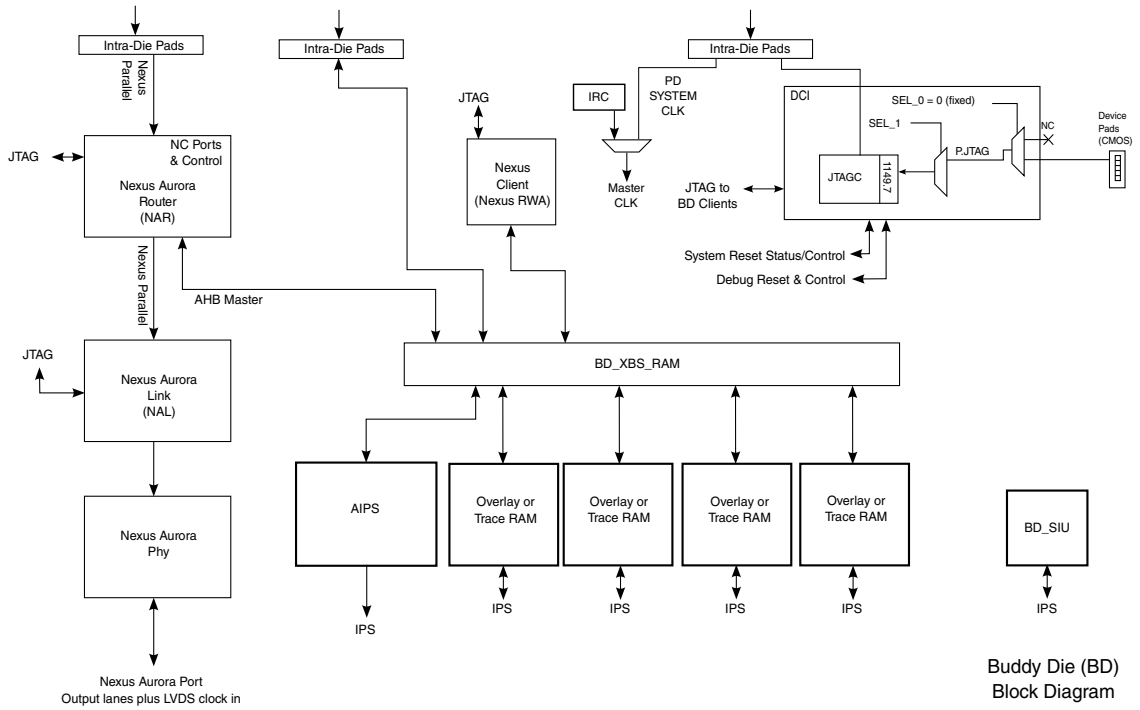

Figure 7. MPC5746R Buddy Die block diagram

There are two other important views of the overall emulation device debug architecture, The JTAG view of the system and the Nexus trace view of the system.

The MPC57xx family of devices implement a JTAG "TAP sharing" scheme to allow access to multiple JTAG clients inside of the microcontroller (MCU). The JTAG view of the debug architecture is shown in the following figure. It shows the hierarchy and access commands of the JTAG clients available in the ED and the split between the PD and the BD. The JTAG Auxiliary Access Command (AUX_ACCESS_PD) is 0x3E. For tool compatibility, the command to switch from the BD to the Production Device die is ignored by the JTAG Controller (JTAGC) in the Production Device die. This allows the tool to implement all commands that access features of the Production Device die in the same manner, regardless of whether the BD is present or not.

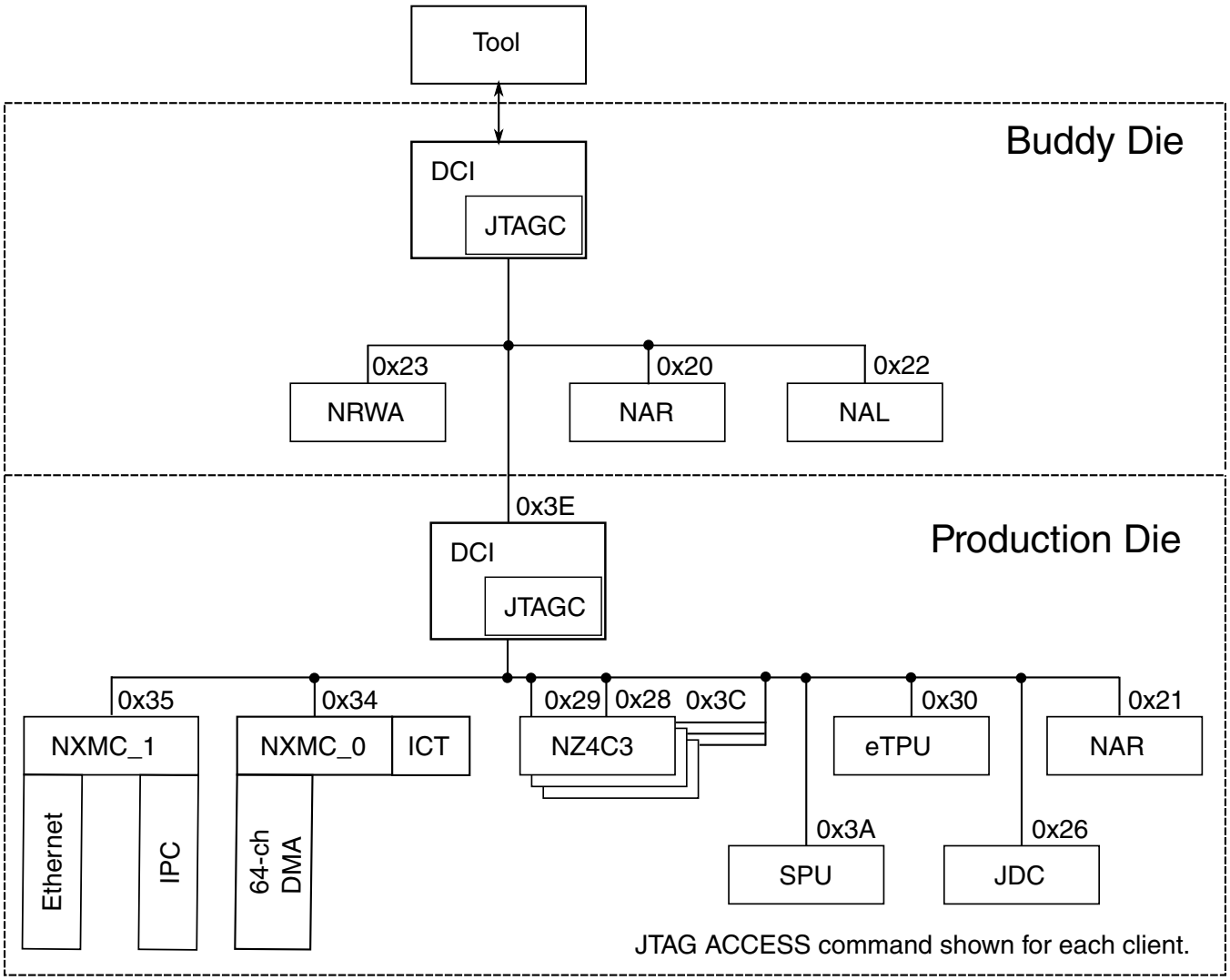

Figure 8. JTAG client hierarchy

The flow of Nexus trace data from the Nexus clients on the PD is shown in the following figure. Trace data is accumulated in the PD NAR before being sent to either the PD on-chip Trace Memory or to the BD NAR. The BD NAR can then filter trace data to be transmitted either to the internal BD trace memory or to the physical Nexus Aurora interface (NAL to NAP).

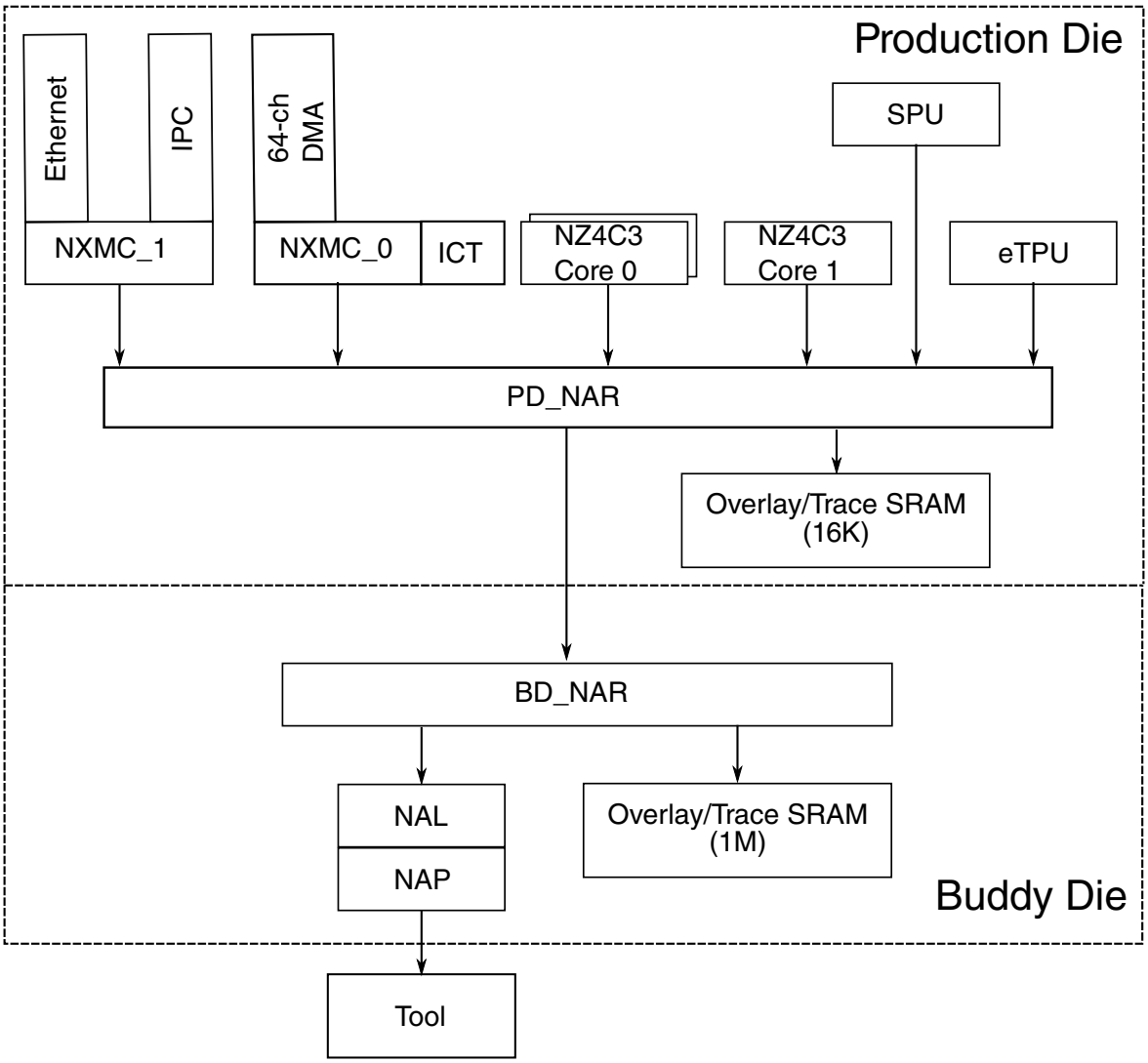

Figure 9. Nexus trace data flow

Both the PD on-chip trace memory and the BD memory can also be used for calibration (overlay SRAM over portions of the internal flash). However, the overlay/trace memory on the BD can be spilt to allocate part of the BD SRAM for the overlay function and part for the trace function. There are four (4) partitions in the BD SRAM. One (1), two (2), three (3), or four (4) partitions can be allocated to either use. The trace memory does need to be continuous since the trace function uses a base address and size to implement the trace memory. Trace can be configured to use the SARM either as a one-shot use (once the trace memory is full, trace stops) or as a circular buffer that continues until stopped.

4 BD Nexus Read/Write Access client

The Emulation Device includes a Nexus Read/Write Access (RWA) client for accessing the memory systems in the buddy die (BD). This Nexus client cannot access the memory space of the production device. The buddy die memory can also be accessed either via the production device die though the Nexus RWA client of one of the two cores or via the cores themselves.

Table 7. Nexus memory access methods

Memory region	Starting address	Accessible through the BD NRWA client	Access via core 0 or core 1[1]
Extended Overlay SRAM	0x0C00_0000	Yes	Yes
Buddy Device registers (BD_SIUL2)	0x0C80_0000	Yes	Yes
Internal (PD) Overlay SRAM	0x0D00_0000	No	Yes

1. Reads of the BD memory space must be enabled by setting the Buddy Device Read Mode (BDRM) bit in the Platform Flash Configuration Register 3 (PFLASH_PCFR3) - 0xFC03_008 = 0x0010_0000.

5 Attaching the MPC5746R Trace Adapter to an EVB

The MPC5746R Trace Adapter (TA) is designed to be used primarily with either a Freescale MPC5746R Evaluation board or to a customer target system. The MPC5746R 252 BGA daughter card is recommended (which attaches to a MPC57xxEVB motherboard). The TA provides:

- A 14-pin Automotive Power Architecture JTAG connector
- A 34-pin Nexus Trace/debug connector
- A 3.3 V power supply for the JTAG and Nexus pins on the Buddy Die (BD) in the Emulation Device (ED)
- A 1.25 V power supply for the internal logic on the BD in the ED
- A 2-pin connector to provide power to the BD regulators.

NOTE

To use a 144 or 176 QFP daughter card, the socket or microcontroller (MCU)[2] would have to be unsoldered from the board and replaced with the appropriate BGA to QFP adapter.

As shipped from Freescale, the 252 PBGA daughter card ships with a 252 PBGA socket mounted on the board. This socket must be removed to allow connection to the TA. To install the TA, perform the following steps.

1. On the bottom of the daughter card, there are four (4) screws that must be removed.
2. Once the screws are removed, the socket can be removed.
3. The TA can then be inserted into the receiver that is soldered to the daughter card. The receiver includes alignment holes to assist in aligning the TA. The TA includes alignment pins that are longer than the pins used by the device.
4. The daughter card with the TA can then be plugged into the MPC57xxEVB to provide power to the Production Die (PD) and provide physical interfaces for some of the Input/Output systems of the MCU. Access to the MCU pins is also available on this motherboard.
5. The TA ships with a short power cable for the nominal 12 V input to the TA. The connector plugs into J4 of the TA. For the EVB, the other ends of the wires can be stripped and connected to the screw terminals on the MPC57xxEVB (B33) or connected to an appropriate supply in the customer target system.

NOTE

The screw terminals (B33) are always powered when the power is connected to the EVB supply (P26).

This allows the On/Off switch (SW5) to control power supplied to the PD, allowing the BD to be powered separately.

The figure below shows a photograph of a MPC5746R TA connected to the MPC5746R daughter card (MPC5746R-252DC) and the MPC57xx motherboard.

2. This depends on whether the board uses a socket to hold the MCU or if the MCU is directly soldered to the daughter card.

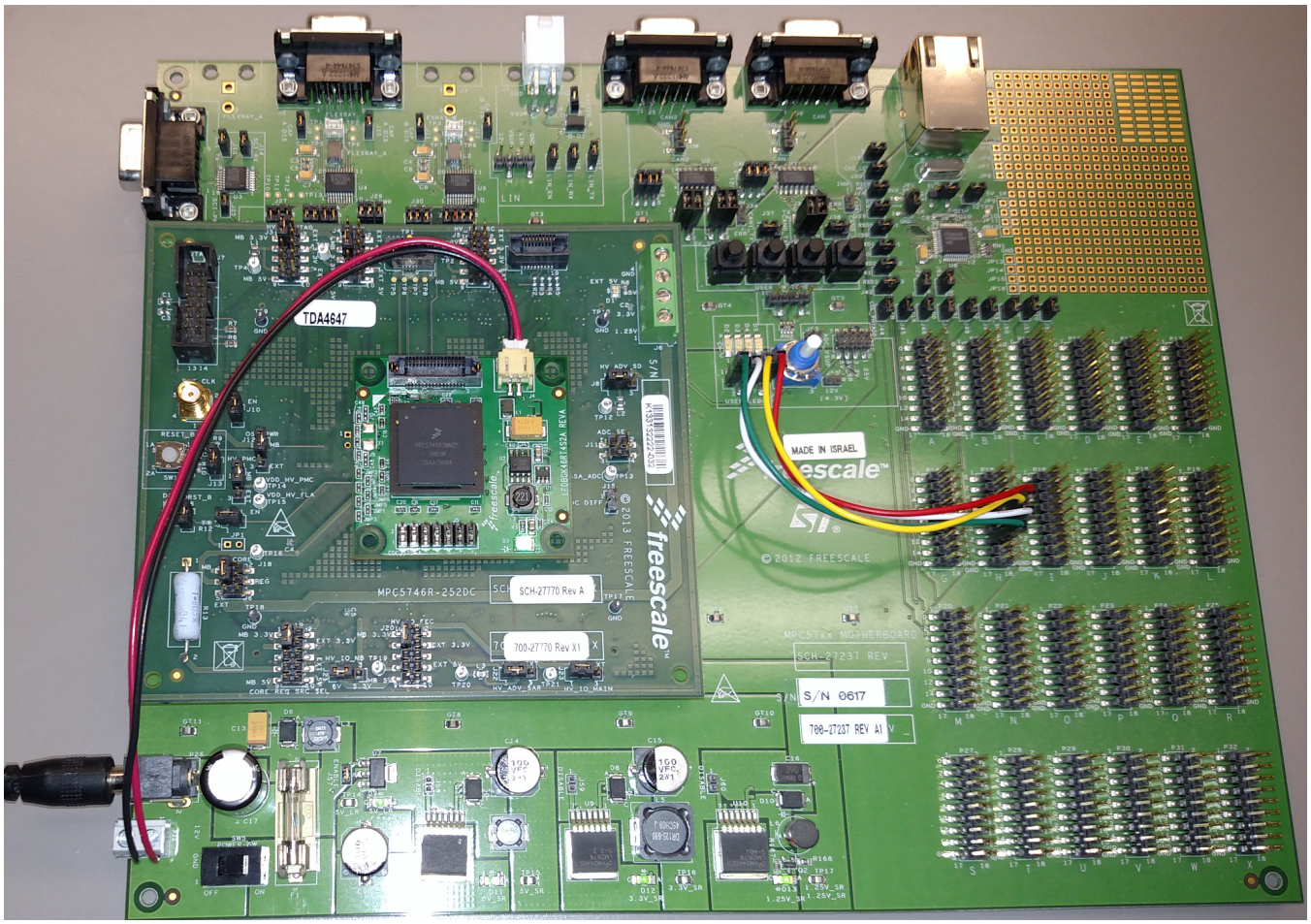

Figure 10. MPC5746R TA mounted on EVB

NOTE

By default, when the TA is connected to the daughter card, the JTAG connector on the daughter card is not connected to the MCU. Only the JTAG connector or the Nexus connector on the TA can be used for debugging the system. The TA does includes an option to connect these signals to the target system, but by default, they are left open.

6 Using the MPC5746R Trace Adapter with a customer target system

The MPC5746R Trace Adapters (TA) are designed to be used in a customer target system for development purposes. This allows the use of trace and the use of the overlay/trace memory in the target system. There are some precautions and actions that must be taken into account when using the TA.

1. Since the TA is mounted via pins, a receiver must be soldered into the target system. For the MPC5746R in the 252 PBGA package, this consists of a simple receiver. The receiver is basically a socket with alignment pins that is soldered to the target board. The TA then plugs into the socket. For the 144 or 174 LQFP devices, an adapter is required to convert the pin-grid TA to the surface mount footprint of the target system. For the MPC5746R, a single TA is used for both the 144 and the 176 LQFP devices. The target adapter for the LQFP packages uses a 208 pin-grid TA that plugs in to either a 208 to 176 target adapter or into a 208 to 144 target adapter. Part numbers for all of the TAs, receivers, and target adapters are shown in MPC5746R Trace Adapter orderable parts .

2. A keep-out area is required for the TA board to insure that components on the TA do not interfere with components in the target system.
3. Power (nominal 12 V) must be supplied to the TA through the supplied power connector. The system power supply must be capable of handing the additional current requirements of the TA and the Emulation Device. See the MPC574xR (device) Data Sheet for the maximum current required for these supplies.
4. Depending on the target system a connection mechanism may be required to allow the debug connectors to be accessible. In other words, if the target system is in a sealed box, a hole may be required to access the JTAG or Nexus connectors on the TA.

7 MPC5746R Trace Adapter orderable parts

The following table shows the orderable components for the MPC5746R Trace Adapters (TA), including the TAs and the receivers or TAs required.

Table 8. Orderable parts

Package footprint	Part Number	Description
252PBGA	LFDBGK46RT4S2A	292 PIN 0.8MM BGA to 252 0.8MM PGA Adapter with Aurora interface for MPC574xR
	LFBGARBS2AO	SURFACE MOUNT PGA SOCKET FOR 252 Pin 0.8MM VertiCal and Microcontrollers with pins[1]
176LQFP[2]	LFDBGK46RT4QA	292 PIN 0.8MM BGA to 208 1.0MM PGA Adapter with Aurora interface for MPC574xR.
	LFTAK46MQM2A	208 pin 1.0mm PGA to 176 pin 0.5mm QFP target Adapter board for MPC574xR
144LQFP[3]	LFDBGK46RT4QA	292 PIN 0.8MM BGA to 208 1.0MM PGA Adapter with Aurora interface for MPC574xR.
	LFTAK46RQLA	208 pin 1.0mm PGA to 144 pin 0.5mm QFP target Adapter board for MPC574xR

1. Also known as a receiver for mounting into a target system
2. For the 176QFP, the TA converts the 292 MAPBGA to a 208 BGA footprint. A separate adapter is required to convert the 208 footprint to the 176 PQFP footprint.
3. For the 144 QFP, the TA converts the 292 MAPBGA to a 208 BGA footprint. A separate adapter is required to convert the 208 footprint to the 144 PQFP footprint.

Appendix A MPC5746R Trace Adapter schematics and drawings

This appendix contains the schematics, bill of materials, and drawings for the 252-pin MPC5746R Trace Adapter (TA). The 208-pin TAs are similar, but are not included. However, since the 208-pin TA has a different outline and component placement, a drawing of the 208-pin TA is also included. In addition, a drawing of the 208 BGA to LQFP footprint adapter and a drawing of the 208-pin TA mounted on the 208 BGA to 176 LQFP adapter to show the stacked dimensions.

The latest version of the schematics and dimension drawings can be downloaded from freescale.com.

A complete list of the schematics and dimension drawings that are included in this application note and which are not included is shown in the following table.

Table A-1. MPC5746R TA schematics and other drawings

Type	Drawing number	Revision	Description	Included in Application Note
Package adapter	LFTAK46RQLA	—	208 PGA to 144 QFP target adapter dimension drawings	Yes
Package adapter	LFTAK46MQM2A	—	208 PGA to 176 QFP target adapter dimension drawings	Yes
Receiver	LFBGARBS2AO	0	252 BGA receiver	Yes
Schematics	LFDBGK46RT4QA	A	MPC5746RR 208 BGA Trace Adapter schematics	No
Schematics	LFDBGK46RT4S2A	A	MPC5746RR 252 BGA Trace Adapter schematics	Yes
Schematics	LFTAK46MQM2A	O	MPC5746R 208 to 176 Trace Adapter schematic	Yes
Schematics	LFTAK46RQLA	—	MPC5746R 208 to 144 adapter schematic	No
Stack dimensions	DBGK46RT4S2A_B-RBS2AO	—	MPC5746R 252 BGA with 252 receiver stack dimension drawing	Yes
Stack dimensions	DBGK46RTQA RevA-TAK46RQLA	—	MPC5746R 208 PGA with 144 adapter stack dimension drawing	Yes
Stack dimensions	DBGK46RTQA RevA-TAK46MQM2A	—	MPC5746R 208 PGA with 176 adapter stack dimension drawing	Yes
TA Board Dimensions	LFDBGK46RT4S2A-LAYOUT	B	MPC5746R 252 BGA Trace Adapter dimension drawing	Yes
TA Board Dimensions	LFDBGK46RT4QA	A	MPC5746R 208 BGA Trace Adapter dimension drawing	Yes

A.1 252 PBGA Trace Adapter

This section contains the schematics, Bill of Materials, 252 PBGA layout drawing, and the stacked side drawing of the 252 PBGA Trace Adapter (TA) with the receivers mounted.

A.1.1 Schematics 252 BGA

The figures below show the schematics of the MPC5746R 252 BGA Trace Adapter (TA).

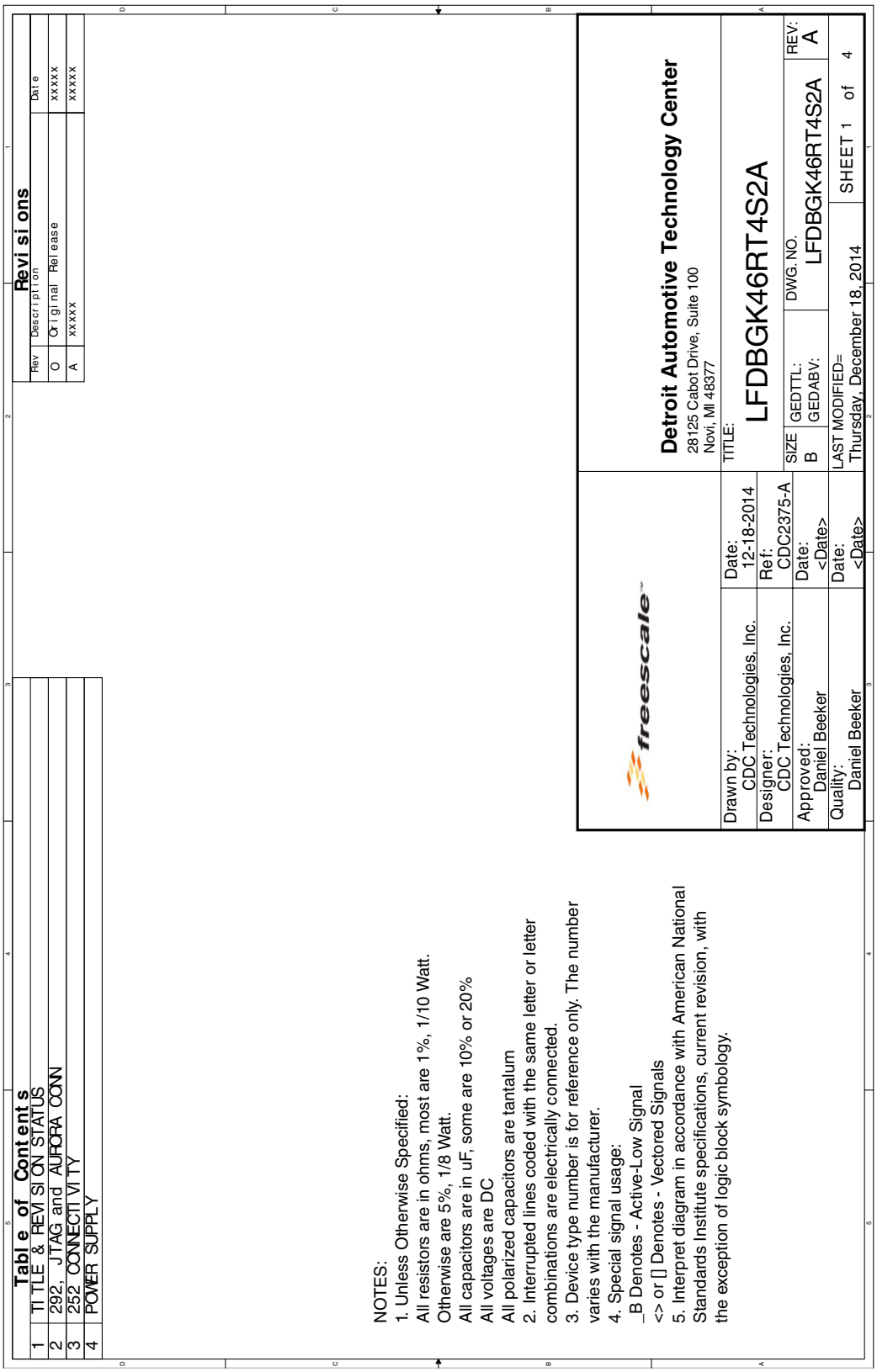

Figure A-1. 292 to 252 Trace Adapter (page 1)

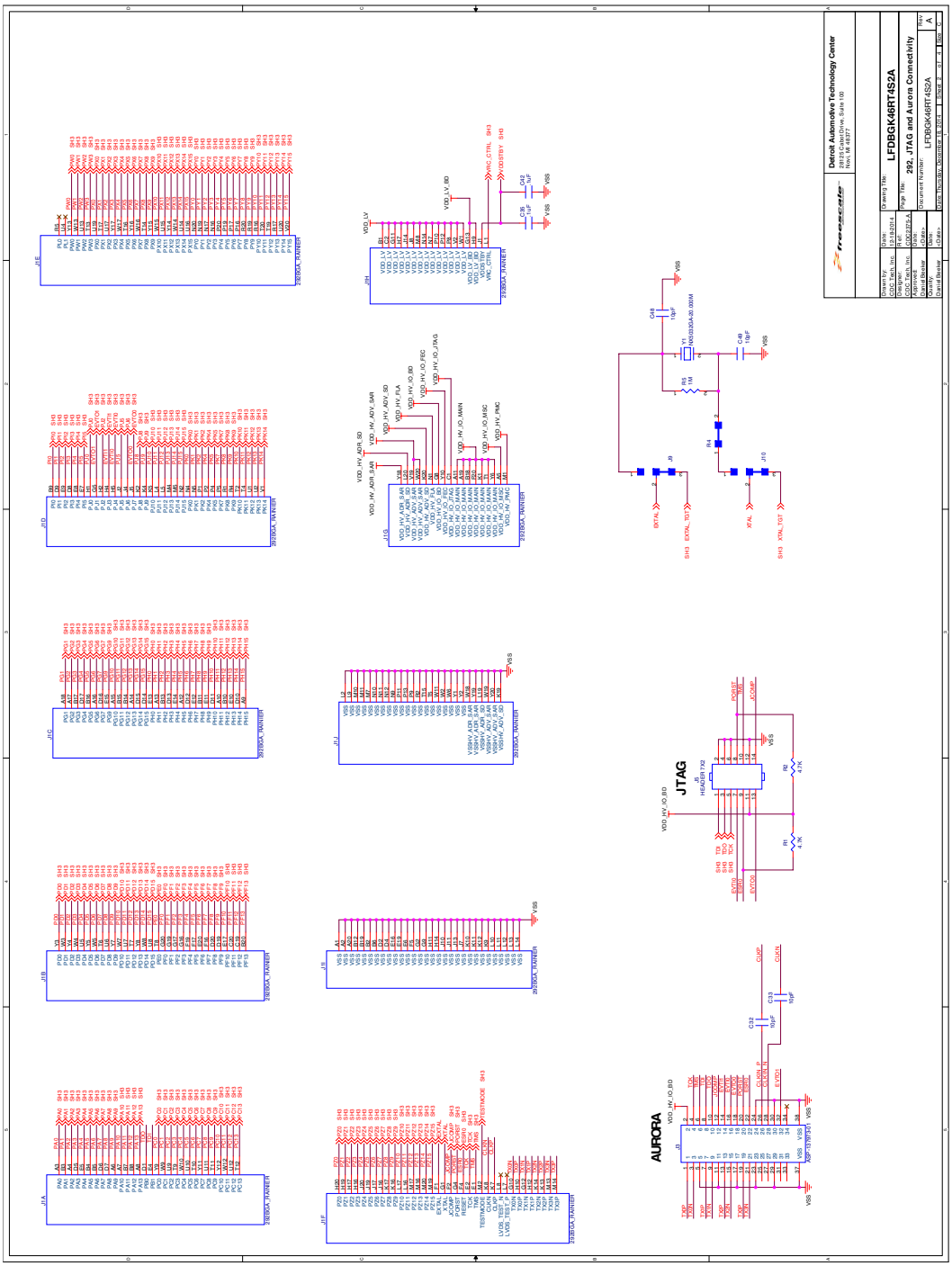

Figure A-2. 292 to 252 Trace Adapter (page 2)

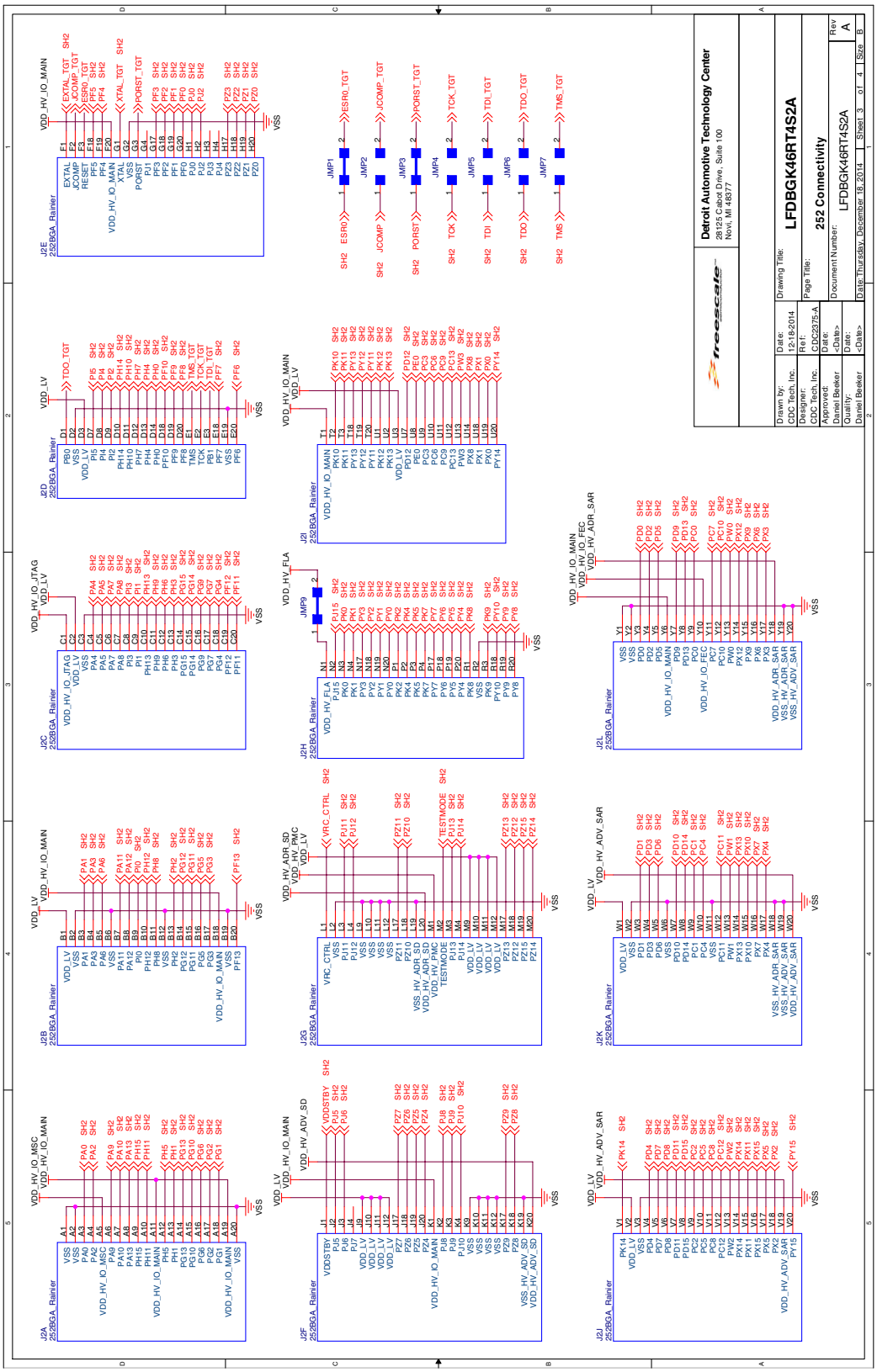

Figure A-3. 292 to 252 Trace Adapter (page 3)

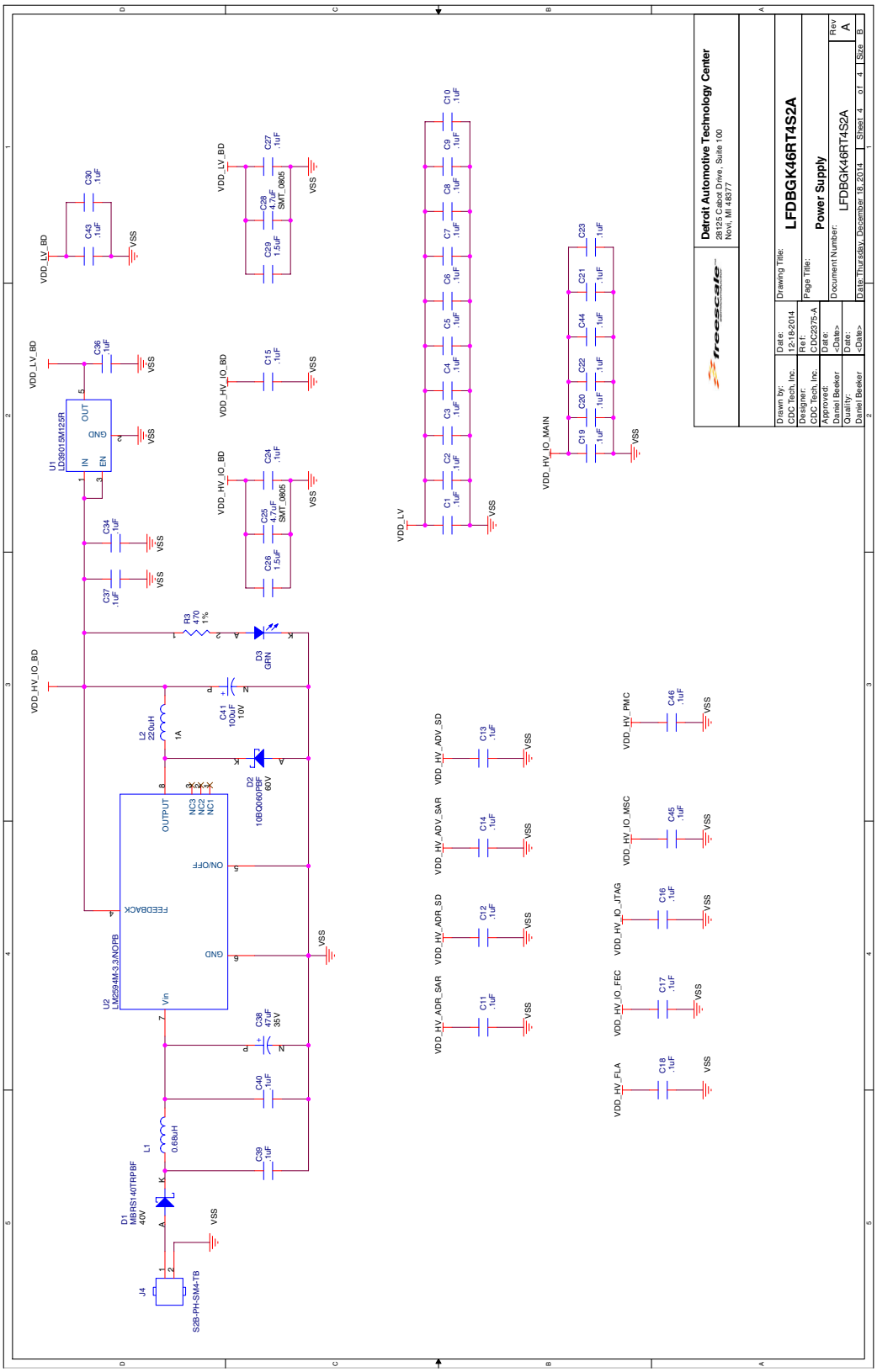

Figure A-4. 292 to 252 Trace Adapter (page 4)

A.1.2 Trace Adapter bill of materials 252 BGA

Below is information about the components used on the MPC5746R 252 BGA Trace Adapter (TA).

Ref Number	Part Type	Value	Vendor/Source	Part Number	Package Type
C32,C33,C48,C49	Capacitor, Ceramic	10pF 16V 10% X5R	TDK Corporation	C1005C0G1H100D 050BA	0402 (1005 Metric)
C1-C24,C27,C30, C34-C37,C39,C40,C42-C46	Capacitor, Ceramic	0.10uF 16V 10% X5R	Taiyo Yuden	EMK105B7104KV-F	0402 (1005 metric)
C26,C29	Capacitor, Ceramic	1.5uF 10V 10% X5R	TDK Corporation	C1005X5R1A155K 050BC	0402 (1005 metric)
C25,C28	Capacitor, Ceramic	4.7uF 16V 10% X5R	Samsung Electro-Mechanics America, Inc	CL21A475KAQNN NE	0805 (2012 Metric)
C38	Capacitor, Tantalum	47 uF, 35 V, 10%	AVX	TAJE476K035R	2917 (7343 Metric)
C41	Capacitor, Tantalum	100uF 10V 10%	Vishay Sprague	293D107X9010C2 TE3	2312 (6032 Metric)
R1,R2	Resistor	4.7k-Ohm 1/16W 5%	Stackpole Electronics Inc	RMCF0402JT4K70	0402 (1005 metric)
R3	Resistor	470 ohm 1/10W 1%	Rohm Semiconductor	MCR03ERTF4700	0603 (1608 metric)
R5	Resistor, Chip	1M-Ohm	Panasonic - ECG	ERJ-2GEJ105X	0402 (1005 Metric)
D1	Diode,Schottky	40V 1A	Vishay/ Semiconductors	VS-MBRS140TRPBF	DO-214AA, SMB
D2	Diode,Schottky	60V 1A	Vishay/ Semiconductors	VS-10BQ060TRPB F	DO-214AA, SMB
D3	LED	523nM Green clear	Avago Technologies	HSMM-A100-S00J1	PLCC-2
L1	Inductor	0.68 uH 614mA Shielded	API Delevan	S1210R-681K	1210 (3225 Metric)
L2	Inductor	220 uH 320mA Shielded	API Delevan	SPD62R-224M	SPD-62
J2	Header, Pin Array	252 Pin 1.0mM Pitch	Advanced Interconnections	10484PT	BGA-252
J3	Connector, Aurora	2x17 Pin 0.8mM Pitch	Samtec	ASP-137973-01	SMT - Special
J4	Connector	2 pos 2mm	JST	S2B-PH-SM4-TB(LF)(SN)	SMT - Special
J5	Header, JTAG	2x7 Pin 2.54mM Pitch	FCI	67996-114HLF	Through - Hole
J1	Socket, Receiver	292 Pin 0.8mM Pitch	Advanced Interconnections	10278PT	BGA-292
U1	IC	REG LDO 1.25V 0.15A	STMicroelectronics	LD39015M125R	SOT-23-5

Table continues on the next page...

U2	Voltage Regulator	4.5-40V DC/DC Conv. 0.5A	National Semiconductor	LM2594M-3.3/ NOPB	SOIC-8
Y1	Crystal	20MHZ 8PF	NDK	NX5032GA 20MHZ AT-W	2-SMD

A.1.3 Trace Adapter drawing

Dimensions of the MPC5746R Trace Adapter (TA) are shown in the following figures.

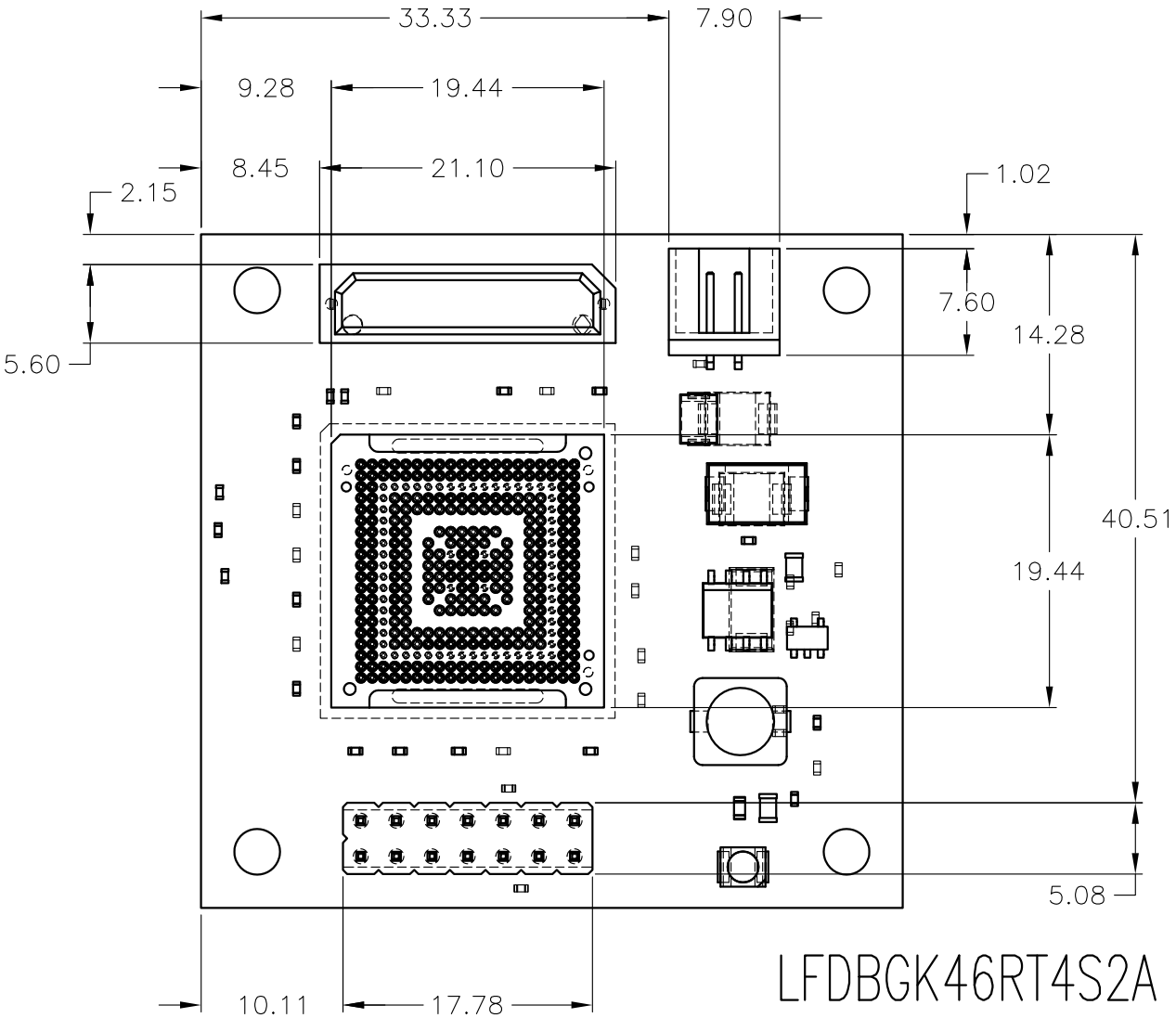

Figure A-5. MPC5746R 252 BGA Trace Adapter dimensions (top)

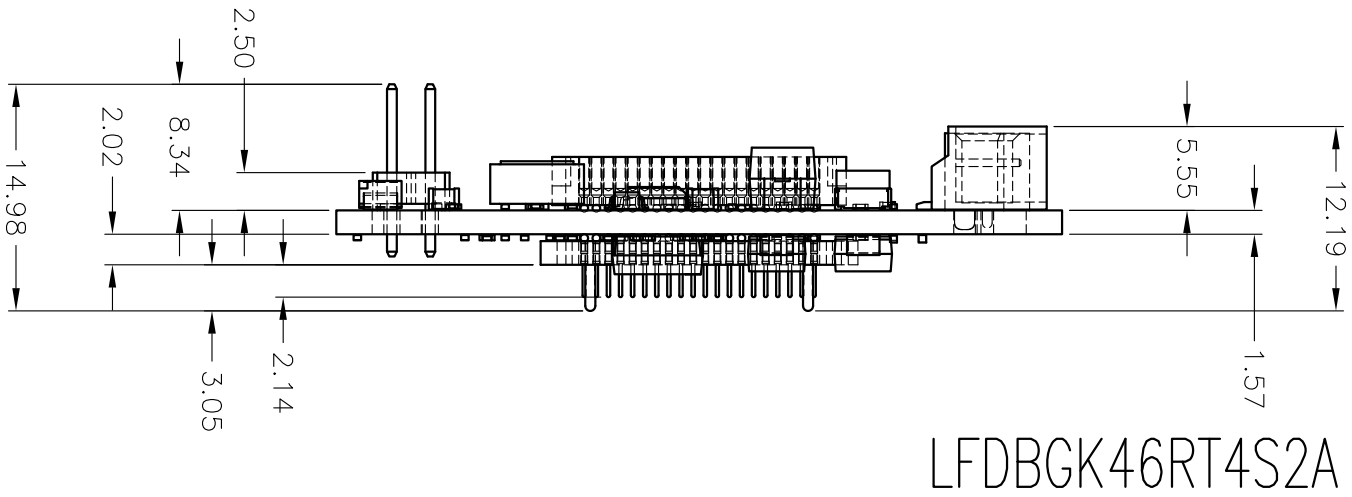

Figure A-6. MPC5746R 252 BGA Trace Adapter dimensions (side)

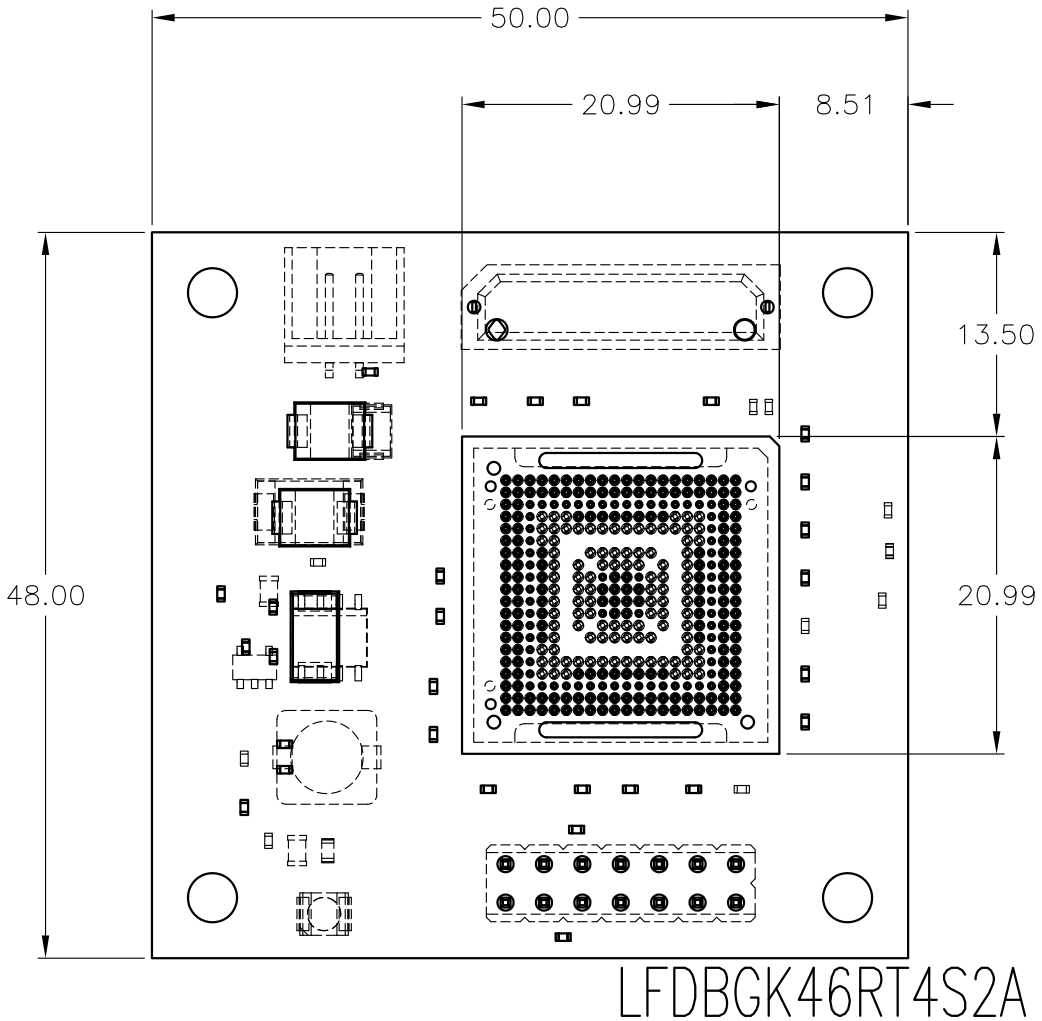

Figure A-7. MPC5746R 252 BGA Trace Adapter dimensions (bottom)

A.1.4 Receiver drawing - 252 BGA

The MPC5746R Trace Adapter (TA) requires that a 252-pin BGA receiver be mounted in the target system. The receivers purchased from Freescale include three (3) alignment holes to assist in plugging the TA into the target board receiver. The receiver is shown in the following figure, including the holes for the guide (alignment) pins (marked "G" in the drawing). The guide pins prevent the TA from being inserted into the receiver rotated. The receiver is soldered into the target system similar to the standard BGA device.

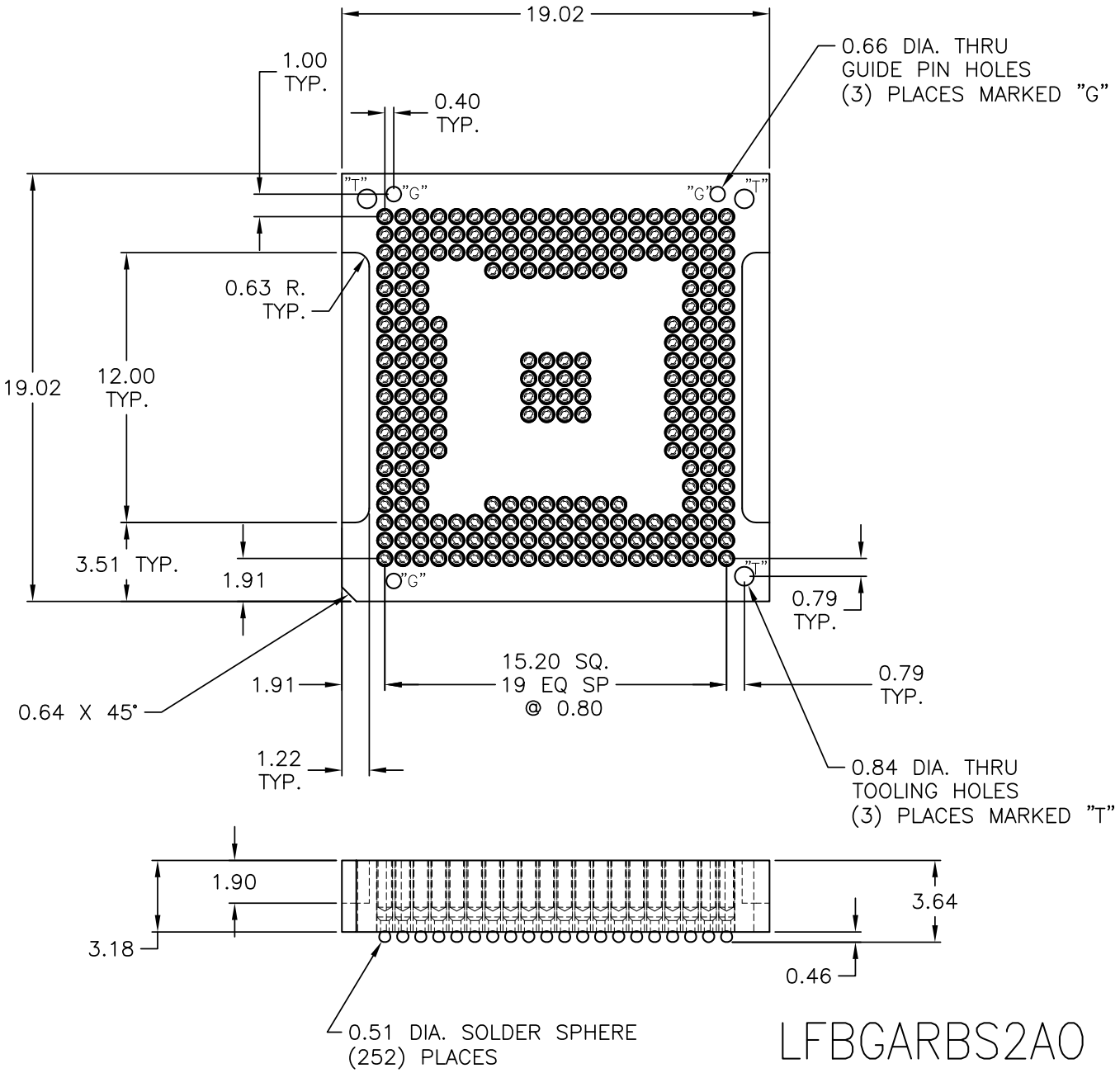

Figure A-8. 252-pin BGA receiver

A.1.5 292 BGA to 252 BGA stack drawing

The figure below shows the dimensions of the MPC5746R 252 BGA Trace Adapter (TA) mounted on the 252 BGA receiver.

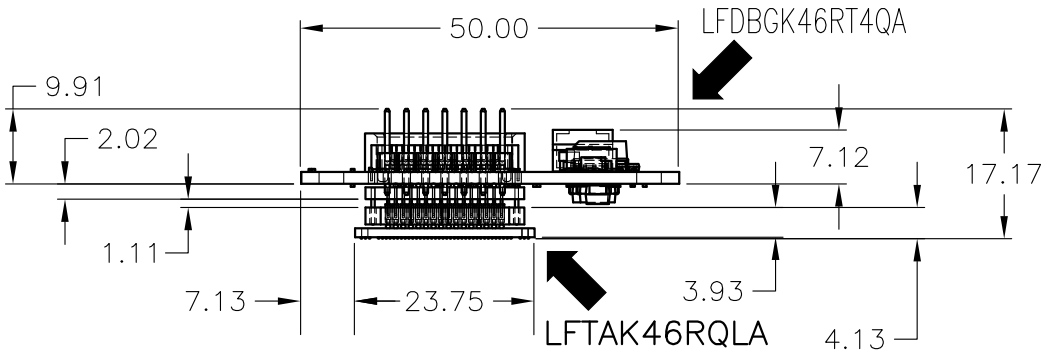

Figure A-9. 292 BGA to 252 receiver stacked drawing

A.2 208 BGA Trace Adapter (for 144 and 176 LQFP)

This section includes the component layout file for the 208 BGA Trace Adapter (TA) and the side view of the TA stacked with the 208 to 176 that is used to match the TA to either the 144 LQFP or 176 LQFP package footprints.

A.2.1 208 PGA Trace Adapter drawing

Dimensions of the MPC5746R 208 pin-grid array (PGA) Trace Adapter (TA) are shown in the following figures.

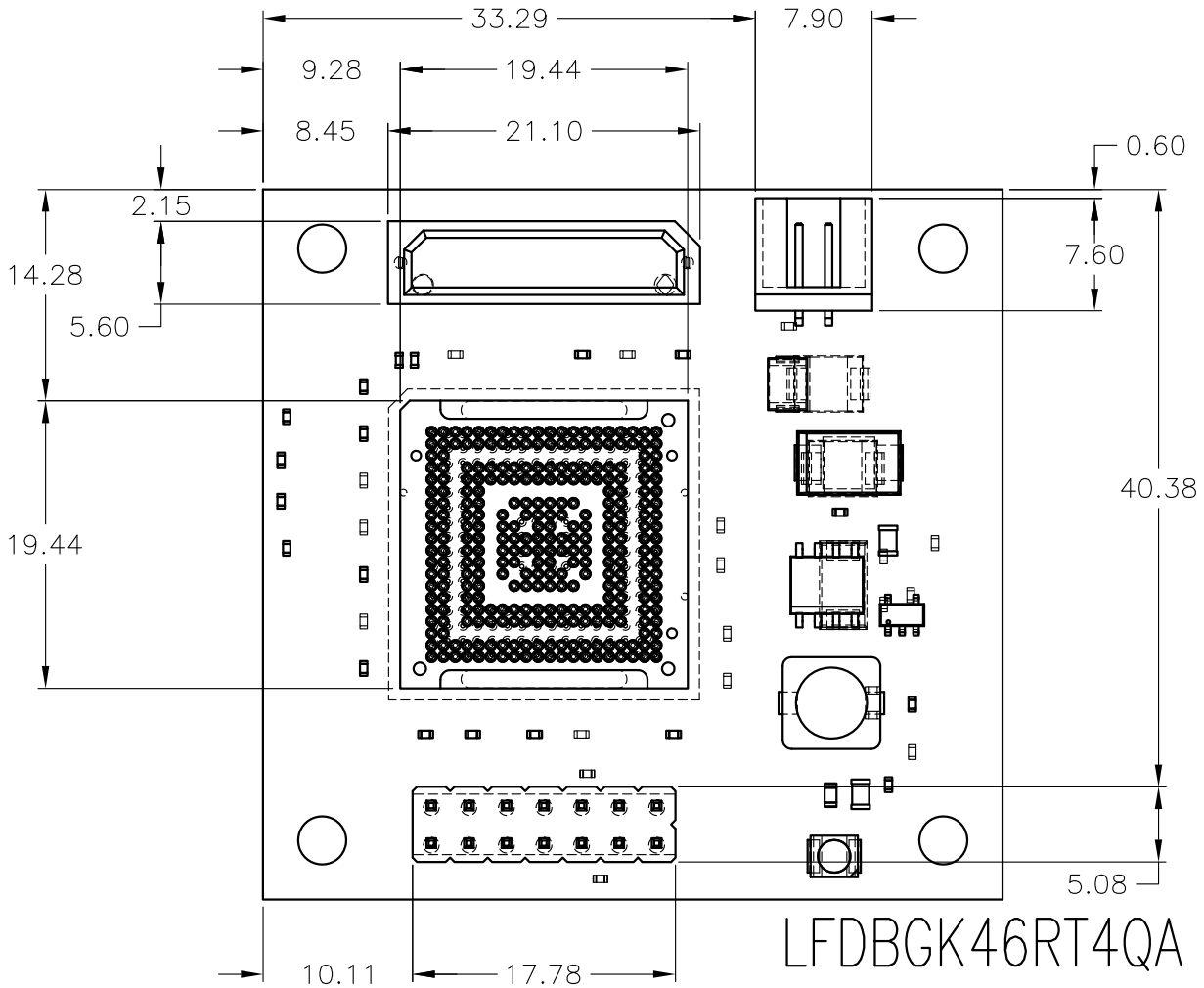

Figure A-10. MPC5746R 208 BGA Trace Adapter dimensions (top)

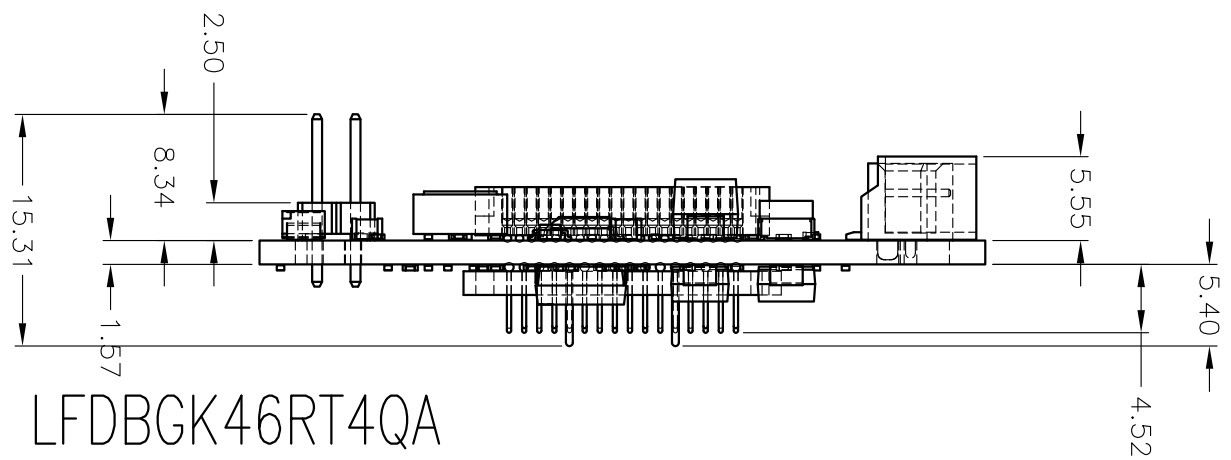

Figure A-11. MPC5746R 208 BGA Trace Adapter dimensions (side)

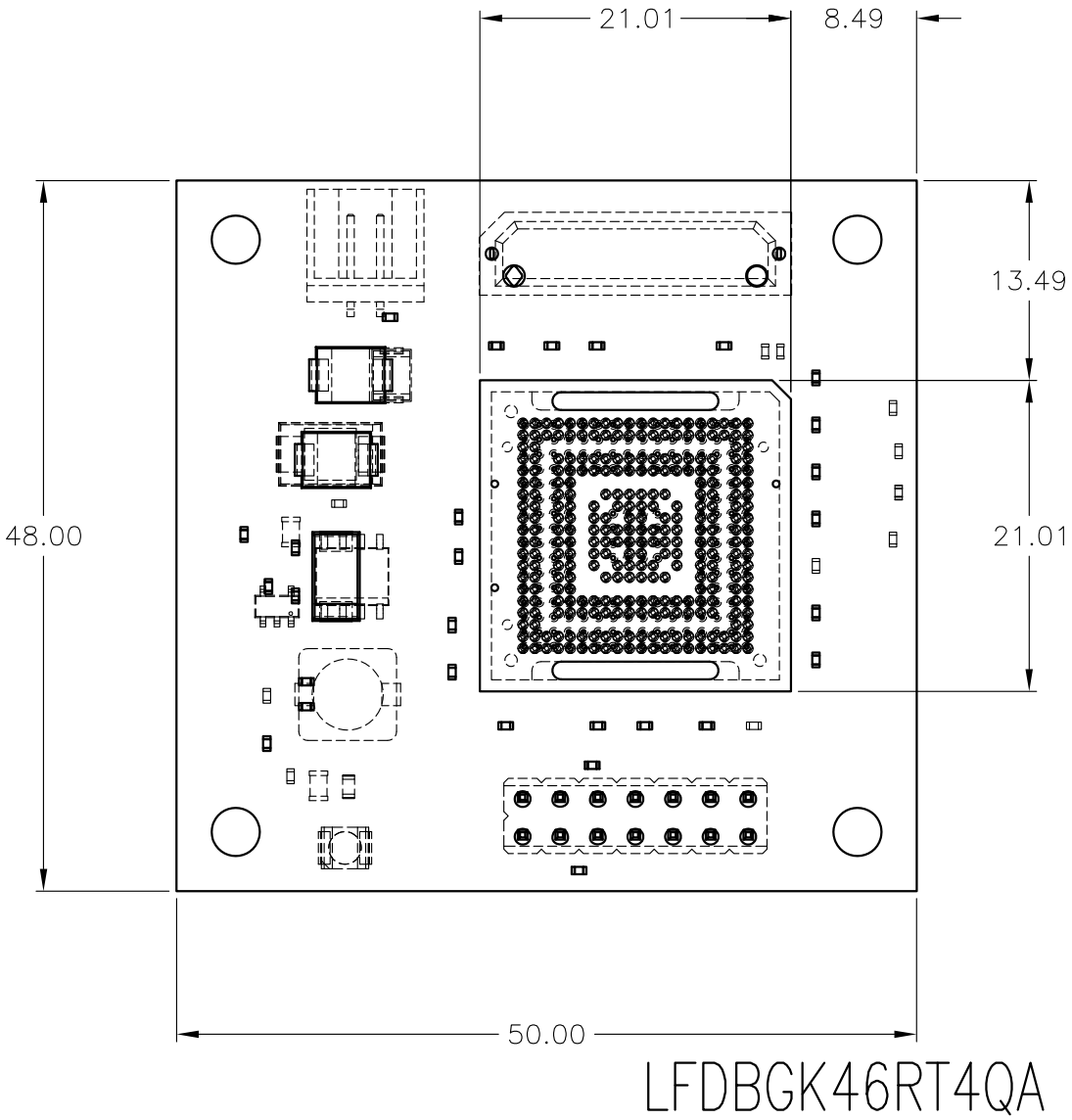

Figure A-12. MPC5746R 208 BGA Trace Adapter dimensions (bottom)

A.2.2 Adapter 208 BGA to 176 or 144 LQFP

The 208-pin Trace Adapter (TA) inserts into a second adapter to match either the 176-pin or 144-pin LQFP packages. An example schematic of the 208 to 176 adapter is shown in section Schematic 208 to 176 adapter. The bottom side of this 208 to 176/144 adapter has solder balls that match the footprint of either the 176-pin or the 144-pin LQFP package. The 208-pin to 176-pin adapter dimension drawing is shown in the following figure.

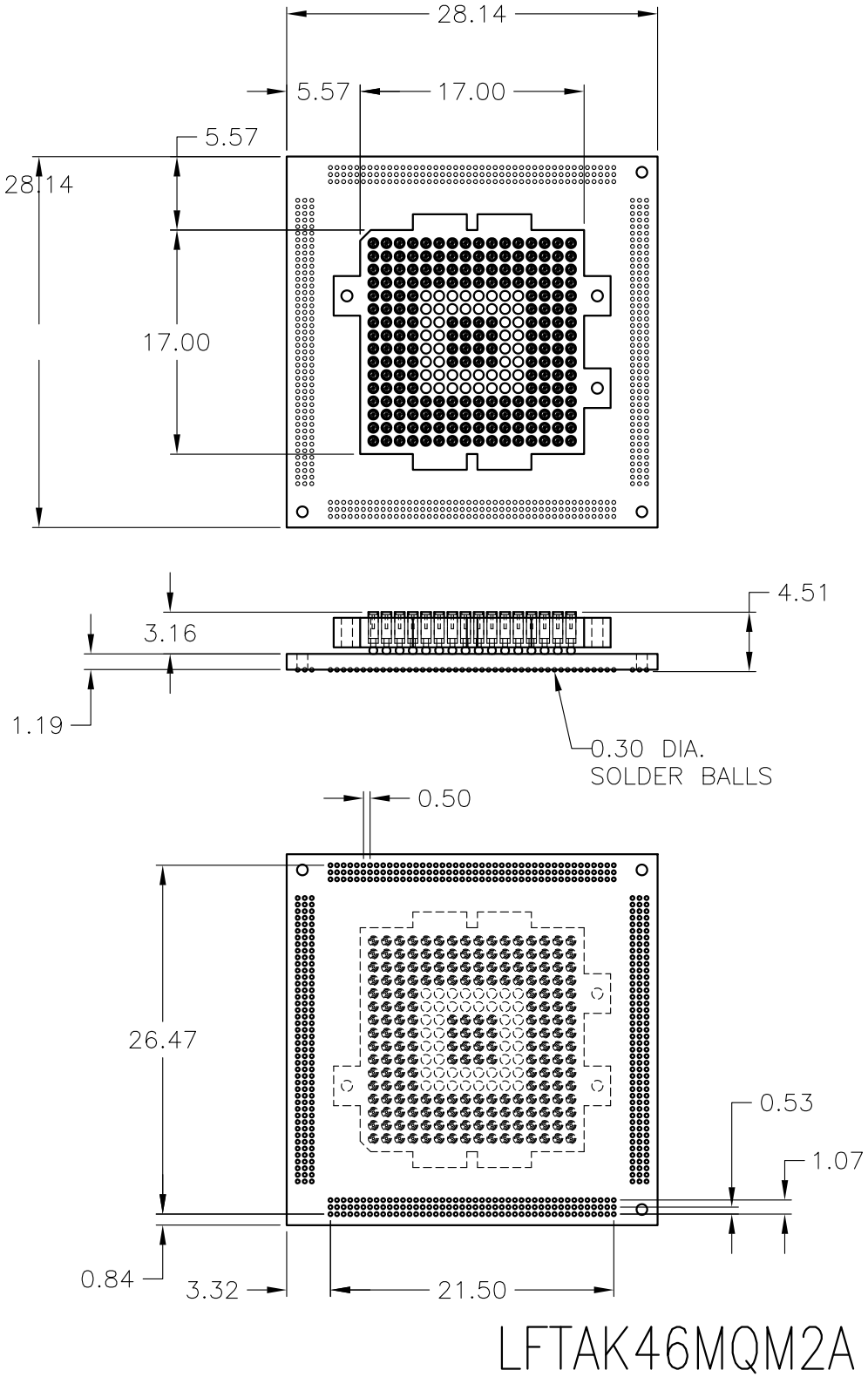

Figure A-13. 208 BGA to 176 LQFP adapter

The 208-pin to 144-pin adapter dimension drawing is shown in the following figure.

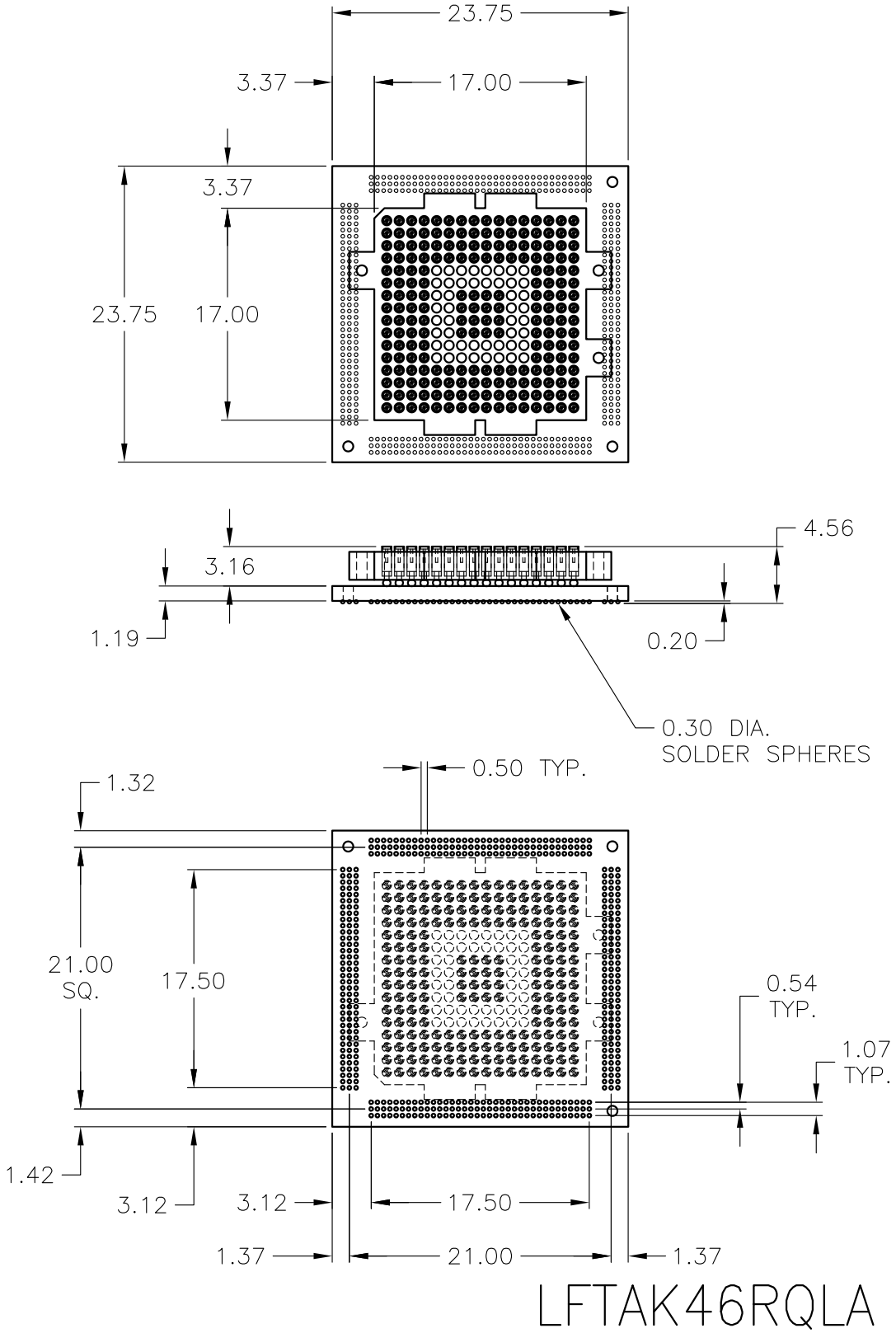

Figure A-14. 208 BGA to 144 LQFP adapter

A.2.3 208 PGA to 176/144 stacked drawings

The figure below shows the stacked view of the 208 PGA Trace Adapter (TA) with the 176 target adapter.

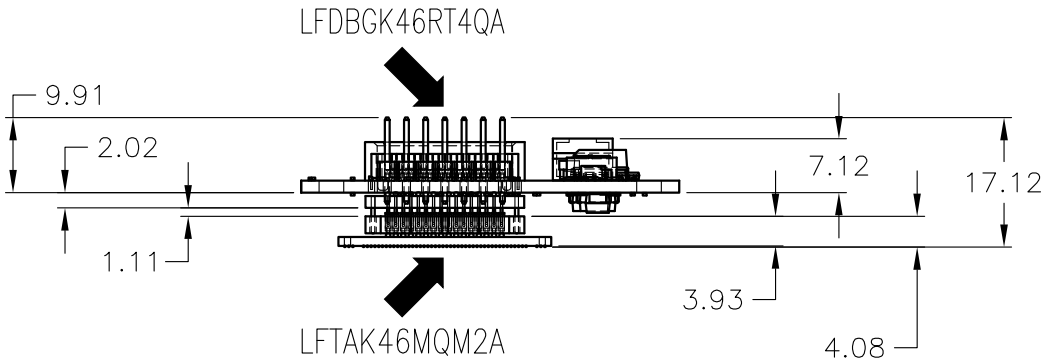

Figure A-15. 208 PGA stacked with the 176 target adapter dimensions

The 208 PGA TA with the 144 LQFP target adapter is shown in the following figure.

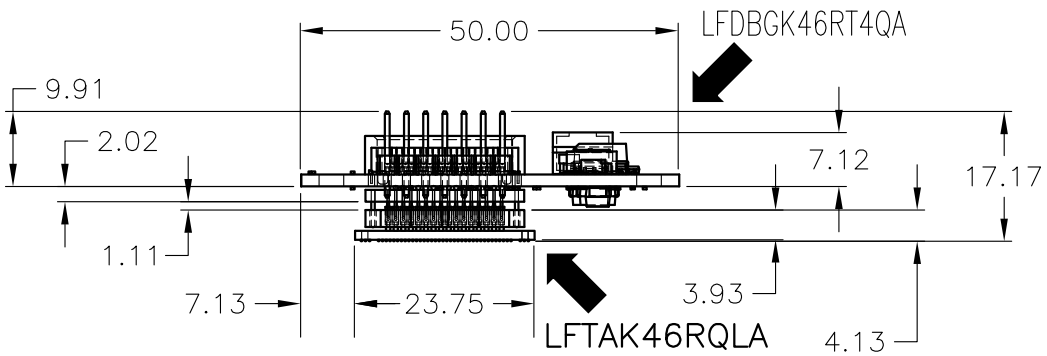

Figure A-16. 208 PGA stacked with the 144 target adapter dimensions

A.2.4 Schematic 208 to 176 adapter

A single adapter is used to convert the 292-pin MPC5746R Emulation Device (ED) to the QFP footprint for both the 176 LQFP and the 144 LQFP packages. The figures below show the schematic (mapping of the 208-pin BGA footprint to the 176 LQFP. The 208 BGA to 144 LQFP is similar and not shown.

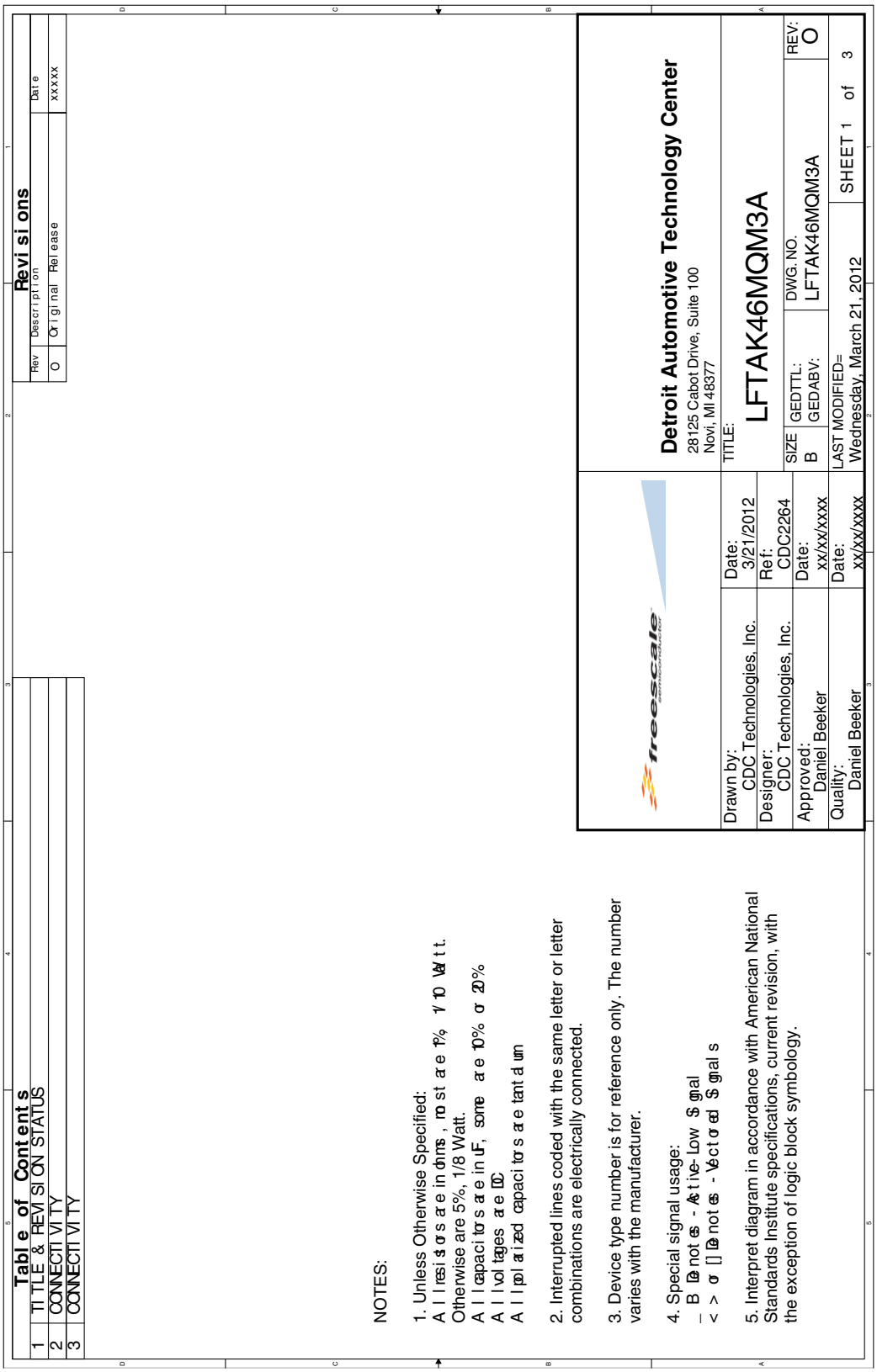

Figure A-17. 208 to 176 adapter (page 1)

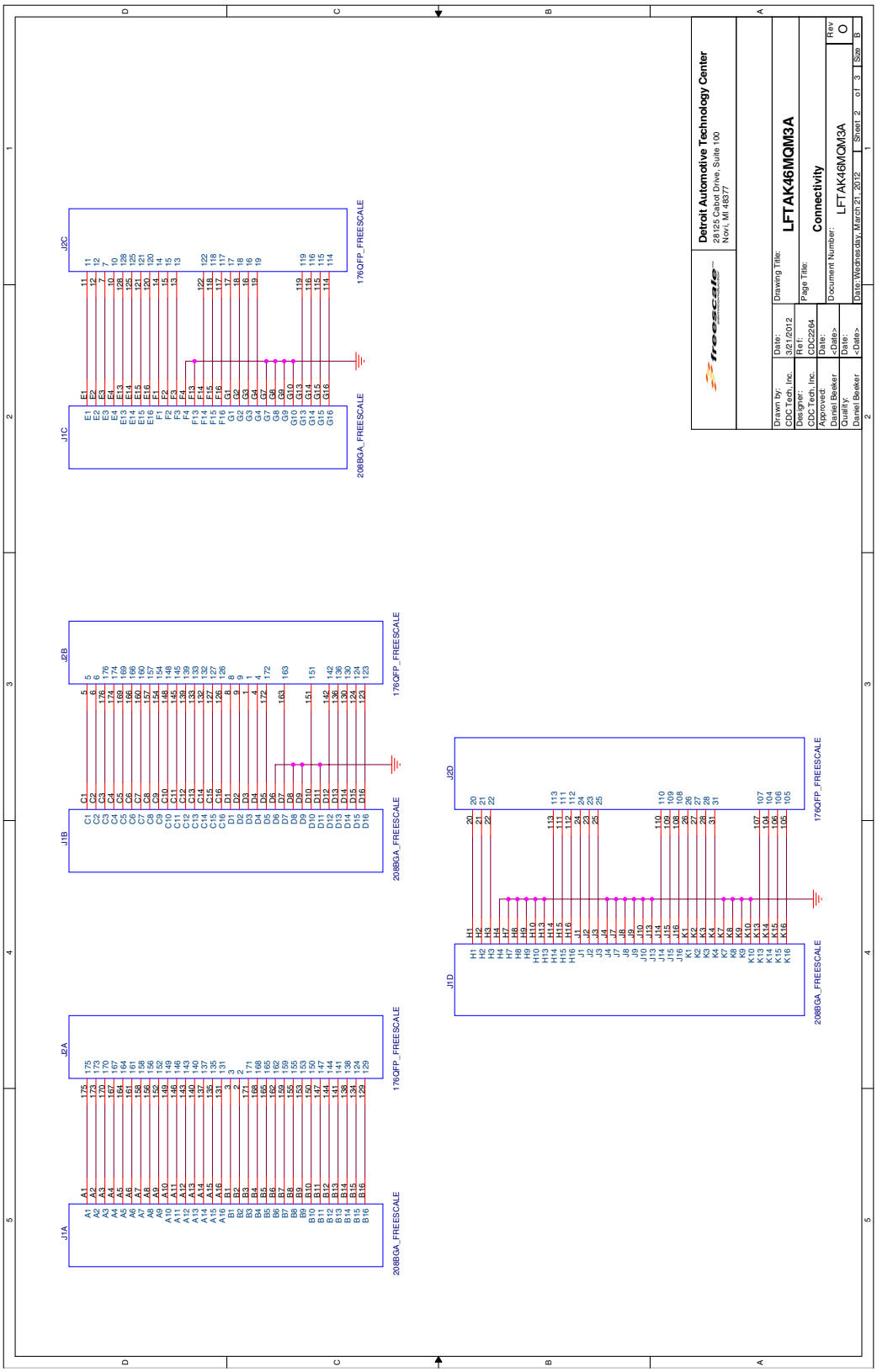

Figure A-18. 208 to 176 adapter (page 2)

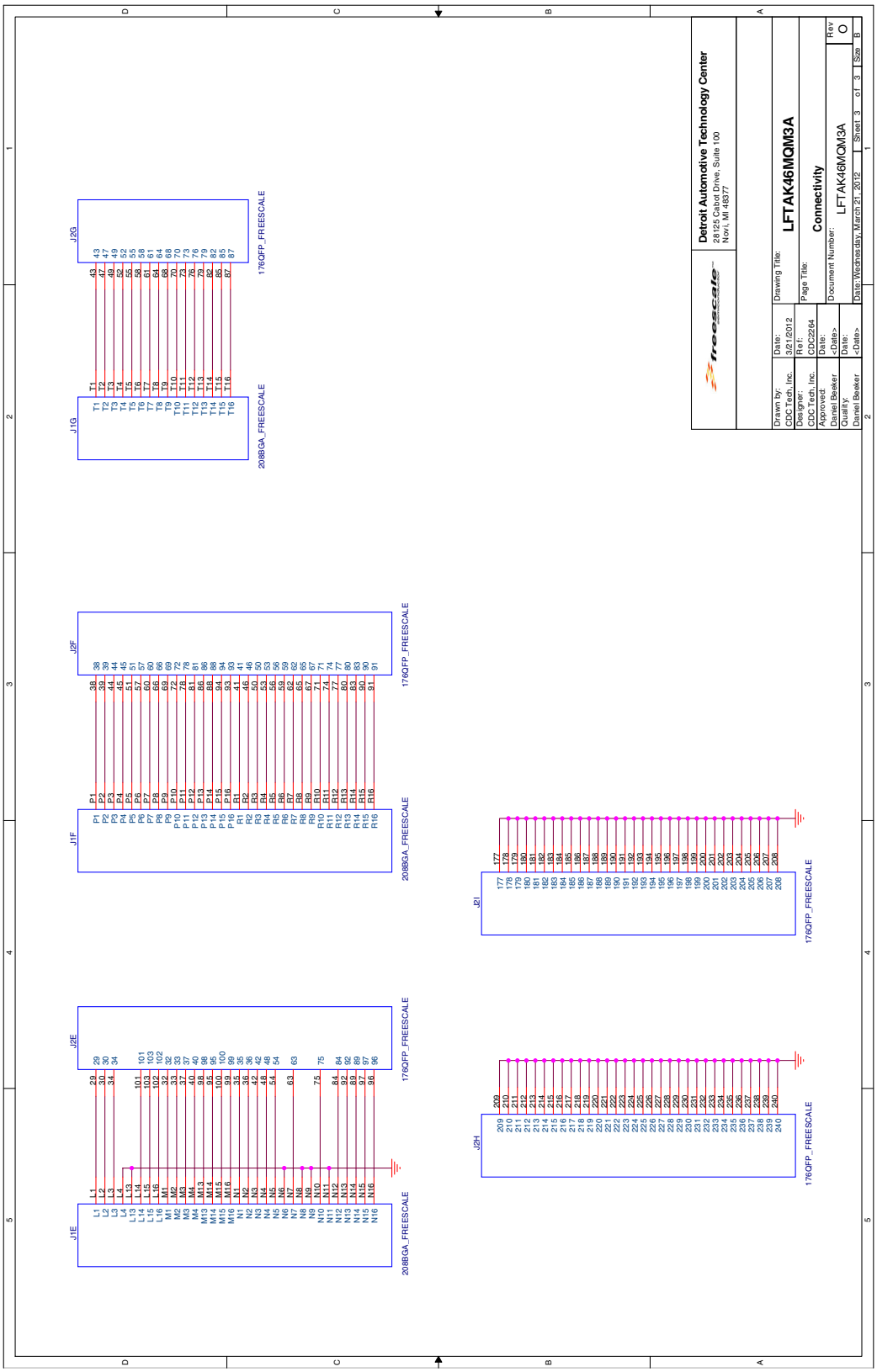

Figure A-19. 208 to 176 adapter (page 3)

Appendix B Debugging Emulation Devices with Lauterbach TRACE32

The emulation devices allow debuggers to connect to the Buddy Die (BD) separately in the case that the Production Die (PD) inside the ED is not yet powered. The script below shows a connection to the BD with the PD disabled.

Here is an example sequence for the MPC5746R. This script defines the device type and assigns both cores to a single instance of the Lauterbach TRACE32 software. Optionally, this sequence can be modified to use the START32 environment for independent instances of the TRACE32 software for each core. The CORE.ASSIGN command would be commented out and the SYStem.CONFIG command would need to be uncommented.

```
;--------------------------------
; Initialize the MPC5746R Emulation Device
; rd 24 October 2013/August 2015
; Assumes that power to the PD is off.
; Initializes 1M of overlay/trace memory
; Opens memory windows on the SRAM and on the SIUL MIDR register area.
;--------------------------------

; make sure system is not connected.
SYStem.Down
; select the correct MCU type
SYStem.CPU MPC5746R
; SYStem.CPU MPC5777M

; Control all cores in a single window
CORE.ASSIGN 1 2 ; MPC5746R
; CORE.ASSIGN 1 2 3 ; MPC5777M
;SYStem.CONFIG.CORE 2. 1. ; MPC5746R - multiple window use with START32
;SYStem.CONFIG.CORE 3. 1. ; MPC5777M - multiple window use with START32

;Make sure the PD is not powered
; Power the MPC5746R Trace Adapter from a separate supply (or prior to switch
; and leave power switch off)
; on the MPC5777M EVB, remove LV_CORE jumper from board
;
 SYStem.Mode.Prepare
```

This will then allow the SRAM on the BD to be accessed through the BD Nexus Read/Write Access client (NRWA). The TRACE32 memory class EEEC uses the NRWA client on the BD to access memory located on the BD. There is also a reduced size System Integration Unit Lite instantiated on the BD that contains registers for identifying the BD and for determining the status of the PD. The SIUL Device Identification registers (1 and 2) show the BD part number, mask revision information, SRAM size, and which BD device is assembled into the Emulation Device.

```
;now you can access BD memory and BD DCI registers
; the debugger reacts similar to when the core is running,
;i.e. you need /DualPort option
;or an extra "E" for the access classes
  NEXUS.Register , /DualPort; read the BD SIUL DIDR registers
  Data.dump EEEC:0xc800000
; Initialize the ECC in the BD SRAM
  Data.Set EEEC:0x0C000000--0x0C0FFFFF %Long 0x11223344
;read the BD SRAM space
  Data.dump EEEC:0x0C000000

ENDDO
```

The figure below shows a memory dump of the DIDR registers of a MPC5746R Emulation Device.

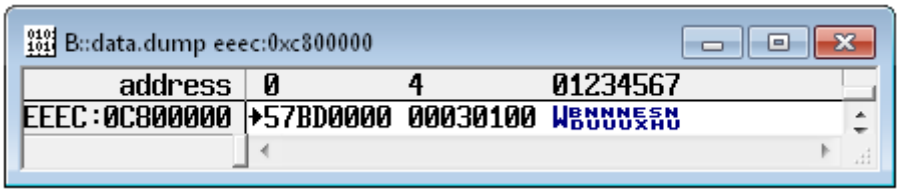

Figure B-1. Trace32 window showing DIDR1 and DIDR2 of the BD

Table B-1. Decoded DIDR1 and DIDR2

Address	Field	Bits	Value	Description
0x0C80_0000	PARTNUM	0:15	57BD	The MPC57BD family of Buddy die
	MASK_MAJOR	24:27	0x0	The initial major revision.
	MASK_MINOR	28:31	0x0	The initial minor revision.
0x0C80_0004	RAM_SIZE	12:15	0x3	1M byte
	PARTNUM	16:23	0x01	Buddy Device 1

At this point the PD can be powered, however, it may be desirable to power up the device with RESET asserted to allow debugger access to the device prior to executing code on the device. This is shown in the following example.

```
; Command file to run after configuring the BD in an emulation device
; rd 24 October 2013/August 2015

LOCAL &PON
;to make the transition from Prepare to up, assert reset
JTAG.PIN NRESET Low

;now power up the PD
; MPC5746R Switch on the EVB power, Trace Adapter powered by 12V supply
;(MPC5777M EVB - connect LV_CORE on board)

; Prompt to turn power on
REPEAT
(
DIALOG.YESNO "Turn on power to the PD in the Emulation Device"
ENTRY &PON
)
WHILE !&PON
IF &PON
(

;attach debugger to core -> status shows running (inactive)
  SYStem.Mode.Attach

;issue debug request
  Break

;release reset
  JTAG.PIN NRESET High

CORE 1
; -> core halted at reset vector, show program code:
  Data.List
; Enable read access to the BD memory space
  Data.Set EA:0xfc030008 %long 0x100000

; view the MIDR register of the PD
  Data.dump EA:0xFFFC0000
)
```

```
ENDDO
```

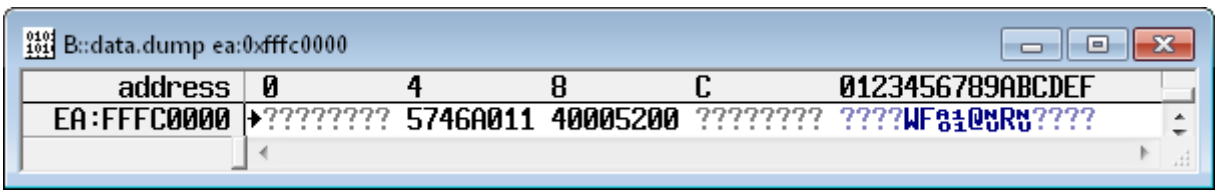

Figure B-2. TRACE32 window showing MIDR1 and MIDR2 of the PD

Table B-2. Decoded MIDR1 and MIDR2

Address	Field	Bits	Value	Description
0xFFFC_0004	PARTNUM	0:15	5746	MPC5746 part of MPC5746R
	ED	16	0b1	Emulation Device
	PKG	17:21	0b0_1000	292 MAPBGA package
	MASK_MAJOR	24:27	0x1	The initial major revision.
	MASK_MINOR	28:31	0x1	The initial minor revision.
0xFFFC_0008	Manufacturer	0	0b0	Freescale Semiconductor
	FLASH SIZE_1	1:4	0b1000	4 MBYTE of Flash
	FLASH_SIZE_2	5:7	0b0000	Needs to be combined with FLASH_SIZE_1 to calculate the size of the Flash = 0 x (Flash_SIZE_1 / 8)
	PARTNUM	16:23	0x52	ASCII "R" character of MCU Part Number MPC5646R

This section was written with assistance from Reinhard Weiß, Lauterbach GmbH.

Appendix C Debugging the MPC5746R Emulation Device with the PLS UDE

The PLS Universal Debug Engine (UDE) debugger can make a connection to the Buddy Die in the MPC5746R Emulation device, even with the Production Die un-powered. This is primarily used for Automotive calibration, but can be very helpful during normal debug as well.

To connect the debugger to the BD with the PD un-powered (called ‘Cold Start’), start with default UDE configuration and modify it via Menu Config->Target Interface following the steps below.

1. Select the ‘KeepRunning’ option in the connect pull down menu to allow a "hot attach" to the target device in the PowerPC JTAG Target Interface Setup window.

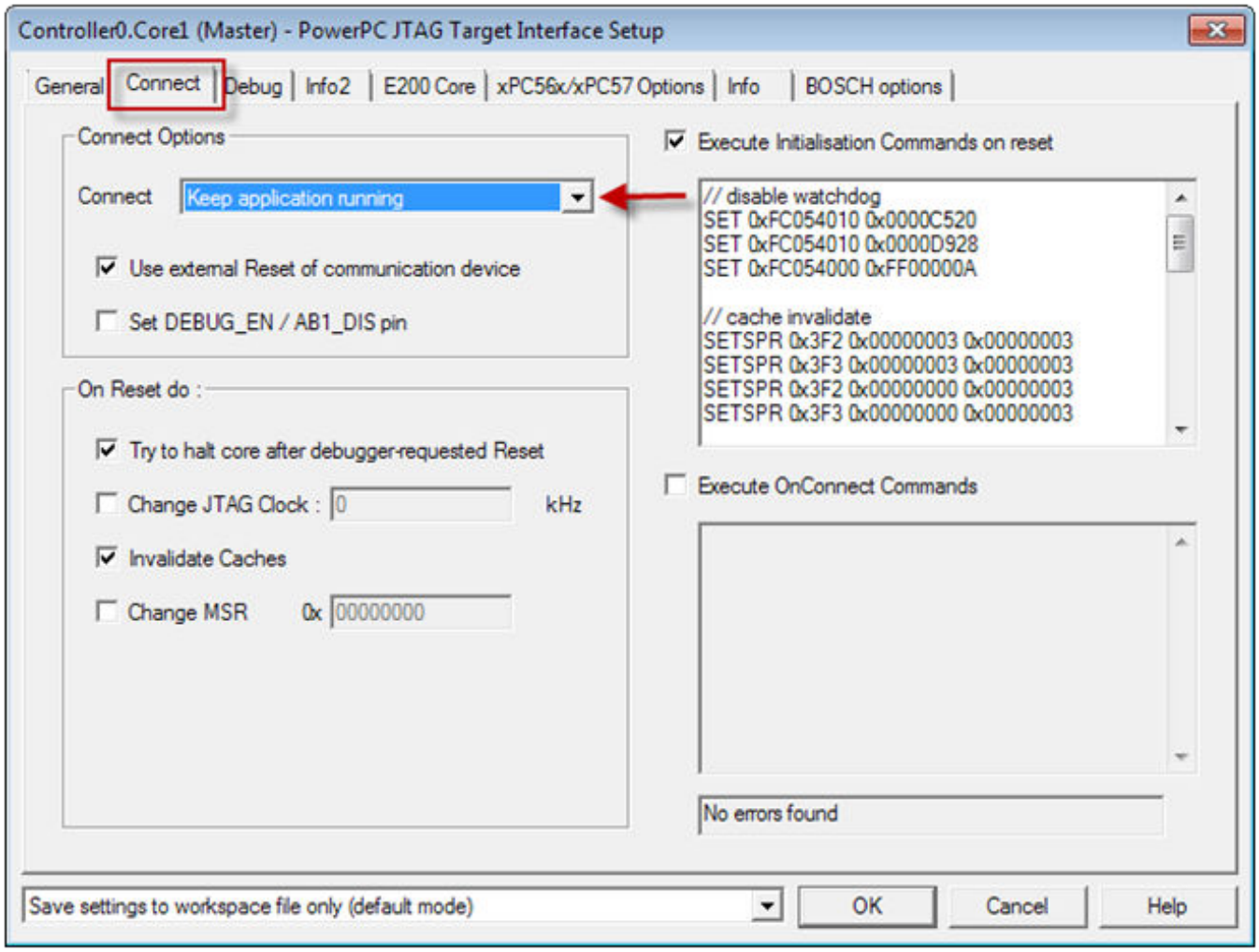

Figure C-1. Target Interface Setup

2. Disable the check for the device JTAG ID, since the JTAG ID of the PD can not be read when the PD in the Emulation Device is not powered:

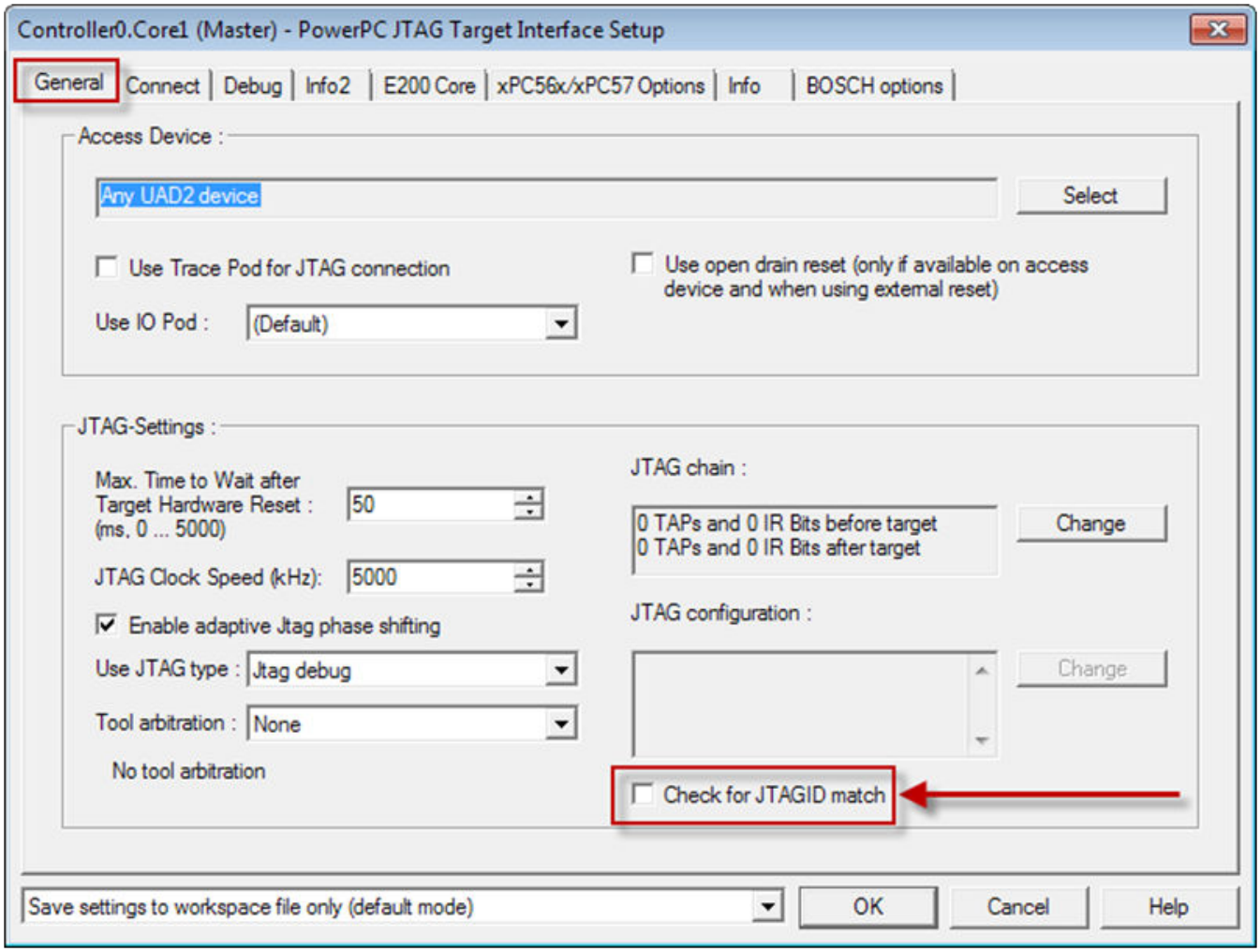

Figure C-2. Disable JTAG ID check

With these settings, a connection to the powered BD can be made. The UDE detects the "Cold Start" condition and both cores of the production device are shown as "inactive".

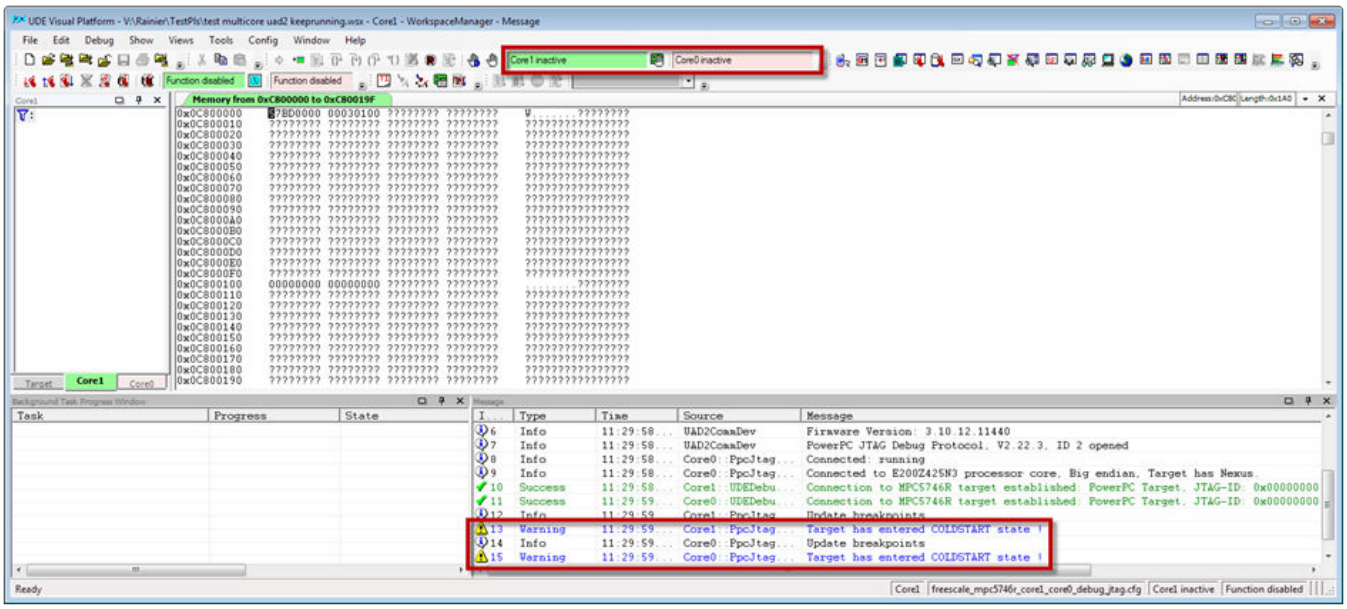

Figure C-3. Cold Start

In this state, the UDE is using the BD Nexus Read/Write Access (NRWA) client to read and write memory of the BD.

Finally when applying power to the rest of the Emulation Device (power up the PD), the UDE recognizes the state change and shows the updated status.

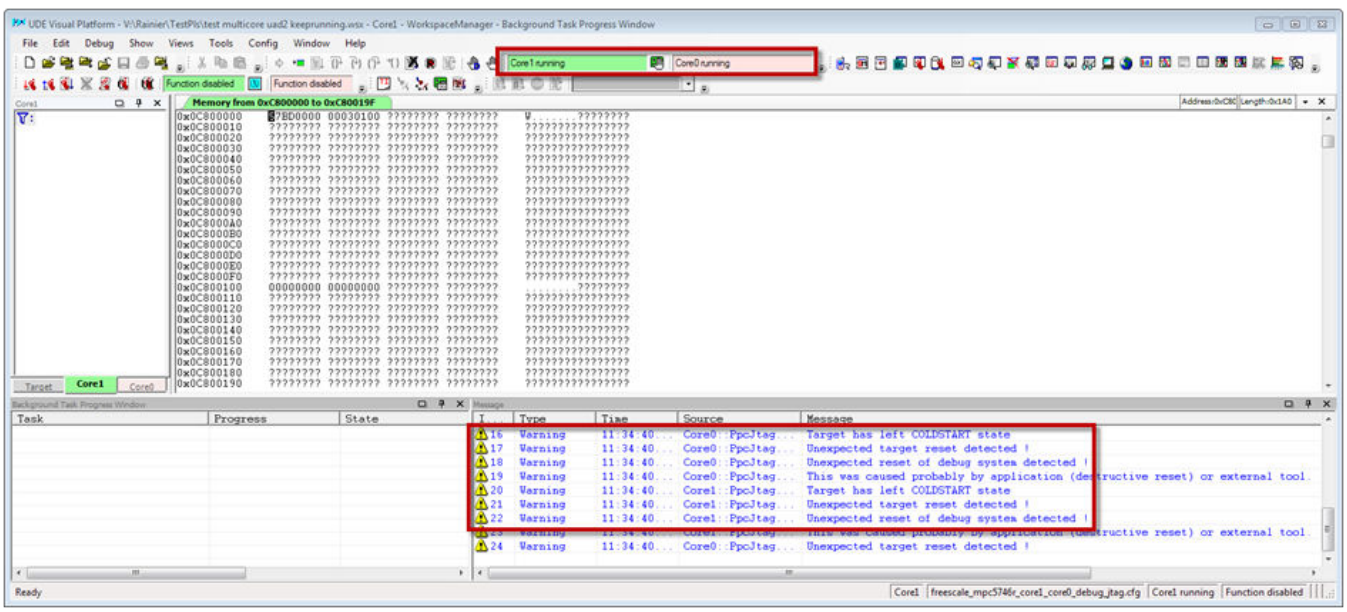

Figure C-4. Ready for debug

This section was written with assistance from Mathias Noack, PLS Programmierbare Logik & Systeme GmbH.

Appendix D MPC56xx and MPC57xx available Trace Adapters

Trace Adapters (TA) are available for a number of devices in the MPC56xx and MPC57xx families of devices. The following table shows TAs that are available. Drawings of these adapters, receivers, and TAs are available by searching the Freescale web site for the part numbers shown.

NOTE

The MPC55xx family of devices implement VertiCal, which can also be used as a TAs for those devices. However, the Nexus/debug connector is on a separate board that plugs into the VertiCal stack. A VertiCal stack can consist of the MCU VertiCal, a trace connector board, and an SRAM board.

Table D-1. Supported Trace Adapters

Device	Trace Adapter part number	Production Package footprint	Adapter	Receiver
MPC560xB	LFMAJO4QJM[1] LFMAJO7QJM[2]	64 LQFP	LFTAJ56E2T	LFTQSE2T
		100 LQFP	LFTAJ56HT	LFTQSHT
		144 LQFP	LFTAJ56LT	LFTQSLT
		176 LQFP	LFTAJ56M2T	LFTQSM2T
MPC560xE	LFMAJ04EE2M	64 LQFP	LFTAJ56EE2T	LFTQSE2T
	LFMAJ04EHM	100 LQFP	LFTAJ56EHT	LFTQSHT
MPC560xP	LFMAJ04PLHT	100 LQFP	Not required	LFTQSHT
	LFMAJ04PLT	144 LQFP	Not required	LFTQSLT
MPC5643L	LFMAJ43LT3LT	144 LQFP	Not required	LFTQSLT
	LFMAJ43LT3A	257 PBGA	Not required	LFBGARBT3AO
MPC5646C	LFMAJ46CS1A	256 PBGA	Not required	LFBGARBS1AO
	LFMAJ46CS1NT	208 LQFP	Not required	LFTQSNT
		208 PBGA	LFTAJ46CNQA	LFBGARBQAO
		176 LQFP	LFTAJ46CNM2T	LFTQSM2T
		144 LQFP	LFTAJ46CNLT	LFTQSLT
MPC5676R	LFJ76DBGWSA	416 PBGA	Not required	LFBGARBWAO
MPC574xG	LFMAK48GU3M	100 PBGA	LFTAK48GH1A	LFBGARBH1AO
		176 TQFP	LFTAK48GM2T	LFTQSM2T
		256 PBGA	LFTAK48GS1A	LFBGARBS1AO
	LFMAK48GU3U3A	324 PBGA[3]	Not required	LFBGARBU3AO
MPC574xR	LFDBGK46RT4QA	144 LQFP	LFTAK46RQLA	Not required
		176 LQFP	LFTAK46MQM2A	Not required
	LFDBGK46RT4S2A	252 MAPBGA	Not required	LFBGARBS2AO
MPC5775K	LFDBGK75KV1A	356 PBGA	Not required	LFBGARBV1AO
MPC5777C	LFDBGK77CWSA	416 PBGA	Not required	LFGARBWAO
	LFK77CIDBZ2W1A	422 PBGA	Not required	LFBGARBW1AO
MPC5777M	LFDBGK77MWA	416 PBGA	Not required	LFBGARBWAO
	LFDBGK77MZ3A	512 PBGA	Not required	LFBGARBZ3AO

1. Uses the MPC5604B die.
2. Uses the MPC5607B die.
3. This is a special (full array, 18x18) 324 PBGA pin out. Other tools/devices use a different 324 PBGA package in a 23x23 1.0 pitch array.

Table D-2. Trace Adapter complete part descriptions

Trace Adapter part number	Description
LFMAJ04QJM	MPC5604B 208 Pin 1.0mm PGA Nexus debug board
LFMAJ04PLHT	MPC560xP 100 pin QFP JTAG Debug Board
LFMAJ04EE2M	MPC5604E 64 Pin 0.5mm QFP JTAG Debug Board
LFMAJ04EHM	MPC5604E 100 Pin 0.5mm QFP Nexus Debug Board
LFMAJ04PLT	MPC5604P 144 Pin 0.5mm QFP Nexus Debug Board
LFMAJ43LT3A	MPC5643L 257 Pin 0.8mm PGA Nexus Debug board
LFMAJ43LT3LT	MPC5643L 257 Pin 0.8mm PGA to 144 Pin 0.5mm QFP Nexus Debug board
LFMAJ46CS1A	MPC5646C 256 Pin 1.0MM PGA Nexus Debug Board
LFMAJ46CS1NT	MPC5646C 256 Pin 1.0MM PGA to 208 Pin 0.5mm QFP Nexus Debug Board
LFJ76DBGWSA	MPC5676 416 Pin 1.0mm Calibration Adapter. Calibrate using special Samtec connector
LFMAK48GU3M	MPC5748G Nexus Debug board
LFMAK48GU3U3A	MPC5748G Nexus Debug board
LFDBGK46RT4QA	292 PIN 0.8MM BGA to 208 1.0MM PGA ADAPTER WITH Aurora interface FOR MPC5746R
LFDBGK46RT4S2A	292 PIN 0.8MM BGA to 252 0.8MM PGA ADAPTER WITH Aurora interface FOR MPC5746R
LFDBGK75KV1A	356 PIN 0.8MM BGA TO PGA ADAPTER WITH AURORA INTERFACE MPC5775K
LFDBGK77CWSA	MPC5777C 416 Pin 1.0mm Calibration Adapter. Calibrate using special Samtec connector
LFK77CIDBZ2W1A	MPC5777C Integrated Debug Board
LFDBGK77MWA	416 PIN 1.0MM BGA TO PGA ADAPTER WITH AURORA INTERFACE MPC5777M
LFDBGK77MZ3A	512 PIN 1.0MM BGA TO PGA ADAPTER WITH AURORA INTERFACE MPC5777M

Table D-3. BGA receivers

BGA receiver part number	Description	Pins	Pitch
LFBGARBH1AO	SURFACE MOUNT PGA SOCKET FOR 100 PIN 1.0mm VertiCal and Microcontrollers with pins	100	1.0mm
LFBGARBQAO	BGA base w/receiver 208 pin, 1.0mm pitch (lead-free)	208	1.0mm
LFBGARBS1AO	SURFACE MOUNT PGA SOCKET FOR 256 Pin 1.0MM VertiCal and Microcontrollers with pins	256	1.0mm
LFBGARBS2AO	SURFACE MOUNT PGA SOCKET FOR 252 Pin 0.8MM VertiCal and Microcontrollers with pins	252	0.8mm
LFBGARBT3AO	SURFACE MOUNT PGA SOCKET FOR 257 Pin 0.8MM VertiCal and Microcontrollers with pins	257	0.8mm
LFBGARBU3AO	SURFACE MOUNT PGA SOCKET FOR 324 Pin 1.0MM Microcontrollers with pins (19x19 packages only)	324	1.0mm
LFBGARBV1AO	SURFACE MOUNT PGA SOCKET FOR 356 Pin 0.8MM VertiCal and Microcontrollers with pins	356	0.8mm
LFBGARBW1AO	SURFACE MOUNT PGA SOCKET FOR 422 Pin 1.0MM VertiCal and Microcontrollers with pins	422	1.0mm
LFBGARBWAO	BGA base w/receivers 416 position, 1.0mm pitch (lead free)	416	1.0mm

Table continues on the next page...

Table D-3. BGA receivers (continued)

BGA receiver part number	Description	Pins	Pitch
LFBGARBZ3AO	SURFACE MOUNT PGA SOCKET FOR 512 PIN 0.8MM VertiCal and Microcontrollers with pins	512	1.0mm

Table D-4. Target Adapter complete part descriptions

Receiver part number	Description
LFGARBWAO	MPC5777C 416 BGA Target Adapter
LFMAJ07QJM	Nexus Debug Board, MPC5607
LFTAJ46CNLT	MPC5646C 144 QFP target adapter
LFTAJ46CNM2T	MPC5646C 176 Pin 0.5mm QFP target adapter
LFTAJ46CNQA	MPC5646C 208 Pin 1.0mm PGA target adapter
LFTAJ56E2T	64 LQFP Target adapter for MPC5600 devices
LFTAJ56EE2T	64 Pin target adapter for MPC5604E
LFTAJ56EHT	100 Pin target adapter for MPC5600E
LFTAJ56HT	100 LQFP target adapter MPC5600
LFTAJ56LT	144 LQFP target adapter MPC5600
LFTAJ56M2T	MPC5600 176 LQFP adapter board
LFTAK46MQM2A	208 pin 1.0mm PGA to 176 pin 0.5mm QFP target adapter board for MPC5746
LFTAK46RQLA	208 Pin 1.0mm pitch PGA to 144 pin 0.5mm QFP target adapter board for MPC5746R
LFTAK48GH1A	MPC57xx 100 Pin 1.0MM BGA Target Adapter Board.
LFTAK48GM2T	MPC57xx 176 Pin 0.5MM LQFP Target Adapter Board.
LFTAK48GS1A	MPC57xx 256 Pin 1.0MM PGA Target Adapter Board.
LFTQSE2T	64 pin 0.5mM QFP Surface Mount Target Interface Set
LFTQSHT	QFP Surface Mount target interface set - 100 pin 0.5mm (Lead free)
LFTQSLT	QFP Surface Mount target interface set - 144 pin 0.5mm (Lead free)
LFTQSM2T	176 PIN 0.5MM QFP Surface Mount Target Interface Set
LFTQSMT	QFP Surface Mount Target Interface Set, 160 PIN

Appendix E References

For more information on the device Trace Adapters and Nexus on the MPC57xx family of devices, see the specific device reference manual and the additional documents listed in the following table.

Table E-1. References

Document	Title	Location/Availability
e200z4RM	e200z4 Power Architecture Core Reference Manual	freescale.com
e200z759N3CRM	e200z759n3 Power Architecture Core Reference Manual	

Table continues on the next page...

Table E-1. References (continued)

Document	Title	Location/Availability
e200z760RM	e200z760 Power Architecture Core Reference Manual	
MPC5746RM	MPC5746R Reference Manual	
MPC5777MRM	MPC5777M Reference Manual	
AN2614	MPC553x, MPC555x, and MPC556x Family Nexus Interface Connector	
AN3968	Nexus Interface Connector for the MPC567xF and MPC5676R Families	
AN4088	Nexus Overview and Nexus Support for the MPC5500 and MPC5600 Families	
AN4224	MPC57xx Nexus Debug Connectors	
IEEE-ISTO 5001-1999	The Nexus 5001 Forum™ Standard for a Global Embedded Processor Debug Interface, Version 1	IEEE-ISTO Nexus web site http://www.nexus5001.org
IEEE-ISTO 5001-2003	The Nexus 5001 Forum™ Standard for a Global Embedded Processor Debug Interface, Version 2.0	
IEEE-ISTO 5001-2012	The Nexus 5001 Forum™ Standard for a Global Embedded Processor Debug Interface, Version 3	Available only to IEEE-ISTO 5001 Consortium Members
IEEE Std 1149.1-1990	IEEE Standard Test Access Port and Boundary-Scan Architecture	IEEE web site http://www.ieee.org

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number AN5181
Revision 0, September 2015