Freescale Semiconductor
Application Note

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S12ZVM Derivatives: Configuring PMF Module

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1 Introduction

The Pulse Width Modulator with Fault protection (PMF) is a specialized and versatile Pulse Width Modulator (PWM) module aimed for motor control. It has several features that allow smooth control of any 3-phase BLDC motor. The PMF module is capable of controlling most motor types: AC Induction Motor (ACIM), both brushless BLDC and brush DC motors, Switched Reluctance Motor (SRM), Variable Reluctance Motor (VRM), and stepper motors. It can also be used as a general purpose PWM module.

This application note focuses on showing how to configure the PMF module to achieve different output combinations.

Contents

2 PMF module overview

The PMF module can be configured for one, two, or three complementary pairs. All PWM outputs can be generated from the same counter, or each pair can have its own counter for three independent PWM frequencies. Complementary operation permits programmable dead-time insertion to avoid shortcuts. Each counter value is programmable to support a continuously variable PWM frequency. Both edge- and center-aligned synchronous pulse width-control and full range modulation from 0 percent to 100 percent are supported.

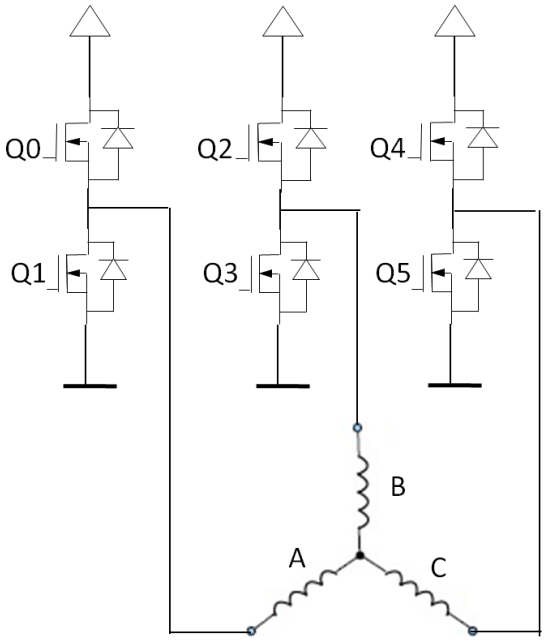

Figure 1-Typical 3-phase BLDC motor application

Figure 1 features a typical 3-phase BLDC motor application with "Q*n*" representing the PWM channel outputs of the PMF module.

3 Module initialization

This application note focuses on the different PMF's output configurations, therefore the initialization will be lightly covered, for a deeper understanding of the module initialization please refer to the reference manual of your device.

The example provided with this application note configures the module in the following manner for each of the available configuration:

Edge aligned mode, the PWM generator A generates the reload event (REV = 1), it is configured to reload and restart the PWM counter on every cycle (LDQFQA = 0 and RSTRTA = 1), the PWM counter runs at the core frequency (PRSCA = 0), a write to value register zero updates all the value registers (VLMODE = 1), the reload interrupt is enabled and the PWM generator A outputs are enabled (PWMRIEA = 1 and PWMENA = 1).

For almost all the configuration examples except for the bipolar configuration the registers are being buffered on commutation event with an external load ok enabled (ENCE = 1 and GLDOKA = 1), for the bipolar configuration the commutation event is not being used as the PINv registers are not buffered on commutation event.

4 Working modes

4.1 Independent high side fixed

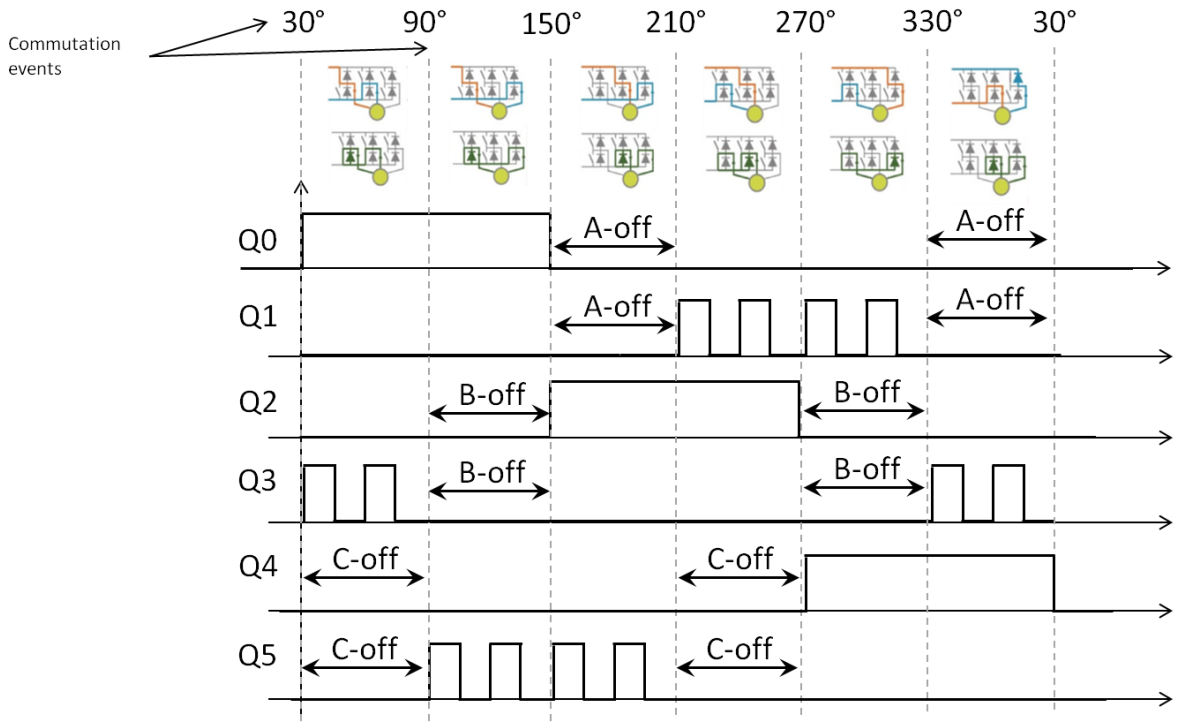

Figure 2- Independent high side fixed

In this configuration, the high side remains active throughout the corresponding phase. In the meanwhile the low side performs the pulse width modulation with the complementary channel turned OFF. This behavior can be observed in **Figure 2**.

This behavior is achieved by modifying the registers PMFCFG2_MSK, PMFOUTC and PMFOUTB as showed in **Table 1**.

PMFCFG2_MSK chooses which channel is capable of generating an output and which channels are turned-off or “masked”. There is a one to one correspondence between the bit position and the channel that it controls, that is to say, bit Q_0 controls Channel 0 and so on and so forth. Setting bit x to 0 will allow channel x to output the desired PWM signal and setting it to 1 will “mask” the channel by setting the duty cycle for that channel to be 0 (therefore turning off the channel output).

In **Table 1** it can be observed how Q_0 and Q_3 are the only enabled channels for the first commutation. This correlates with the expected behavior in **Figure 2**.

PMFOUTC_OUTCTL enables the control of the channel output with respect the PMFOUTB bits, namely, if OUTCTLx is enabled (value of 1) the output of channel x will be controlled by the value of PMFOUTBx. PMFOUTB can only set a channel to “active” or “inactive” (on or off respectively) therefore it serves as a mechanism to set the fix the output of a channel without modifying the duty cycle assigned to this channel.

It can be observed in **Table 1** how PMFOUTC is configured in a way such that Q_0 is being controlled by the value of PMFOUTB0 which in this case is set to 1 therefore activating channel 0.

PMFOUTB controls the outputs of the channels if the corresponding PMFOUTC_CTL bit is set, otherwise the value of PMFOUTB does not have effect on the output and this is solely driven by PMFCFG2_MSK.

In this example the high sides are being configured to become active (100 duty cycle) whenever the corresponding bit in PMFOUTCL is set and the output is not being masked by PMFCFG2_MSK as can be seen in **Table 1**, where in the first stage (30° - 90°) Q_0 is enabled by PMFCFG2_MSK (clear), PMFOUTC_CTL is enabled (set) and PMFOUTB is set as well.

Table 1 - High side fixed

Register	Bits	30°- 90°						90°- 150°						150°- 210°						210° - 270°						270° - 330°						330° - 30°					
PMFCFG2	Mask (PWM channels)	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0
	Value	1	1	0	1	1	0	0	1	1	1	1	0	0	1	1	0	1	1	1	1	1	0	0	1	1	0	1	1	0	1	1	0	0	1	1	1
	Value in hexadecimal	0x36						0x1E						0x1B						0x39						0x2D						0x27					
PMFOUTC	Mask (PWM channels)	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0
	Value	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0
	Value in hexadecimal	0x01						0x01						0x04						0x04						0x10						0x10					
PMFOUTB	Mask (PWM channels)	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0
	Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	Value in hexadecimal	0x15						0x15						0x15						0x15						0x15						0x15					

4.2 Independent low side fixed

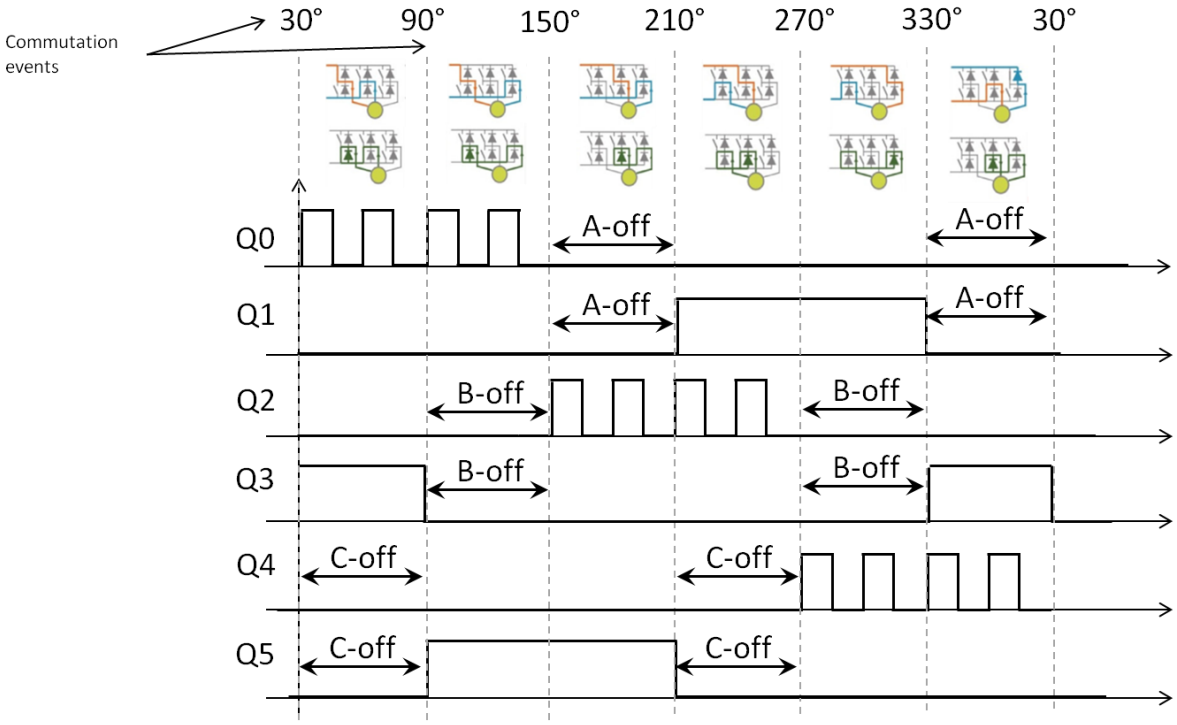

Figure 3- Low side fixed

In this configuration the low side remains active throughout the phase, meanwhile the modulation is being performed by the high side, as can be observed in **Figure 3**.

This behavior is achieved by following the same logic as in described in section **4.1**. The register configuration is shown in **Table 2**.

Table 2 - Low side fixed

Register	Bits	30°- 90°						90°- 150°						150°- 210°						210° - 270°						270° - 330°						330° - 30°					
PMFCFG2	Mask (PWM channels)	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0
	Value	1	1	0	1	1	0	0	1	1	1	1	0	0	1	1	0	1	1	1	1	1	0	0	1	1	0	1	1	0	1	1	0	0	1	1	1
	Value in hexadecimal	0x36						0x1E						0x1B						0x39						0x2D						0x27					
PMFOUTC	Mask (PWM channels)	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0
	Value	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0
	Value in hexadecimal	0x08						0x20						0x20						0x02						0x02						0x08					
PMFOUTB	Mask (PWM channels)	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0
	Value	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
	Value in hexadecimal	0x2A						0X2A						0x2A						0x2A						0x2A						0x2A					

4.3 Complementary high side fixed

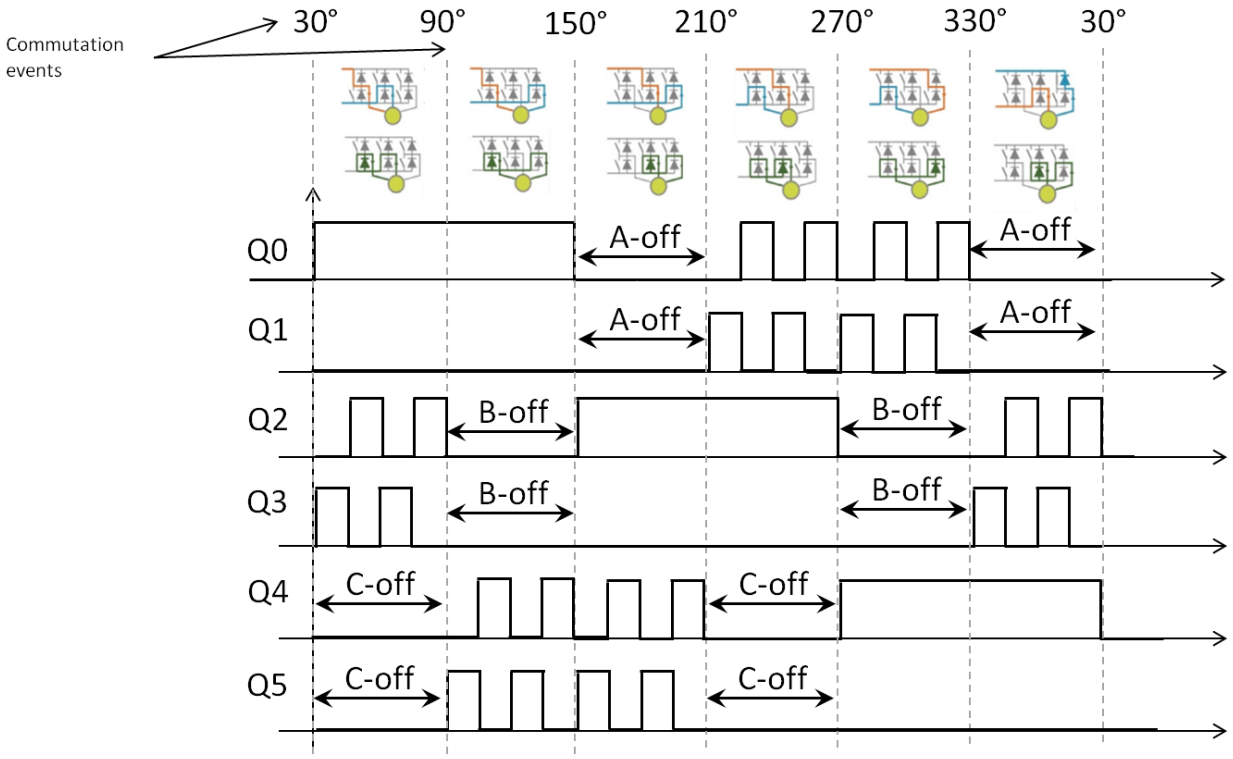

Figure 4 - High side fixed complementary mode

In this configuration the high side remains active throughout the phase, meanwhile the low side performs the modulation in complementary mode, in other words, once the low side goes to its inactive state the high side of the phase pair (i.e. Q_0-Q_1, Q_2-Q_3, Q_4-Q_5) goes to its active state. This allows a better power dissipation and decreases the temperature increment in the power MOSFETs.

In order to achieve this behavior the pairs that will act in complementary mode must be enabled simultaneously, such as in **Table 3**.

It can be seen how Q_3-Q_2 are being enabled by PMFCG2_MSK as well as Q_0, but in the case of Q_0 the control of the channel is being carried out by PMFOUTB, because PMFOUTC_CTL is being enabled for this channel. Since PMFOUTB0 is being set this means Q_0 will be in the active state and Q_1 will remain inactive.

Table 3 - High side fixed complementary mode

Register	Bits	30°- 90°						90°- 150°						150°- 210°						210° - 270°						270° - 330°						330° - 30°					
	Mask (PWM channels)	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0
PMFCFG2	Value	1	1	0	0	1	0	0	0	1	1	1	0	0	0	1	0	1	1	1	1	1	0	0	0	1	0	1	1	0	0	1	0	0	0	1	1
	Value in hexadecimal	0x32						0x0E						0x0B						0x38						0x2C						0x23					
	Mask (PWM channels)	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0
PMFOUTC	Value	0	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	0	0
	Value in hexadecimal	0x03						0x03						0x0C						0x0C						0x30						0x30					
	Mask (PWM channels)	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0
PMFOUTB	Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	Value in hexadecimal	0x15						0x15						0x15						0x15						0x15						0x15					

4.4 Complementary low side fixed

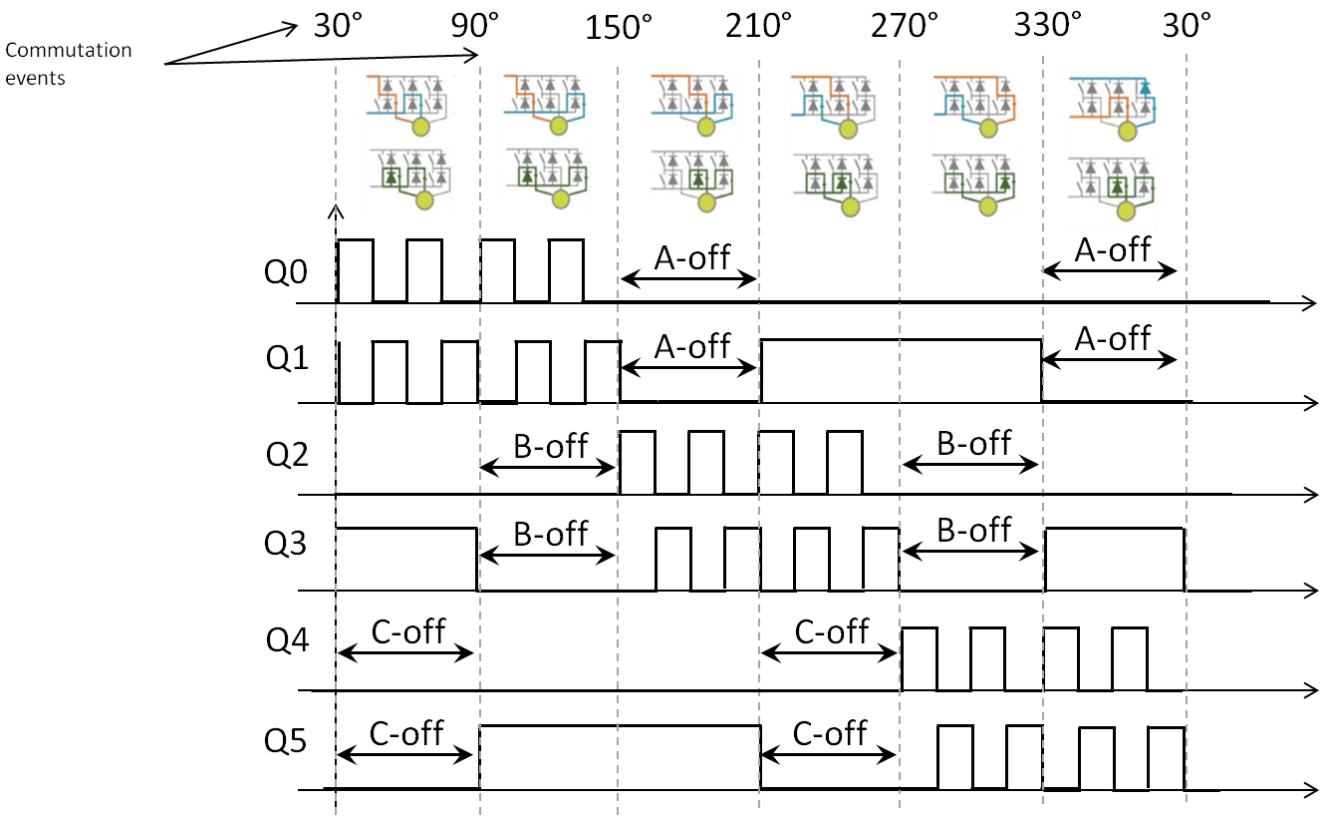

Figure 5- Low side fixed complementary mode

In this configuration the low side remains active throughout the phase, meanwhile the low side performs the modulation in complementary mode. The logic followed to achieve this behavior remains the same as in section **4.3**.

The register configuration can be observed in **Table 4**.

Table 4 - Low side fixed complementary mode

Register	Bits	30°- 90°						90°- 150°						150°- 210°						210° - 270°						270° - 330°						330° - 30°					
	Mask (PWM channels)	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0
PMFCFG2	Value	1	1	0	1	0	0	0	1	1	1	0	0	0	1	0	0	1	1	1	1	0	0	0	1	0	0	1	1	0	1	0	0	0	1	1	1
	Value in hexadecimal	0x34						0x1C						0x13						0x31						0x0D						0x07					
	Mask (PWM channels)	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0
PMFOUTC	Value	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0
	Value in hexadecimal	0x0C						0x30						0x30						0x03						0x03						0x0C					
	Mask (PWM channels)	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0
PMFOUTB	Value	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
	Value in hexadecimal	0x2A						0x2A						0x2A						0x2A						0x2A						0x2A					

4.5 Complementary bipolar

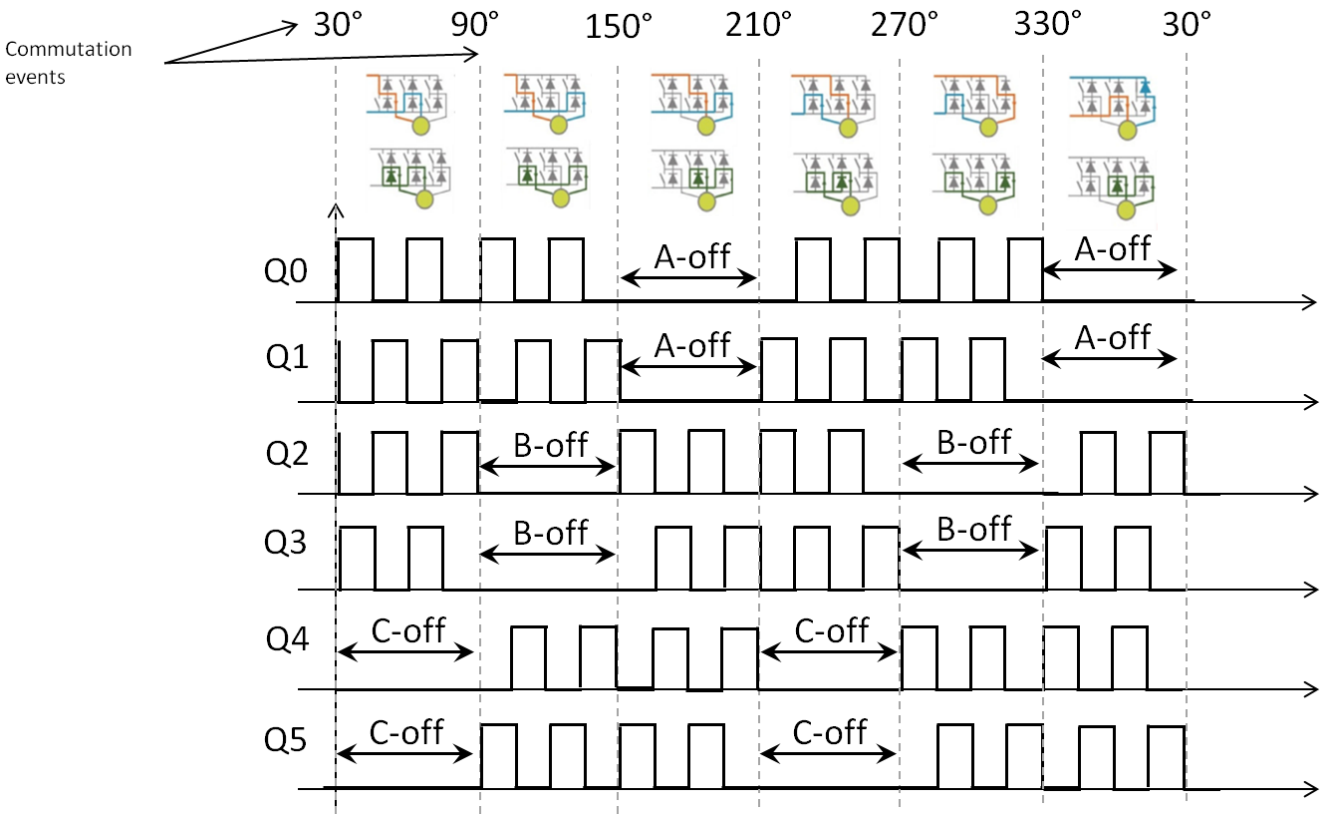

Figure 6 -Complementary bipolar

In this configuration two phase pairs are being driven in complementary mode simultaneously. For this configuration only the PMFCFG2_MSK and PMFCFG3_PINVx registers need to be modified, since none of the channels are being hold in a given state PMFOUTC_CTL is not used and must be cleared.

The PMFCFG2_MSK mechanism remains the same as in the other configurations, the channels that will be active during the commutation phase must be enabled by clearing their corresponding bits, as can be seen in **Table 5**.

Since both pairs are being enabled at the same time high sides and low sides will become active at the same time, thus "blocking" the motor so to speak, since the commutation won't take place (High side phase A with Low side phase B). In order to comply with the electrical requirements one pair must be inverted. This is achieved by modifying the value of the registers in PMFCFG3.

In this example the pair Q_3-Q_2 and Q_1-Q_0 are being enabled simultaneously and the pair Q_3-Q_2 (phase B) is being inverted by modifying PMFCFG3, this can be seen in **Table 5**.

Table 5- Complementary bipolar

Register	Bits	30°- 90°						90°- 150°						150°- 210°						210° - 270°						270° - 330°						330° - 30°					
PMFCFG2	Mask (PWM channels)	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0	Q5	Q4	Q3	Q2	Q1	Q0
	Value	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	
	Value in hexadecimal	0x30						0x0C						0x03						0x30						0x0C						0x03					
PMFCFG3	PINVx	C		B		A		C		B		A		C		B		A		C		B		A		C		B		A		C		B		A	
	Value	0		1		0		1		0		0		1		0		0		0		0		1		0		0		1		0		1		0	
	Value in hexadecimal	0x02						0x04						0x04						0x01						0x01						0x02					

5 Software Configuration

Within the software that comes along with this application note, there is a configuration file named "config_me.h" in the folder "Drivers" inside the Sources folder. This header must be modified with respect the desired behavior of the module. At the end of the file there are three definitions that will define the overall configuration:

- PMF_MODE – Selects the configuration for the module, for example: Independent low side fixed.
- ROUTE – Selects if the signal is routed to GPIOs or directly to the power MOSFETs.
- rotdir – Selects the direction in which the motor will rotate.

Other parameters such as Duty cycle, period of the PWM signal and dead time can also be configured within this file.

WARNING

This example does not have any speed control implemented; therefore caution must be taken while changing parameters such as the duty cycle or PWM period to avoid any hazard.

6 Jumper Configuration

J15: Must be set to 2-3 Phase A from Hall/encoder interface is connected to port PT1.

J16: Must be set to 1-2 Phase B from Hall/encoder interface is connected to port PT2.

J14: Must be set to Port PP0 is connected to EVDD at Hall sensor interface.

J9: Must be open ON/OFF switch disabled.

Rest of the switches must be set as stated in the quick start guide of the development kit.

7 References

Following references are available at freescale.com

- *MC9S12ZVM*: Reference Manual, Rev 2.2
- *AN4704*: 3-phase Sensorless BLDC Motor Control Kit with the S12 MagniV MC9S12ZVM

8 Revision History

Revision	Date	Substantial Changes
0	September 2015	Initial release

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