MPC574xP Hardware Design Guide

by: NXP Semiconductors

Contents

1. Introduction

The MPC574xP is a Power Architecture® based microcontroller targeting automotive chassis and safety applications. This microcontroller features a number of analog, communication, and safety modules, as well as two e200z4 core complexes running in delayed lock step at up to 200 MHz

The MPC574xP requires both 3.3 V and 1.25 V supplies. These supplies can either both be provided externally, or the 3.3 V supply can be used to generate the 1.25 V supply via an internal regulator and external ballast transistor. In the simplest configuration, a single 3.3 V supply can power the entire device.

The intention of this application note is to provide:

- Power supply requirements and the correct external circuitry required for each supply
- Guidelines for handling injection current, including requirements for power supply ramp rates
- Proper configuration of the external PLL circuitry
- Example external interfaces for the communication and analog modules

Please note that information from the MPC574xP Reference Manual, Datasheet, and/or Errata report may be repeated in this application note for the convenience of the reader. The reference manual, datasheet, and errata report are the official specification for the MPC574xP and should be reviewed for the most up-to-date information available for this device.

2. Package Options

The MPC574xP is available in the following packages:
- 144 pin Low Profile Quad Flag Package (144 LQFP)
- 257 pin Molded Array Process Ball Grid Array (257 MAPBGA)

The table below compares the features between the two packages:

Table 1. MPC574xP features differing by package

Feature	144 LQFP	257 MAPBGA
FlexPWM1	A[0-2]/B[0-2]	A[0-3]/B[0-3]/X[0-3]/Fault[0:3]
eTimer2	ETC2-5	ETC0-5
GPIO	79 GPIO, 26 GPI	112 GPIO, 29 GPI
CTU external trigger(s)	CTU0	CTU0, CTU1
ADCs	22 analog pads assigned to ADC0, ADC1, ADC2, and ADC3 Shared channels between ADC0/ADC1, ADC0/ADC2, and ADC1/ADC3	25 analog pads assigned to ADC0, ADC1, ADC2, and ADC3 Shared channels between ADC0/ADC1, ADC0/ADC2, ADC1/ADC3, and ADC2/ADC3
SIPI/LFAST	No	Yes
Ethernet	No	Yes
Nexus	Yes (MDO interface)	Yes (MDO interface)
Nexus Aurora Port	No	Yes (TX0/TX0_P/TX1/TX1_P/CLK/CLK_P)

The package selection should be based on the number of input/output pins required for the application and the area available for the target system. The following table shows the size differences between the packages. Package drawings are provided as separate documents from the NXP website. To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number.

Table 2. Size differences between packages

Package	Dimension	Pitch	Case Outline Document Number
144 LQFP	20 mm x 20 mm	0.5 mm	98ASS23177W
257 MAPGBA	14 mm x 14 mm	0.8 mm	98ASA00081D

3. Pinouts and Ball Maps

3.1. 144 LQFP Pinout

Figure 1. LQFP pinout

257 MAPBGA Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS_HV_IO	VSS_HV_IO	A[14]	A[9]	D[3]	JCOMP	H[12]	C[15]	VDD_HV_IO	I[3]	E[13]	J[1]	F[15]	H[13]	F[13]	VSS_HV_IO	VSS_HV_IO
B	VSS_HV_IO/VSS_LV_COR	VDD_HV_IO	F[3]	D[2]	B[6]	F[0]	D[4]	D[0]	VSS_HV_IO	E[14]	A[10]	B[3]	H[9]	C[10]	J[3]	VDD_HV_IO	VSS_HV_IO
C	I[15]	J[0]	VSS_HV_IO	FCCU_F[1]	A[13]	I[0]	H[10]	E[15]	H[11]	I[14]	J[2]	B[2]	H[6]	B[1]	VSS_HV_IO	B[0]	H[15]
D	A[6]	I[7]	A[15]	C[6]	N/C	EXT_POR_B	A[12]	VDD_HV_IO	VSS_HV_IO	A[11]	I[2]	F[14]	J[4]	VDD_HV_IO	VPP_TEST	A[4]	F[12]
E	F[4]	F[6]	D[1]	NMI_B										N/C	C[13]	G[3]	D[14]
F	F[5]	H[7]	H[5]	H[4]		VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR		C[14]	D[12]	G[4]	G[2]
G	MDO0	VDD_HV_IO	C[5]	A[7]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		B[4]	A[3]	J[8]	G[6]
H	A[8]	VSS_HV_IO	C[4]	A[5]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		G[12]	TMS	VDD_HV_FLA	TCK
J	C[7]	I[4]	F[8]	F[7]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		G[13]	H[1]	VDD_LV_NEXUS	B[5]
K	J[9]	F[10]	F[9]	I[8]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		G[15]	H[0]	VSS_LV_NEXUS	J[10]
L	H[8]	F[11]	I[9]	D[8]		VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR		A[2]	G[14]	N/C	J[11]
M	VDD_HV_OSC	VDD_HV_IO	I[10]	D[5]									H[14]	C[12]	I[6]	G[7]	G[5]
N	XTAL	VSS_HV_IO	D[9]	VSS_LV_PLL	I[12]	I[13]	B[8]	J[5]	J[6]	J[7]	B[14]	A[0]	BCTRL	G[8]	I[5]	VDD_LV_LFAST	VSS_LV_LFAST
P	VSS_HV_OSC	RESET_B	D[6]	VDD_LV_PLL	B[7]	E[6]	VDD_HV_ADRE0	B[10]	VDD_HV_ADRE1	B[13]	B[15]	C[0]	E[0]	G[9]	N/C	C[11]	D[11]
R	EXTAL	FCCU_F[0]	VSS_HV_IO	D[7]	E[5]	E[7]	VSS_HV_ADRE0	B[11]	VSS_HV_ADRE1	VDD_HV_ADV	E[10]	E[12]	N/C	N/C	VSS_HV_IO	D[10]	G[10]
T	VSS_HV_IO	VDD_HV_IO	I[1]	C[1]	C[2]	E[2]	B[9]	B[12]	VSS_HV_ADV	E[9]	E[11]	N/C		A[1]	G[11]	VSS_HV_IO	VSS_HV_IO
U	VSS_HV_IO	VSS_HV_IO	I[11]	E[4]										VDD_HV_PMU/IO	N/C	VSS_HV_IO	VSS_HV_IO

3.2. 257 MAPBGA Ball Map

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Figure 2. 257 MAPBGA ball map

4. Power Supplies

The MPC574xP includes a robust power management infrastructure that enables applications to select among various operational and low-power modes and to monitor internal voltages for high- and low-voltage conditions. The monitoring capability is also used to ensure supply voltages and internal voltages are within the required ranges before the microcontroller can exit reset.

The MPC574xP requires two types of voltage supplies:

- "High Voltage" (HV) supplies which are a nominal 3.3 V.
- "Low Voltage" (LV) supplies which are a nominal 1.25 V.

The table below lists the power supply pins on the MPC574xP.

Table 3. MPC574xP power supply pins

Name	Type	Description
VDD_HV_ADRE01	Reference (3.3 V or 5 V)	ADC0 high reference voltage
VDD_HV_ADRE11	Reference (3.3 V or 5 V)	ADC1 high reference voltage
VDD_HV_ADV	Supply (3.3 V)	High voltage supply for the ADC modules
VDD_HV_IO	Supply (3.3 V)	High voltage power supply for the I/Os
VDD_HV_PMU	Supply (3.3 V)	High voltage power supply for the internal Power Management Unit (PMU)
VDD_HV_OSC	Supply (3.3 V)	High voltage power supply for the internal crystal oscillator circuitry
VDD_HV_FLA	Supply (3.3 V)	High voltage supply for the internal Flash memory
VDD_LV_LFAST2	Supply (1.25 V)	Low voltage power supply for the LFAST module
VDD_LV_NEXUS2	Supply (1.25 V)	Low voltage power supply for the Nexus module
VDD_LV_PLL	Supply (1.25 V)	Low voltage power supply for the PLLs
VDD_LV_COR	Supply (1.25 V)	Low voltage power supply for the core digital logic
VSS_LV_LFAST2	Ground	Ground supply for the LFAST module
VSS_LV_NEXUS2	Ground	Ground supply for the Nexus module
VSS_LV_PLL	Ground	Ground supply for the PLLs
VSS_LV_COR	Ground	Ground supply for the core digital logic
VSS_HV_IO	Ground	Ground supply for the I/Os
VSS_HV_OSC	Ground	Ground supply for the oscillator
VSS_HV_ADRE0	Ground/Reference	ADC0 ground and low reference voltage
VSS_HV_ADRE1	Ground/Reference	ADC1 ground and low reference voltage
VSS_HV_ADV	Ground	Ground supply for the ADC modules

1. Either 3.3 V or 5 V can be used for the analog high voltage reference. However, these references cannot operate at different voltages. Both VDD_HV_ADRE0 and VDD_HV_ADRE1 must be connected to the same voltage source.

2. The 144 LQFP does not include the LFAST or NEXUS supply signals.

The MPC574xP provides an on-chip linear voltage regulator through the Power Management Controller (PMC) to derive the 1.25 V supply from 3.3 V. When using the on-chip regulator, an external bipolar junction transistor (BJT) must be added which serves as a ballast transistor. The recommended transistor is the ON Semiconductor™ NJD2873. The figure below provides a simplified diagram of this setup:
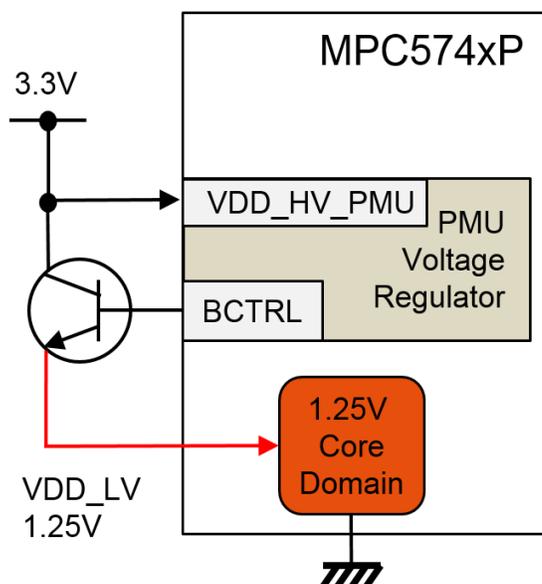
Figure 3. Using an external ballast transistor to generate 1.25 V

Alternatively, an external linear or switching regulator can be used to supply 1.25 V. The internal regulator becomes inactive when an external regulator is used, and the external ballast transistor should be removed in this case. When external power supply is used the internal regulator must be switched off by setting PMC_PMCCR[INT_REG_BYPASS] to 1. The reason is that the regulator is still working and could create some noise. The figure below provides a simplified diagram of this setup:

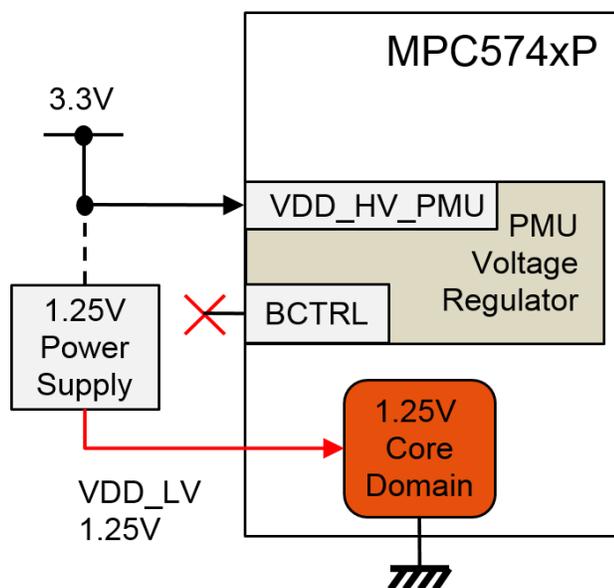**Figure 4. Supplying 1.25 V with an external power supply**

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NOTE

- When using an external power supply it is ok to leave BCTRL floating or to connect it to any of the supply or ground pins through a large resistor (> 10 kΩ). It must not be connected directly to any supply or ground pin.

- The device must always be operated within the correct voltage range of the data sheet, especially, if the internal LVDs are disabled. Device voltages must be in valid operating range, when device is booting up after a long/short functional reset, destructive RESET or POR. In case of synchronous or asynchronous abort during the self test execution the nominal current transient of 30 mA/us (Offline BIST)/120 mA/us (Online BIST) can occur.

4.1. Voltage Monitoring

The PMC senses the supply voltage continuously to keep the chip in the safe operating range. Destructive resets or interrupts are triggered when the voltage exceeds or falls below the recommended electrical operating conditions.

4.1.1. Core Supply (VDD_LV_COR) Monitor

The digital core is able to operate within the voltage limits given by the data sheet. The lower limit is reduced by the amount of on-chip IR drop. The upper limit is defined by the beginning of lifetime degradation.

The available range for external supply voltage is further restricted by the tolerance of high voltage detect (HVD) and low voltage detect (LVD) monitors. See the data sheet for exact values. To ensure safe operating conditions for the core, the LVD/HVD are calibrated. Calibration of LVD/HVD occurs after the core is in the functional safe operating range. It is performed in a way that the LVD/HVD cover the allowed core operating range, i.e. by increasing the minimum value for LVD and decreasing the maximum value for HVD.

The HVD determines whether the core supply has exceeded an upper limit. It has a 5% uncalibrated tolerance that can be reduced to ~1.5% by calibration. The LVD determines whether the core supply has exceeded a lower limit. It has a 5% uncalibrated tolerance that can be reduced to ~1.5% by calibration. The figure below illustrates the operating range of VDD_LV_COR, in relation to HVD and LVD.
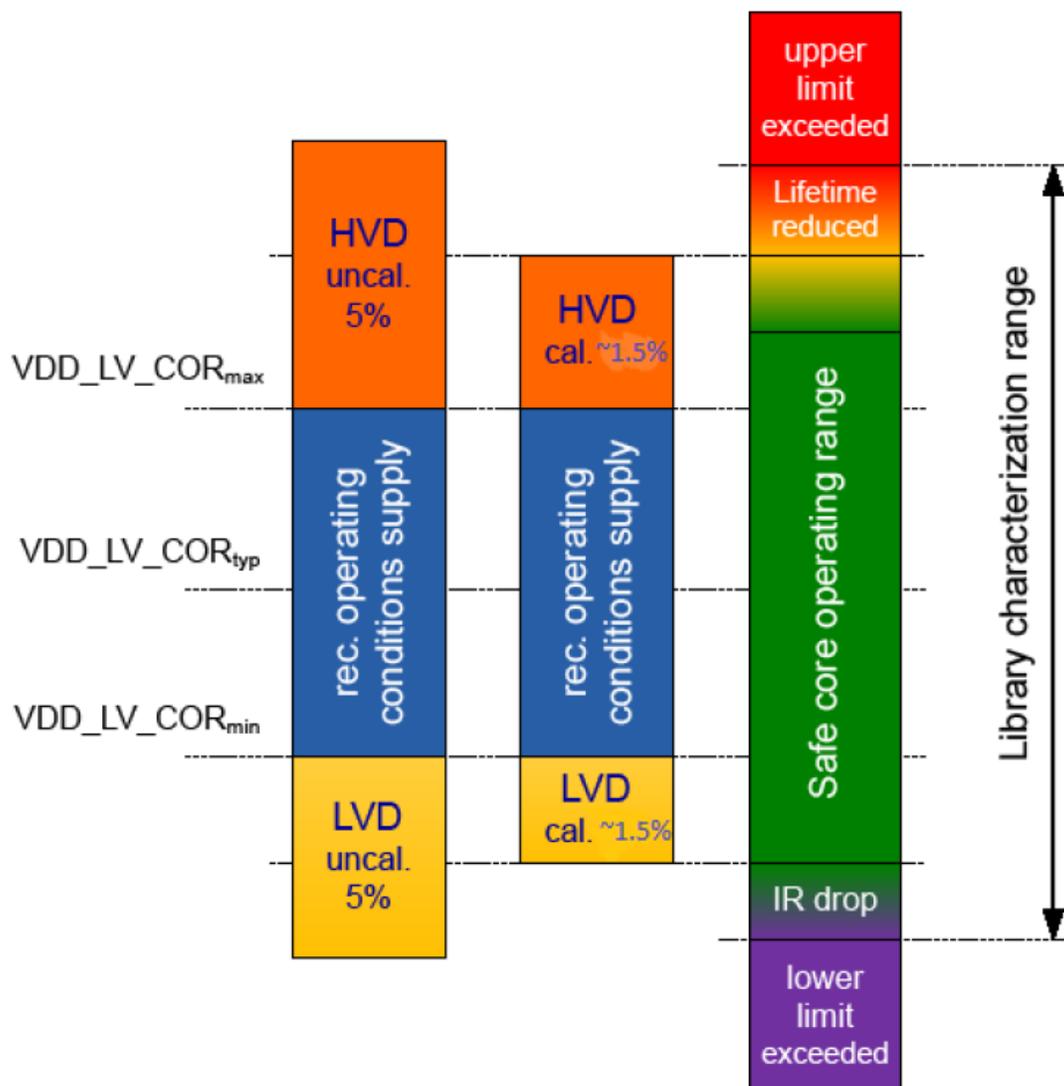
Figure 5. VDD_LV_COR operating range

If LVD and HVD are disabled, the external core supply can have an extended operating range. External voltage monitors should be used in that case to ensure functional safety.

4.1.2. High Voltage (VDD_HV_xxx) Supply Monitors

All other 3.3 V, non-core supplies are compared to a lower limit only by means of LVDs. All 3.3 V supplied modules must remain fully functional in an extended operating range that includes the LVD calibrated tolerance. The 3.3 V LVDs have 5% uncalibrated and 2% calibrated tolerance. Calibration takes place when the core supply is within a safe operating range. After calibration, the typical LVD value is centered within the recommended operating conditions low limit and the safe operating conditions low limit to provide margins for supply undershoots.

If the internal LVDs are disabled, external voltage monitors shall be used to ensure functional safety. The external monitors shall provide sufficient hysteresis or low-pass characteristics to prevent bouncing in case of short 3.3 V supply undershoots. The figure below illustrates the operating range of VDD_HV_xxx.

Figure 6. VDD_HV_xxx operating range

4.2. Power-up Sequence

When using the on-chip regulator if the VDD_HV_PMU voltage exceeds the minimum voltage threshold for turning on the core regulator, POR_REG$_{rise}$ in the figure below (POR_VDD33_REG in the data sheet), all 3.3 V LVDs are reset to their uncalibrated state and armed and the core voltage regulator starts to work and the core supply voltage rises.
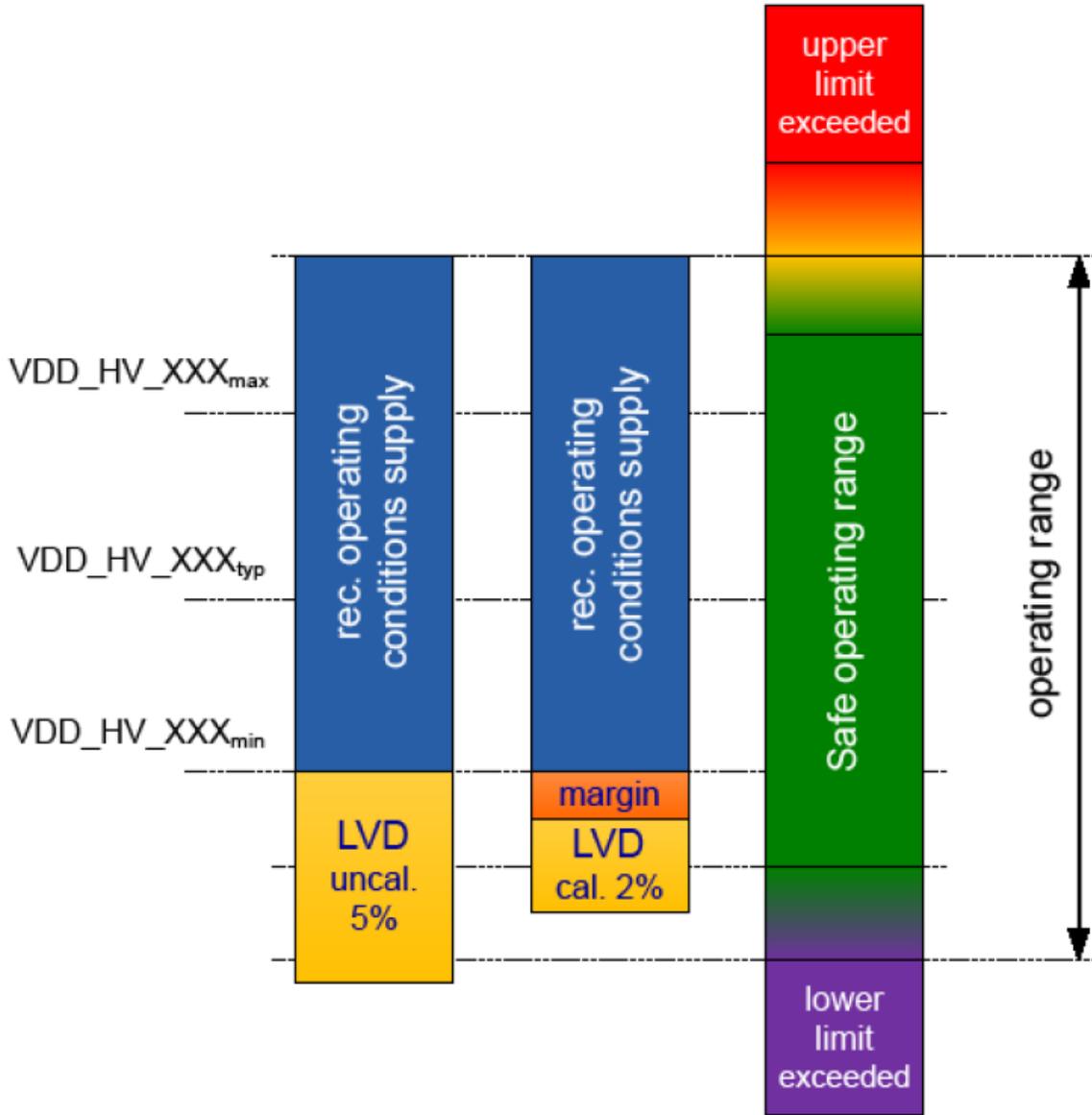
When the core voltage crosses its power on reset threshold, POR_CORE$_{rise}$ in the figure below (POR_VDD12 in the data sheet), the core LVDs and HVDs are reset to their uncalibrated state and armed.

When the core supply and the regulator voltage reach their minimum value according to the recommended operating conditions, the system reset is released and the system boot process starts. The LVDs/HVDs are now calibrated to provide tighter limits for voltage over/undershoot detection.

As soon as the core or any 3.3V supply falls below the limit of the corresponding LVD thresholds, a destructive reset is triggered. The system is held in reset state until all LVD threshold levels are exceeded again. If the core voltage exceeds the threshold of the HVD, a destructive reset is asserted. It is released when the core voltage falls below the HVD threshold.

When the core or the regulator supply fall below the POR_CORE$_{fail}$ or POR_REG$_{fail}$ limit, respectively, the system is reset and the core supply is disabled. The chip will restart with a complete power-up cycle.
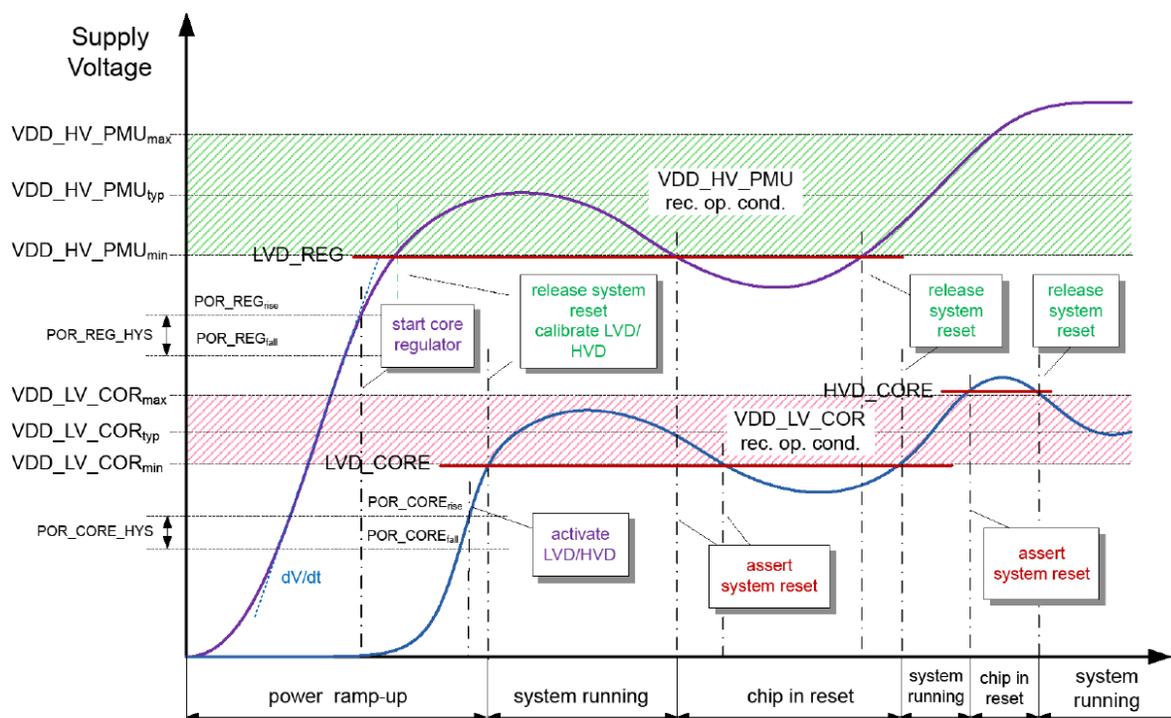
Figure 7. Power-up events and operating ranges

The individual VDD_HV_xxx supplies can be powered-up in any order. There is no risk in damaging the part or causing latch-up when some supplies rise before others. When using an external regulator for the core supply, the external 1.25 V supply can be applied before or after the 3.3V supplies power-up, though it is recommended (but not necessary) to drive EXT_POR_B low until all supplies are in the operational range. The datasheet specifies ramp rate limits which the external power supplies must satisfy.

Once all supplies are within the operating range (above LVD for VDD_HV supplies and within LVD/HVD limits for the core supply) the MCU begins to proceed through the reset process. If the STCU is configured to run BIST, the ADC reference voltages (VDD_HV_ADREx) must be available

and within the proper operating range. BIST may fail if the ADC reference voltages are not within the operating range.

4.3. Decoupling Capacitors

The table below lists recommended decoupling capacitors to use on various supply pins. Note that these are general recommendations which attempt to compensate for various board designs. It is not a strict requirement to exactly match these recommendations. It is far more important to select capacitors based on the intended application, temperature, noise, and operating conditions. Make sure to place smaller capacitors closer to the supply pairs and distribute the capacitors evenly around the supply pins.

Table 4. Recommended decoupling capacitors

Supply	Decoupling Capacitors
VDD_HV_IO[1]	2 uF (x4), 0.1 uF (x4), 0.047 uF (x4)
VDD_HV_PMU	10 µF (x2), 0.1 µF (x1)
VDD_HV_FLA	0.1 µF (x1), 0.01 µF (x1)
VDD_HV_OSC	0.1 µF (x1), 0.01 µF (x1)
VDD_HV_ADVx	1.0 µF (x1), 0.047 µF (x1), 0.01 µF (x1)
VDD_HV_ADRx	1.0 µF (x1), 0.047 µF (x1), 0.01 µF (x1)
VDD_LV_COR[2]	3.3 uF (x4), 47 nF (x6)
VDD_LV_PLL	0.047 µF (x1)
VDD_LV_NEXUS	0.22 µF (x1)
VDD_LV_LFAST	0.22 µF (x1)

5. Clock Circuitry

Care must be taken in the layout and design of the circuitry around the external crystal oscillator and PLL power supplies. The PLLs are powered from VDD_LV_PLL/VSS_LV_PLL and the external crystal oscillator is powered from VDD_HV_OSC/VSS_HV_OSC. Noise on either of these supplies can affect the accuracy and jitter performance of the crystal oscillator and PLLs.

The figure below shows the typical connections to the crystal oscillator.
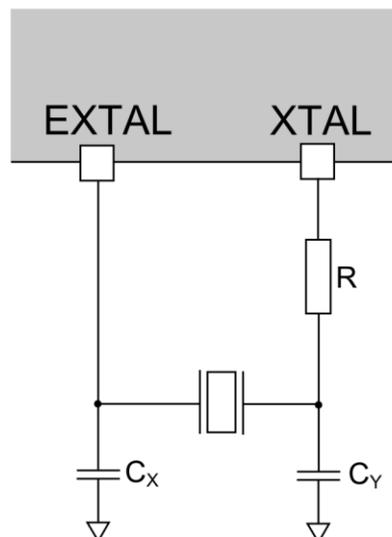
[1] Customer should check with chose

[2] For LQFP. For MAPBGA: 3.3 uF (

Figure 8. Typical crystal oscillator connections

The recommendations from the crystal manufacturer will include a series resistor value and the load capacitance required for the crystal. The total load capacitance is usually specified in the crystal data sheet. Keep in mind that the load capacitance is the sum of:

- External capacitors (C_X and C_Y)
- Capacitance of the MCU
- Capacitive loading of the board
- EXTAL and XTAL pin capacitance

The oscillator circuit should be placed as close as possible to the MCU. In order to minimize signal degradations, the circuitry should be placed entirely on only one PCB layer, avoiding unnecessary vias where possible. Do not allow any signals to cross the crystal connections to the device. Absolutely no high current or high speed signals should be run near any of the crystal components.

Another option is to use an external clock source to drive EXTAL, as shown in the figure below. In this setup, XTAL drive is disabled and the external clock source should satisfy CMOS level transitions. The figure below illustrates using an external clock to drive EXTAL.

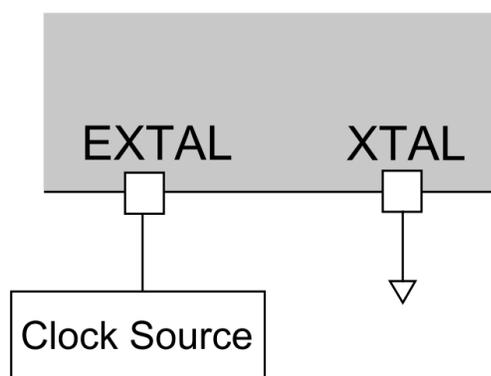**Figure 9. Driving EXTAL with an external clock**

Other than the connections shown in the above figures, no other connections should be made to the crystal or EXTAL and XTAL device pins. Do not use XTAL to drive any circuitry other than what is shown.

6. Reset

6.1. Reset Pins

The MPC574xP has two external reset pins.

- RESET_B: External functional reset
- EXT_POR_B: External power-on reset

Both RESET_B and EXT_POR_B are open drain, active low, bidirectional pins with internal weak pull down resistors. An external 4.7 kΩ - 10 kΩ pull up resistor should be added to these pins. A simplified diagram of RESET_B and EXT_POR_B is shown below.
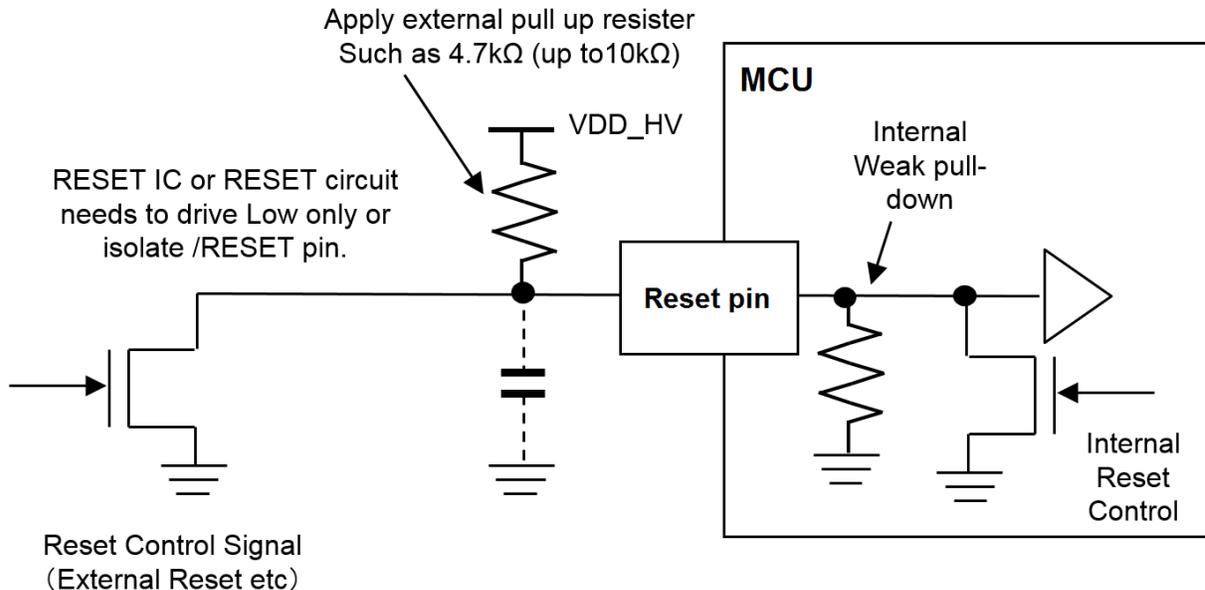
Figure 10. Simplified diagram of the reset pins

EXT_POR_B is driven low by the MCU during the POWERUP[3] sequence of the reset process. The MCU will not exit POWERUP until EXT_POR_B is externally driven high. Once the MCU is out of POWERUP, EXT_POR_B can be externally driven low at any point in time in order to bring the MCU back to the POWERUP stage of the reset sequence.

RESET_B is also driven low by the MCU starting at the POWERUP sequence of the reset process, but the MCU will continue to assert this signal throughout the entire reset process. The MCU will not exit PHASE3[FUNC] until RESET_B is externally driven high. RESET_B can be externally driven low at any point in time in order to bring the MCU back to PHASE1[FUNC] or PHASE3[FUNC], depending on the setting in MC_RGM_FESS[SS_EXR].

6.2. Boot Configuration

The device detects the boot mode based on external pins and device status.

- To boot either from FlexCAN or LINFlexD, the device must be forced into an Alternate Boot Loader Mode via the Force Alternate Boot (FAB) Mode pin which must be asserted before initiating the reset sequence. The type of alternate boot mode is selected according to the Alternate Boot Selector (ABS) pins.

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[3] See the reset chapter in the MPC574xP reference manual for definitions and details on the reset process.

- If the FAB pin is not asserted, the device boots from the first flash memory sector which contains a valid boot signature.
- If no flash memory sector contains a valid boot signature, the device will go into static mode.

The table below shows the boot modes that correspond to the boot mode pin levels.

Table 5. MPC574xP boot modes

FAB	ABS2, ABS0	Boot mode
0	XX	Boot from Flash
1	00	Boot from UART
1	01	Boot from CAN

In order to ensure that the boot mode is correctly captured, the application needs to apply the valid boot mode value to the pins the entire time that RESET_B is asserted. The application must also continue to apply the boot mode values to the pins for 5µs after RESET_B has been de-asserted. When booting from flash keep the FAB pin 0 at all times by connecting it to ground.

FAB, ABS2, and ABS0 pins all contain internal weak pull down resistors.

6.3. Pin Startup and Reset States

The following table provides the startup state and reset state information for device pins.

Table 6. Pin startup and reset states

Pin	State during and after reset
GPIOs	Hi-Z
Analog inputs	Hi-Z
JCOMP	Input, weak pull-down
TDI	Input, weak pull-up
TDO	Output, Hi-Z
TMS	Input, weak pull-up
TCK	Input, weak pull-up
XTAL/EXTAL	Hi-Z
FCCU_F[0]	Input/Output, Hi-Z
FCCU_F[1]	Input/Output, Hi-Z
EXT_POR_B	Input, weak pull-down
RESET_B	Input, weak pull-down
NMI_B	Input, weak pull-up
FAB	Input, weak pull-down
ABS[2]	Input, weak pull-down
ABS[0]	Input, weak pull-down

7. Debug Connections

The MPC574xP supports the following types of debug interfaces for run control and device access:

- 14-pin JTAG interface (IEEE 1149.1)
- 38 pin or 50 pin Nexus parallel trace interface (IEEE-ISTO 5001-2003)
- 34 pin Nexus serial (Aurora) trace interface (IEEE-ISTO 5001-2012)

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The recommended connectors for each interface are listed in the table below.

Table 7. Recommended debug connectors

Connector type	Connector style	Part number
JTAG only	14 pin Berg	3M 2514-6002UB
Nexus parallel trace up to 16 MDO signals	25 position (2 x 25, 50 pin) Samtec	Samtec ASP-148422-01
Nexus parallel trace up to 12 MDO signals	38 pin Mictor	Tyco 767054-1
Nexus serial trace up to 8 simplex lanes	17 position (2 x 17, 34 pin) Samtec	Samtec ASP-137973-01

See NXP application note AN4224, "MPC57xx Nexus Debug Connectors", for further details and design guidelines for JTAG and Nexus debug interfaces.

7.1. JTAG Interface

The table below shows the pinout for the JTAG interface. If there is enough room in the target system, a full Nexus connector is recommended because of its enhanced debug capabilities.

Table 8. JTAG connector pinout

MPC574xP Signal	Pin	Pin	MPC574xP Signal
TDI	1	2	GND
TDO	3	4	GND
TCK	5	6	GND
EVTI	7	8	EXT_POR_B
RESET_B	9	10	TMS
VDD_HV_IO	11	12	GND
NEX_RDY_B	13	14	JCOMP

7.2. Nexus Parallel Trace Interface

The following table shows the recommended pinout for the Mictor connector:

Table 9. Nexus parallel trace Mictor connector pinout

MPC574xP Signal	Pin	Pin	MPC574xP Signal
-	1	2	-
-	3	4	-
-	5	6	-
FAB	7	8	-

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MPC574xP Signal	Pin	Pin	MPC574xP Signal
RESET_B	9	10	EVTI
TDO	11	12	VDD_HV_IO
-	13	14	NEX_RDY_B
TCK	15	16	-
TMS	17	18	-
TDI	19	20	-
JCOMP	21	22	-
-	23	24	MDO[3]
-	25	26	MDO[2]
-	27	28	MDO[1]
-	29	30	MDO[0]
VSUP	31	32	EVTO
VSUP	33	34	MCK0
-	35	36	MSEO_B[1]
-	37	38	MSEO_B[0]

The following table shows the recommended pinout for the Samtec connector:

Table 10. Nexus parallel trace Samtec connector pinout

MPC574xP Signal	Pin	Pin	MPC574xP Signal
MSEO_B[0]	1	2	VDD_HV_IO
MDEO_B[1]	3	4	TCK
GND	5	6	TMS
MDO[0]	7	8	TDI
MDO[1]	9	10	TDO
GND	11	12	JCOMP
MDO[2]	13	14	NEX_RDY_B
MDO[3]	15	16	EVTI
GND	17	18	EVTO
MCKO	19	20	RESET_B
-	21	22	EXT_POR_B
GND	23	24	GND
-	25	26	-
-	27	28	-
GND	29	30	GND
-	31	32	-
-	33	34	-
GND	35	36	GND
-	37	38	-
-	39	40	-
GND	41	42	GND
-	43	44	-

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MPC574xP Signal	Pin	Pin	MPC574xP Signal
-	45	46	-
GND	47	48	GND
-	49	50	-

7.3. Nexus Serial Trace Interface

The Samtec ERF8 series of connectors is intended for high speed applications requiring a minimum footprint size with a reliable, latching connection. The recommended connector has two rows of 17 contacts each, with a spacing of 0.8 mm. The connector provides isolation between high-speed trace signals and the low-speed JTAG and control signals. It also provides ample ground connections to ensure signal integrity.

If possible, the connector should be placed onto the target system with the even numbered pins nearest the edge of the PCB in order to facilitate a direct connection to the debug tool. Additionally, care should be taken in the layout of the high speed Aurora signals (TXn+, TXn-, CLK+, and CLK-) with a good return path (usually to ground).

The table below shows the recommended pinout for the Samtec connector.

Table 11. Nexus serial trace Samtec connector pinout

MPC574xP Signal	Pin	Pin	MPC574xP Signal
AUR_TX0_P	1	2	VDD_HV_IO1
AUR_TX0_N	3	4	TCK
GND	5	6	TMS
AUR_TX1_P	7	8	TDI
AUR_TX1_N	9	10	TDO
GND	11	12	JCOMP
-	13	14	-
-	15	16	EVTI
GND	17	18	EVTO
-	19	20	EXT_POR_B
-	21	22	RESET_B
GND	23	24	GND
-	25	26	AUR_RXCLK_P
-	27	28	AUR_RXCLK_N
GND	29	30	GND
-	31	32	NEX_RDY_B
-	33	34	WDT[2]

1. Provides a reference for the signal levels of the MCU. All input high and low voltages should be referenced to this pin.
2. WDT is an optional Watchdog Disable signal. It has no defined connection to the MCU. For systems that implement an external hardware watchdog circuit, this signal allows an external tool to disable that watchdog for debug purposes.

7.4. External Components

Some additional pull-up or pull-down resistors are required or recommended on some of the debug pins.

Table 12.   Required or recommended pull resistors on debug pins

JTAG signal	Pull resistor	Description
JCOMP	10 kΩ pull down resistor	JCOMP has an internal weak pull down, but an external pull down is recommended for safety reasons. This holds the debug port in reset and prevents any debug commands from interfering with normal operation of the MCU.
EVTI	10 kΩ pull up resistor	A pull up resistor prevents debug mode from being forced after reset if debug mode is enabled (JCOMP = high). It also prevents breakpoints from being forced if debug mode is enabled.
RESET_B	4.7 kΩ pull up resistor	RESET_B is an open collector bidirectional pin; therefore, it requires a pull resistor.
EXT_POR_B	4.7 kΩ pull up resistor	EXT_POR_B is an open collector bidirectional pin; therefore, it requires a pull resistor.

The MPC574xP includes internal pull devices on the other debug pins to ensure that the pins remain in a safe state. However, if there is additional circuitry connected to the pins or long traces that could be affected by other signals (e.g. due to crosstalk), optional external pull resistors can be added to ensure proper operation under all conditions.

8. I/O Pins

8.1. Unused Pin Termination

In some applications, not all pins of the device may be needed. Good CMOS handling practices state that all unused pins should be terminated and not left floating. There are a few options for terminating unused pins:

- Use an external pull-down or pull-up resistor. The benefit of this option is that the state of the pin is guaranteed during power up, but this option does cost more due to the extra external components.
- Connect the pin directly to VDD or ground.
- Configure the pin as an input and enable the internal pull-up or pull-down resistor.
- Configure the pin as an output and set the output high or low by software. This option cannot be used for input pins.

8.2. **Current Injection**

All pins implement protection diodes that protect against electrostatic discharge (ESD). In many cases, both digital and analog pins need to be connected to voltages that are higher than the operating voltage of the device pin. In addition to providing protection from ESD, these diode structures will also clamp the voltage to a diode drop above the supply of that pin segment. This is permissible, as long as the current injection is limited as defined in the device specification. Current can be limited by adding a series resistor on the signal. The input protection diodes will keep the voltage at the pin to a safe level (per the absolute maximum ratings of the device) as long as it is less than the maximum injection current specification.

The following are some guidelines to follow with respect to current injection.

- Max. injected input current:
    - Digital or analog pin - +/- 3 mA
    - Shared analog pin - +/- 3.6 mA
- The ADC input pads must never exceed their own IO segment power supply voltage. If an input pin is higher than the IO power supply then this will cause the ESD diodes in the pads to forward bias.
- Applying signals to pins during power off must be considered as a kind of overload condition. Series resistors should be used to limit the injection current.
- In general, any overload conditions to pins should be avoided.
- Injection current leads to increased leakage current on the pins next to the injected pin.

9. ADC Circuitry

The MPC574xP includes 4 separate Analog-to-Digital converters (ADC) and associated support modules:

- 4 independent 12-bit Successive-Approximation-Register (SAR) ADCs
- 2 ADC Cross-Triggering Units (CTU) each controlling a pair of ADCs

The input signal conditioning circuit, component layout, power supply, and clock selection can all have a great impact on the performance and accuracy of the ADCs. Refer to NXP application notes AN4881, "MPC57xx SAR ADC Implementation and Use", and AN5032, "Reference Circuit Design for a SAR ADC in SOC", for guidelines on how to handle the ADC circuitry.

10. Communication Modules

There are a wide range of peripheral pins available on the MPC574xP. Many of these have fairly standard definitions for their use. This section provides example connections for some of the most commonly used communication peripherals, such as LIN, CAN, RS-232, Ethernet and ZipWire communication interfaces.

10.1. Example RS232 Interface

The MPC574xP supports RS-232 communication using the LINFlexD module configured to operate in UART mode. The RS-232 (TIA/EIA-232-F) standard is a common interface once available on most computers. Adapters are available to allow the use of RS-232 peripherals though other interfaces, such as USB.

The figure below shows the typical connections between the serial port of the MCU and the MAX3232-EP RS-232D transceiver from Texas Instruments (http://www.ti.com/). The transceiver operates from either a 3.3 V or a 5 V supply and includes two charge pumps to generate the output voltages that are required. This device contains two transmit drivers and two receivers. The charge pumps require four external capacitors.
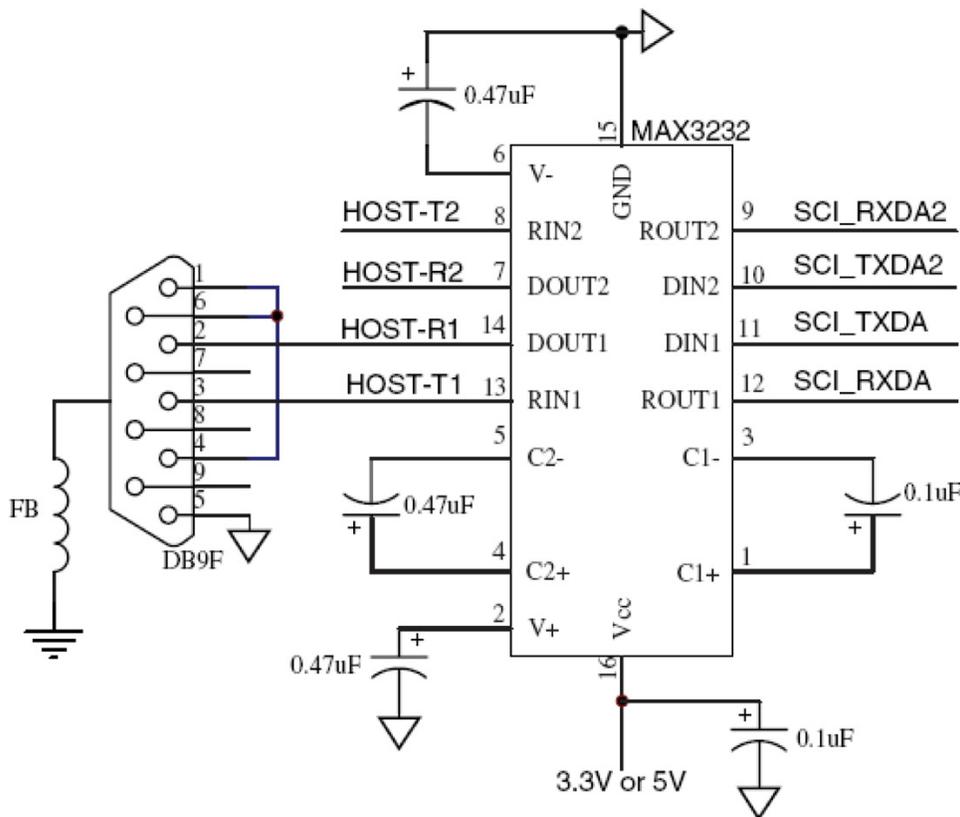

Table 13. Typical SCI to RS-232 circuit

NOTE

The commercial grade MAX3232 device is not rated for the full automotive temperature of –40 to +125° C and is not intended for automotive applications. This device should not be used in a production module intended for automotive use. However, in many cases, the RS-232 interface is intended only as a development interface; therefore, the commercial device can be used for prototyping purposes. Texas Instruments offers a device option with an operating temperature range of –40 to +85° C and an enhanced version of the device, MAX3232-EP, that is intended for aerospace, medical, and defense

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applications. This version is available with an operating temperature range of –
55 to +125° C.

The table below shows the typical DB-9 connector pin assignments.

Table 14. Typical RS-232D connections

PIN	Description
1	Connect to pin 4 and 6
2	RS-232 TX (Transmit)
3	RS-232 RX (Receive)
4	Connect to pin 1 and 6
5	GND
6	Connect to pin 1 and 4
7	N/C
8	N/C
9	N/C

NOTE

N/C pins are not connected. The shell of the connector should be connected
through a ferrite bead to ground.

10.2. Example LIN Interface

Local Interconnect Network (LIN) is a commonly used low-speed network interface that consists of a
master node communicating with multiple remote slave nodes. Only a single wire is required for
communication and is commonly included in the vehicle wiring harness. The figure below shows a
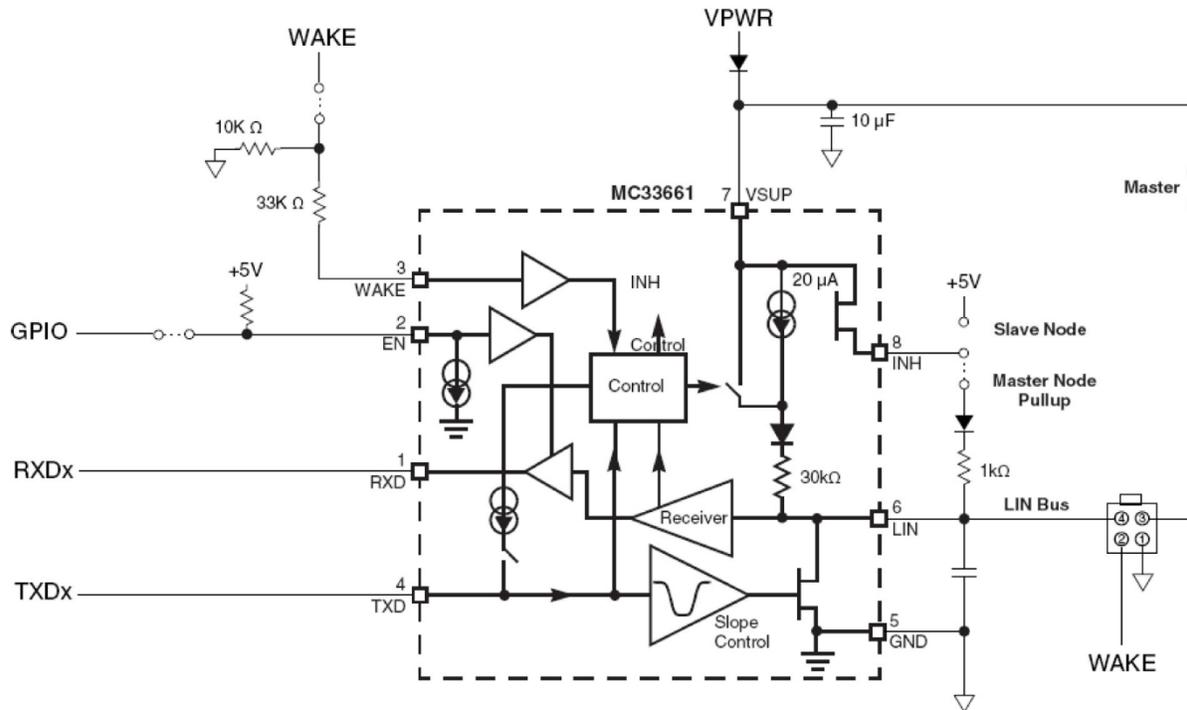typical interface implemented using the NXP MC33661 LIN transceiver.

Figure 11. Typical LIN connections using the NXP MC33661

The table below shows the pins of the MC33661 and their typical connections to an MCU.

Table 15. MC33661 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	RXD	Output	Receive Data Output	MCU LIN RXD	LIN receive data output to the MCU
2	EN	Input	Enable Control	MCU GPIO	Enable operation of the device
3	Wake	Input	Wake Input	LIN Bus Wake1	Pulls the device out of sleep mode
4	TXD	Input	Transmit Data Input	MCU LIN TXD	LIN transmit data input from the MCU
5	GND	Input	Ground	System Reference Ground	Device ground reference
6	LIN	Input/Output	LIN Bus	LIN Bus	Bi-directional pin for single-wire transit and receive
7	VSUP	Input	Power Supply	Protected Battery Voltage	Device power supply, typically connected to a nominal 12V supply
8	INH	Output	Inhibit Output	LIN Bus (if master)	The inhibit pin controls either an external regulator to turn on a slave node or is connected through a resistor to the LIN bus or master nodes

1. WAKE is an optional signal on the LIN connector, but may come directly from a switch

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10.2.1. Recommended LIN Connector

There is not a standard industry-defined LIN connector. NXP uses a 4-pin Molex© connector that allows for the LIN bus pin, a power supply source (VPWR), a wakeup signal, and a ground reference. Slave nodes will often implement two connectors to allow a daisy-chain of multiple nodes to be easily implemented. The table below shows the NXP pinout.

Table 16. LIN connector pinout recommendation

Pin Number	Function
1	Ground
2	Wake
3	VPWR
4	LIN Bus

In a typical system, these pins would be used as follows:

- **LIN Bus**: single-wire LIN bus that connects between the master LIN node and the slave LIN nodes.
- **VPWR**: can be used as the power input to a slave node. Care should be taken that sufficient current is available for the total number of LIN slaves that are powered through this connection. In some systems, this may come from the master LIN node.
- **WAKE**: typically used for each individual slave node to enable the LIN physical interface of that node and to consequently enable the power supply (using the INH output) to power up the MCU to perform some action. For example, when the handle on a car door is lifted, to turn on the MCU that controls a function inside the vehicle, such as powering a smart dome light or enabling the controls of a smart seat.
- **Ground**: ground reference for the module.

Part numbers for the 4-pin Molex connector are shown in the table below.

Table 17. Recommended connector part numbers

Description	Manufacturer part number (Molex)
4-pin right-angle connector with flange for target system, tin contacts, with latch	39-29-1048
4-pin right-angle connector with pegs for target system, tin contacts, with latch	39-29-1040
4-pin vertical connector with pegs for target system, tin contacts, with latch	39-29-9042
4-pin right-angle connector with flange for target system, gold contacts	39-29-5043
Mating connector with latch for cable assemblies	39-01-2040
Female terminal for mating cable assembly	39-00-0077

10.3. Example CAN Interface

Controller Area Network (CAN) is commonly used in almost all automotive applications to allow communication between various microchips in the car.

The MPC574xP incorporates 3 CAN modules on-chip. A separate CAN transceiver is required for each CAN module, although some CAN transceivers may have more than one transceiver on a single chip. It is possible to connect two CAN modules to a single transceiver if the transmit pins are put into open-collector mode with an external pull-up resistor. However, the value of this resistor may limit the

maximum speed of the CAN module if not sized properly for the speed. The MPC574xP CAN modules conform to CAN protocol specification version 2.0B. The transceivers shown in this application note comply with the ISO 11898 physical layer standard.

Typically, CAN is used at either a low speed (5 Kbit/s to 125 Kbit/s) or a high speed (250 Kbit/s to 1 Mbit/s). Powertrain applications typically use a high speed (HS) CAN interface to communicate between the engine control unit and the transmission control unit. Body and chassis applications typically use a low speed (LS) CAN interface. In the dashboard of a vehicle, there is typically a gateway device that interfaces between HS and LS CAN networks.

NXP has a high-speed standalone CAN physical interface device with built-in diagnostic capabilities (MC33902), as well as CAN transceivers integrated with other functions[4]. Other popular CAN transceivers include the NXP devices shown in the following table.

Table 18.   NXP CAN transceivers

Device	Bitrate (Kbit/s)	Modes of operation
TJA1050	1000	Normal, Listen-only
TJA1054	125	Normal, Standby, Sleep
TJA1040	1000	Normal, Standby
TJA1041	1000	Normal, Listen-only, Standby, Sleep

10.3.1. High-speed CAN with Diagnostics: MC33902

For target systems that require full diagnostics of the CAN interface, the NXP MC33902 high-speed CAN transceiver is available. Features of this device are:

- High-speed CAN interface for baud rates of 40 Kbit/s to 1.0 Mbit/s
- Compatible with ISO 11898 standard
- Single supply from battery; no need for a 5.0 V supply for CAN interface
- I/O compatible from 2.75 V to 5.5 V via a dedicated input terminal (3.3 V or 5.0 V logic compatible)
- Low-power mode with remote CAN wakeup and local wake-up recognition and reporting
- CAN bus failure diagnostics and TXD/RXD pin monitoring, cold start detection, and wake-up sources reported through the ERR pin
- Enhanced diagnostics for bus, TXD, RXD, and supply pins available through pseudo-SPI via existing terminals EN, STBY, and ERR
- Split terminal for bus recessive level stabilization
- INH output to control external voltage regulator

[4] An example device is the MC33905 that includes a 5 V power supply controller, a CAN transceiver physical interface, and a LIN transceiver physical interface.

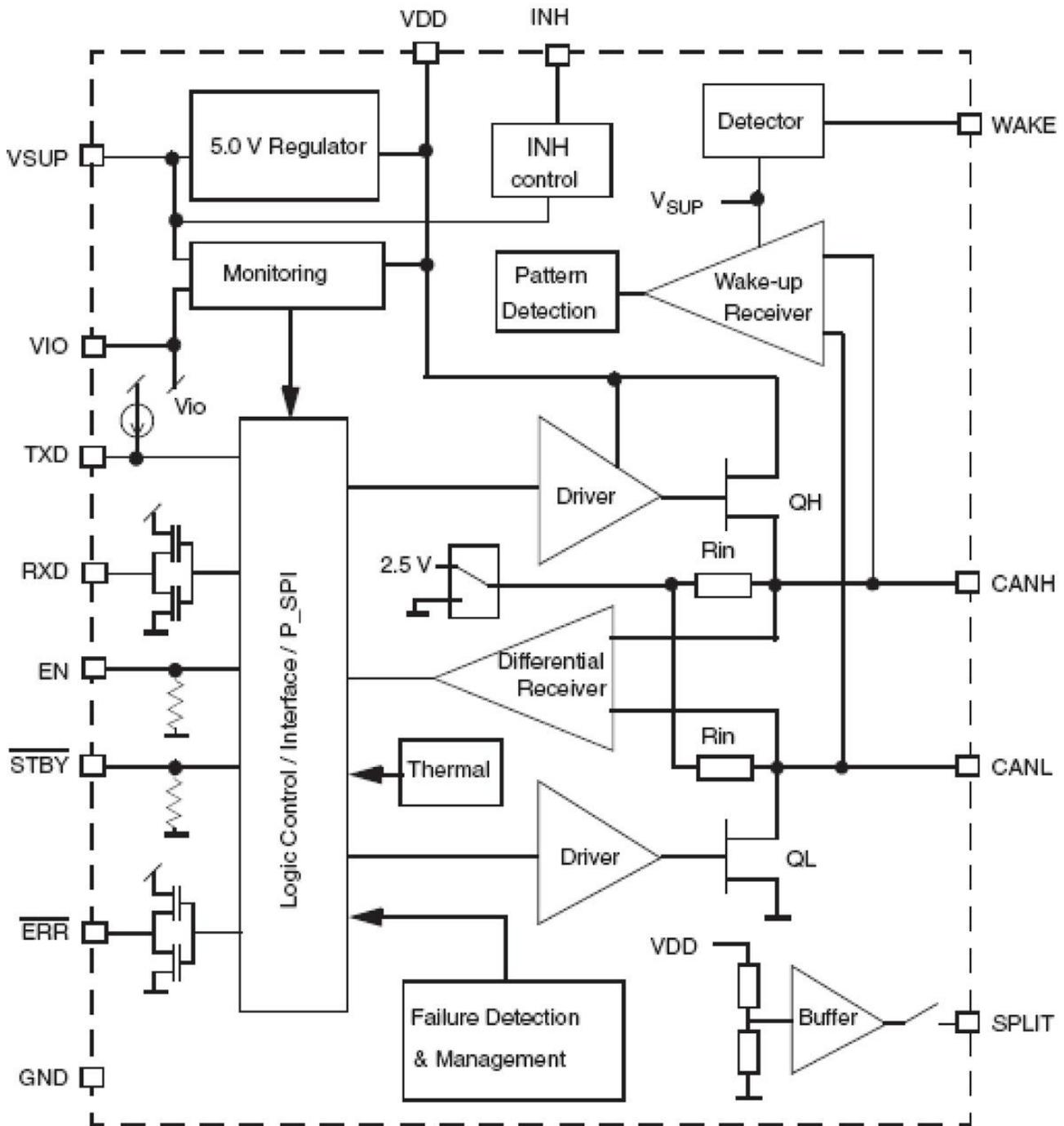A block diagram of this transceiver is shown below.

Figure 12. MC33902 block diagram

The table below shows the pins of the MC33902 and the possible connections to a MCU and the target system.

Table 19. MC33902 pin definitions and system connections

Pin	Name	Direction	Full Pin Name	Connection	Description
1	TXD	Input	Transmit data	MCU CAN TXD	CAN transmit data input from the MCU
2	GND	Output	Ground	Ground	Ground termination
3	VDD	Output	VDD internal regulator output	Bypass capacitors	5 V power supply output, requires external bypass capacitors.
4	RXD	Output	Receive data	MCU CAN RXD	CAN receive data output to the MCU
5	VIO	Input	Voltage supply for IO	3.3V or 5 V	Supply voltage input for the digital input and output pins. This should be matched to the IO voltage supply of the MCU. Typically this is 5 V, but can also be 3.3 V.
6	EN	Input	Enable	MCU	This is the enable input for the device in static mode control. This is the master output/slave input when used in SPI mode, and the MOSI (master out, slave in) during SPI operation.
7	INH	Output	Inhibit	Use depends on intended operation1	Inhibit output for control of an external power supply regulator
8	ERR	Output	Active low error	MCU	Pin for static error and wakeup flag reporting MISO (master in, slave out) during SPI operation
9	WAKE	Input	Wake		Wake input
10	VSUP	Input	Voltage supply	Battery voltage	Battery supply pin, nominally 12 V
11	SPLIT	Output	Split		Output for connection of the CAN bus termination middle point
12	CANL	Input/Output	CAN bus low	CAN bus connector	CAN bus low pin
13	CANH	Input/Output	CAN bus high	CAN bus connector	CAN bus high pin
14	NTSB	Input	Standby	MCU	Standby input for device static mode control, CLK (clock) during P_SPI operation

1. The use of the Inhibit pin (INH) is dependent on the selected target system operation. INH can turn an external power supply on and therefore wake a connected MCU for operation to save power when MCU operation is not required

10.3.2. High-speed CAN: TJA1050

The figure below shows the typical connections for the physical interface between the MCU and the
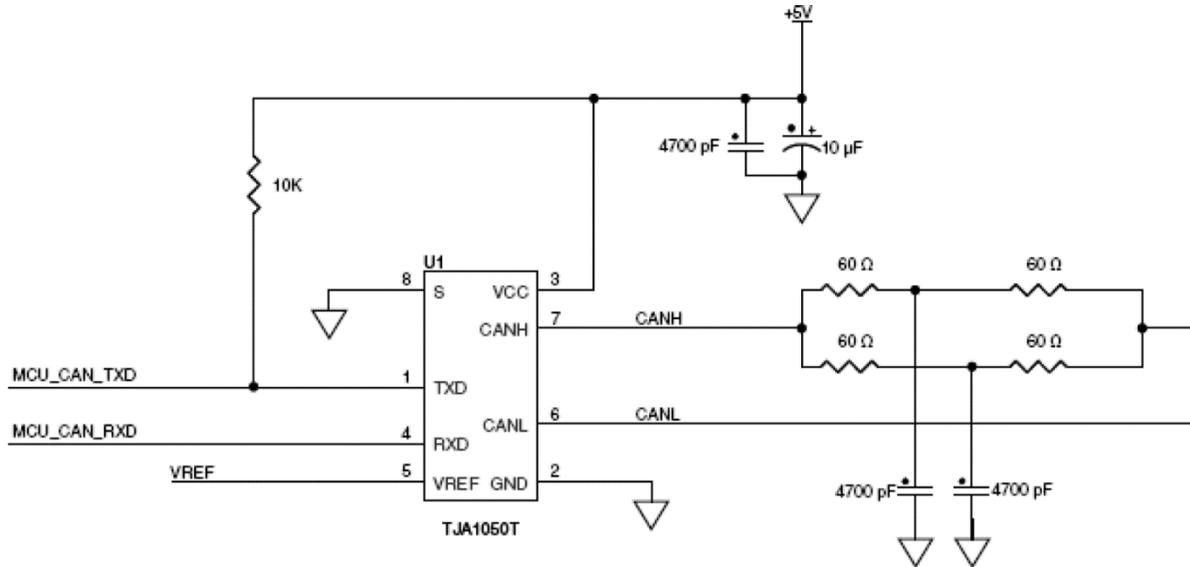
CAN bus for high-speed applications using the NXP TJA1050 HS CAN transceiver.

Figure 13. Typical high-speed CAN circuit using TJA1050

NOTE

Decoupling shown as an example only. TXD/RXD pull-up/pull-down may be required, depending on device implementation.

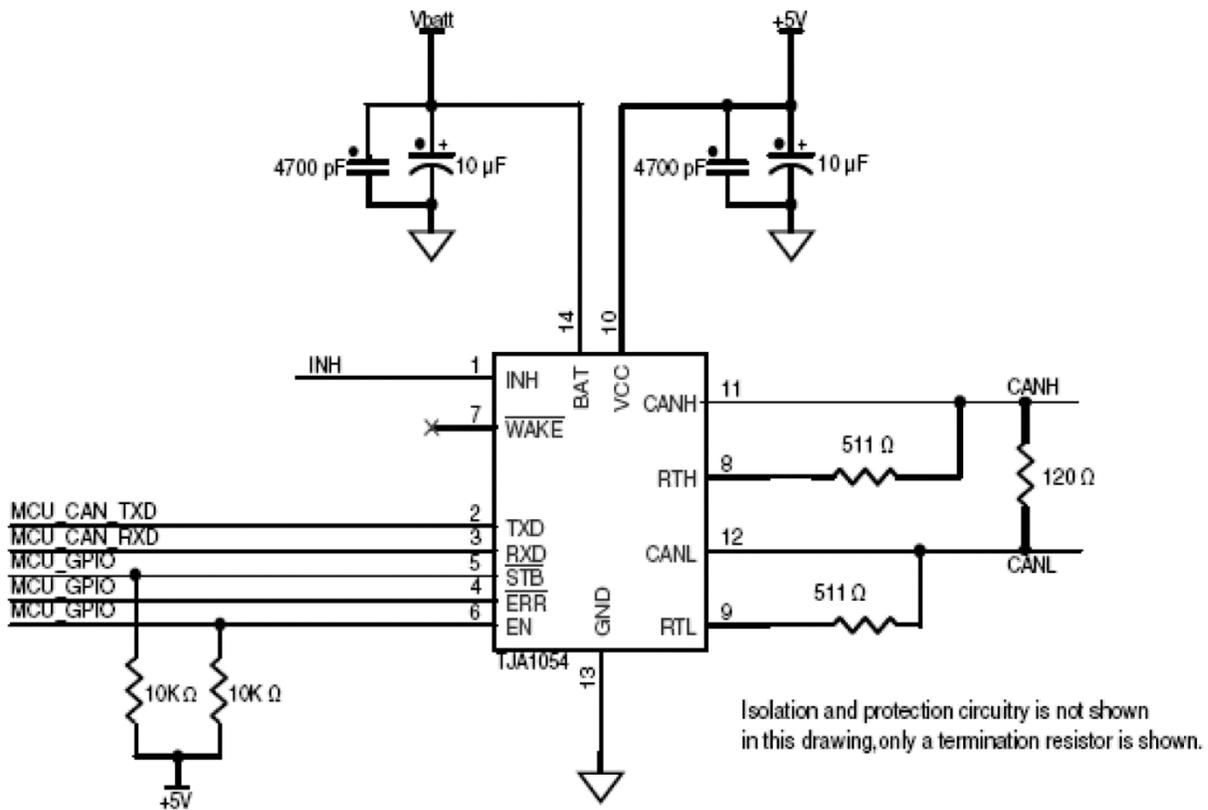The table below describes the TJA1050 pin and system connections.

Table 20. TJA1050 pin definitions and system connections

Pin	Name	Direction	Full Pin Name	Connection	Description
1	TXD	Input	Transmit data	MCU CAN TXD	CAN transmit data input from the MCU
2	GND	Output	Ground	Ground	Ground termination
3	VCC	Input	–	5V	Voltage supply input (5V)
4	RXD	Output	Receive data	MCU CAN RXD	CAN receive data output to the MCU
5	VREF	Output	Reference voltage output	Not used	Mid-supply output voltage. This is typically not used in many systems, but can be used if voltage translation needs to be done between the CAN transceiver and the MCU.
6	CANL	Input/ Output	CAN bus low	CAN bus connector	CAN bus low pin
7	CANH	Input/ Output	CAN bus high	CAN bus connector	CAN bus high pin
8	$\overline{\text{S}}$	Input	Select	Grounded or MCU GPIO	Select for high-speed mode or silent mode. Silent mode disables the transmitter, but keeps the rest of the device active. This

				may be used in the case of an error condition.

10.3.3. Low-speed CAN: TJA1054

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for low-speed applications using the NXP TJA1054 LS CAN transceiver. Optionally, the standby and enable pins can be connected to MCU GPIO pins for additional control of the physical

interface.

Figure 14. Typical low-speed CAN circuit using TJA1054

NOTE

Decoupling shown as an example only. STB and EN should be pulled high for Normal mode. These signals can optionally be connected to MCU GPIO pins to allow MCU control of the physical interface.

The table below describes the TJA1054 pins and system connections.

Table 21. TJA1054 Pin definitions and system connections

Pin	Name	Direction	Full Pin Name	Connection	Description
1	INH	Input	Inhibit	Typically not connected.	Inhibit output for control for an external power supply regulator if a wake up occurs.

Pin	Name	Direction	Full Pin Name	Connection	Description
2	TXD	Input	Transmit data	MCU CAN TXD	CAN transmit data input from the MCU
3	RXD	Output	Receive data	MCU CAN RXD	CAN receive data output to the MCU
4	ERR	Output	Error	MCU GPIO	The error signal indicates a bus failure in normal operating mode or a wake up is detected in Standby or Sleep modes.
5	STB	Input	Voltage Supply for IO	MCU GPIO	Standby input for device. It is also used in conjunction with the EN pin to determine the mode of the transceiver.
6	EN	Input	Enable	MCU GPIO	Enable input for the device. It is also used in conjunction with the STB pin to determine the mode of the transceiver.
7	WAKE	Input	Wake	Typically not connected.	Wake input (active low), both falling and rising edges are detected.
8	RTH	Input	Termination resistor high	Resistor to CANH	Termination resistor for the CAN bus high
9	RTL	Input	Termination resistor low	Resistor to CANL	Termination resistor for the CAN bus low
10	VCC	Input	Voltage supply	5V	Digital IO supply voltage, 5V
11	CANH	Output	CAN bus high	CAN bus connector	CAN bus high pin
12	CANL	Input/output	CAN bus low	CAN bus connector	CAN bus low pin
13	Ground	Output	Ground	Ground	Ground return termination path
14	BAT	Input	Standby	Battery voltage	Battery supply pin, nominally 12V

10.3.4. Recommended CAN Connector

Generally DB-9 connectors are used for evaluation boards to connect CAN modules together, whereas there are various connectors used for production hardware. The following figure shows the DB-9 connector and socket configuration of a typical evaluation board connector. A socket (female) is used on the evaluation board and a cable with a connector (male) connects with it

Figure 15. DB-9 connector and socket

The table below shows the typical connector pinout definition.

Table 22. DB-9 signal mapping

Pin number	Signal name
1	N/C
2	CAN_L
3	GND
4	N/C
5	CAN_SHEILD (optional)
6	GND
7	CAN_H
8	N/C
9	CAN_V+ (optional)

10.4. Ethernet Interface

The 10/100 Mbit/s Ethernet MAC (ENET) implemented on the MPC574xP is compliant with the IEEE802.3-2002 standard. It provides compatibility with half- or full duplex 10/100 Mbit/s Ethernet LANs.

An external transceiver interface and transceiver function are required to complete the connection to the physical interface. The figure below shows a typical set up of the complete interface to the network. Here a TJA1100 from NXP is used as the Ethernet PHY.
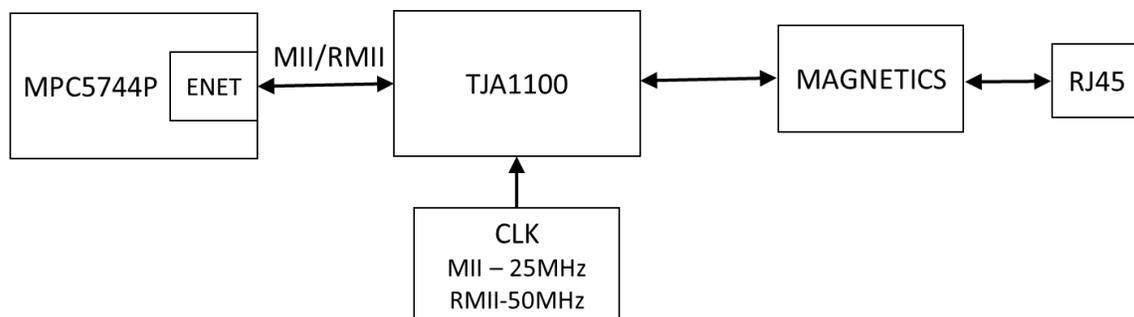
Figure 16. Ethernet application configuration example

As shown in Figure above the ENET can interface to a PHY using either the 10/100 Mbit/s MII operating at 2.5/25 MHz, a non-standard MII-Lite operating at 2.5/25 MHz or RMII operating at 50 MHz. The ENET signals from the MCU take their voltage level from the VDD_HV_IO supply domain. The ENET signals are summarized in the table below and their use in each interface type is highlighted. Note that the signals required by different PHYs will vary in some cases for each interface option; see the Data Sheet for your selected PHY.

Table 23. MPC574xP Ethernet Signals

MII	RMII	Description	I/O
MII_COL	-	Asserted upon detection of a collision and remains asserted while the collision persists. This signal is not defined for full-duplex mode.	I
MII_CRS	-	Carrier sense. When asserted, indicates transmit or receive medium is not idle. In RMII mode, this signal is present on the RMII_CRS_DV pin.	
MII_MDC	RMII_MDC	Output clock provides a timing reference to the PHY for data transfers on the MDIO signal.	O
MII_MDIO	RMII_MDIO	Transfers control information between the external PHY and the media-access controller. Data is synchronous to MDC. This signal is an input after reset.	I/O
MII_RXCLK	-	In MII mode, provides a timing reference for RXDV, RXD[3:0], and RXER.	I
MII_RXDV	RMII_CRS_DV	Asserting this input indicates the PHY has valid nibbles present on the MII. RXDV must remain asserted from the first recovered nibble of the frame through to the last nibble. Asserting RXDV must start no later than the SFD and exclude any EOF. In RMII mode, this pin also generates the CRS signal.	I
MII_RXD[3:0]	RMII_RXD[1:0]	Contains the Ethernet input data transferred from the PHY to the media-access controller when RXDV is asserted.	I
MII_RXER	RMII_RXER	When asserted with RXDV, indicates the PHY detects an error in the current frame.	I
MII_TXCLK	-	Input clock, which provides a timing reference for TXEN, TXD[3:0], and TXER.	I
MII_TXD[3:0]	RMII_TXD[1:0]	Serial output Ethernet data. Only valid during TXEN assertion.	O
MII_TXEN	RMII_TXEN	Indicates when valid nibbles are present on the MII. This signal is asserted with the first nibble of a preamble and is de-asserted before the first TXCLK following the final nibble of the frame.	O
MII_TXER	-	When asserted for one or more clock cycles while TXEN is also asserted, PHY sends one or more illegal symbols.	O
	RMII_REF_CLK	In RMII mode, this signal is the reference clock for receive, transmit, and the control interface.	I
1588_TMR*n*	1588_TMR*n*	Capture/compare block input/output event bus. When configured for capture and a rising edge is detected, the current timer value is latched and transferred into the corresponding ENET_TCCRn register for inspection by software. When configured for compare, the corresponding signal 1588_TMRn is asserted for one cycle when the timer reaches the compare value programmed in register ENET_TCCRn.	I/O

MII	RMII	Description	I/O
		An interrupt or DMA request can be triggered if the corresponding bit in ENET_TCSRn[TIE] or ENET_TCSRn[TDRE] is set.	
ENET_1588_CLKIN	ENET_1588_CLKIN	Alternate IEEE 1588 Ethernet clock input; Clock period should be an integer number of nanoseconds	I

10.5. Zipwire Interface

The Zipwire interface is intended to be used to communicate between two nodes implemented on a single board. The interface uses a "low speed" reference clock that is shared between the two nodes. A single-ended 10, 13, 20 or 26 MHz reference clock is used to generate the Zipwire high speed operation of approximately 320 MHz. A termination resistor is required at the receiving end of the clock for best performance of the interface. The value of the resistor depends on the board layout and impedance. See NXP application note AN5134, "Introduction to the Zipwire Interface" for further details.

The data signals use a low voltage differential signaling (LVDS) that is internally terminated on the MCU. The following diagram shows the connection between two devices.
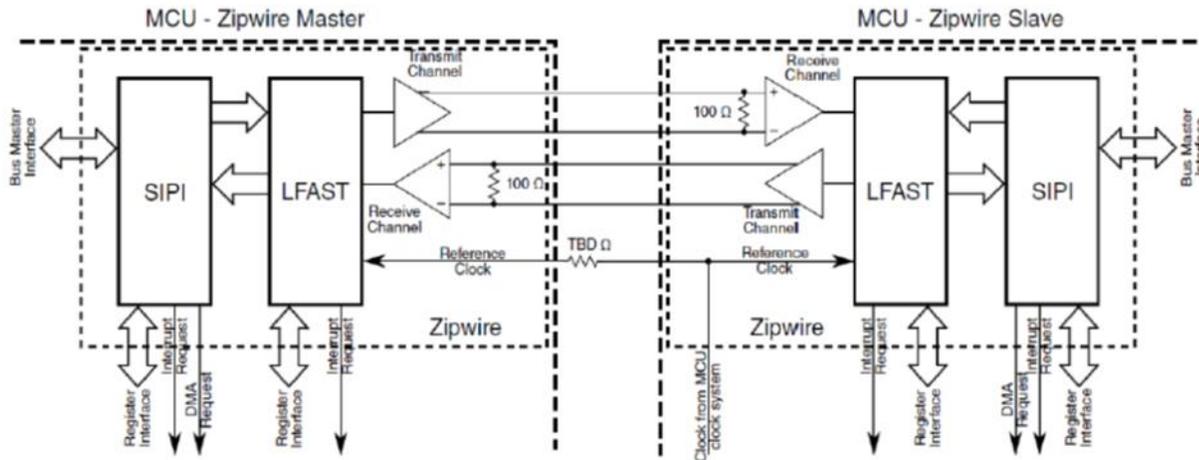
Figure 17. Typical Zipwire hardware interface

The Zipwire interface is a high-speed interface, therefore care should be taken in laying out the signals on a printed circuit board. The following guidelines are suggested.

- A controlled impedance PCB is required for the LVDS signals.
- The differential LVDS + and – pair should be routed parallel and close to each other. The length of the + and - pairs should be matched to less than 0.05 inches of difference.
- The LVDS transmit pairs should be of the same approximate length (within 0.1 inches). The receive pins should also be the approximate length (within 0.1 inches), but are not required to be the same length as the transmit signals.
- The differential pair should be routed with a maximum of two vias. Ideally, the differential pair should be routed without vias on a single plane of the board preferably on the top or bottom plane of the board. However, due to pin escape issues with the placement of the high speed signals on the surface mounted devices, routing on a single layer is not possible.

- Keep necking of the signal to less than 0.01 inch to avoid discontinuities. Some necking is usually required in escaping the signals for the BGA or LQFP signal feeds to other layers on the board.
- The differential pair must be routed on a layer that is one dielectric away from ground.
- A connector is not recommended for the Zipwire interface, but if a connector is used, a high speed connector system, such as the Samtec ERF8 0.8 mm Edge Rate Rugged High Speed Socket, should be used with twin-ax cabling. The odd side of the connector should be placed parallel and nearest to the MCU package on the board to allow direct connection to the package signals. See Zipwire connector.

11. References

- AN4224
- AN4881
- AN5032
- AN5134

12. Revision history

Table 24. Revision history

Rev No.	Updates
0	Initial release
1	- In Table 4. Recommended decoupling capacitors for row set VDD_LV_COR changed the entry under Decoupling Capacitors column from "4.7 uF (x6), 0.1 uF (x6)" to "3.3 uF (x4), 47 nF (x6)". - Added footnotes to row set VDD_HV_IO and VDD_LV_COR.
2	- In Table 1. MPC574xP features differing by package deleted the DSPI row. - In Power Supplies changed the text from "It can be assumed that the internal regulator has no undesirable impact if the ballast transistor is not present (however, the internal regulator can be switched PMC_PMCCR[INT_REG_BYPASS] to 1)" to "When external power supply is used the internal regulator must be switched off bysetting PMC_PMCCR[INT_REG_BYPASS] to 1.

	The reason is that the regulator is still working and could create some noise " and added the note "When using an external power supply it is ok to leave BCTRL floating or to connect it to any of the supply or ground pins through a large resistor (> 10 kΩ). It must not be connected directly to any supply or ground pin".
3	• In Power Supplies added a note "The device must always be operated within the correct voltage range of the data sheet, especially, if the internal LVDs are disabled. Device voltages must be in valid operating range, when device is booting up after a long/short functional reset, destructive RESET or POR. In case of synchronous or asynchronous abort during the self test execution the nominal current transient of 30 mA/us (Offline BIST)/120 mA/us (Online BIST) can occur."

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