NXP Semiconductors
Application Note

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MPC5777C Hardware Requirements/Example Circuits

Including Operation of the On-Chip Regulators and Regulator Controller

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Contents

1 Introduction

The MPC5777C is an advanced microcontroller initially intended for automotive powertrain applications. It is based on the e200z7 Power Architecture® core and features two, identical e200z759 cores, one of which may optionally be run in lockstep with a companion e200z758 checker core for added safety.

The MPC5777C requires multiple internal power supply voltages, but the device can run from a single 5 V power supply by generating the other voltages with internal regulators and an internal regulator controller. The major power supplies for the device are 5 V, 3.3 V, and 1.25 V. The 5 V supply is for powering the internal regulator, the Analog to Digital Converters, and can be used for the pin input and output voltages. In addition, 3.3 V is required for the internal pad prebuffers and flash memory. The majority of the internal logic is powered by 1.25 V. The SRAM has a separate supply input for keep-alive features, if SRAM keep-alive functionality is required. 3.3 V (for the flash module only) and 1.25 V can be generated from the internal regulators and regulator controller. If using the external bus or external debug trace features or if any of the pin input/output segments require 3.3 V, an external 3.3 V supply is also required.

This application note shows the options of the MPC5777C power supplies and the correct external circuitry required:

- Power supplies, including digital supplies, analog supplies, SRAM standby supply, and phase-locked loop supply
- Proper configuration of the PLL circuitry
- Other major external hardware required for the device
- Examples of other common external interfaces for communication as well as typical analog circuitry
- Handling of injection current, including requirements for power supply ramp rates

Please note that information from the MPC5777C Reference Manual, Datasheet, and/or Errata report may be repeated in this application note for the convenience of the reader. The reference manual, datasheet, and errata report are the official specification for the MPC5777C and should be reviewed for the most up-to-date information available for this device.

2 MPC5777C package options overview

The MPC5777C is available in two package options. Both of the packages are Molded Array Process Ball Grid Arrays (MAPBGA).

Table 1. MPC5777C Package Options

Package	Feature differences due to the package
416 MAPBGA	Primary device with the base features of the device. No development bus (including no CLKOUT). BOOTCFG0 not available since there is no external bus from which to boot.
516 MAPBGA	All of the features of the 416 MAPBGA package with the addition of access to the development bus (External Bus Interface).

The following table shows the available package sizes. See the device data sheet for complete package dimensions and ball placement.

Table 2. Package Sizes

Package	Physical Size	Configuration
416 MAPBGA	27 mm x 27 mm	1 mm ball pitch with four outer rows of balls with a center section of balls for thermal enhancement and power supplies
516 MAPBGA	27 mm x 27 mm	1 mm ball pitch with six outer rows of balls with a center section of balls for thermal enhancement and power supplies; outermost and innermost rows are not fully populated

NOTE

This document uses the terms pins, balls, and pads interchangeably when referencing the external signals of the device.

3 Power supply options

The MPC5777C MCU is designed for a wide range of applications. Based on system requirements and available power supplies, some applications may require different methods of powering the device. The table below summarizes the options available for powering the MCU. Two options require only a single 5 V supply and a few external components to power the MCU. The MCU will generate its own 1.25 V digital logic and 3.3 V flash supplies. The final option is to provide 5 V, 3.3 V, and 1.25 V from an external power supply. Other options are available that use combinations of the internal and external power supplies.

NOTE

The 1.25 V regulator controller requires external circuitry when used. The 3.3 V flash regulator is completely internal, with the exception of requiring external bypass capacitance.

Table 3. MPC5777C power supply options

Configuration	Mode Name	3.3 V Flash Supply	1.25 V regulator controller	REGSEL	VDDFLA	VDDPMC & VDDPWR	Reference
Internal 3.3 V flash regulator with 1.25 V linear regulator controller	LDO5V	Internal regulator	Internal linear mode	Low/GND	Bypass caps	External 5 V supply	See Using the internal regulator and regulator controller
Internal 3.3 V flash regulator with 1.25 V SMPS[1] regulator controller	SMPS5V	Internal regulator	Internal SMPS	High/5 V	Bypass caps	External 5 V supply	
External 3.3 V regulator with internal 1.25 V linear regulator controller	LDO3V	External	Internal linear mode	Low/GND	External 3.3 V supply	External 3.3 V supply	See Using internal and external supplies
External 3.3 V regulator with internal 1.25 V SMPS regulator controller	SMPS3V	External	Internal SMPS	High/3.3 V	External 3.3 V supply	External 3.3 V supply	
External supplies with on-chip low voltage detect	External[2]	External	External supply	Low/GND	External 3.3 V supply	External 3.3 V supply	See Using external supplies
External Supplies, except flash powered by internal regulator[3]	External	Internal regulator	External Supply	Low/GND	Bypass caps	External 5 V supply	See Internal linear 3.3 V regulator

1. Switch Mode Power Supply (SMPS).
2. This mode is the same as LDO3V, except the internal low voltage (1.25 V) regulator controller is not used.
3. This option allows the use of the external power supplies, except that it allows the internal 3.3 V regulator to power the flash. It is highly recommended that flash be powered by the internal 3.3 V regulator in all systems.

3.1 Power supply signals

The following table shows all pins related to the power supply. The nominal voltages are shown, the device data sheet should be referenced for the minimum and maximum voltages allowed on each of the pins.

Table 4. Power supply pins

	Pin name	Nominal voltage	Direction (relative to MCU)	Description
Standby supply	VSTBY	0.95 V to 5.5 V	In	SRAM standby supply — V_{STBY} is the power supply input that is used to maintain a portion of the contents of internal SRAM during power-down. If not used, tie V_{STBY} to VSS.

Table continues on the next page...

Table 4. Power supply pins (continued)

	Pin name	Nominal voltage	Direction (relative to MCU)	Description
PMC pins	VDDPMC	5 V or 3.3 V	In	PMC analog supply.
	VDDPWR	VDDPMC (5V or 3.3 V)	In	PMC digital supply for SMPS regulator. Whether or not the SMPS regulator is being used, this pin should be tied to the same voltage supply as VDDPMC.
	REGSEL	0 or VDDPMC (5 V or 3.3 V)	In	Regulator select determines the PMC regulator mode (linear/ switch mode). Low selects the linear 1.25 V regulator controller. High selects the SMPS 1.25 V regulator controller. If using the SMPS regulator, tie REGSEL to VDDPMC.
	REGCTL	—	Out	Regulator control is the output from the regulator that controls the external transistor for the 1.25 V regulator. In linear mode this is a current that is varied to change the gain of the external NPN transistor to hold a constant voltage on the transistor emitter (connected to the VDD signals). In SMPS mode this is a pulse width modulated (PWM) signal that drives the gate of an external P-MOSFET transistor. The duty cycle of the PWM is varied. The filter network, connected between the drain of the transistor and the VDD supply signals of the MCU, creates an analog DC voltage.
	VDDFLA	3.3 V	In/Out	Provides bypass capacitance for the internal 3.3 V flash regulator. May be used as a 3.3 V supply input to externally supply the flash voltage if, and only if, VDDPMC and VDDPWR are supplied the same 3.3 V level. Otherwise this pin should be connected only to bypass capacitance as specified in the datasheet.
Internal Logic Supply	VDD	1.25 V	In	Internal voltage input — V_{DD} supplies the internal circuitry and can be powered by the 1.25 V internal regulator controller or an external 1.25 V supply.
I/O Supplies	VDDEH1	5 V	In	"High Voltage" Input and Output Power Supply Input - V_{DDEH1} supplies the high voltage input and output pins including reset and configuration inputs. Must be supplied nominal 5 V.
	VDDEH3 VDDEH4 VDDEH5 VDDEH6 VDDEH7	3.3 V or 5 V	In	"High Voltage" Input and Output Power Supply Input - V_{DDEHx} are the supplies for the high voltage input and output pins. Each segment can be set to different voltages if required (3.3 V or 5 V).
	VDDEH3A	3.3 V or 5 V	In	Split from V_{DDEH3} to allow separate supply of Ethernet MII I/O Pin Voltage if required.
	VDDE2	3.3 V or 5 V	In	"Low Voltage" Clock Output and Debug Supply Input - V_{DDE2} is the supply for the development debug port (Nexus trace, JTAG, and Engineering Clock [ENGCLK]) signals.

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Table 4. Power supply pins (continued)

	Pin name	Nominal voltage	Direction (relative to MCU)	Description
	VDDE2A	3.3 V or 5 V	In	Split from V_{DDE2} to allow separate supply of Ethernet RMII I/O Pin Voltage if required.
	VDDE8 VDDE9 VDDE10	3.3 V or 5 V	In	V_{DDEn} are the supplies for the development bus signals (data, address, and control). These should be supplied from an external power supply.
Analog Supplies	VDDA_EQ VDDA_SD	5 V	In	Analog Power Supply Input — V_{DDA_EQ} and V_{DDA_SD} are the analog supply input pins for eQADC and SDADC modules, respectively.
	VDDA_MISC	5 V	In	True Random Number Generator (TRNG), Temperature Sensor, and IRC Voltage Supply
	VSSA_EQ VSSA_SD	Ground	In	Analog Ground Return — V_{SS_EQ} and V_{SS_SD} are the analog supply return pins for eQADC and SDADC.
	VRH_EQ VRH_SD	5 V	In	Analog High Reference — V_{RH_EQ} and V_{RH_SD} are the voltage reference high input pins for eQADC and SDADC.
	VRL_EQ VRL_SD	Ground	In	Analog High Reference — V_{RL_EQ} and V_{RL_SD} are the voltage reference low input pins for eQADC and SDADC.
	REFBYPCA75 REFBYPCB75	Approximately 3.75 V (output)	Out	ADC Internal Reference Bypass Capacitor — REFBYPCA75 and REFBYPCB75 require external bypass capacitors pins for the eQADC 75% reference.
	REFBYPCA25 REFBYPCB25	Approximately 1.25 V (output)	Out	ADC Internal Reference Bypass Capacitor — REFBYPCA25 and REFBYPCB25 require external bypass capacitors pins for the eQADC 25% reference.

3.1.1 I/O power and ground segmentation

Some of the supplies can be configured with different supply voltages. In particular, the MCUs allow flexibility in the selection of voltage levels on many of the supplies that power input and output pins. These supplies are labeled VDDE or VDDEH and are broken into segments. Each segment can be connected to different supply voltages if required. The VDDE supplies are generally 3.3 V (nominal voltage) or lower. The VDDEH supplies are "high" supplies and usually connected to a nominal 5.0 V. However, any of these supply segments may be connected to 3.3 V or 5 V nominal voltage. VDDEH1 is an exception and must be supplied a nominal 5 V level.

Refer to the "System I/O Definition" spreadsheet attached to the MPC5777C reference manual for a detailed listing of supply segment to pin assignments.

3.1.2 Power supply package differences

There are different numbers of balls available for the power supply in each of the different package options. In addition, for some package options, some power supplies are not available. The table below shows, for each package, the number of balls available for the power supply input to the device. All supply balls that are available on the package should be connected to a supply voltage.

Table 5. Number of power supply balls versus package

Power supply	Nominal voltage	416 PBGA package	516 PBGA package
VDD	1.25 V	14	15
VSTBY	1 V, or 2 V to 6 V	1	1
VDDPMC	3.3 V or 5 V	1	1
VDDPWR	3.3 V or 5 V	1	1
VDDEH1	5 V	2	2
VDDE2	3.3 V to 5 V	14	14
VDDE2A	3.3 V to 5 V	1	1
VDDEH3	3.3 V to 5 V	1	1
VDDEH3A	3.3 V to 5 V	1	1
VDDEH4	3.3 V to 5 V	2	2
VDDEH5	3.3 V to 5 V	2	2
VDDEH6	3.3 V to 5 V	2	2
VDDEH7	3.3 V to 5 V	2	2
VDDE8	3.3 V	0	6
VDDE9	3.3 V	0	7
VDDE10	3.3 V	0	7
VDDA_EQ	5 V	2	2
VDDA_SD	5 V	1	1
VDDA_MISC	5 V	1	1

3.2 PMC overview

The power management controller (PMC) handles all of the on-chip voltage regulators, regulator controllers, power-on reset, and the voltage detect (HVD/LVD) circuitry. The figure below shows a block diagram of the PMC.

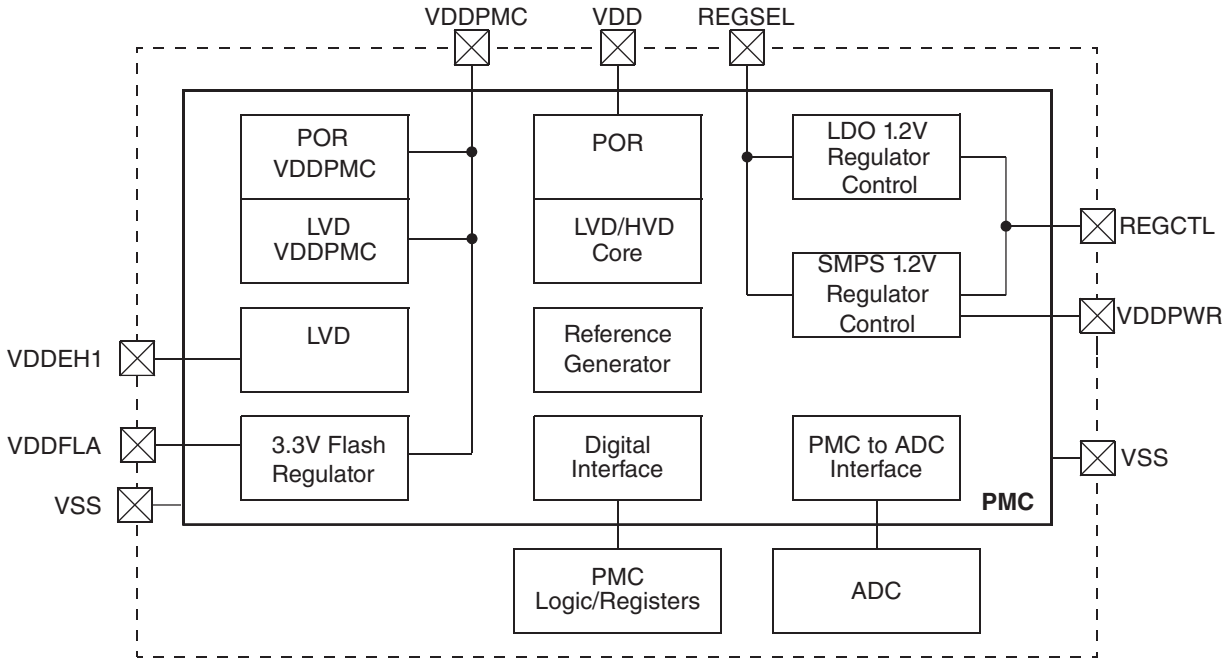

Figure 1. MPC5777C PMC analog block diagram

The various sub-blocks of the PMC will be discussed in the other sections of this application note, but the features of the PMC include:

- Supporting the use of internal or external voltage regulators
- Two options for a 1.25 V regulator controller: either a linear regulator that uses an external NPN transistor or a switch-mode regulator with an external PMOS FET, Schottky diode, and external inductor. The operating mode of the 1.25 V regulator controller is selectable with the REGSEL pin.

3.3 Power-on reset

The PMC controls the internal power-on reset (POR) for the MCU. When the critical power supplies are below minimum levels, the MCU is held in a reset state. The PMC POR holds the device in reset until the power supplies have reached a level high enough that the $\overline{\text{RESET}}$ input can be propagated through the device. The key supplies that are monitored by the PMC are:

- The 1.25 V core voltage
- VDDPMC regulator input voltage
- The 3.3 V flash voltage
- VDDEH1 power supply that powers the $\overline{\text{RESET}}$ pin

During POR the device I/O pins are held in a safe state that depends on which power supplies are on and which are turned off.

The table below lists the voltage levels monitored for POR assertion. The latest version of the MPC5777C Data Sheet should be consulted for the latest specifications.

Table 6. Supplies that control $\overline{\text{POR}}$ Assertion

Supply	Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
VDD	POR098_c	LV internal supply power on reset threshold	Rising	960	1010	1060	mV

Table continues on the next page...

Table 6. Supplies that control $\overline{\text{POR}}$ Assertion (continued)

Supply	Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
			Falling	940	990	1040	
VDDPMC	POR_HV	HV internal supply power on reset threshold	Rising	2444	2600	2756	mV
			Falling	2424	2580	2736	
VDDFLA	LVD_FLASH	Flash supply low voltage monitoring[1]	Rising	2956	3010	3053	mV
			Falling	2944	2998	3041	
VDDEH1	LVD_IO	$\overline{\text{RESET}}$ low-voltage detect (Enabled during reset)	Rising	3390	3420	3450	mV
			Falling	3360	3390	3420	

1. VDDFLA range is guaranteed when internal flash regulator is used.

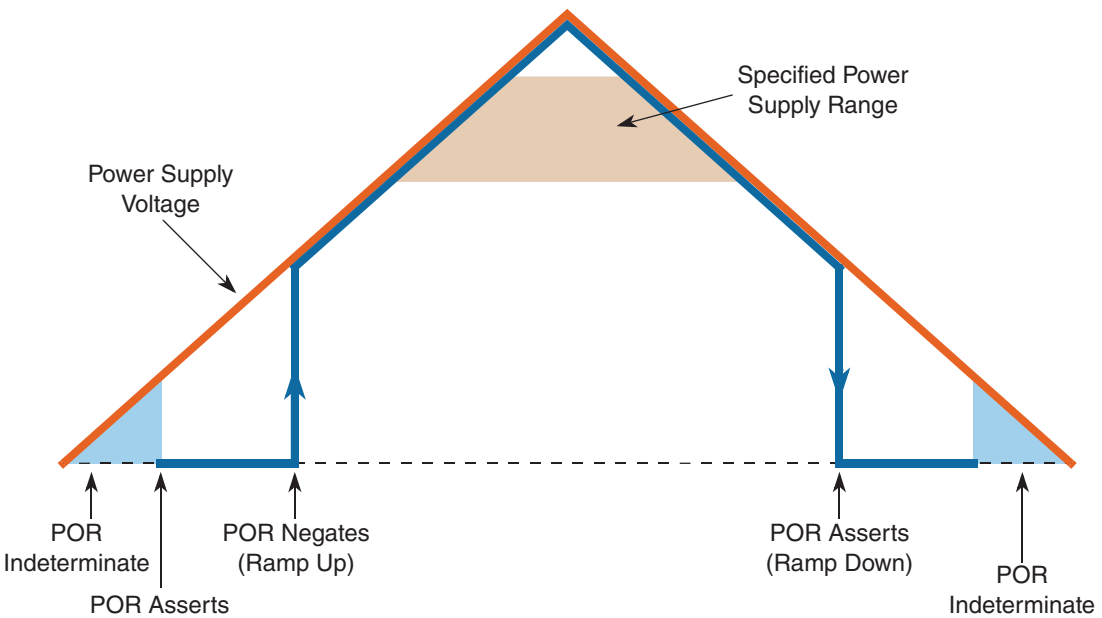

Figure 2. POR assertion/negation diagram

The figure above shows POR assertion and negation during power ramp-up and ramp-down. During the initial POR, the voltage on VDDEH1 (the power supply that powers the RESET input), as well as several other supplies, controls the exit of the power-on reset. After the MCU exits reset, user software can enable even more supplies to cause a reset assertion if the supplies dip below or rise above the specified voltages. See the Power Management Controller Module Reset Event Enable register (PMC_REE) in the MPC5777C Reference Manual for a complete list of the bits in this register. The bits shown in the table below affect the internal RESET assertion initially after a POR (and consequently $\overline{\text{RSTOUT}}$): the first assertion of reset during POR, and also the Low Voltage Detect (LVD) and High Voltage Detect (HVD) circuits. They can be enabled or disabled by the user.

Table 7. LVD/HVD reset control bits in the PMC_REE

PMC_REE Bit	Description	Default setting (following any reset)
HVD_FLASH	Flash supply high-voltage reset enable	1 (enabled)
HVD_HV	VDDPMC high-voltage reset enable	1 (enabled)
HVD_CORE	VDD (1.25 V) high-voltage reset enable	1 (enabled)
LVD_CORE_COLD	VDD (1.25 V) low-voltage reset enable	1 (enabled)

The figure below shows the relationship of the POR levels and the low-voltage detect circuits. The low-voltage detect circuits can be set to force a reset or an interrupt. An interrupt allows software to perform an orderly, controlled shut down of the MCU.

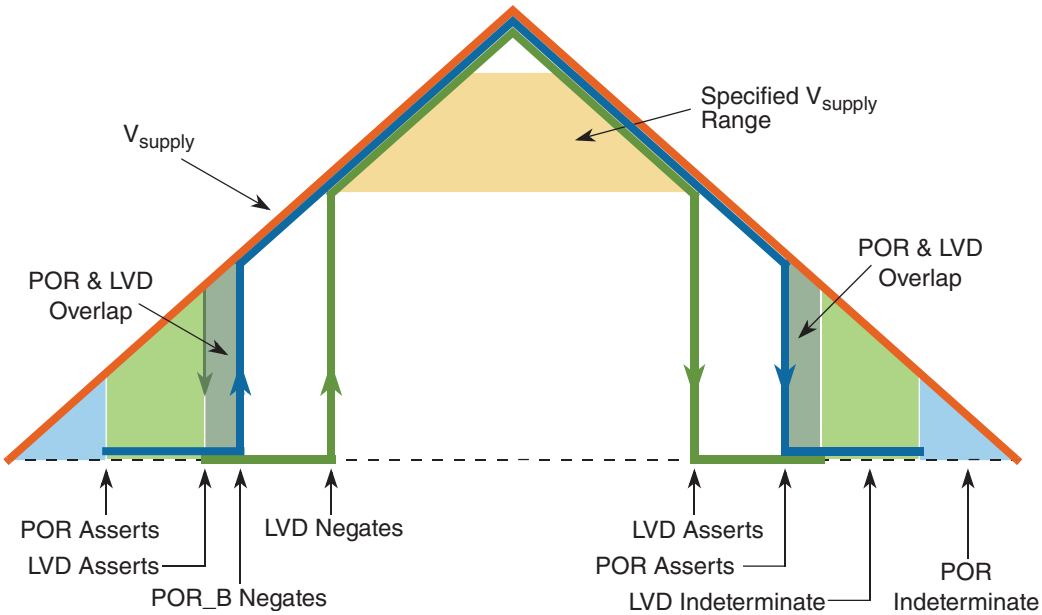

Figure 3. Low-voltage detect ramp up and down

3.4 Power up/down sequencing

The following rules apply for power supply sources during power up and power down in order to operate within specification:

- When V_{DDPMC} is tied to a nominal 3.3 V supply, V_{DDPWR} and V_{DDFLA} must both be shorted to V_{DDPMC} and star routed to minimize mutual noise. A star route layout means a track split as close as possible to the power supply source. Each of the split tracks is routed individually to the intended end connection.
- When V_{DDPMC} is tied to a 5 V supply, V_{DDPWR} must be tied to the same 5 V supply and star routed. V_{DDFLA} must be connected only to bypass capacitors.
- V_{DDA_MISC} must reach its specified minimum operating voltage before or at the same time as the monitored voltages: V_{DDPMC}, V_{DD}, and V_{DDEH1}. This ensures that the internal RC osciallator (IRC) is powered and operating correctly before the device is released from reset.
- Ramp up V_{DDA_EQ} before V_{DD}. Otherwise, a reset might occur.

The recommended power supply behavior is as follows: Use 25 V/ms or slower rise time for all supplies. Power up V_{DDPMC}/V_{DDPWR}, V_{DDA_MISC}, V_{DDA_EQ}, and all V_{DDEx}/V_{DDEHx} supplies first and then power up V_{DD}. For power down, drop V_{DD} to 0 V first, and then drop all other supplies. There is no limit on the fall time for the power supplies.

The state of the I/O pins during power up/down varies according to the following table.

Table 8. Power sequence pin states for output pads

V_{DD}	V_{DDEx} / V_{DDEHx}	Pad state
Low	High	Outputs tri-stated
High	Low	Outputs disabled
High	High	Normal operation

3.4.1 Power sequencing and POR dependent on V_{DDA}

During power-up or power-down, V_{DDA} can lag other supplies (of magnitude greater than $V_{DDEH}/2$) within 1 V. This prevents any forward-biasing of device diodes that cause leakage current and/or POR. If the voltage difference between V_{DDA} and V_{DDEH} is more than 1 V, the following will result:

- Triggering of POR (ADC monitors on $V_{DDEH}1$ segment which powers the $\overline{\text{RESET}}$ pin) if the leakage current path created, when VDDA is sufficiently low, causes sufficient voltage drop on $V_{DDEH}1$ node monitored crosses low-voltage detect level.
- If V_{DDA} is between 0–2 V, powering all the other segments (especially $V_{DDEH}1$) will not be sufficient to get the part out of reset.
- Each V_{DDEH} will have a leakage current to V_{DDA} of a magnitude of ($V_{DDEH} - V_{DDA} - 1$ V(diode drop)/200 KΩ) up to ($V_{DDEH}/2 = V_{DDA} + 1$ V).
- Each V_{DD} has the same behavior; however, the leakage will be small even though there is no current limiting resistor since V_{DD} = 1.32 V max.

3.4.2 Power-down

If V_{DD} is powered down before V_{DDE}/V_{DDEH}, then all drivers are tri-stated.

If V_{DDE}/V_{DDEH} is powered down before V_{DD}, then all pads are loaded through the drain diodes to V_{DDE}/V_{DDEH}. This presents a heavy load that pulls the pad down to a diode above V_{SS}. Current injected by external devices connected to the pads must meet the current injection specification found in the device datasheet.

3.4.3 Power-up

If V_{DDE}/V_{DDEH} is powered up before V_{DD}, then a threshold detector tri-states all drivers connected to V_{DDE}/V_{DDEH}. The various V_{DDE}/V_{DDEH} supply segments can be powered up in any order. For each V_{DDE}/V_{DDEH} supply not powered up, the drivers in that V_{DDE}/V_{DDEH} segment exhibit the characteristics described in the next paragraph.

If V_{DD} is powered up first, then all pads are loaded through the drain diodes to V_{DDE}/V_{DDEH}. This presents a heavy load that pulls the pad down to a diode voltage drop above V_{SS}. Current injected by external devices connected to the pads must meet the current injection specification found in the device datasheet.

3.5 Using the internal regulator and regulator controller

MPC5777C contains an internal regulator that can be used to generate 3.3 V for the internal flash memory. This regulator can be used along with the regulator controller for the low-voltage core supply (1.25 V). External capacitors are required for both the 3.3 V and the 1.25 V supplies. Additional external circuitry is required for the 1.25 V regulator controller. The 1.25 V regulator can operate in either linear or switch mode.

Optionally, an external 3.3 V supply can be used to bypass the internal flash regulator if the same 3.3 V supply is connected to all three of the following supply inputs: V_{DDPMC}, V_{DDPWR}, and V_{DDFLA}.

If used, the internal 3.3 V regulator only supplies the flash and not the 3.3 V I/O power segments. If 3.3 V I/O is required, then it must be supplied externally.

3.5.1 Internal linear 3.3 V regulator

The 3.3 V internal flash regulator is enabled automatically if V_{DDPMC} is greater than 4.5 V. If V_{DDPMC} is less than 4.5 V, then the 3.3 V regulator drive strength may be reduced (and not capable of sustaining the full load current during a flash erase procedure).

The following figure shows the recommended configuration for using the internal flash regulator and external 3.3 V and/or 5 V I/O supplies.

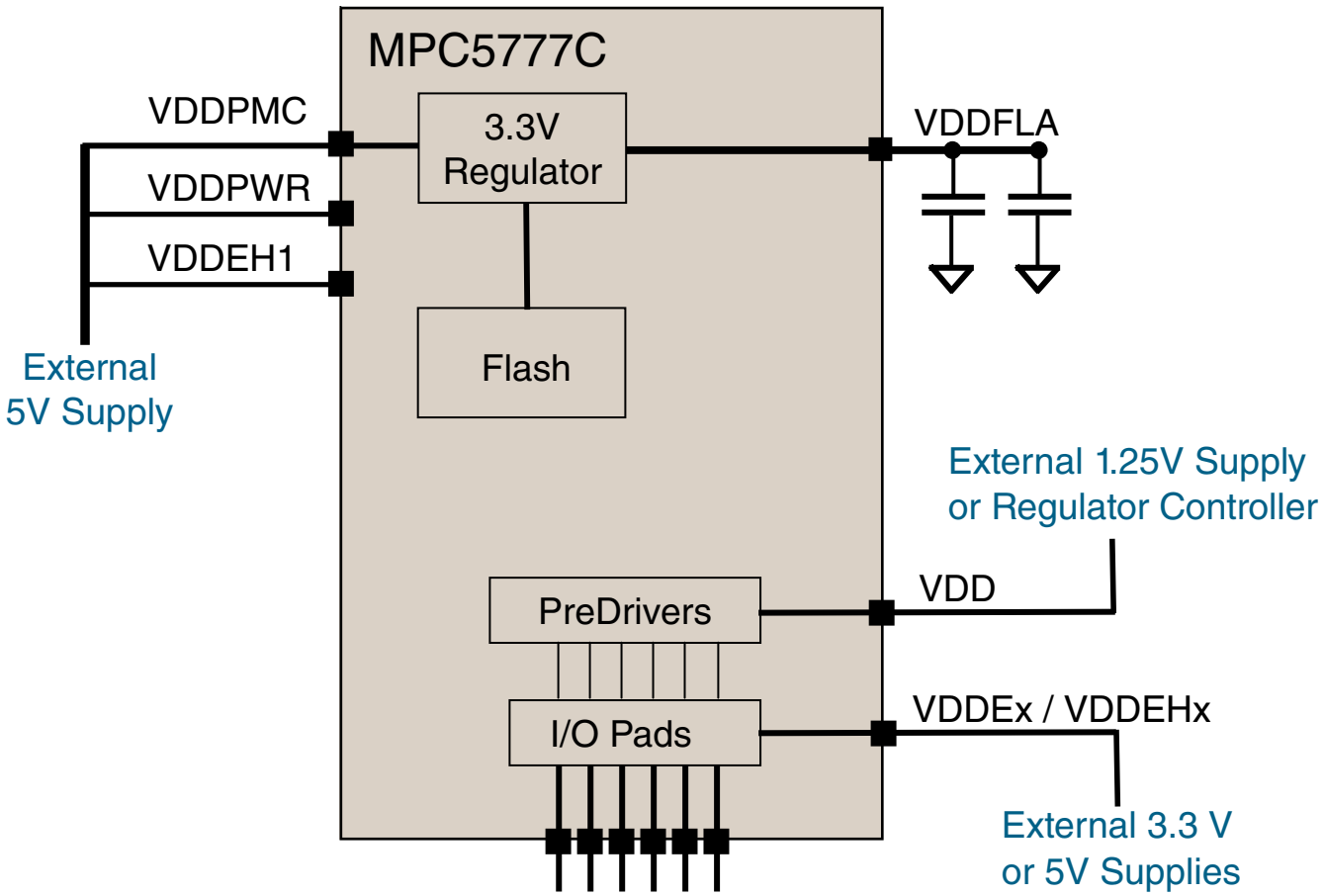

Figure 4. Recommended 3.3V power connections

3.5.2 1.25 V low-voltage regulator controller

The majority of the internal circuitry in MPC5777C operates on a 1.25 V nominal supply voltage. The device includes an on-chip regulator controller for providing this voltage. However, there are two options for the 1.25 V regulator controller: a linear regulator controller or a switch mode regulator controller. The linear regulator controller requires an external NPN transistor and the switch mode regulator controller requires an external PMOS[1] FET[2] with an external rectifier and inductor. The linear regulator circuit provides a low-noise, stable 1.25 V supply, but requires appropriate levels of current and power dissipation. The switch mode regulator also provides a stable 1.25 V supply, but has a lower overall power dissipation. Care is needed to insure that the switching frequency is isolated from any noise-sensitive circuitry in the target system.

1. P-Channel Metal Oxide Semiconductor
2. Field-Effect Transistor

3.5.2.1 Linear 1.25 V regulator controller

The linear 1.25 V regulator controller requires an external transistor and bypass capacitors. It operates in a closed loop mode. The figure below shows a typical configuration of the regulator circuit.

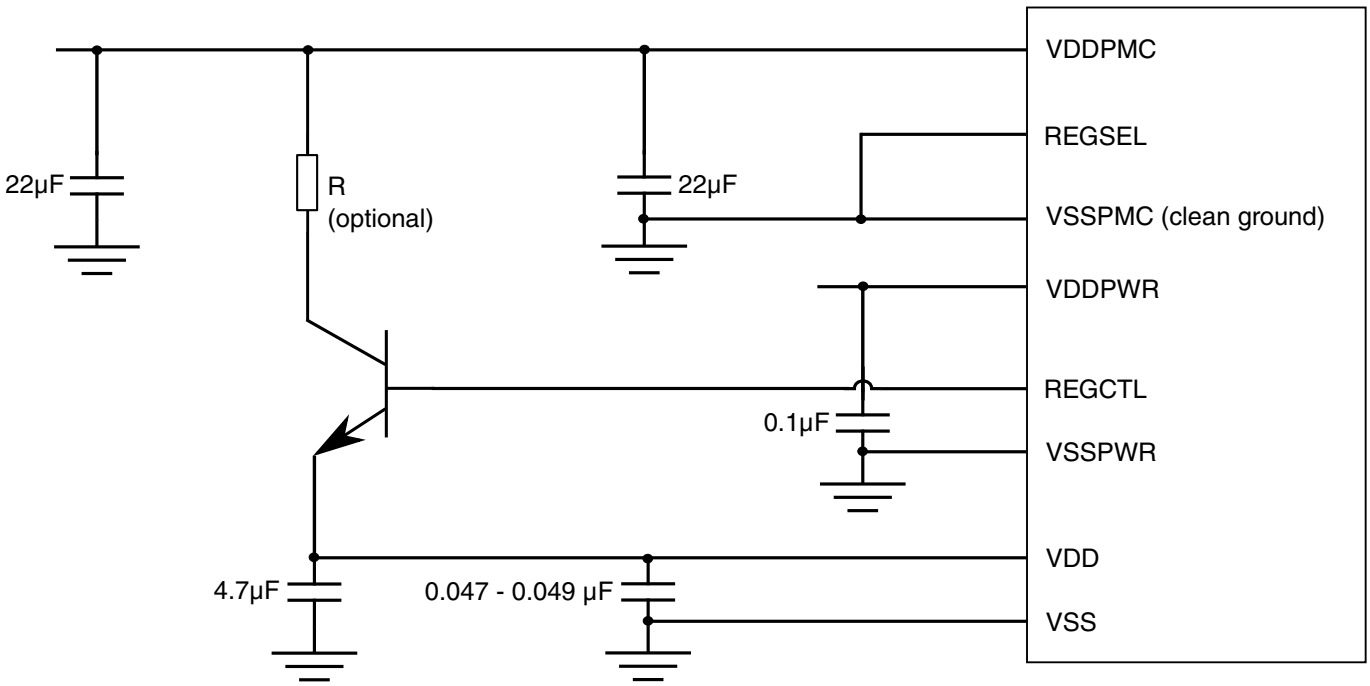

Figure 5. 1.25 V linear regulator circuitry

The PMC monitors the voltage on VDD via the VDD_{SENSE} signal. The VDD_{SENSE} signal is internal to the package of the device and does not have a physical ball on the package. The PMC controls the current on REGCTL, which drives the base of the external NPN transistor. This current is then amplified by the transistor to power VDD of the MCU.

3.5.2.1.1 Bipolar transistor requirements

The table below shows the characteristics required for the external bipolar NPN pass transistor.

Table 9. Bipolar NPN Transistor Requirements

Symbol	Characteristic	Value	Unit
hfe	Transistor gain (Beta)	60 - 550[1]	—
P_D	Absolute minimum power dissipation	1.6	W
I_{CMaxDC}	Minimum peak collector current	2.0	A
VCE_{SAT}	Collector to emitter saturation voltage	300[2]	mV
V_{BE}	Base to emitter voltage	0.95	V
V_C	Minimum voltage at transistor collector	2.5	V

1. The minimum gain required depends on the current required by the MCU (on VDD) and the available current from the REGCTL (See the MPC5777C Data Sheet).
2. Adjust collector to voltage supply source resistor value to avoid VCE < VCE_{SAT}

3.5.2.1.2 1.25 V linear regulator recommended components

The recommended bipolar NPN pass transistor is the NJD2873. A series resistor is recommended to assist in power handling of the drop from 5 V to 1.2 V. Proper heat-sinking may also needed. The NJD2873 has been specified to meet the requirements for the MPC5777C and is therefore the preferred transistor. In addition, the NJD2873 is in a DPAK package that allows a higher power dissipation.

Table 10. Recommended Transistor

Part	Type	Manufacturer
NJD2873T4	NPN transistor	ON Semiconductor™

The linear pass transistor should be placed near the MCU with a minimum of trace resistance and inductance. VDD should be placed on a layer near the ground layer and should be laid out to make maximum utilization of the board inter-capacitance. VDD should not be routed, it should be a maximum size plane (placed under the MCU) with low inductance.

The rest of the components for the regulator circuit, including the bypass capacitors, are shown in the following table.

Table 11. Passive Components

Component	Value	Quantity	Description
Capacitor	4.7 µF, 20 V	1	Ceramic low ESR
Capacitor	47 - 49 nF, 7 V	1 per VDD pin	Ceramic
Capacitor	22 µF, 20 V	1	Ceramic V_{DDPMC} (optional 0.1 µF)
Capacitor	22 µF, 20 V	1	Ceramic supply decoupling capacitor, ESR < 50 mΩ (as close as possible to NPN collector)
Capacitor	0.1 µF, 7 V	1	Ceramic V_{DDPWR}
Resistor	Application specific	1	Optional; reduces thermal loading on the NPN with high V_{DDPMC} levels

3.5.2.2 Switch mode 1.25 V power supply (SMPS)

MPC5777C includes an optional 1.25 V switching regulator controller that can be used instead of the linear 1.25 V on-chip regulator controller. The switching regulator is much more efficient than the linear regulator. This allows the overall current requirements (power dissipation) to be lower when using the switching regulator.

The switch mode regulator is selected by connecting the regulator select input (REGSEL) to the regulator voltage input (VDDPMC), instead of connecting REGSEL to 0 V. The switching regulator uses an external PMOS transistor, along with an external inductor, a Schottky rectifier, and a bulk capacitor. See the figure below for the recommended SMPS regulator circuitry.

The switch mode regulator controller circuitry contains a pulse-width modulated (PWM) controller that uses the duty cycle of the switching frequency to control the voltage that is applied to the VDD power supply input of the MCU. The switching frequency of the PWM circuit is between 825 KHz and 1.175 MHz. A voltage sense on VDD controls the actual duty cycle to control the voltage output of the regulator circuitry.

The layout of any switch mode regulator circuit is always critical and should be done with great care (see Switch mode supply layout guidelines).

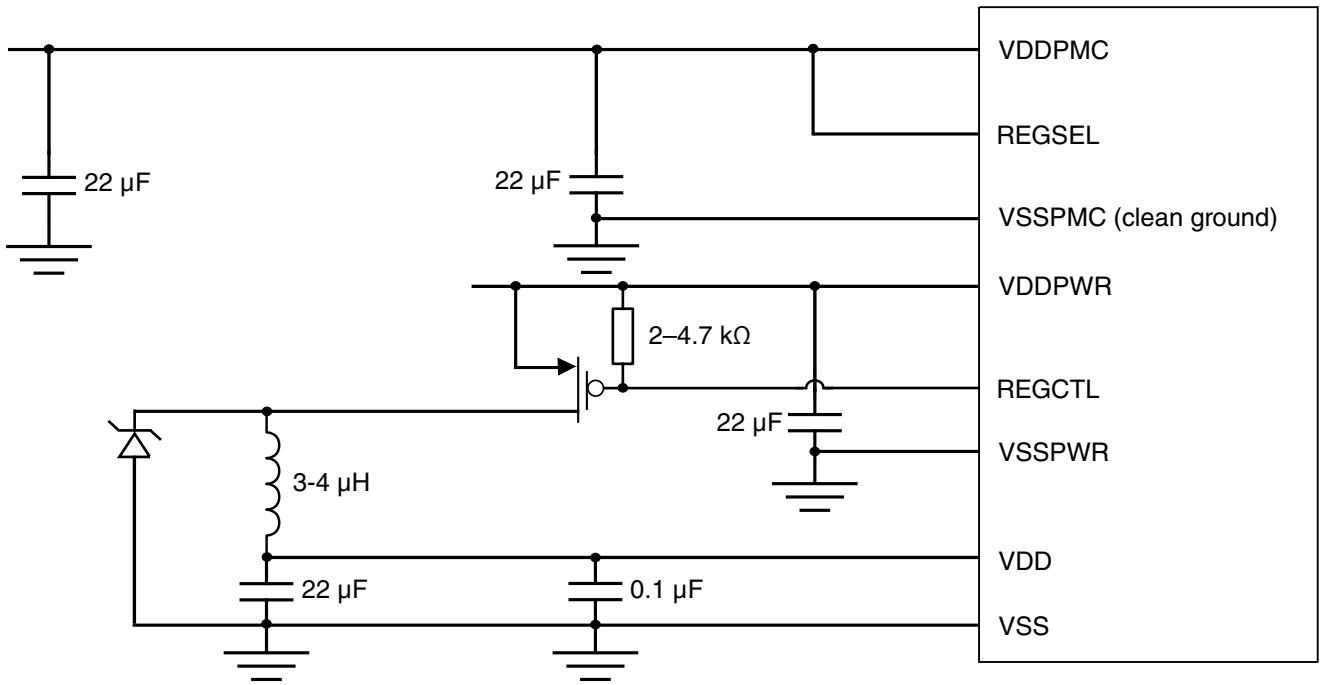

Figure 6. 1.2V SMPS regulator circuitry

3.5.2.2.1 SMPS PMOS transistor requirements

The table below shows the characteristics of the PMOS FET used for the SMPS.

Table 12. PMOS Transistor Requirements

Symbol	Characteristic	Minimum	Maximum	Unit
V_{TH}	Threshold voltage	—	2.0	V
$R_{DS(on)}$	Static drain-to-source on-resistance	—	100	Ω
C_G	Gate capacitance	—	5	nF

3.5.2.2.2 1.25 V SMPS recommended components

The SMPS regulator requires an external PMOS FET. This can either be a PMOS FET with an integrated low Vf Schottky diode or a separate PMOS FET and a separate low Vf Schottky diode.

Table 13. Recommended PMOS FET transistor

Part	Type	Manufacturer
SQ2301ES	Power MOSFET and Schottky diode	Vishay™
FDC642P	Power MOSFET and Schottky diode	Fairchild Semiconductor™
SS8P3L	Low V_f Schottky diode	Vishay™

The rest of the components for the SMPS regulator circuit, including the bypass capacitors, are shown in the following table. It should be noted that the component selection for the SMPS is more critical than for the linear regulator option, but has the benefit of overall lower current requirements.

Table 14. Passive components

Component	Value	Quantity	Description
Inductor	3 - 4 µH, 1.5 A	1	Buck shielded coil low ESR
Capacitor	22 µF, 20 V	1	Ceramic capacitor, total ESR < 70 mΩ
Capacitor	0.1 µF, 7 V	1 per VDD pin	Ceramic
Capacitor	22 µF, 20 V	1	Ceramic V_{DDPMC} (optional 0.1 µF capacitor in parallel)
Capacitor	22 µF, 20 V	1	Ceramic supply decoupling capacitor, ESR < 50 mΩ (as close as possible tothe p-MOS source)
Resistor	2 - 4.7 KΩ	1	Pullup for power p-MOS gate
Capacitor	22 µF, 20 V	1	Ceramic, connect 100 nF capacitor in parallel (as close as possible to packageto reduce current loop from V_{DDPWR} to V_{SSPWR})

3.5.2.2.3 Switch mode supply layout guidelines

The layout of the switch mode regulator circuit is critical to the proper operation and performance of the regulator.

- The input power supply capacitor, the output capacitor, and inductor should be located very close to the power MOS-Schottky diode.
- The output capacitor should be connected close to the inductor to the MCU ground.
- The common power ground for nodes with high switching currents should be separated from nodes with low switching currents.
- Minimize the inductance between the switching supply node and the decoupling/filtering capacitor, so that decoupling is effective and minimum energy is radiated.
- Star-connect all grounds to the ground plane below the MOS-Schottky device.
- Keep the gate control signal REGCTL far away from any other switching signals on the board and shield it with VSS.
- Place the smaller EMI/bypass capacitors underneath the microcontroller.
- Use the 5 V power trace exclusively as power to the source of the power MOS by means of star connection to the global 5 V power supply.

3.6 Using internal and external supplies

An external 3.3 V supply can be used for flash while still using the internal regulator controller. In this case, the three supply inputs V_{DDPMC}, V_{DDPWR}, and V_{DDFLA} must be shorted together and powered by the same 3.3 V supply. The figure below shows an example of this configuration using the linear regulator controller. However, it does not show all of the external 1.25 V circuitry. See Linear 1.25 V regulator controller for the complete requirements. An external 5 V supply is required for the V_{DDEH1} segment, which supplies reset circuitry. External 3.3 V and/or 5 V supplies may be used for all other I/O supply segments as needed by the application.

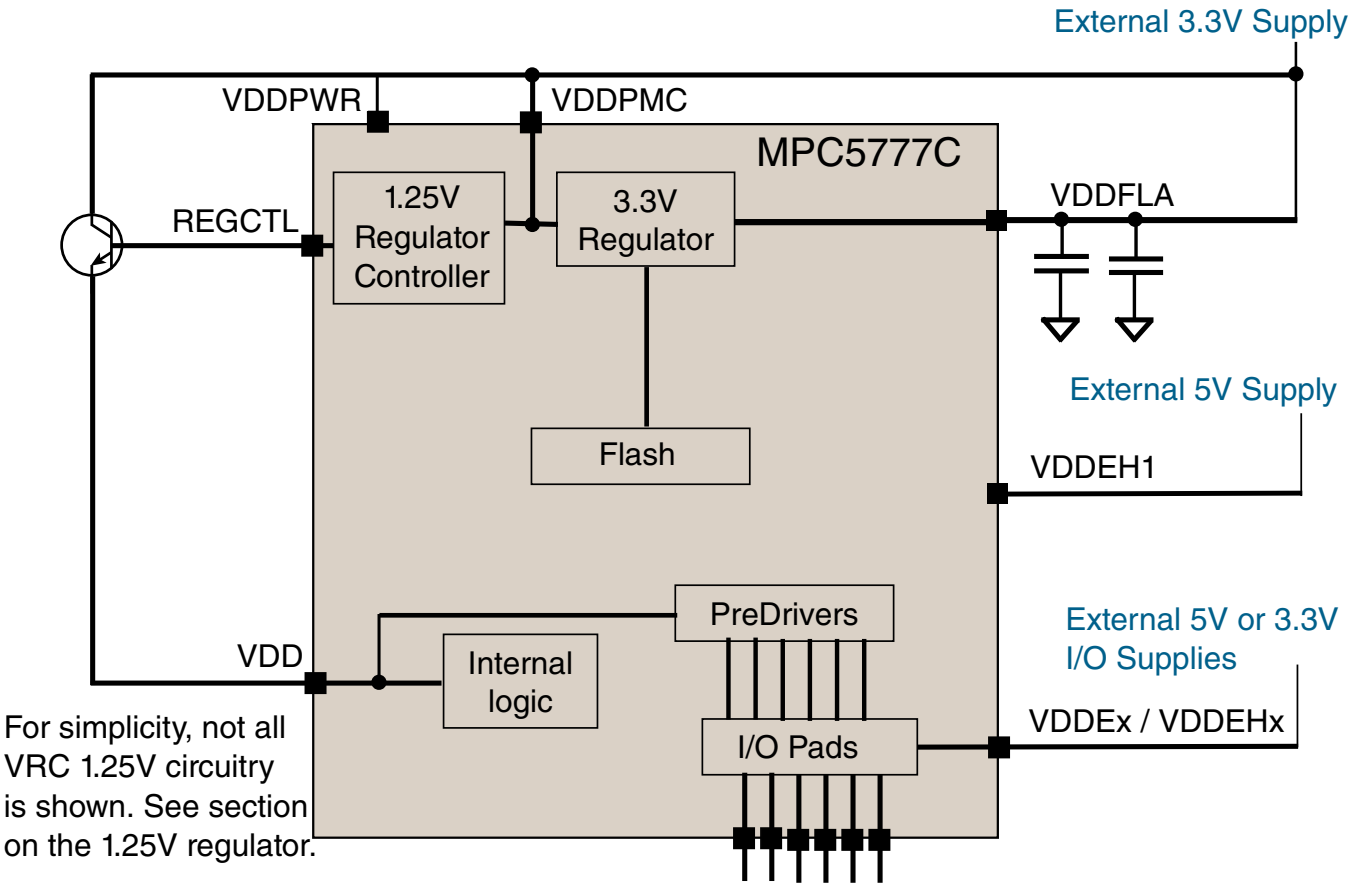

Figure 7. Internal 1.2V regulator with an external (only) 3.3V supply

NOTE

Though this configuration is allowable, it is highly recommended that the internal 3.3 V regulator still be used to supply the flash memory. This regulator ensures proper operating voltage for the flash memory at all times. When using the above configuration to bypass the internal 3.3V flash regulator, the external supply must adhere strictly to the datasheet operating range for the flash memory supply. Refer to the device datasheet "Voltage Monitoring" section for details on the flash low/high voltage detection limits.

3.7 Using external supplies

The MPC5777C can be powered entirely by external supplies. The 3.3 V internal flash regulator is disabled by connecting V_{DDPMC},V_{DDPWR}, and V_{DDFLA} to the same 3.3 V external supply. If an external 1.2 V supply will also be used, REGCTL should be left open.

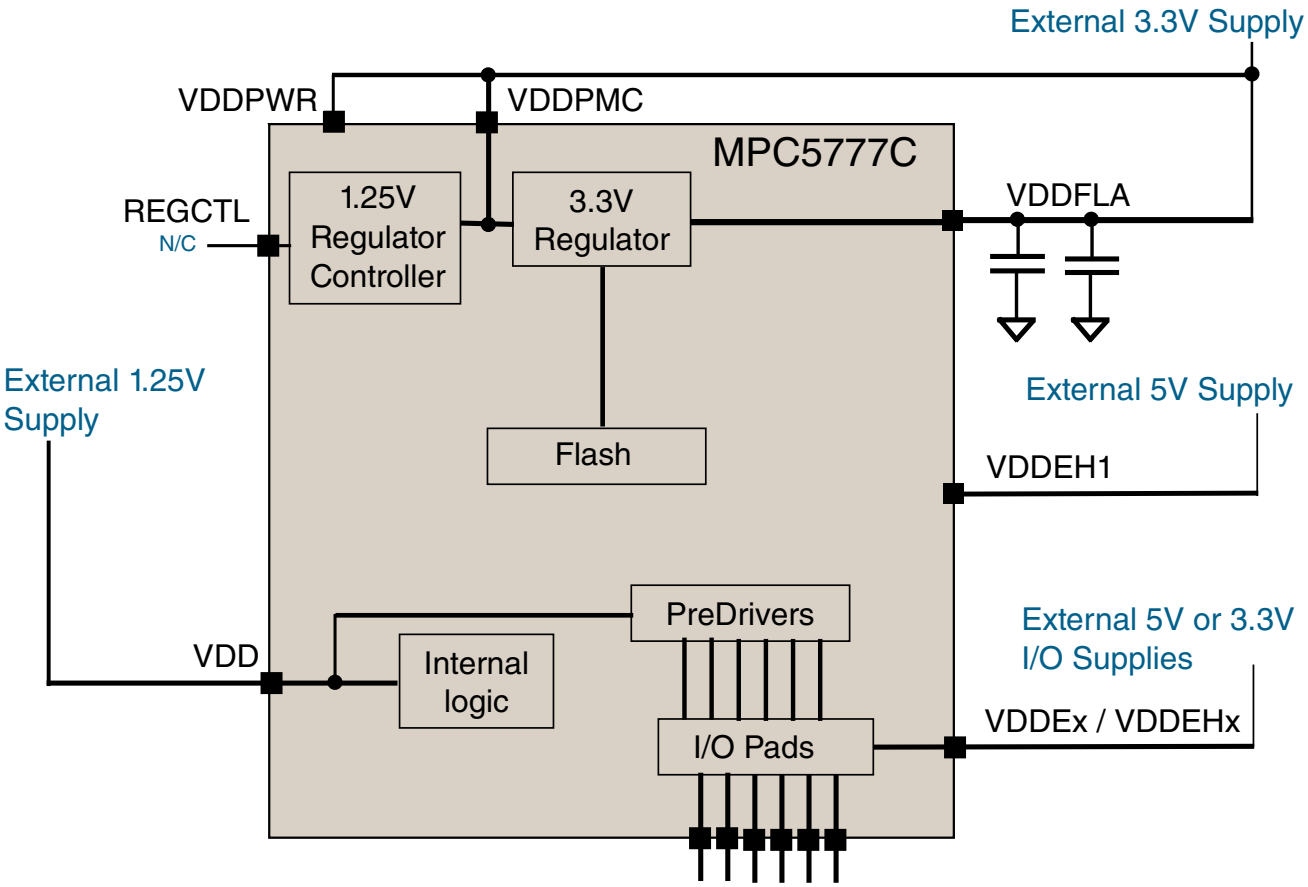

Figure 8. External power supply configuration

3.8 eQADC and SDADC (analog) power supply connections

To obtain the best analog performance, it is essential to use correct bypassing and configuration of the eQADC power supply and reference pins. The overall analog performance can be directly linked to noise on either the analog power supplies and/or the reference voltages (VRH and VRL). The figure below shows the recommended supply and reference circuitry for the eQADC.

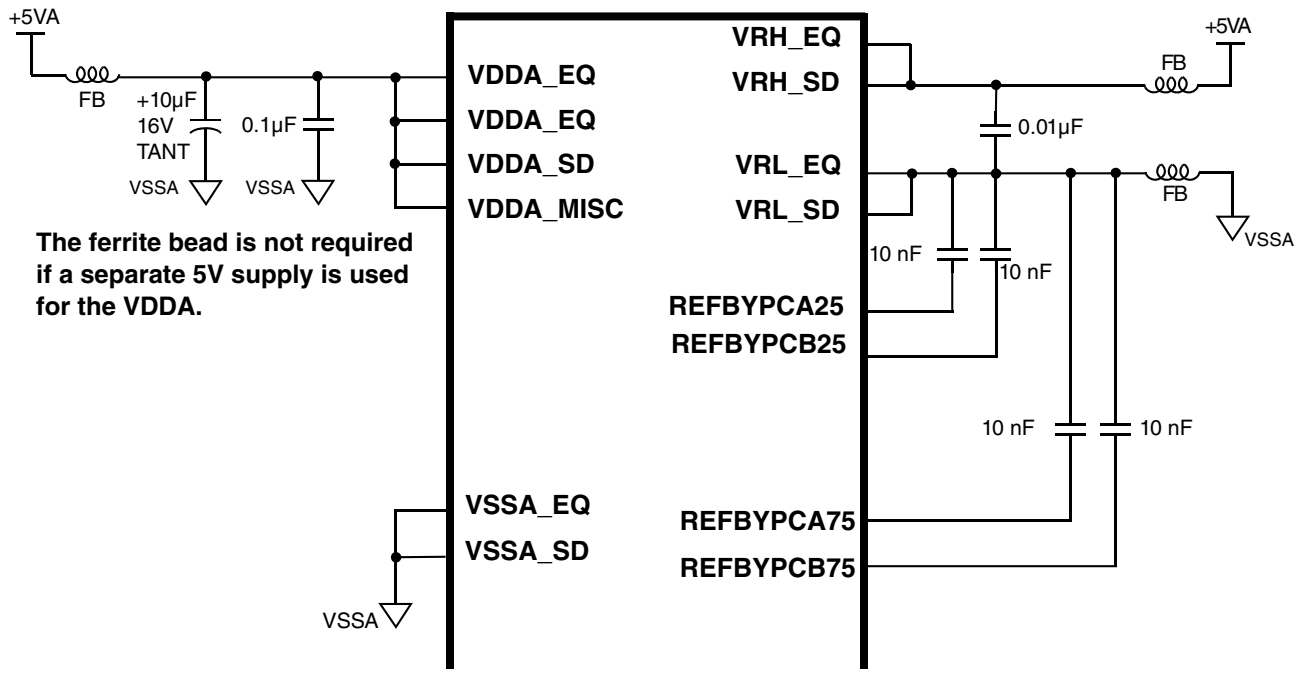

Figure 9. eQADC supply and reference circuitry

The reference bypass capacitor pins (REFBYPCn) require a capacitor to reduce noise on the internal 25% and 75% references used by the EQADC. These capacitors may be as high as 100 nF, however, this requires additional settling time on start up of the ADC module but may provide a more stable internal reference in some systems.

VSSA should always be connected directly to the ground plane of the board.

For slightly lower analog performance in low-cost systems, the ferrite bead isolation can be removed from the 5V analog VDDA supply. In addition, the ferrite bead on VRL can and should be removed if the system has a good (solid) ground plane. The ferrite bead on VRH is always recommended.

For the best analog performance, good layout techniques should be used for all signals connected to the analog inputs. It is important that the return path of each analog signal not be interrupted with discontinuities in the return path (either ground or power). Crossing "slots" in the return path will affect the signal integrity.

3.9 SRAM standby supply

The MPC5777C includes a power supply option for maintaining the contents of a portion of the internal SRAM when power to the rest of the device is off. If the SRAM standby feature is not required in the system, the best option is to connect the SRAM standby pin (VSTBY) to ground. This completely disables the standby SRAM function. It is also possible to connect VSTBY to either an external 3.3 V supply or to the 5 V supply that powers the rest of the device, however this provides no additional benefit over just grounding the VSTBY input if standby operation is not required. The table below lists the VSTBY options available on this device.

Table 15. VSTBY Options

	VSTBY connection	VSTBY voltage
Standby SRAM operation required	Nominal 1.0 V, 3.3 V, or 5 V supply that remains powered when all other supplies are off.	0.95 V to 5.5 V

Table continues on the next page...

Table 15. VSTBY Options (continued)

	VSTBY connection	VSTBY voltage
Standby SRAM operation is not required	Ground reference.	0 V
	An external nominal 3.3 V or 5 V supply that is turned on and off with the device.	3.0 V to 5.5 V

The table below shows the electrical specifications for VSTBY; however, the latest version of the device data sheet should be consulted.

Table 16. Standby power supply specifications

Characteristic	Minimum	Maximum	Units
No SRAM standby operation	0	0.2	Volts
Illegal VSTBY voltage range	0.2	0.95	Volts
SRAM standby voltage	0.95	5.5	Volts

If the proper voltage is on VSTBY, then VSTBY will provide power to the SRAM anytime the device is in power-on reset (POR). POR is an internal signal that is asserted if any of the monitored supplies are lower than their specified values.

4 Hardware system requirements for oscillator

The most important aspects of an accurate clock source require that some care be taken in the layout and design of the circuitry around the crystal and FMPLL power supplies. Any noise in these circuits can affect the accuracy of the clock source to the FMPLL. The figure below shows the typical connections required for the PLL power supply and the crystal connections. The power supply for the FMPLL is VDD, which is also the core and internal logic supply.

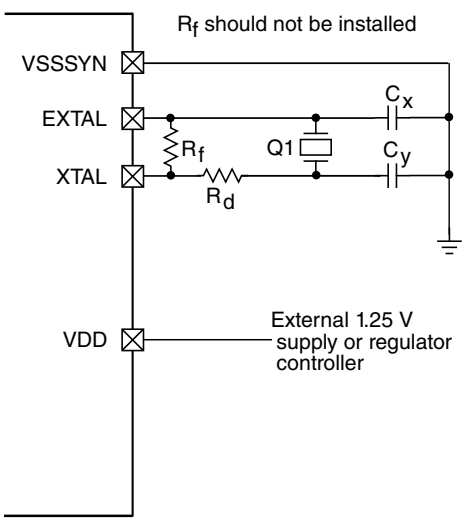

Figure 10. Oscillator and VDDPLL supply connections

In the figure above, R_f should not be installed with any current devices or crystals, as there is an internal feedback resistor. Room should be left in the layout in case a resistor is needed in the future for new types of crystals. Since the layout of the module/board can affect the component values required, customers should have their board characterized by their crystal

vendor to recommend values for R_d, C_x, and C_y. The values shown in this document should be used as a starting point. These should be re-characterized for any change to the oscillator circuit layout, including routing changes of other circuitry near the crystal circuit.

NOTE

The oscillator circuit should be placed as close as possible to the MCU. In order to minimize signal degradation, the circuitry should be placed entirely on only one PCB layer, avoiding unnecessary vias where possible. The schematic also illustrates the recommended layout; the VSSSYN trace should be used as a shield around the crystal components and then connected to the ground plane.

NOTE

Do not allow any signals to cross the crystal connections to the device. **Absolutely no high current or high speed signals should be run near any of the crystal components.**

NOTE

Other than the connections shown in the above schematics, no other connections should be made to the crystal or EXTAL and XTAL device pins. Do not use XTAL to drive any other circuitry than shown.

The recommendations from the crystal manufacturer will include not only a series resistor value but also the load capacitance required for the crystal (the total crystal load capacitance is usually specified in the crystal data sheet). Keep in mind that the load capacitance is the sum of

- Physical capacitors (C_x and C_y)
- Capacitance of the MCU
- Capacitive loading of the board (C_{PCB})
- Pin capacitance (C_{MCU_PIN}) of the MCU EXTAL and XTAL balls (BGA balls are specified as 7 pF maximum)

The requirement for the crystal vendor to measure the customer board is due to the board capacitance effect on the crystal load capacitors.

Generally, the method to calculate the capacitors values to use for C_x and C_y is given by the following:

$$C_A = C_B = 2 \times C_L$$
$$C_A = C_X + C_{MCU\_PIN} + C_{PCB}$$
$$C_B = C_Y + C_{MCU\_PIN} + C_{PCB}$$

C_L should come from the crystal specifications (requirements). C_{PCB} should also include any socket capacitance if a socket is used. This is listed in the device data sheet as the discrete load capacitance to connect to EXTAL and XTAL:

$$C_{L\_EXTAL} = (2 \times C_L) - C_{SOCKET\_EXTAL} - C_{PCB\_EXTAL}$$
$$C_{L\_XTAL} = (2 \times C_L) - C_{SOCKET\_XTAL} - C_{PCB\_XTAL}$$

In some cases, the crystal vendor may recommend different values for C_X and C_Y (not equal).

4.1 Oscillator and predivider circuitry

MPC577xC can use either the on-chip oscillator with an external crystal, the internal RC oscillator, or an external reference clock as the reference clock to the device. This reference is qualified in multiple manners before the PLL will begin lock operation. The “pre” FMPLL circuitry consists of an automatic level-controlled amplifier and comparator as shown in the figure below.

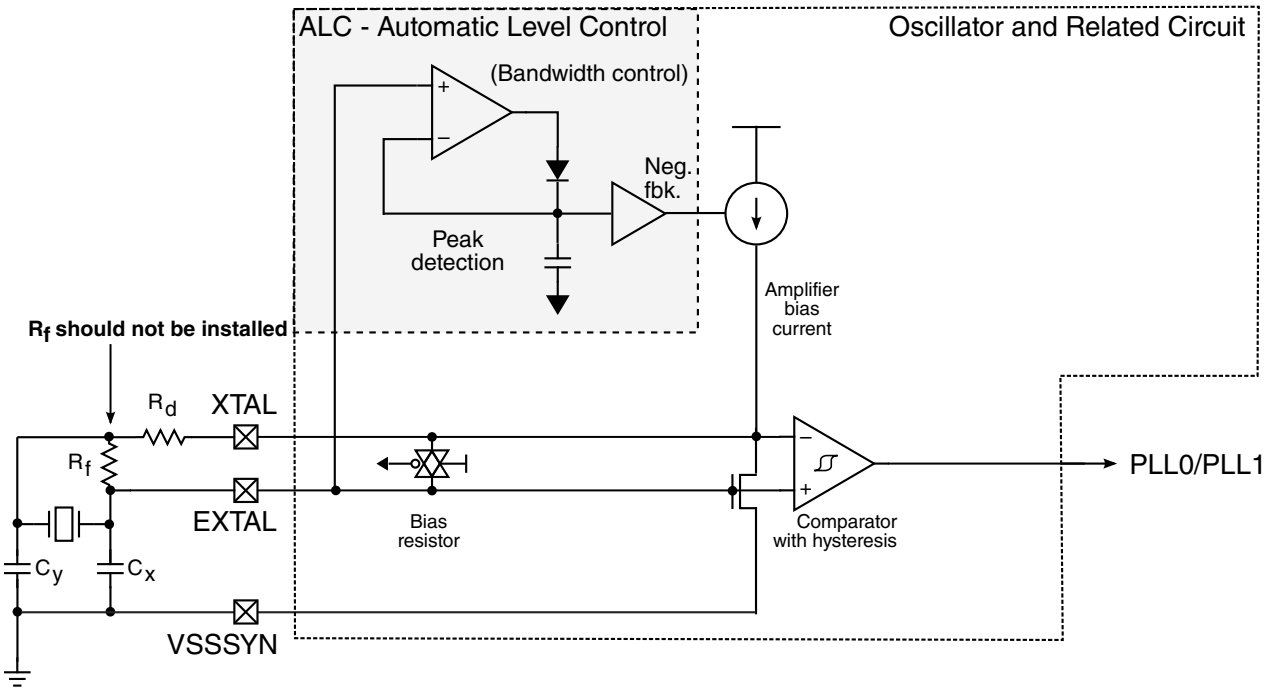

Figure 11. Pre-FMPLL circuitry (oscillator, comparator, and loss-of-clock circuits)

5 Device reset configuration

The basic configuration of the FMPLL, boot location, and timer pull values are set during reset. These settings may be controlled either by Device Configuration Record (DCF) or by the states of the control pins. The Miscellaneous DCF Legacy bit (LEG) controls the selection of DCF or reset configuration pins. If the pin values are used, these values are latched four clocks prior to the negation of the $\overline{\text{RSTOUT}}$ input of the device. The following table shows all of the reset configuration pins which are in effect when the Miscellaneous DCF Legacy bit is set to 1. When Legacy mode is not selected, the configuration values are read from the Miscellaneous DCF record.

NOTE

MPC5777C powers up operating with an internal RC oscillator and therefore does not require the PLLCFG[0:1] pins. Software should set the proper values of the FMPLL configuration registers to the desired frequency prior to switching the MCU to the Phase Lock Loop (PLL) output[3].

Table 17. Device reset configuration pins and modes

Configuration	Configuration pins	Description
Boot configuration	BOOTCFG[0:1][1]	The BOOTCFG[0:1] pins control the boot configuration of the device - booting from internal memory, external memory, or serial boot.
FMPLL configuration	PLLCFG[0:1]	The state of these pins at reset has no effect on MPC5777C. They are provided for pin compatibility with previous generation devices.

Table continues on the next page...

3. Use of the Progressive Clock Switch (PCS) feature may be desirable to limit sudden changes in operating current.

Table 17. Device reset configuration pins and modes (continued)

Configuration	Configuration pins	Description
FMPLL reference configuration	PLLCFG[2]	PLLCFG[2] = 1 selects the "high" reference for the crystal oscillator (XOSC). This is typically used with crystal frequencies greater than 20 MHz up to 40 MHz.
Timer pin default pull configuration	WKPCFG	WKPCFG selects the pull direction (either up or down) for the timer pins of the device. The timer pins are defined as the device pins that have a primary intended use of eTPU and eMIOS functions.

1. BOOTCFG[0] is not available in all packages. For packages without this pin, BOOTCFG[0] has a value of 0.

Since multiple external devices could assert the MCU $\overline{\text{RESET}}$ signal (power supply reset out, debugger, external independent watchdog), all devices connected to $\overline{\text{RESET}}$ should be configured for open drain (or open collector depending on the technology) with a strong pull-up (less than 4.7 K Ω) resistor installed in the system on the $\overline{\text{RESET}}$ signal.

5.1 Boot configuration

The BOOTCFG pins or Miscellaneous DCF record select the boot operating mode of the device. The following table shows the boot options.

Table 18. BOOTCFG configuration

BOOTCFG[0]	BOOTCFG[1]	Description
0	0	Boot from internal flash memory (default)[1]
	1	Boot from FlexCAN or eSCI interface
1[2]	0	Boot from external memory (no bus arbitration)
	1	Reserved (not valid for this device)

1. If no valid boot configuration exists in the internal flash, the device will then go into serial boot mode.
2. BOOTCFG[0] is not available in all package options and defaults to zero. In other words, external boot is not supported in packages that do not have a BOOTCFG[0] pin (416 PBGA).

In the internal flash memory boot process, the Boot Assist Module looks for a valid Reset Configuration Half-Word (RCHW) in the internal flash at the various possible boot locations. If a valid RCHW is not found, then serial boot mode is entered.

Serial boot mode allows the device to boot over either the eSCI (a simple, standard RS-232D type interface) or via the FlexCAN module. Both interfaces are monitored until activity is seen on one interface. Once an initial activity is seen on an interface, that interface becomes the boot interface. The boot protocol allows software to be downloaded into the device via the serial interface. Control will be passed to that software once loaded into memory. See the documentation for the device for additional information on the serial boot process.

5.2 PLL configuration

MPC5777C begins operation using the internal RC oscillator and does not require any boot-time configuration of the FMPLL. Previous generation devices allowed selection of PLL mode and external reference via the PLLCFG[0:1] pins. These pins are provided on the MPC5777C only for pin compatibility with previous designs. The state of these pins at reset has no effect on the FMPLL configuration. The application may configure the FMPLL registers in its initialization code while running on the internal RC oscillator.

PLLCFG[2] may be used to set the range of the crystal oscillator (XOSC) input frequency. When Miscellaneous DCF Legacy mode LEG = 1 and PLLCFG[2] = 1, then the "high" reference setting is selected. This setting is typically used with crystal frequencies greater than 20 MHz up to 40 MHz.

Table 19. XOSC Input Frequency Range Select

PLLCFG[2]	Clock input frequency	Default XOSC mode
0	> 8 to 20 MHz	Medium
1	> 20 to 40 MHz	High

The XOSC mode is dependent on both XOSC_LF_EN and XOSC_EN_HIGH bits in the Miscellaneous DCF record. When the Legacy mode (LEG=1) is selected, then the value of XOSC_EN_HIGH is taken from the PLLCFG[2] pin rather than the Miscellaneous DCF record value. XOSC "low" mode (typically used with crystals equal to 8MHz frequency) may only be selected by setting XOSC_LF_EN in the DCF record. There is no corresponding reset configuration pin for that field. XOSC_LF_EN and XOSC_EN_HIGH should not both be set to 1 at the same time.

5.3 Weak pull configuration

The default configuration of the pull devices connected to the timer pins of the device can be controlled with the state of the Weak Pull Configuration pin (WKPCFG) during reset if Miscellaneous DCF Legacy bit (LEG) is set to 1, otherwise the BOOTCFG value is read from the Miscellaneous DCF record. In legacy mode, the value of this signal is latched by the device four clocks prior to the negation of $\overline{\text{RSTOUT}}$ (low to high transition). The pull device can either be a pull-up or a pull-down. This default value remains in effect until disabled in the Pad Configuration Register (PCR) for the signal.

Table 20. WKPCFG Configuration

WKPCFG state	Description
0	The timer pins, by default, will have pull-down devices enabled.
1	The timer pins, by default, will have pull-up devices enabled.

The timer pins consist of all the pins for which the primary intended use is either eTPU functions or the eMIOS module. The System I/O Definition spreadsheet attached to the device reference manual lists the pins that are controlled by the WKPCFG pin.

5.4 Minimum reset configuration example

NOTE

The configuration pin examples in this section and the next are provided for backward compatibility with previous generation devices such as MPC5674F and MPC5676R. New designs which do not require compatibility with those devices should use the

Miscellaneous DCF record to configure these settings as this external circuitry is no longer required. Where necessary, differences between those devices and MPC5777C will be mentioned below.

By default, the PLLCFG and WKPCFG external signals have internal weak pull-up devices enabled during and after reset. The BOOTCFG external signals have internal weak pull-down devices enabled. The figure below shows the absolute minimum configuration required on previous generation devices to configure the FMPLL to use an external 8 to 20 MHz crystal and to boot from the internal flash. An option to allow selection between internal flash boot and serial boot can be added with a jumper on the BOOTCFG[1] external signal. If the system requires that the timer channels (eTPU and eMIOS) be configured with the internal weak pull-down devices by default, the resistor on WKPCFG should be installed.

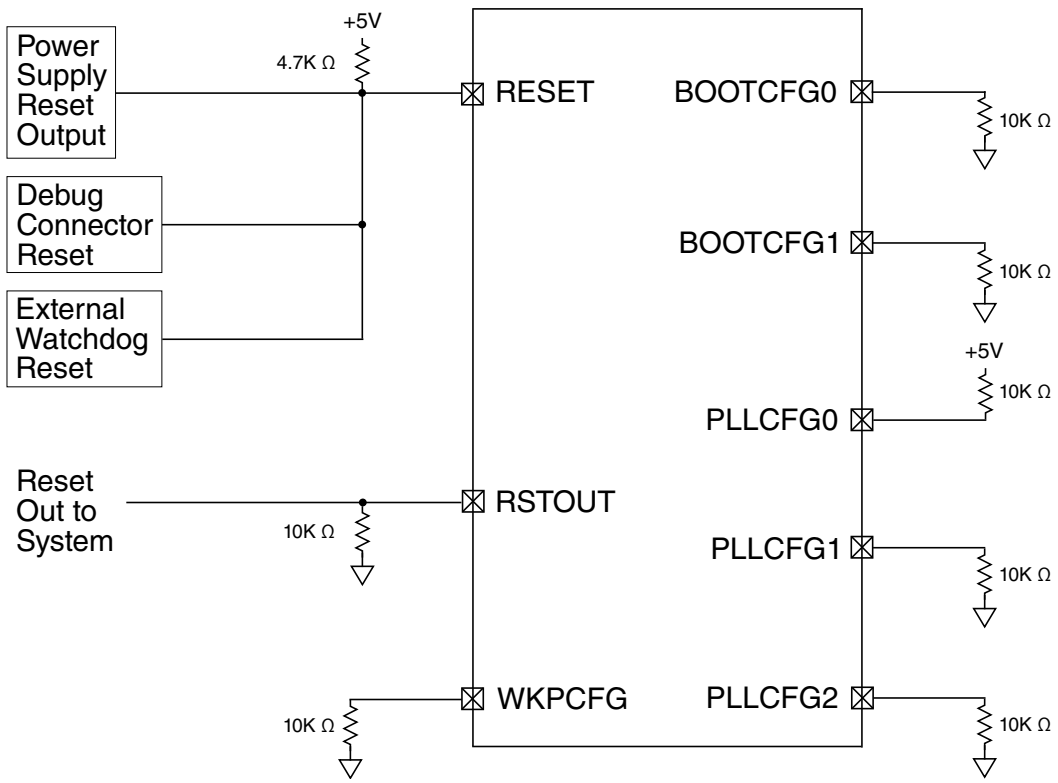

Figure 12. Minimum reset configuration for an 8 to 20 MHz crystal example

The absolute minimum configuration required to configure the FMPLL to use an external crystal with frequency greater than 20 MHz up to 40 Mhz and to boot from the internal flash is shown in the figure below.

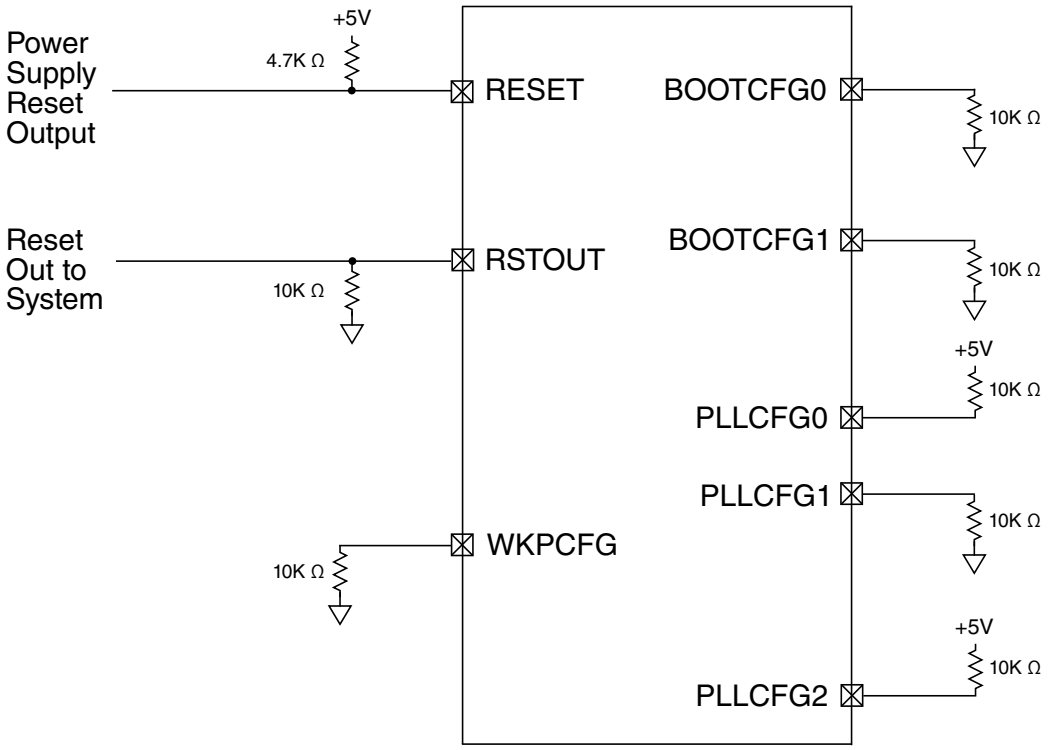

Figure 13. Minimum reset configuration for a greater-than 20 MHz up to 40 MHz crystal example

In both of the above examples, on MPC5777C, the PLLCFG[0:1] pins no longer have any effect on the FMPLL mode and external reference selection. These values must instead be programmed by the application using the internal FMPLL configuration registers. Also, for the 8 to 20 MHz example, programming of the Miscellaneous DCF record XOSC_LF_EN field may be necessary to select between the "low" and "medium" XOSC modes. Low mode is used typically for crystals of 8 MHz frequency, while medium mode is used for crystals greater than 8 MHz up to 20 MHz. Note that these are typical guidelines for gain mode selection by frequency and may vary due to crystal load capacitance, board layout, and other factors.

5.5 Fully selectable reset configuration example

In some cases (such as an initial prototype/evaluation board/module), a fully selectable option is helpful to set any configuration of the PLL options (PLLCFG[0:1]) , boot options (BOOTCFG[0:1]), and timer pins pull default state (WKPCFG). The figure below shows a circuit example.

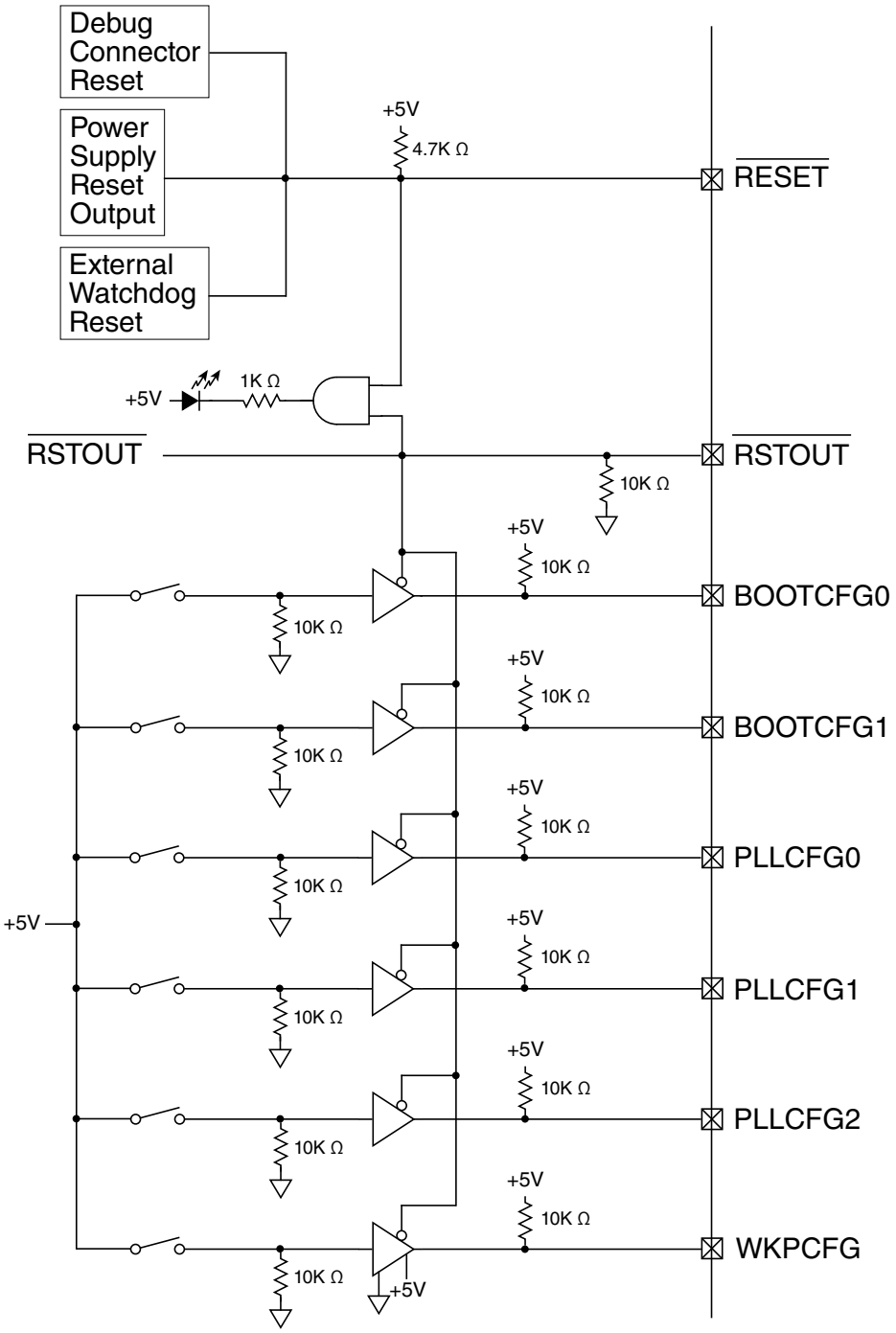

Figure 14. Schematic of fully configurable reset configuration example

5.6 Using the configuration pins for I/O

In some systems, it is a requirement to use the configuration pins for either input or output functions after the MCU exits reset. During reset the configuration pins need to be in the proper state for configuring the device. Therefore a tristate buffer can be used that is enabled while $\overline{\text{RSTOUT}}$ is asserted (low). After reset, another set of buffers that are enabled when

$\overline{\text{RSTOUT}}$ is negated (high) can be used to drive the pin or an external signal. When used as an output, the state of the signal during reset should be set by an external resistor. This resistor should be strong enough to overcome any internal resistor on the device that this tristate buffer is driving.

The figure below shows an example circuit that can be used to isolate the configuration pins during and after reset.

NOTE

The tristate buffers used during reset assertion are active low and the buffers used after reset are active high.

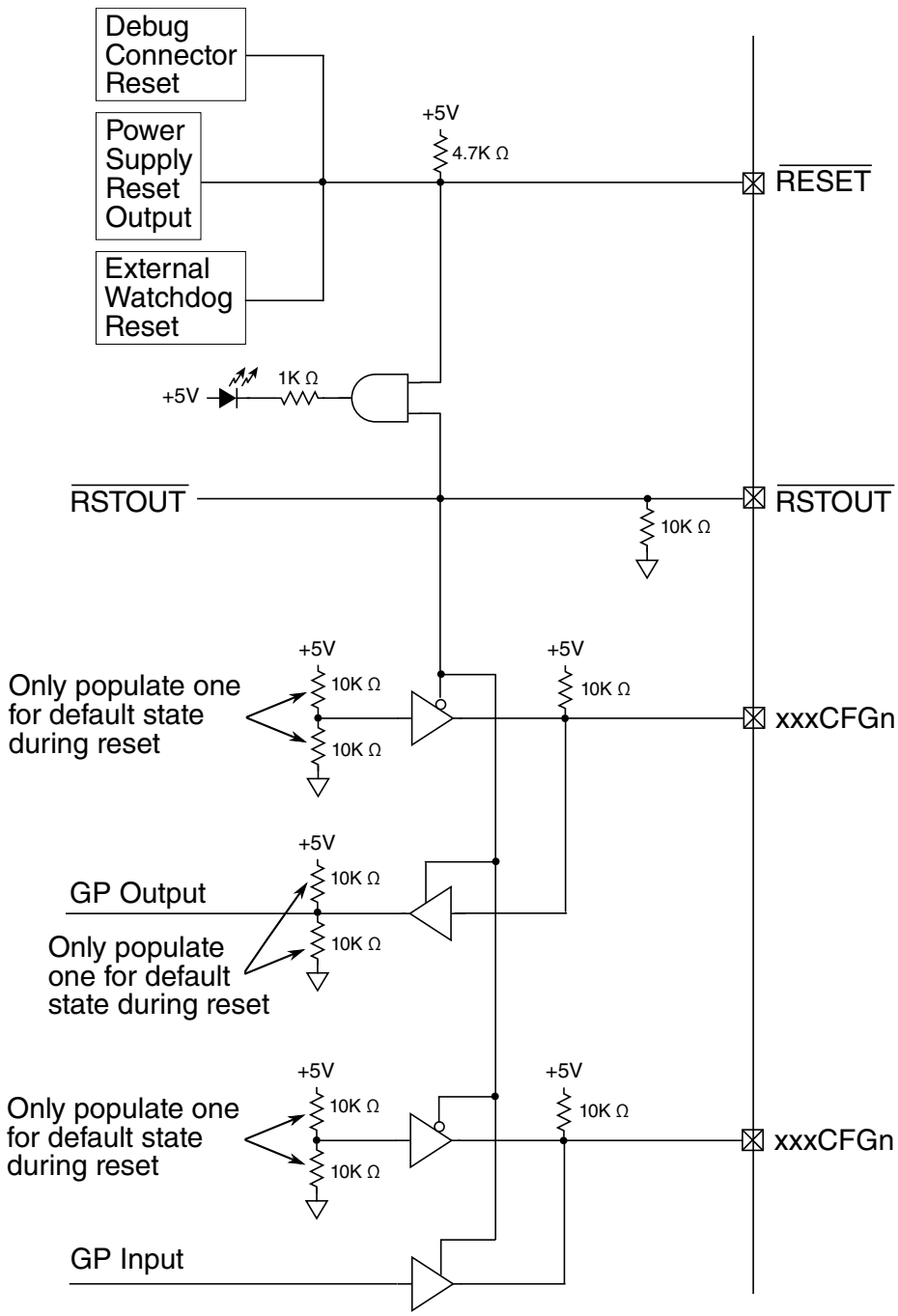

Figure 15. Typical I/O circuitry for configuration signals

6 Recommended debug connectors and connector pin out definitions

The debug interface of this device uses a single IEEE-ISTO 5001™ Nexus Combined JTAG IEEE1149.1/Auxiliary Out interface. It combines an IEEE 1149.1 JTAG interface with a high-speed parallel 16-bit wide Message Data Output port. The Nexus interface allows access to trace data from multiple internal Nexus clients.

The table below shows the recommended connectors for different debug configurations for the MPC5777C.

Table 21. Recommended connectors

Connector style	Target system part number	Debug configuration
14-pin BERG JTAG only	3M 2514-6002UB	JTAG-only configuration
25-position (2 × 25, 50-pin) Samtec	Samtec ASP-148422-01	Full Nexus configuration

NOTE

For each connector, "keep-out" areas may be required by some tools. Consult the preferred tool vendor to determine any area that must remain clear around the debug connector. Some tool vendors may include an extension cable to minimize "keep-out" areas, but use of an extension will degrade the signal. In many cases, this degradation will be insignificant, but the amount of degradation depends on many factors, including clock frequency and target board layout.

6.1 MPC5777C JTAG connector

The table below shows the pin-out of the recommended JTAG connector to support MPC5777C. If there is enough room allowed in the target system, a full Nexus connector is preferred over the simple 14-pin JTAG connector since it allows a higher degree of debug capability. It can be used as a minimum debug access or for BSDL board testing.

Table 22. Recommended JTAG connector pinout

Description	Pin	Pin	Description
TDI	1	2	GND
TDO	3	4	GND
TCK	5	6	GND
$\overline{\text{EVTI}}$[1]	7	8	—
$\overline{\text{RESET}}$	9	10	TMS
VREF	11	12	GND
$\overline{\text{RDY}}$	13	14	JCOMP

1. $\overline{\text{EVTI}}$ is optional and was not included in the original (very early) definitions of the JTAG-only connector.

6.2 MPC57xx high-speed parallel trace connector

This device features a full 16-bit Message Data Out (MDO) port. For high speed trace applications using more than eight MDO signals, a Samtec ERF8 series connector is highly recommended due to better signal integrity than other available connectors such as the MICTOR-38. The part number of the Samtec connector is shown in the following table.

Table 23. Recommended high-speed parallel trace connector part number

Connector	Part number (Samtec)	Style	Description
HP50	ASP-148422-01	Samtec ERF8 Series, 25 position by 2 row	Vertical mount for MCU module

The Samtec ERF8 series of connectors is intended for high speed applications requiring a minimum footprint size with a reliable, latching connection. The recommended connector has two rows of twenty-five contacts each with a spacing of 0.8 mm. The connector provides isolation between the high-speed trace signals and the low-speed JTAG and control signals. It also provides ample ground connections to ensure signal integrity.

The following picture is courtesy of Samtec U.S.A (http://www.samtec.com/search/NEXUS.aspx).

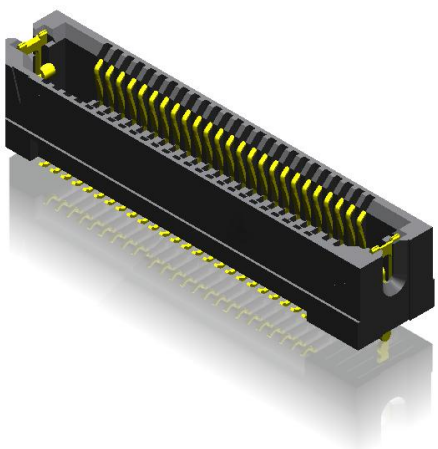

Figure 16. HP50 (ASP-148422-01) connector

The table below shows the recommended pinout for the Samtec connector.

Table 24. MPC57xx high-speed parallel trace connector

Position	Signal	Direction	Pin number	Pin number	Direction[1]	Signal	IEEE-5001-2011 GEN_IO signal name
	GND					GND[2]	
1	$\overline{\text{MSEO0}}$	Out	1	2	Out[3]	VREF	
2	$\overline{\text{MSEO1}}$	Out	3	4	In	TCK	
3	GND		5	6	In	TMS	
4	MDO0	Out	7	8	In	TDI	
5	MDO1	Out	9	10	Out	TDO	
6	GND		11	12	In	JCOMP	

Table continues on the next page...

Table 24. MPC57xx high-speed parallel trace connector (continued)

Position	Signal	Direction	Pin number	Pin number	Direction[1]	Signal	IEEE-5001-2011 GEN_IO signal name
7	MDO2	Out	13	14	Out	$\overline{\text{RDY}}$	
8	MDO3	Out	15	16	In	$\overline{\text{EVTI}}$	
9	GND		17	18	Out	$\overline{\text{EVTO}}$	
10	MCKO	Out	19	20	In	$\overline{\text{RESET}}$	
11	MDO4	Out	21	22	Out	$\overline{\text{RSTOUT}}$	GEN_IO0
12	GND		23	24		GND	
13	MDO5	Out	25	26	Out	CLKOUT	
14	MDO6	Out	27	28	In/Out	TD/WDT	GEN_IO1
15	GND		29	30		GND	
16	MDO7	Out	31	32	In/Out	DAI1	GEN_IO2
17	MDO8	Out	33	34	In/Out	DAI2	GEN_IO3
18	GND		35	36		GND	
19	MDO9	Out	37	38		ARBREQ	GEN_IO4
20	MDO10	Out	39	40		ARBGRT	GEN_IO5
21	GND		41	42		GND	
22	MDO11	Out	43	44	Out	MDO13	
23	MDO12	Out	45	46	Out	MDO14	
24	GND		47	48		GND	
25	MDO15	Out	49	50		N/C[4]	
	GND[2]					GND[2]	

1. Viewed from the MCU.
2. The connector locking mechanism provides additional ground connections on each end of the connector.
3. This is an output from the connector standpoint. It may or may not be from the MCU.
4. No connection — should be left open. Reserved for MDO16 on devices with more than sixteen MDO signals (future compatibility). In some applications this may be used as an SRAM voltage detect to determine when voltage for a standby SRAM is disconnected.

6.3 Minimum debug external circuitry

In general, other than the connector, no additional circuitry is required for the Nexus/JTAG debug circuitry. MPC5777C includes internal pull devices that ensure the pins remain in a safe state. However, if there is additional circuitry connected to the Nexus/JTAG pins, or the signals have long traces, a minimum number of external pull resistors can be added to ensure proper operation under all conditions. Long traces could be affected by other signals, due to crosstalk from high-current or high-speed signals. The recommended external resistors are shown in the following table.

Table 25. Optional minimum debug port external resistors

Nexus/JTAG signal	Resistor direction and value	Description
JCOMP	10 kΩ pulldown	Holds debug port in reset and prevents any debug commands from interfering with the normal operation of the MCU.

Table continues on the next page...

Table 25. Optional minimum debug port external resistors (continued)

Nexus/JTAG signal	Resistor direction and value	Description
$\overline{\text{RESET}}$	4.7 kΩ pullup	The $\overline{\text{RESET}}$ input should be driven from an open collector output; therefore, it requires a pull-up resistor for the MCU.
TD/WDT[1]	10 kΩ pulldown	With no tool attached, this signal should be held low and may or may not be connected to a pin of the MCU, depending on the system definition.
$\overline{\text{EVTI}}$	10 kΩ pullup	A pull-up resistor prevents debug mode from being forced after reset if debug mode is enabled (JCOMP = high). It also prevents breakpoints from being forced if debug mode is enabled. **NOTE:** In almost all situations, a resistor is not required on this signal.
TCK	series isolation resistor	A termination resistor or an isolation (0Ω) resistor may be required in systems that use a debug connector on the VertiCal connector since the TCK signal may have multiple endpoints that can cause reflections.

1. This is an optional signal and is not actually required for the MCU.

In addition to the pull-up and pull-down resistors, some systems may want to use buffers between the Nexus/JTAG connector inputs and the MCU. This will prevent over-voltage conditions from causing damage to the MCU pins. Normal systems should not require this circuitry, but it is helpful in systems that can be exposed to improper connections that provide voltages that are outside the operating conditions of the MCU. A common device to use is the Texas Instruments SN74CBTLV3861[4]. This device is a bus switch that implements a bidirectional interface between two terminals with less than 5 Ω of resistance. It should be powered by the same supply that powers the debug port. The device enable should be connected to ground for the interface to be enabled whenever the debug port on the MCU is powered. This circuit provides a high impedance to the tool when the debug port is powered off.

NOTE

It is recommended that at least the reduced port configuration Nexus signals be made available (somewhere) on production boards. This facilitates debugging of new boards and analysis of errors in software, even on boards that have restricted space and normally provide a JTAG-only connection. If the Nexus signals are available on the production board, an adapter could be built to provide a Nexus connection on boards that do not have a complete footprint for one of the standard Nexus connectors. Likewise, the JTAG connector does not have to be populated on production boards and could even utilize a smaller connector footprint that could be used with an adapter to the standard debug connections.

In systems that use a VertiCal mounted debug connector and have a JTAG connector/footprint in the target system, termination may be required on the JTAG Test Clock (TCK) to avoid ringing due to the multiple signal endpoints.

7 Monitoring internal analog signals

4. SN74CBTLV3861-Q1 is automotive qualified if required.

Many of the PMC reference and output voltages can be monitored by the on-chip analog-to-digital converter (eQADC). These can be monitored by the application software. Some of these signals can be converted by only one of the on-chip ADCs. The available PMC signal channels are shown in the following table.

Table 26. Power supply ADC monitor channels

ADC Channel	ADC	Description
128	ADC0, ADC1 of eQADC_A	Temperature sensor 0
129	ADC0, ADC1 of eQADC_A	Temperature sensor 1
145[1]	ADC0 of eQADC_A	PMC band gap voltage (1200 mV)
145	ADC0 of eQADC_A	Core 1.25 V LVD cold sense
145	ADC0 of eQADC_A	Core 1.25 V LVD hot sense
145	ADC0 of eQADC_A	Core 1.25 V hot reference
145	ADC0 of eQADC_A	Flash 3.3 V LVD divider tap
145	ADC0 of eQADC_A	Flash 3.3 V LVD reference
145	ADC0 of eQADC_A	PMC 5 V LVD reference

1. Select the desired PMC voltage to measure on channel 145 using the channel select field ADC_CS of the ADC Channel Select Register (PMC_ADC_CS)

8 eQADC overview

MPC5777C includes two separate enhanced Queued Analog-to-Digital Converters (eQADC). Each eQADC module contains two actual analog-to-digital converters (ADC). The ADC supports both single-ended and differential analog inputs. In addition, on the differential channels the eQADC modules support programmable pull-up and pull-down resistors to allow for on-chip biasing of the external differential signals. These internal resistors can be independently controlled to allow diagnostics to be performed on the analog channels to check for shorts to ground, shorts to 12 V, and open circuits (no sensor) by switching the different resistors in and out and by performing single-ended conversions of both halves of the differential channel pair. In addition, the differential channels provide a programmable gain stage that allows a unity gain, gain of two, or gain of four. Any output value from the ADC can be routed to a separate decimation filter that provides either decimation only, a filtered result through a 16-bit fourth-order IIR (Infinite Impulse Response) filter, or an eighth-order FIR (Finite Impulse Response) filter.

The block diagram below of the eQADCs shows the four (total) ADCs. The majority of the analog inputs are connected to either eQADC_A or to eQADC_B. However, there are some channels that are shared between the two modules. This is also shown in the figure below. A more detailed input model is shown in MPC5777C ADC Input Model (Appendix B).

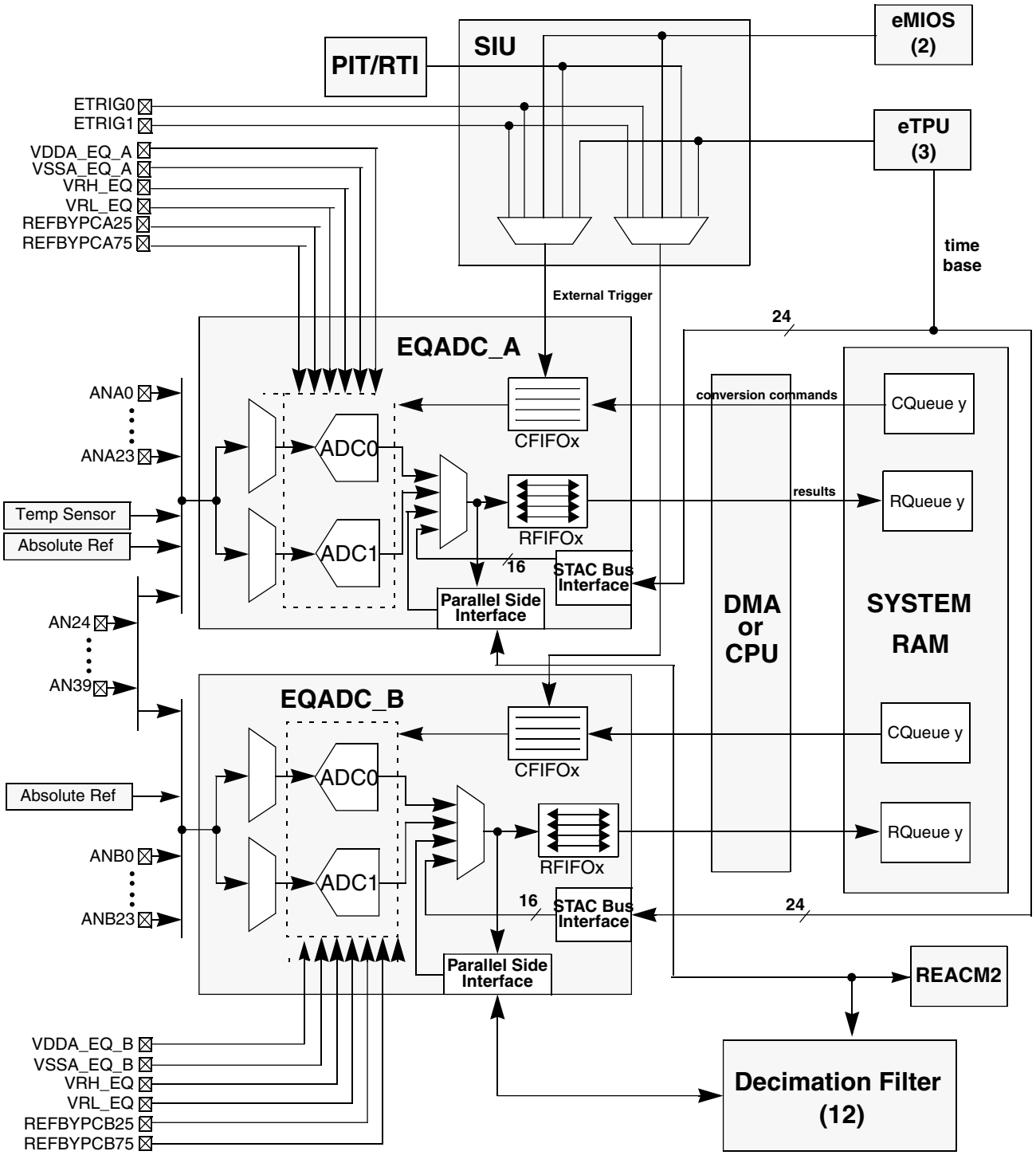

Figure 17. MPC5777C eQADC Sub-system

Internal to the device package, there are separate connections to the die for the analog power (VDDA_AN) and the digital power (VDDA_DIG) supplies to the eQADC module. These are connected inside the package for a single VDDA pin. Likewise, the analog (VSS_AN) and digital (VSS_DIG) grounds are isolated internal to the package.

Each eQADC can have up to four differential analog channels. There are sixteen channels that are shared between both eQADC modules. The following table shows the number of available external channels by eQADC instance and channel type.

Table 27. Number of external ADC channels

Module	Channel type	Total channels when using the maximum differential channels	Total channels when no differential channels are used
eQADC_A	Differential channels	4	8
	Dedicated single channels	16	16
eQADC_A and eQADC_B	Shared A and B single-ended channels	16	16
eQADC_B	Differential channels	4	8
	Dedicated single channels	16	16
Total ADC channels		56[1]	64[2]

1. Of these 56 channels, 8 are differential channels.
2. No differential channels.

The eQADC provides the capability of expanding the number of analog inputs by using external multiplexers. Up to eight external multiplexers can be used. The external multiplexers require three digital pins that are used as multiplexer address select signals. An external multiplexer can only be used with one of the eQADC modules, either eQADC_A or eQADC_B. This is selectable by software. The external multiplexers feed the analog signals into eight ADC channels. This allows up to fifty-six additional channels (sixty-four externally multiplexed analog signals minus the eight channels that are lost for the multiplexed inputs). The following diagram shows how to connect the maximum of eight external multiplexers to this device's internal eQADC modules.

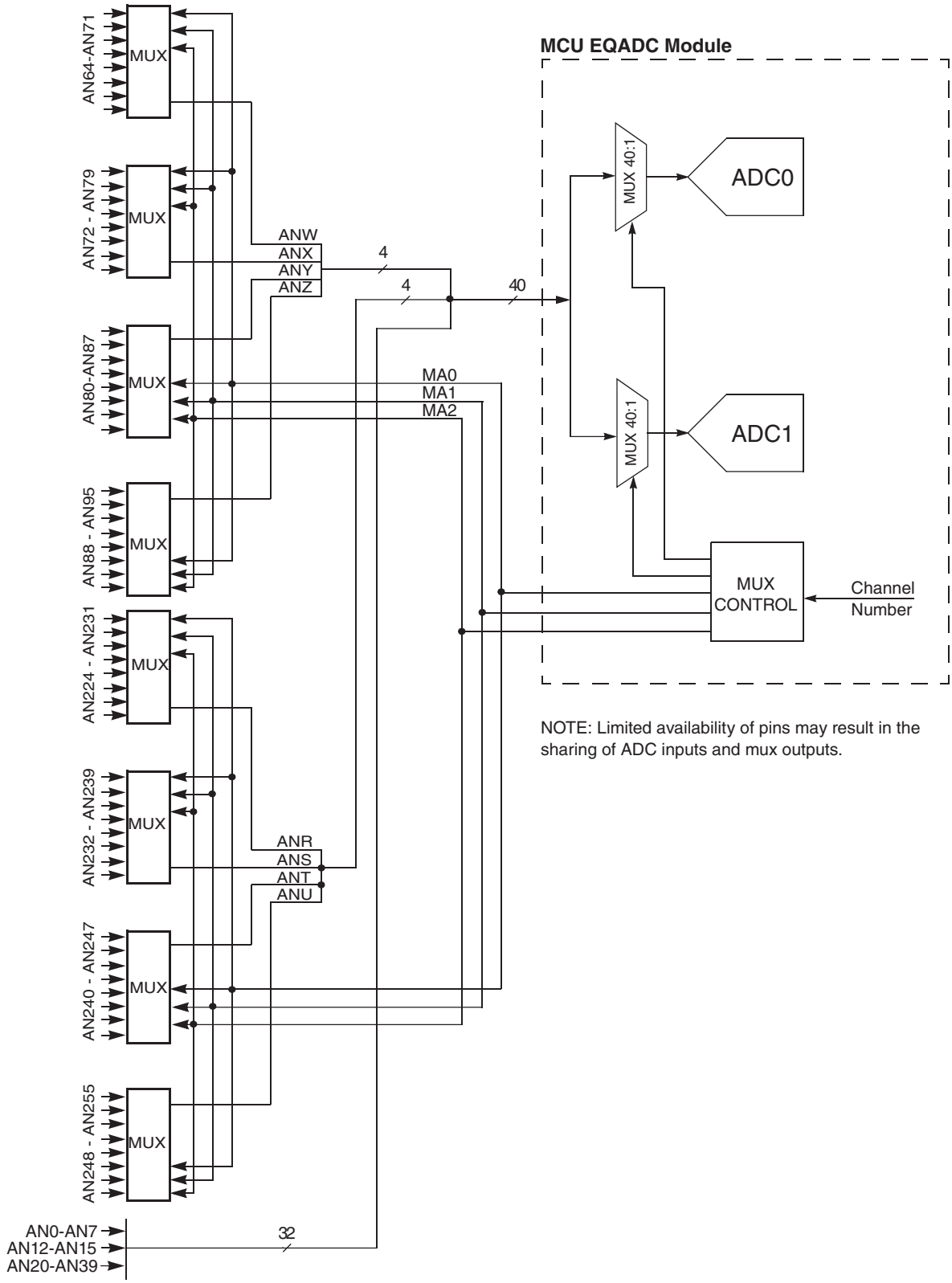

Figure 18. External multiplexer options

In addition, the following board schematic and layout guidelines should be followed:

- Isolate the analog power supplies (VDDA) from digital power supplies (see eQADC and SDADC (analog) power supply connections).

- Isolate analog traces from digital high-frequency traces
- Incorporate robust bypassing of power supplies (analog and digital supplies) to ensure lowest possible voltage ripple on the power supplies (see the bypassing guidelines eQADC and SDADC (analog) power supply connections)
- Use linear power supplies when possible, or minimize or isolate the switching noise when using a switching power supply
- Incorporate low-pass filter on ADC inputs to remove unwanted higher frequency components as shown in the following sections

The eQADC requires calibration before it can be used. See AN2989 "Design, Accuracy, and Calibration of Analog to Digital Converters on the MPC5500 Family" for information on calibrating the eQADC.

8.1 eQADC single-ended analog input example

The figure below shows a typical single-ended analog input circuit. The resistor and capacitor values will vary depending on the circuitry connected to the analog input. The values shown may not be appropriate for all types of signal input. There are several criteria required for selecting this circuitry that depend on the source impedance, the maximum voltage allowed (including under error conditions), the required accuracy (including resolution), and the actual specifications of the ADC of the MCU (input impedance, and injection current limits). Care should be taken (by sizing the series resistor) to keep the currents within the injection limits of the device (see the device data sheet). In addition, in some environments. additional protection may be needed. However, the resistors and capacitors shown provide some protection, along with the MCU on-chip ESD protection diodes, for over current and over voltage conditions. See Injection Current section.

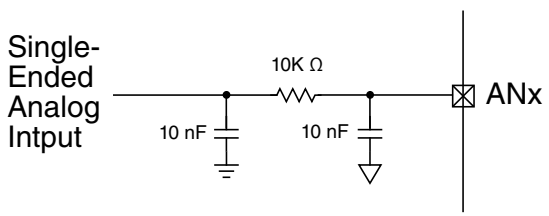

Figure 19. Typical single-ended analog input

The approximate filter cut off frequency is shown in the following equations. For the equations, the following definitions apply:

- R is the series resistor value (ohms)
- C is the capacitor value (farads)

$$\text{Filter\_Cut\_Off\_Frequency} = \frac{1}{2(\pi)(R)(C)}$$

$$\text{Filter\_Cut\_Off\_Frequency} = \frac{1}{2(\pi)(10K)(10\text{nF})} = \frac{1}{2(3.14)(0.0001)} = 1.592\text{KHertz}$$

In addition, if the incoming signal is being measured at a repetitive sample rate without other channels being converted, compensation may be required as the ADC sampling capacitor may begin to appear as a resistive component and therefore create a resistor divider. For the following equation, the follow definitions apply:

- C_s is the internal ADC sample capacitance, this is approximately 0.5 pF for the eQADC in this device (farads).
- F_s is the sample rate (repetitive rate, not the clock frequency of the ADC itself). In this example 200 thousand samples per second is used (Hertz).

$$\text{Filter\_Sample\_Rate\_Equivalent\_Resistance} = \frac{1}{(\text{Cs})(\text{Fs})} = \frac{1}{(0.5\text{pF})(200K\text{samples/sec})} = \frac{1}{1x10^{-7}} = 10M$$

Taking this equivalent resistance in to account results in a slight reduction in the voltage that is actually seen by the ADC as shown in the following equation:

- R is the external series filter resistor (ohms)

- R_s is the internal routing resistance (ohms)
- R_{equ} is the equivalent resistance due the switched capacitor effect of the internal sample capacitor (ohms).
- V_{in} is the input voltage into the filter network (volts).

$$\text{ADC\_Actual\_Equivalent\_Voltage} = \frac{\text{Requ}}{(R+\text{Rs}+\text{Requ})}(\text{Vin}) = \frac{10M}{(10K+8K+10M)}(\text{Vin}) = \frac{10M}{10.028\text{M}} = 99.7\,\%\,(\text{Vin})$$

8.2 eQADC differential analog input example

The figure below shows a typical differential analog input circuit.

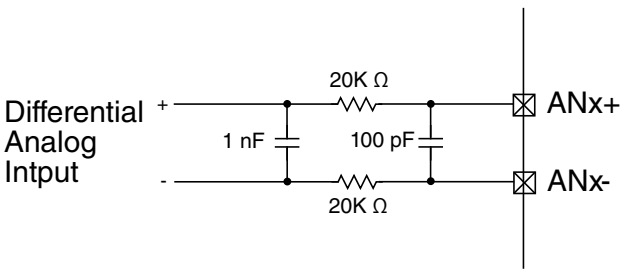

Figure 20. Typical differential analog input

The differential inputs are limited to a maximum differential amplitude of 2.5 V. The signal should be biased around the mid supply of the references = (VRH - VRL)/2. See the device data sheet for the allowable differential offset voltage from the mid-point, however, it is typically ± 5% of (VRH-VRL). This is shown in the following figure.

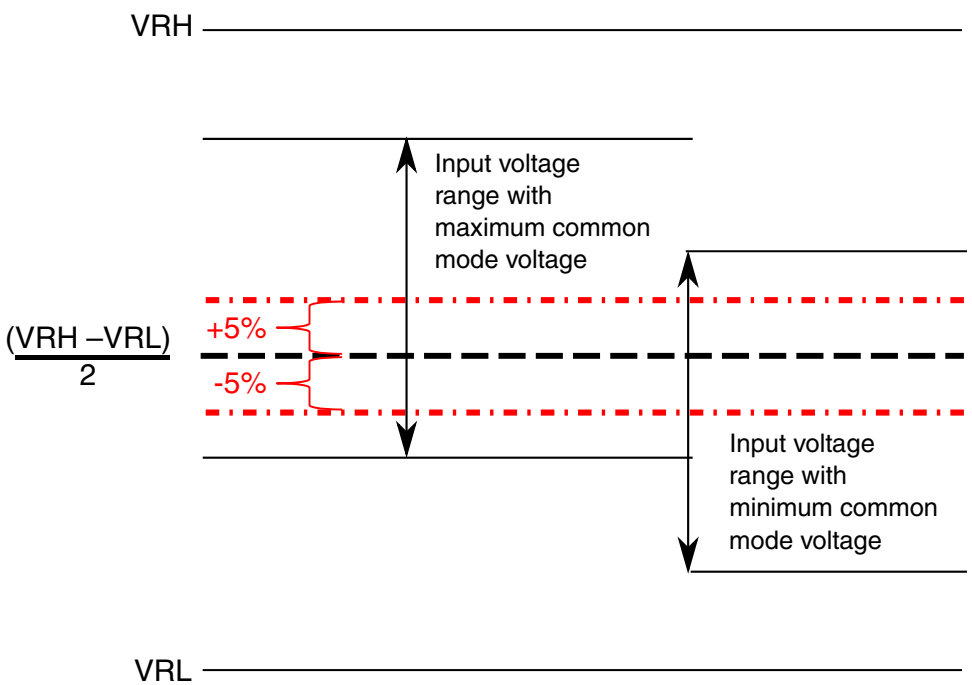

Figure 21. Differential voltage range (Gain = x1)

Another feature of the differential inputs of the eQADC is a variable gain amplifier[5]. This "amplifier" can be enabled in the ADC conversion command and can be set to a gain of two (x2) or a gain of four (x4) (normally the gain is set to one). It should be noted that when the x2 or x4 gain is enabled, the maximum input voltage level of the ADC is reduced. See the following table.

Table 28. Maximum differential input voltage for the different gain settings

Gain Setting	Maximum Differential Voltage[1]
x1	±2.5 V
x2	±1.25 V
x4	±0.625 V

1. Although the eQADC cannot accurately convert voltages greater than a differential voltage 2.5 V (x1 gain), 1.25 V (x2), or 0.625 V (x4), the inputs will not be damaged by voltages that are within the range of VRL to VRH.

An additional feature available on the differential inputs is bias resistors. Three values of pull-up and pull-down resistors are available on each of the differential pins. In addition to providing a DC bias voltage for AC signals, these resistors can be used to perform some diagnostic tests by enabling different combinations and determining the effect on the input voltages. The following figure shows the placement of these bias resistors in the ADC input model.

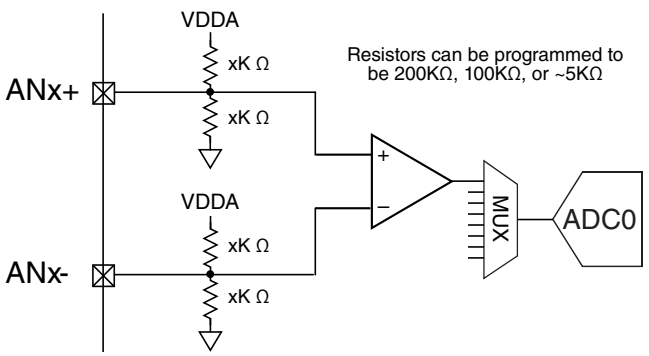

Figure 22. Differential ADC input pull up and pull down resistors

NOTE

Some documentation shows that the pull-up and pull-down resistors are connected to VDDE, this is due to the generic designation that VDDE stood for an external power supply. The pull-up resistors are connected to the external analog power supply (VDDA) on devices.

The following table shows the specifications of the bias resistors. In addition to the value specifications, there is an additional specification on the 100 KΩ and 200 KΩ resistors, matching. The ratio of the pull up and pull down resistors match within 2.5%. This specification does not apply to the ~5 KΩ resistor.

Table 29. ADC pull-up and pull-down resistor specifications

Description	Minimum	Maximum	Units
Weak pull-up/pull down resistance 200 KΩ selected	130	280	KΩ
Weak pull-up/pull down resistance 100 KΩ selected	65	140	KΩ
Weak pull-up/pull down resistance 5 KΩ selected	1.4	7.5	KΩ
Pull-up/down matching ratio (100K and 200K resistors only)		5%	—

5. This gain stage is actually not implemented as a traditional op-amp and therefore does not have the normal amplifier specifications. The gain is implemented by the controlling the references to the ADC. However, the performance of the "amplifier" stage is included in the integral nonlinearity (INL) and differential nonlinearity (DNL) specifications of the ADC.

9 Sigma Delta ADC

MPC5777C has 4 Sigma Delta Analog-to-Digital Converter (SDADC) modules. The SDADC consists of a cascaded sigma delta modulator coupled to a high pass filter and digital interface to the system bus. Both single ended and differential conversions are supported on a number of input channels. Conversions can be started by software or hardware triggers.

9.1 Differential and Single Ended Operation

Three of the SDADC modules on this device (SDADC_1, SDADC_2, and SDADC_3) have four inputs each while SDADC_4 has eight inputs. These inputs can be used separately for singe-ended conversion or in pairs for differential conversion. The differential pairs are grouped as follows:

- AN[0] (+) and AN[1] (-)
- AN[2] (+) and AN[3] (-)
- AN[4] (+) and AN[5] (-)
- AN[6] (+) and AN[7] (-)

Refer to the MPC5777C Reference Manual for complete details on configuring the analog input channels of the SDADC.

9.2 SDADC External Circuitry

The following figure shows the typical circuitry for single ended SDADC channel with filtering components.

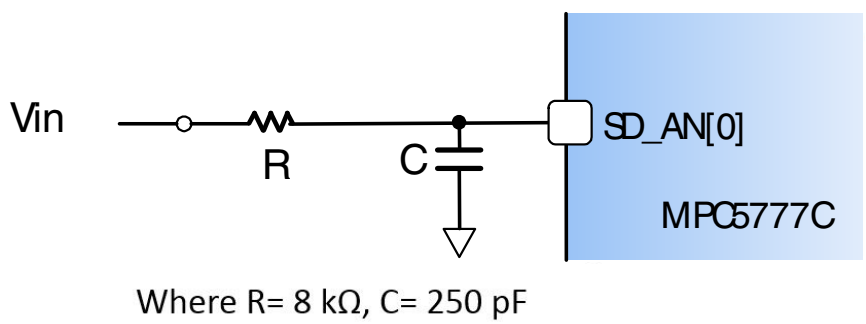

Figure 23. Single-ended SDADC External Circuit

For an anti-aliasing filter, the minimum capacitor size (C) is 220 pF and maximum resistor size (R) is 20 KΩ. R & C values should be chosen such that the filter pole formed by them (1/(2×π×R×C) satisfies the following two conditions:

- It needs to be placed well above the maximum frequency of the input signal (up to 100KHz) in order to minimize input signal attenuation
- It needs to be placed at or below the SDADC sampling clock frequency minus the input signal bandwidth in order to avoid aliasing (sampling clock is half the SDADC clock, min 4 MHz / 2 = 2 MHz)

The figure below shows an example of differential ended SDADC channels with filtering components. Inputs need to be 180 degrees out of phase and in the 10 Hz - 100 kHz range.

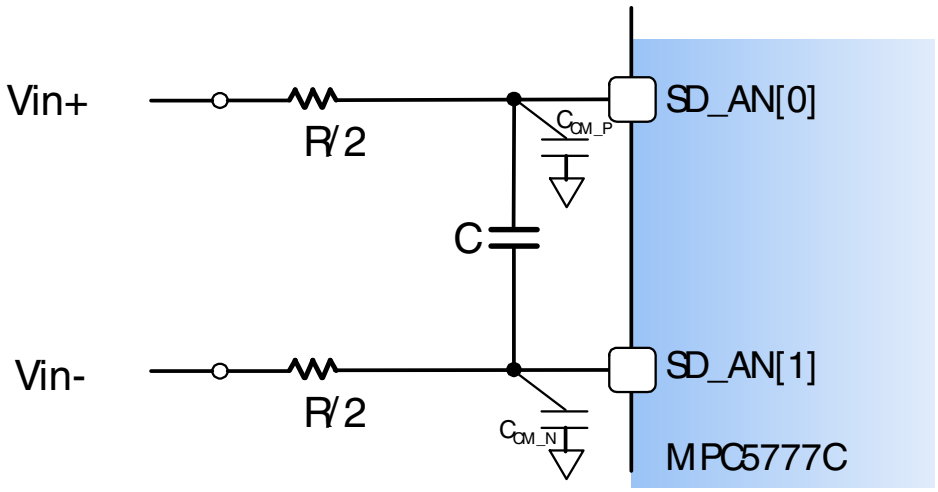

Figure 24. Differential SDADC External Circuit

NOTE

External common mode voltage of differential signals should be VDDA_SD/2. Depending on the system noise levels the user can place C_{CM_P} / C_{CM_N} to improve the external common mode noise. As a rule of thumb, the capacitor values should be less than or equal to the filter capacitor value C divided by 10.

- Internal common-mode for MPC5777C SDADC is VDDA_SD/2, set by the bias generator.
- External C_{CM_P}/C_{CM_N} capacitors filter external common-mode noise.
- External C_{CM_P}/C_{CM_N} have a 2nd order effect on the filter pole.Without external common-mode filter caps, the application would rely on common-mode noise rejection of the ADC.
- External C_{CM_P}/C_{CM_N} should be 1/10th or less the value of C filter.
- External C_{CM_P}/C_{CM_N} ideally connected to V_{CM} (VDDA_SD/2), but can be connected to ground (VSSA_SD).

10 Example communication peripheral connections

There are a wide range of peripheral pins available on this device. Many of these have fairly standard definitions for their use. This section provides example connections for some of the most commonly used communications peripherals, such as Local Interconnect Network (LIN), Controller Area Network (CAN), Ethernet, and RS-232 communication interfaces.

The table below summarizes the maximum communication speed and general overview information of the different types of interfaces.

Table 30. Communication module comparison

Common name	Standard	Distributed timebase	Speed (maximum Kbits/second)	Channels	Time triggered	Arbitration
RS-232D	EIA RS-232 revision D	No	115.2	Single	No	None (optional flow control)
K Line	ISO 9141	No	150[1]	Single	No	None
LIN	LIN 1.0, LIN 2.0, and LIN 2.1[2]	No	100[3]	Single	No	None (master/ slave)
CAN	Bosch 2.0B ISO11898	No	1,000[4]	Single	No (additional function)	CSMA[5]

Table continues on the next page...

Table 30. Communication module comparison (continued)

Common name	Standard	Distributed timebase	Speed (maximum Kbits/second)	Channels	Time triggered	Arbitration
Ethernet	IEEE® 802.3	No	10,000/100,000	Single	No	CSMA

1. Typical speed is 10.4Kbits/s.
2. Many NXP devices only support the LIN 1.0 and 2.0 standards. LIN2.1 requires a different sampling scheme covered by an erratum to the LIN standard..
3. Typical speed is 10 or 20 Kbits/s, but supports a fast mode of 100 Kbits/s.
4. Two different speed classes are supported by CAN, a fast (250K to 1Mbits/s) and a low speed CAN (5K to 125Kbits/s).
5. Carrier Sense Multiple Access

In a typical system, the battery reverse bias and over-voltage protection may be shared between all of the communication devices in the target system. The below figure shows a typical protection circuit.

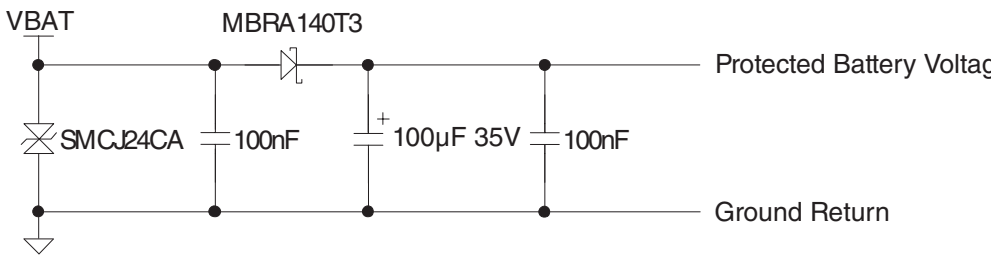

Figure 25. Typical protection circuit

10.1 Example LIN interface for eSCI

Local Interconnect Network (LIN) is a commonly used low-speed network interface that consists of a master node communicating with multiple remote slave nodes. Only a single wire is required for communication and is commonly included in the vehicle wiring harness.

The enhanced Serial Communication Interface (eSCI) module implements Local Interconnect Network (LIN) interface. This same module (eSCI) also supports the standard Universal Asynchronous Receiver/Transmitter (UART) functions (with a different physical layer device).

The following figure shows a typical interface implemented using the NXP MC33661 LIN transceiver.

Example communication peripheral connections

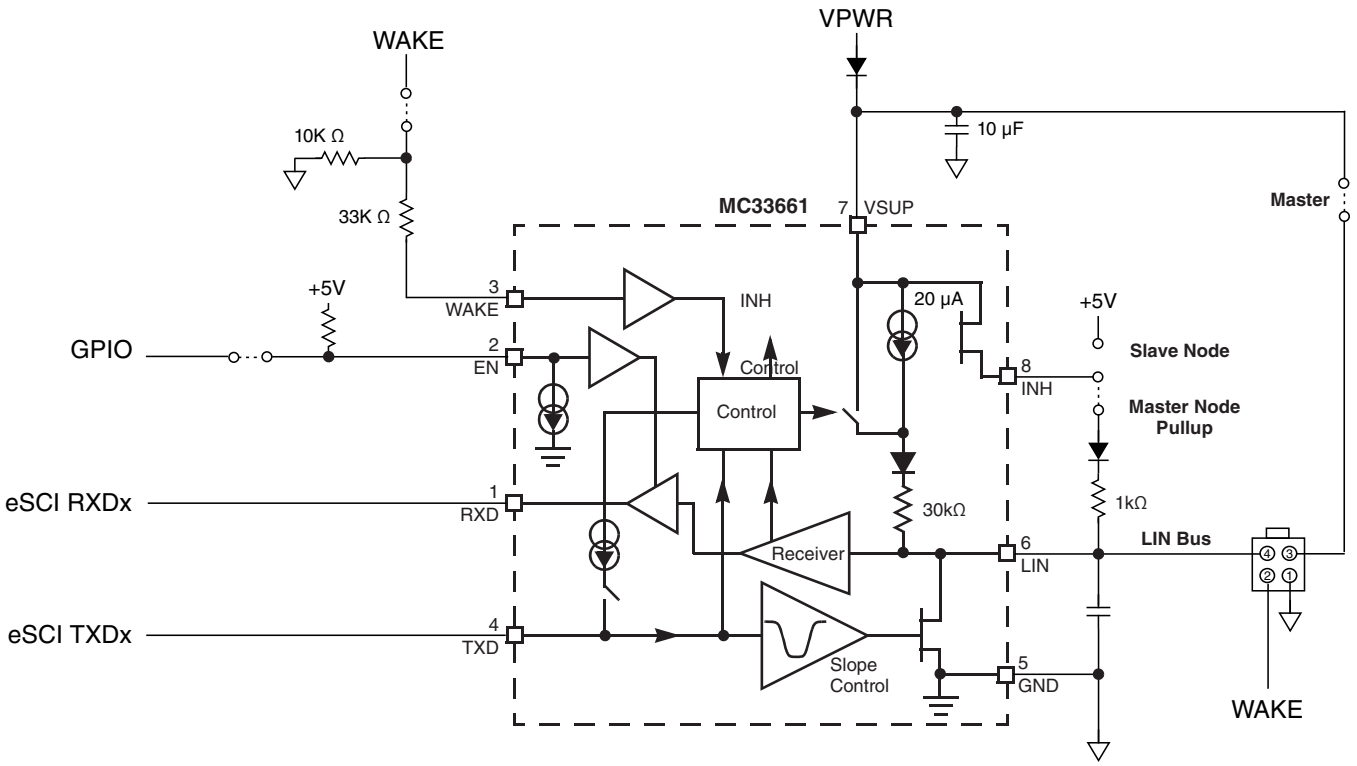

Figure 26. Typical eSCI to LIN connections

The table below shows the pins of MC33661 and their typical connections to an MCU.

Table 31. MC33661 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	RXD	Output	Receive Data Output	MCU LIN RXD	LIN Receive Data Output to the MCU.
2	EN	Input	Enable Control	MCU GPIO	Enables operation of the device.
3	Wake	Input	Wake Input	LIN Bus Wake[1]	Wake enables the devices out of sleep mode.
4	TXD	Input	Transmit Data Input	MCU LIN TXD	LIN Transmit Data Input from the MCU.
5	GND	Input	Ground	System Ground Reference	Device ground reference.
6	LIN	Input/Output	LIN Bus	LIN bus	Bidirectional pin that represents the single-wire transmit and receiver.
7	VSUP	Input	Power Supply	Protected battery voltage	This is the power supply for the device and is typically connected to a nominal 12 V.

Table continues on the next page...

Table 31. MC33661 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
8	INH	Output	Inhibit Output	LIN Bus (if master)	The Inhibit pin controls either an external regulator to turn on a slave node or is connected through a resistor to the LIN bus on master nodes.

1. Wake is an optional signal on the LIN connector, but may come directly from a switch.

There is no standard industry-defined LIN connector. NXP uses a 4-pin Molex that allows for the LIN bus pin, a power supply source (VPWR), a wakeup signal, and a ground reference. Slave nodes will often implement two connectors to allow a daisy-chain of multiple nodes to be easily implemented. The NXP Molex connector definition is shown in the following table.

Table 32. LIN connector pin-out recommendation

Function	Pin number	Pin number	Function
LIN Bus	4	3	VPWR
Wake	2	1	Ground

In a typical system, these pins would be used as follows:

- LIN Bus - This is the single-wire LIN bus that connects between the master LIN node and the slave LIN nodes.
- VPWR - This connector input can be used as the power input to a slave node. Care should be taken that sufficient current is available for the total number of LIN slaves that are powered through this connection. In some systems, this may come from the master LIN node.
- Wake - The Wake signal is typically used for each individual slave node to enable the LIN physical interface of that node and consequently enable the power supply (using the INH output) to power up the MCU to perform some action. For example, when the handle on a car door is lifted, turn on the MCU that controls a function inside the vehicle, such as power a smart dome light or enable the controls of a smart seat.
- Ground - Ground reference for the module.

Part numbers for the 4-pin Molex Mini-Fit Jr.™ connector are shown in the table below.

Table 33. Recommended 4-pin Molex Mini-Fit Jr.™ connector part numbers

Description	Manufacturer part number (Molex)
4-pin right-angle connector with flange for target system, tin contacts, with latch	39-29-1048
4-pin right-angle connector with pegs for target system, tin contacts, with latch	39-30-1040
4-pin vertical connector with pegs for target system, tin contacts, with latch	39-29-9042
4-pin right-angle connector with flange for target system, gold contacts, latch	39-29-5043

Table continues on the next page...

Table 33. Recommended 4-pin Molex Mini-Fit Jr.™ connector part numbers (continued)

Description	Manufacturer part number (Molex)
Mating connector with latch for cable assemblies	39-01-2040
Female terminal for mating cable assembly	39-00-0077

10.2 Example RS-232 interface for eSCI

The RS-232 (TIA/EIA-232-F) standard is a fairly common interface that was once available on nearly all computers. While this interface is disappearing, adapters are available to allow the use of RS-232 peripherals though other interfaces, such as USB. RS-232 was intended to be a very low-cost, low-performance interface. This interface was originally specified with signal voltages of +12 V and -12 V typically. However, this has been lowered to a typical minimum voltage of +5 V and -5 V in recent years.

The enhanced Serial Communication Interface (eSCI) module implements the standard Universal Asynchronous Receiver/ Transmitter (UART) functions. This same module (eSCI) also supports the Local Interconnect Network (LIN) interface (with a different physical layer device).

The figure below shows the typical connections between the serial port of an MCU and the MAX3232-EP RS-232D transceiver from Texas Instruments (http://www.ti.com/). The transceiver operates from either a 3.3 V or a 5 V supply and includes two charge pumps to generate the output voltages that are required. This device contains two transmit drivers and two receivers. The charge pumps require four external capacitors.

NOTE

The commercial grade MAX3232 device is not rated for the full automotive temperature range of -40 to +125° C and is not intended for automotive applications. This circuit should not be used or populated in a production module intended for automotive use. However, in many cases, the RS-232 interface is intended only as a development interface; therefore the commercial device can be used for prototyping purposes. TI does offer a device option with an operating temperature range of -40 to +85° C. TI has an enhanced version of the device, MAX3232-EP, which is intended for aerospace, medical, and defense applications. This version is available with an operating temperature range of -55 to +125° C.

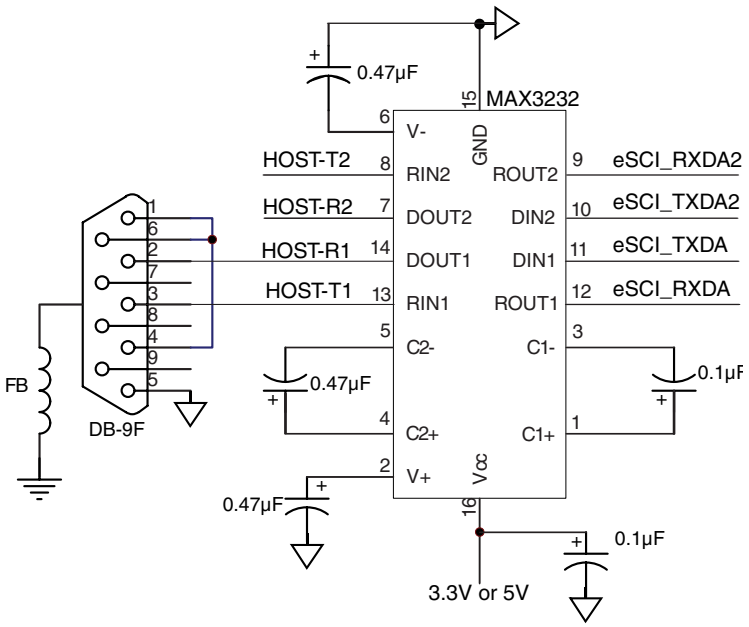

Figure 27. Typical eSCI to RS-232D circuit

The following table shows the standard connection of the RS-232 connector, as used on the NXP evaluation boards.

Table 34. Typical RS-232D Connector Definition

6 Connect to pin 1 and 4	**1** Connect to pin 4 and 6
7 N/C	**2** RS-232 TX (Transmit)
8 N/C	**3** RS-232 RX (Receive)
9	**4** Connect to pin 1 and 6
	5 GND

NOTE

N/C pins are not connected. Shell of connector should be connected through a ferrite bead to ground.

10.3 Example K LINE interface for eSCI

ISO9141, also known as K Line, is a low-speed diagnostic interface that provides a bi-directional half-duplex single-wire communication channel. A K Line interface can be implemented with a standard UART type function, such as is implemented in the eSCI module. The K Line interface is used primarily for a low cost on-board diagnostic interface.

MC33290 implements a K line interface in an 8-pin SOICN package. Below is the list of features and a block diagram of MC33290.

- Operation over wide supply voltage of 8.0 V to 18 V
- Operating temperature of -40 to 125 °C
- Interface directly to standard CMOS microprocessors
- ISO K Line pin protected against shorts to ground
- Thermal shutdown with hysteresis
- ISO K Line pin capable of high currents
- ISO K Line can be driven with up to 10 nF of parasitic capacitance
- 8.0 kV ESD protection attainable with few additional components

- Standby mode: no battery current drain with VDD at 5.0 V
- Low current drain during operation with VDD at 5.0 V

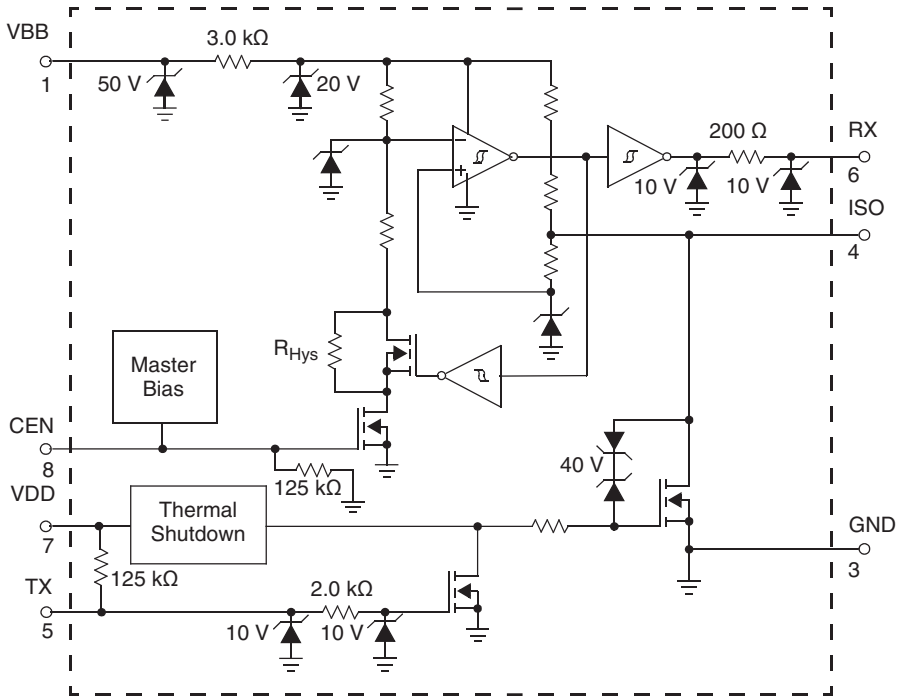

Figure 28. MC33290 block diagram

The following figure shows a typical interface between the MCU and MC33290.

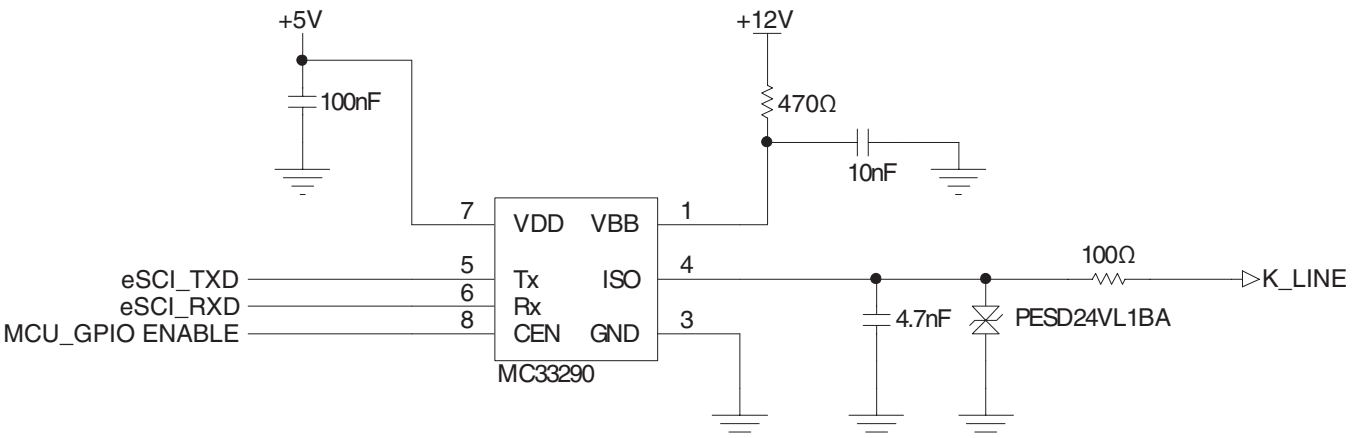

Figure 29. Typical eSCI to K Line connections

The following table shows the pins of MC33290 and the typical connection in a target system.

Table 35. MC33290 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	VBB	Input	Battery Voltage	Protected battery voltage	VBB is the protected battery voltage supply for the device. It should have a reverse bias

Table continues on the next page...

Table 35. MC33290 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
					protection diode and a series resistor to the over-voltage protected battery.
2	NC	—	—	None	This pin should have no connection in the system.
3	GND	Input	Ground	Ground	Ground reference and power return for the device.
4	ISO	Input/Output	ISO9141 bus	K-Line connector	ISO9141 bus connection.
5	TX	Input	Transmit data input	eSCI TXD	Input data to be transmitted on the ISO bus.
6	RX	Output	Receive Data Output	eSCI RXD	Output of the data received on the ISO bus.
7	VDD	Input	Digital Interface logic supply	5 V supply	Logic power source.
8	CEN	Input	Chip Enable	MCU GPIO (output)	Chip enable for the MC33290.

NOTE

In a typical system, the battery reverse bias and over-voltage protection may be shared between all of the communication devices in the target system.

10.4 CAN Interface Circuitry

Controller Area Network (CAN) is commonly used in almost all automotive applications to allow communication between various microchips in the car.

A separate CAN transceiver is required for each CAN module used on the device, although some CAN transceiver chips may have more than one transceiver on a single chip. It is possible to connect two CAN modules to a single transceiver if the transmit pins are put into open-collector mode with an external pullup resistor. However, the value of this resistor may limit the maximum speed of the CAN module if not sized properly for the speed.

NXP CAN modules conform to CAN protocol specification version 2.0 B, and the transceivers shown in this application note comply with ISO 11898 physical layer standard.

Typically, CAN is used at either a low speed (5 Kbit/s to 125 Kbit/s) or a high speed (250 Kbit/s to 1 Mbit/s). Powertrain applications typically use a high speed (HS) CAN interface to communicate between the engine control unit and the transmission control unit. Body and chassis applications typically use a low speed (LS) CAN interface. In the dashboard of a vehicle, there is typically a gateway device that interfaces between HS and LS CAN networks. Some devices support the updated ISO11898-2 specification with support for CAN with flexible data-rate (CAN FD).

Other popular CAN transceivers include the NXP devices shown in the following table. Example TJA1050 HS, TJA1054 LS, and TJA1057 FD circuits are shown in this application note.

Table 36. NXP CAN transceiver comparison

	TJA1050	TJA1054	TJA1040	TJA1041	TJA1057
Frame data rate (Kbit/s)	1000	125	1000	1000	5000

Table continues on the next page...

Table 36. NXP CAN transceiver comparison (continued)

Modes of operation	Normal, Listen-only	Normal, Standby, Sleep	Normal, Standby	Normal, Listen-only, Standby, Sleep	Normal, Listen-only

10.4.1 High-Speed CAN TJA1050 Interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for high-speed applications using the NXP TJA1050 HS CAN transceiver.

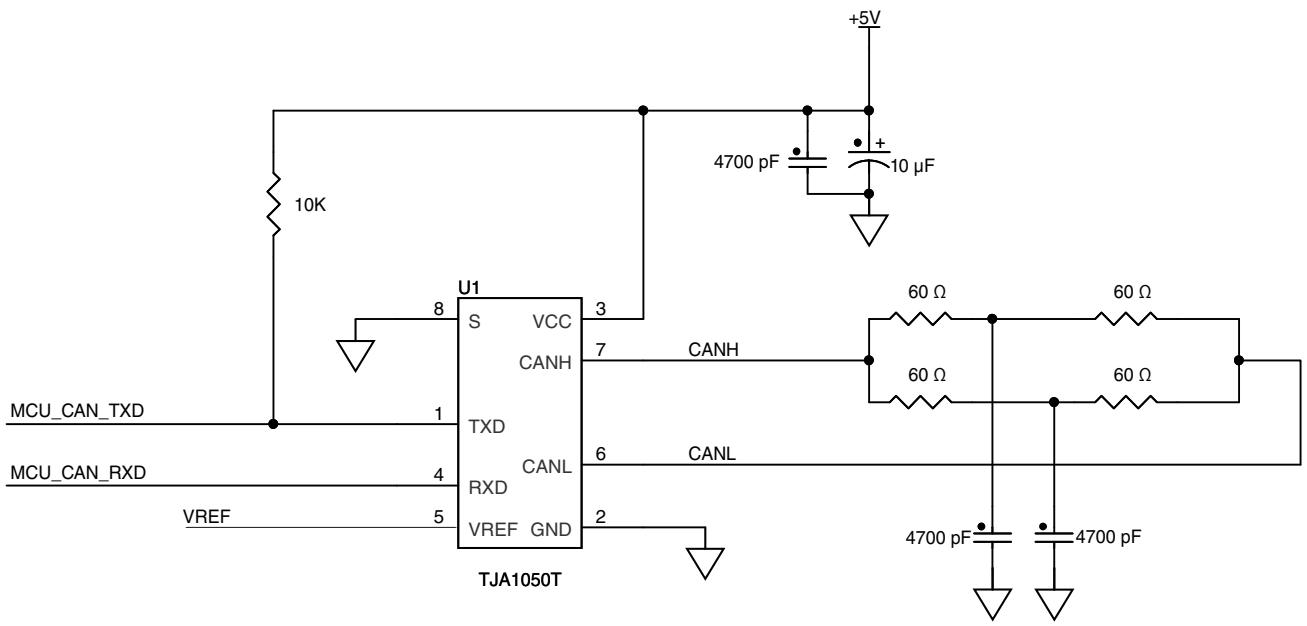

Figure 30. Typical high-speed CAN circuit using TJA1050

NOTE

- Decoupling shown as an example only.
- TXD/RXD pullup/pulldown may be required, depending on device implementation.

The table below describes the TJA1050 pin and system connections.

Table 37. TJA1050 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
2	GND	Output	Ground	Ground	Ground return termination
3	VCC	Input	—	5 V	Voltage supply input (5 V)
4	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU

Table continues on the next page...

Table 37. TJA1050 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
5	VREF	Output	Reference voltage Output	Not used	Mid-supply output voltage. This is typically not used in many systems, but can be used if voltage translation needs to be done between the CAN transceiver and the MCU.
6	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
7	CANH	Input/Output	CAN Bus High	CAN Bus Connector	CAN bus high pin
8	S	Input	Select	Grounded or MCU GPIO	Select for high-speed mode or silent mode. Silent mode disables the transmitter, but keeps the rest of the device active. This may be used in case of an error condition.

10.4.2 Low-Speed CAN TJA1054 Interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for low-speed applications using the NXP TJA1054 LS CAN transceiver. Optionally, the standby and enable pins can be connected to MCU GPIO pins for additional control of the physical interface.

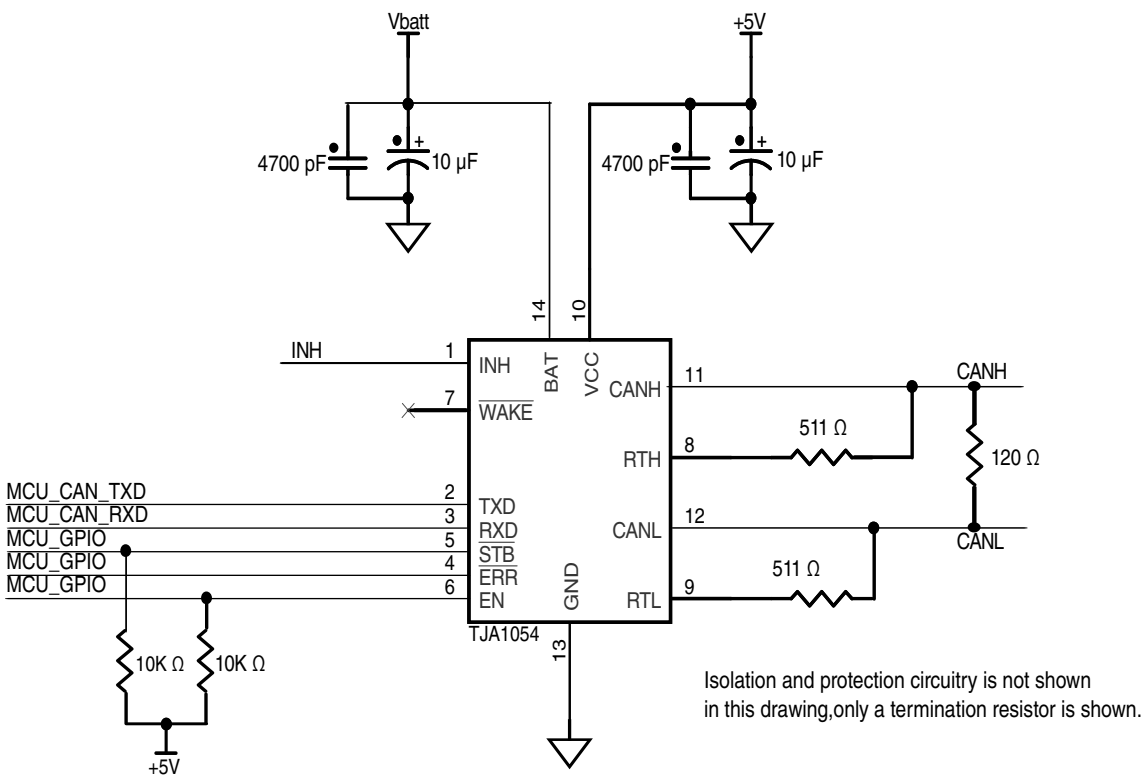

Figure 31. Typical low-speed CAN circuit using TJA1054

NOTE

- Decoupling shown as an example only.
- $\overline{\text{STB}}$ and EN should be pulled high for Normal mode. These signals can optionally be connected to MCU GPIO pins to allow MCU control of the physical interface.

The table below describes the TJA1054 pins and system connections.

Table 38. TJA1054 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	INH	Input	Inhibit	Typically not connected	Inhibit output for control of an external power supply regulator if a wake up occurs
2	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
3	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU
4	$\overline{\text{ERR}}$	Output	Error	MCU GPIO	The error signal indicates a bus failure in normal operating mode or a wake-up is detected in Standby or Sleep modes.
5	$\overline{\text{STB}}$	Input	Voltage Supply for IO	MCU GPIO	Standby input for device. It is also used in conjunction with the EN pin to determine the mode of the transceiver.
6	EN	Input	Enable	MCU GPIO	Enable input for the device. It is also used in conjunction with the STB pin to determine the mode of the transceiver.
7	$\overline{\text{WAKE}}$	Input	Wake	Typically not connected	Wake input (active low), both falling and rising edges are detected
8	RTH	Input	Termination Resistor High	Resistor to CANH	Termination resistor for the CAN bus high
9	RTL	Input	Termination Resistor Low	Resistor to CANL	Termination resistor for the CAN bus low[1]
10	VCC	Input	Voltage Supply	5 V	Digital IO supply voltage, 5 V
11	CANH	Output	CAN Bus High	CAN Bus Connector	CAN bus high pin
12	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
13	Ground	Output	Ground	Ground	Ground return termination path
14	BAT	Input	Standby	Battery voltage	Battery supply pin, nominally 12 V

1. This allows the transceiver to control the CAN bus impedance under an error condition.

10.4.3 CAN with Flexible Data-Rate TJA1057 Interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for high-speed CAN with flexible data-rate applications using the NXP TJA1057 CAN FD transceiver. CAN FD supports variable frame sizes and data rates up to 5 Mbps.

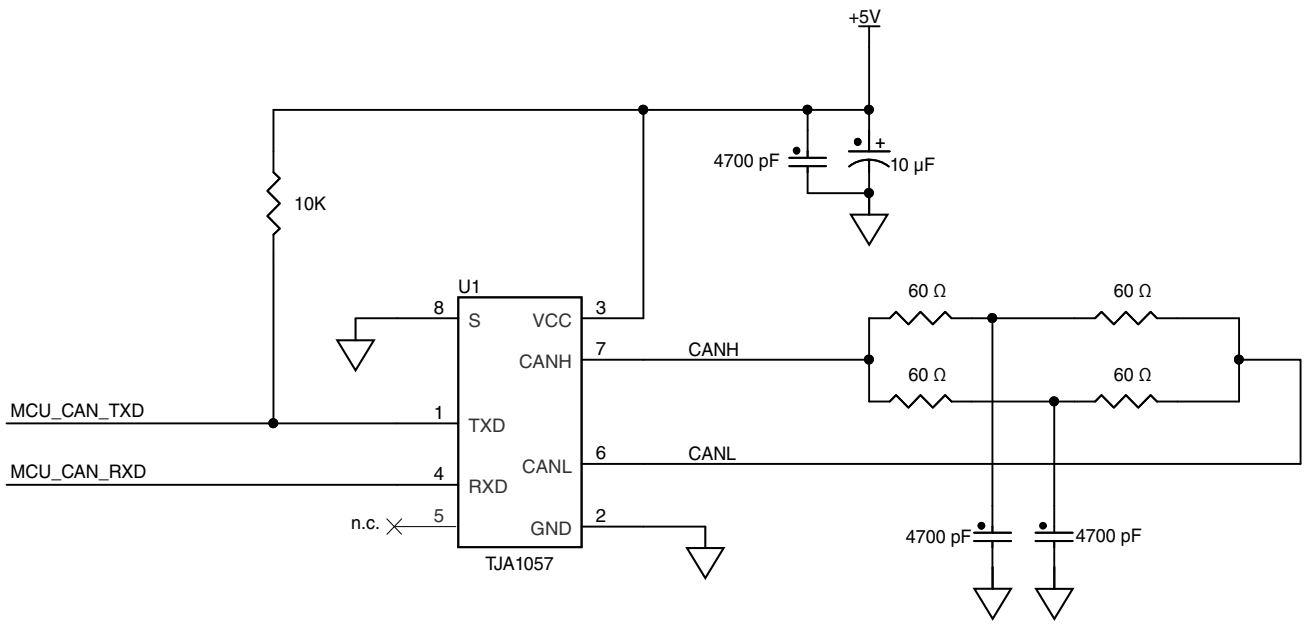

Figure 32. Typical CAN FD circuit using TJA1057

NOTE

- Decoupling shown as an example only.
- TXD/RXD pullup/pulldown may be required, depending on device implementation.
- Backward compatible with NXP TJA1050 high-speed CAN transceiver.

The table below describes the TJA1057 pin and system connections.

Table 39. TJA1057 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
2	GND	Output	Ground	Ground	Ground return termination
3	VCC	Input	—	5 V	Voltage supply input (5 V)
4	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU
5	n.c.	—	—	Not used	Not connected
6	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
7	CANH	Input/Output	CAN Bus High	CAN Bus Connector	CAN bus high pin
8	S	Input	Silent Mode	Grounded or MCU GPIO	Silent mode control input. A high level on this pin selects Silent mode. This mode disables the transmitter, but keeps the rest of the device active. This may be used in case of an error condition.

10.4.4 Recommended CAN Connector

Generally DB-9 connectors are used for evaluation boards to connect CAN modules together, whereas there are various connectors used for production hardware. The following figure shows the DB-9 connector and socket configuration of a typical evaluation board connector. A socket is used on the evaluation board and a cable with a connector connects with it.

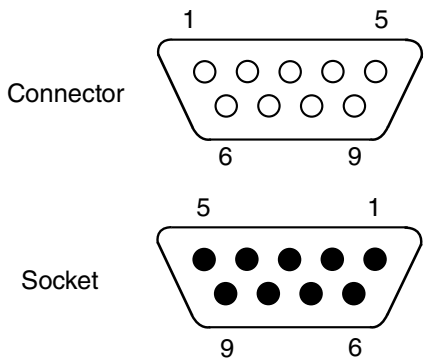

Figure 33. DB-9 connector and socket

The table below shows the typical connector pin-out definition.

Table 40. DB-9 pin signal mapping

Pin number	Signal name
1	N/C
2	CAN_L
3	GND
4	N/C
5	CAN_SHIELD (OPTIONAL)
6	GND
7	CAN_H
8	N/C
9	CAN_V+ (OPTIONAL)

NOTE

The metal shell of the socket should be connected through a ferrite bead to the chassis ground.

10.5 Ethernet Interface

Ethernet is a communication technology that was originally developed for creating local area networks (LANs) between computers. Over time, it has become the standard wired communications network for the PC and is widely used within telecommunications and industrial applications. In recent years, Ethernet has found its way into automotive electronics with deployment in diagnostic and camera applications. The Fast Ethernet Controller (FEC) implemented on the MPC5777C devices is a communication controller that supports 10 and 100 Mbit/s Ethernet/IEEE 802.3 networks. An external

transceiver interface and transceiver function are required to complete the connection to the physical interface. The figure below shows a typical set up of the complete interface to the network. Here a TJA1100 from NXP is used as the Ethernet PHY.

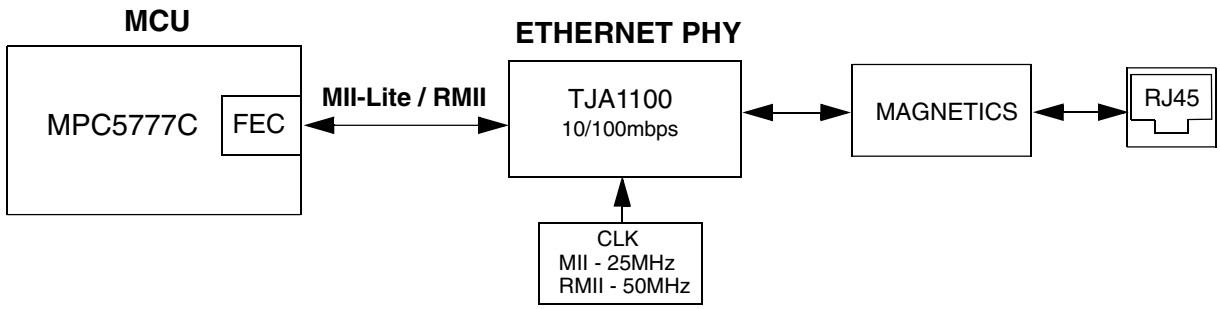

Figure 34. Ethernet application example

As shown in the figure above, the FEC can interface to a PHY using either the 10/100 Mbit/s MII-Lite or RMII. The FEC signals from the MCU take their voltage level from the VDDE2A and VDDEH3A supply domains. These domains have been separated from the VDDE2 and VDDEH3 domains in order to allow 3.3V Ethernet signal levels while maintaining the option to have 5V levels on other peripherals connected to those domains. Most PHYs require signals in the 3.3 V range, so VDDE2A and VDDEH3A should be supplied accordingly. The FEC signals are summarized in the table below and their use in each interface type is highlighted. Note that the signals required by different PHYs will vary in some cases for each interface option; see the Data Sheet for your selected PHY.

Table 41. FEC Signal Overview

Signal Name	Description	Direction	MII-Lite	RMII
FEC_MDC	Management Data Clock	O	Optional	Optional
FEC_MDIO	Management Data I/O	I/O	Optional	Optional
FEC_RXCLK	Receive Clock	I	Required	N/A
FEC_RXDV	Receive Data Valid	I	Required	Required[1]
FEC_RXD0	Receive Data 0	I	Required	Required
FEC_RXD1	Receive Data 1	I	Required	Required
FEC_RXD2	Receive Data 2	I	Required	N/A
FEC_RXD3	Receive Data 3	I	Required	N/A
FEC_TXCLK	Transmit Clock	I	Required	Required[2]
FEC_TXD0	Transmit Data 0	O	Required	Required
FEC_TXD1	Transmit Data 1	O	Required	Required
FEC_TXD2	Transmit Data 2	O	Required	N/A
FEC_TXD3	Transmit Data 3	O	Required	N/A
FEC_TXEN	Transmit Enable	O	Required	Required

1. FEC_RXDV in RMII mode functions as both RXDV and CRS (Carrier Sense) signals.
2. FEC_TXCLK in RMII mode functions as both transmit and receive clock input.

10.6 Zipwire hardware and layout

Example communication peripheral connections

The Zipwire interface is intended to be used to communicate between two nodes implemented on a single board. The interface uses a "low speed" reference clock that is shared between the two nodes. A single-ended 10 to 26[6] MHz reference clock is used to generate the Zipwire high speed operation of approximately 240 MHz. A termination resistor is required at the receiving end of the clock for best performance of the interface. The value of the resistor depends on the board layout and impedance. For more information, see AN5134, "Introduction to the Zipwire Interface".

The data signals use a low voltage differential signaling (LVDS) that is internally terminated on the MCU.

The following diagram shows the connection between two devices.

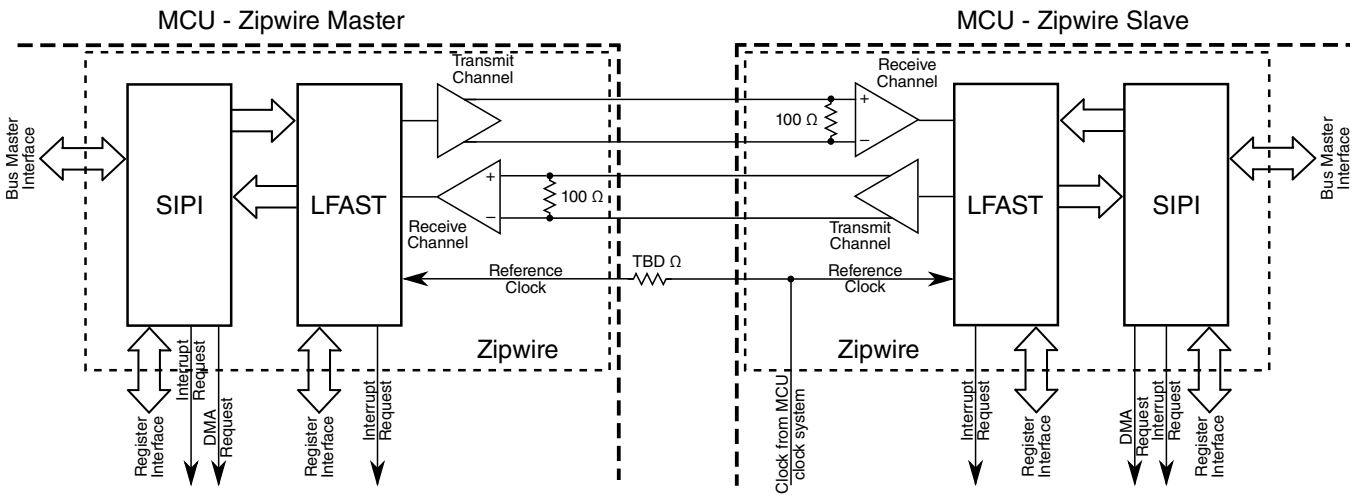

Figure 35. Typical Zipwire hardware interface

The Zipwire interface is a high-speed interface, therefore care should be taken in laying out the signals on a printed circuit board. The following guidelines are suggested.

- A controlled impedance PCB is required for the LVDS signals.
- The differential LVDS + and – pair should be routed parallel and close to each other. The length of the + and - pairs should be matched to less than 0.1 inches of difference.
- The LVDS transmit pair length is not required to be the same length as the LVDS receive pair.
- The differential pair should be routed with a maximum of two vias. Ideally, the differential pair should be routed without vias on a single plane of the board preferably on the top or bottom plane of the board. However, due to pin escape issues with the placement of the high speed signals on the surface mounted devices, routing on a single layer is usually not possible.
- Keep necking of the signal to less than 0.01 inch to avoid discontinuities. Some necking is usually required in escaping the signals for the BGA or LQFP signal feeds to other layers on the board.
- The differential pair must be routed on a layer that is one dielectric away from ground.
- A connector is not recommended for the Zipwire interface, but if a connector is used, a high speed connector system, such as the Samtec ERF8 0.8 mm Edge Rate Rugged High Speed Socket, should be used with twin-ax cabling. The odd side of the connector should be placed parallel and nearest to the MCU package on the board to allow direct connection to the package signals.

6. 20 MHz is the most commonly used frequency, 10 MHz can also be used. 26 MHz is not recommended.

11 Pin Overview

Since there are many different requirements for the input and output signals of the pins of the MCU, several different pad types are used to drive these signals. The following table summarizes the pad types available on the MCU. Information on the pad types and signal multiplexing is available in the device Reference Manual and the device Data Sheet. This section helps interpret this information.

Table 42. Pad Types

Pad type	Abbreviation	Description
General-purpose I/O pads	SR	Most of the peripheral signals are medium-speed, slew-rate (SR) controlled pads, such as the eMIOS, and the eTPU. The pads may implement digital input circuitry, digital output circuitry or both. They can be powered by 3.3 V or 5.0 V supplies.
EBI pads	FC	Provide necessary speed for fast external memory interfaces on the EBI CLKOUT, address, and control signals. These pads have drive-strength control and may implement digital input circuitry, digital output circuitry or both. They can be powered by 3.3 V or 5.0 V supplies.
LVDS pads	LVDS	Low Voltage Differential Signal interface pads.
Input-only pads	AE or Analog	The input-only analog pads are low leakage and have no digital input or output circuitry. Some Analog pins (analog pads that support being used as a differential analog signal) also contain pull up and pull down resistors incorporated into the pad that can be independently selected.

Each of these pad types have programmable features that are controlled in a Pad Configuration Register (PCR). All pads, except single purpose pads without special properties that need to be controlled, on the device have a PCR. In a few cases, some signals are grouped together and a single PCR controls multiple pads. The PCR is identified by the GPIO number. The PCR controls the pad function, direction, and other capabilities.

11.1 Pin multiplexing

A majority of the Input/Output pins[7] on the MCU have multiple functions that are selectable by software[8]. The figure below shows a typical excerpt from the MPC577xC System IO Definition spreadsheet. This table shows the different functions that are available on each pin. The full spreadsheet is available as a file attachment within the device reference manual.

7. Ball grid array (BGA) packages have balls instead of pins. Pins are used on packages that have pins for signals. Pads refers to the bonding pad on the physical die that is contained inside the package. These terms are typically used interchangeably. The actual correct term depends on the package type.
8. In some cases, hardware overrides the software settings. Consult the device reference manual and data sheet.

Pin Name	SIU_A PCR#	PCR PA	Function	Module	Description	Direction	Pad Type	416 PBGA	516 PBGA	I/O Power Domain	I/O Power Segment	Pad State During Reset	Pad State After Reset	PCR								
														PA[2:0]	OBE	IBE	DSC[1:0]	ODE	HYS	SRC[1:0]	WPE	WPS
ETPUA5	119	0b00	GPIO[119]	SIU_A	General Purpose I/O 119	I/O	pad_sr_hv	K3	H1	VDDEH1	seg0	-/WKPCFG	-/WKPCFG	00	0	0	-	0	0	00	1	U
		0b01	ETPUA5	eTPU_A	eTPU A Channel 5	I/O																
		0b10	ETPUA17	eTPU_A	eTPU A Channel 17	O																
		0b11	RCH3_A	REACM	Reaction Module Channel 3_A	O																
ETPUA6	120	0b00	GPIO[120]	SIU_A	General Purpose I/O 120	I/O	pad_sr_hv	K4	K5	VDDEH1	seg0	-/WKPCFG	-/WKPCFG	00	0	0	-	0	0	00	1	U
		0b01	ETPUA6	eTPU_A	eTPU A Channel 6	I/O																
		0b10	ETPUA18	eTPU_A	eTPU A Channel 18	O																
		0b11	RCH4_A	REACM	Reaction Module Channel 4_A	O																

Figure 36. Typical Device Pin Multiplexing

The first example shown above shows the ETPUA5 pin. It can function as either enhanced Timing Processing Unit instantiation A (eTPU A) channel 5, eTPU A channel 17, General Purpose Input/Output, or Reaction Module (REACM) channel 3. In this particular case, the GPIO and the eTPU A Channel 5 can be used either as an input to the eTPU or GPIO, or can be used as an output. However, if the eTPU A Channel 17 or REACM channel 3 function is selected, it can only be used as an output.

NOTE

In some cases, whether a channel can be an input or an output depends on the other signals available on the pin. This should be checked carefully when designing a board. Although, for example, the internal signal to the eTPU A for channel 17 can either be input or an output, this particular pin can only support channel 17 being an output. Other modules such as enhanced Modular Input/Output Subsystem (eMIOS) may also have this restriction. In particular, even though the eMIOS channels are all orthogonal on the MPC577xC, the input of some channels can only come from the Deserial/Serial Peripheral Interface (DSPI) and cannot be defined to come directly from a pin. This functionality of each pin needs to be reviewed in the Reference Manual and Data Sheet.

Other information shown in the above table extract is important when designing a board. These other fields are:

- **Pad Type**: This column of the table contains the pad type of the pin. This is required to understand the characteristics of the pin.
- **I/O Power Domain**: The power domain column of the table lists the power supply that powers the pin. All of the pins are broken up into separate power segments such that the input and output voltages for the pins match the voltage of the circuits connected to the pins.
- **Package Location:** These columns, labeled by package type, show the ball map location of the signal for each of the package types..
- **Pad State During Reset and After Reset**: The columns for the state of the pad during and after reset are important in the design of the system. The user needs to ensure that these states do not cause any issues with external circuitry, such as turning on a motor during reset.
- **PCR Settings**: These columns show the Pad Control Register (PCR) settings available which are configurable in the PCR for each pin. If a default value is shown, the setting is available for that pin. A dash indicates the setting is not available and changing the value of the corresponding field in the pin's PCR will have no effect.

11.2 Injection Current

All pins implement protection diodes that protect against electrostatic discharge (ESD). In many cases, both digital and analog pins need to be connected to voltages that are higher than the operating voltage of the device pin. In addition to providing protection from ESD, these diode structures will also clamp the voltage to a diode drop above the supply of that pin segment. This is permissible, as long as the current injection is limited as defined in the device specification. Current can be limited by adding a series resistor to the signal path. The input protection diodes will keep the voltage at the pin to a safe level (per the absolute maximum ratings of the device) as long as current injected at the pin is less than the maximum injection current specification.

Additional protection circuits on the pins are enabled only by fast ESD transients. In normal operation, these circuits have no effect on the pin characteristics. To avoid turning on these circuits during normal power-up sequences, the ramp rate of the power supplies (all external supplies, 5V, 3.3V, and if the internal regulator is not used, 1.25V) must be no faster than the voltage ramp rate (V_{RAMP}) specified in the datasheet.

Below is an extract from the MPC577xC Data Sheet. These specifications may change. Consult the latest revision of the data sheet to determine if there have been updates to these specifications.

Table 43. Injection currents allowed

Data Sheet Table	Pin type	Maximum inject current allowed
DC Electrical Specifications	DC Injection Current (per pin)	DC ±3 mA
Absolute Maximum Ratings	Maximum Digital Input Current, (per pin, applies to all digital pins)	±5 mA
Absolute Maximum Ratings	Maximum Analog Input Current (per pin, applies to all analog pins)	±5 mA

The figure below shows a typical digital pin and the protection diodes. Controls for all of the pad options are found in the Pad Configuration Register for the pin.

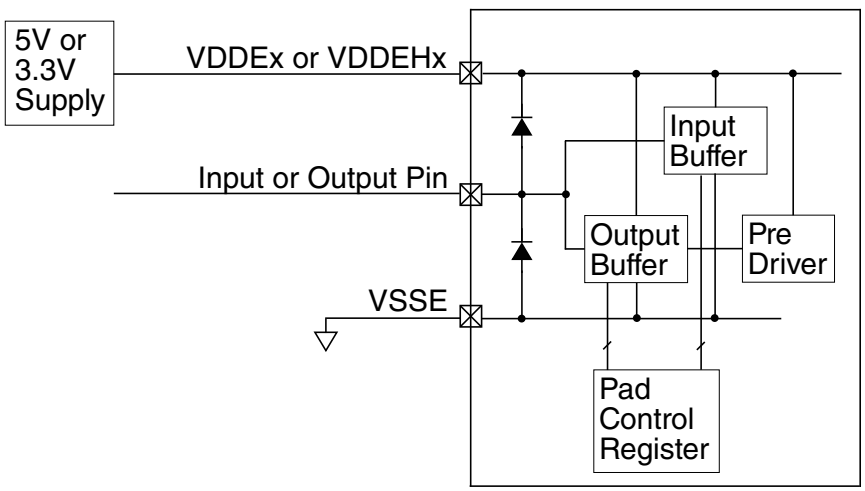

Figure 37. Typical input protection

The value of a series resistor to limit the injected current can be calculated simply. For a 1mA injection current limit, a 20KΩ resistor provides protection for a 20V DC injection current:

DC_{max} = 20kΩ/1mA = 20V

This voltage is sufficient for signals that are connected to a typical 12V battery.

In addition to the DC current, typically the data sheet includes a maximum accumulation specification for short periods of time over this DC level, such as 5mA for up to 60 hours over the entire life of the device.

$AC_{max\_current}$ = 20kΩ/5mA = 100V

If there are 5mS excursion events over the 1mA injection current limit of up to 5mA, then a total of 43.2K events can occur over the lifetime of the device.

$AC_{max\_duration}$ = 60 hours/5 ms per event = (60 hours x 60 minutes/hour x 60 seconds/minute) / 5ms = 43,200,000 events

11.3 Special Pins

There are a few pins on the device that should always be treated in the same manner. There are no options for how these pins are connected in a system.

- TEST - The Test pin should always be connected directly to ground.
- VSSSYN - The VSSSYN pin is a special ground signal for the external oscillator. It must be tied directly to ground.

11.4 Handling unused pins

In some applications, not all pins of the device may be needed. Good CMOS handling practices state that all unused pins should be tied off and not left floating. On the MCU, unused digital pins can be left open in the target system. Almost all pins have internal pull devices (either pull-up or pull-down devices[9]). For unused digital pins, it is recommended that software disable both the input buffers and the output buffers of the pads in the Pad Control Register for the pins. In addition, the weak pull-down device should be enabled. This keeps the pad in a safe state under all conditions.

For analog pins, it is recommended that they be pulled down to VSSA (the analog return path to the MCU).

One exception for this device is the internal core voltage regulator control pin, REGCTL. If the regulator is not being used, this pin should be left unconnected as described in the power supply options section of this document.

Appendix A Summary of recommended power supply bypass capacitors

The table below shows the recommended number and values of bypass capacitors for each of the digital power supply pins.

Table A-1. Recommended digital power supply bypass capacitors

Supply	Quantity	Value	Notes
VDDPMC	1	22 µF	These capacitors should be placed near the collector of the external pass transistor and to the VDDPMC pin.
	1	100 nF	
VDDPWR	1	22 µF (SMPS mode)	SMPS driver supply capacitance
		100 nF (LDO or external mode)	
VDD	6	4.7 µF (LDO mode)	Locate at the 4 corners and on 2 sides.
		22 µF (SMPS mode)	
	7	10 nF[1]	
VDDFLA	1	2 µF	Flash regulator bypass capacitor.
VDDEx/VDDEHx	1 per pin	4.7 µF	I/O supply pins.
VSTBY	1	10 nF	

1. Low ESR capacitors should be used.

9. Technically, these devices are not resistors. They are active weak transistors that pull the input either up or down.

The table below shows the recommended bypass capacitors for the analog power supplies of the device.

Table A-2. Recommended analog power supply bypass capacitors

Supply	Quantity	Value	Notes
VDDA_EQ	1	10 µF	For optimum analog performance, the VDDA supplies should be isolated/ filtered from the digital 5 V supplies. However, if analog injection current is allowed, no isolation should be used to prevent VDDA from rising due to injection current.
VDDA_SD	1	100 nF	
VRH_EQ VRH_SD	1	10 nF	Connect to VRL_EQ/SD. VRH_EQ/SD and VRL_EQ/SD should be isolated from VDDA and system ground.
REFBYPCA25	1	10 nF	Connect capacitor between each pin and VRL_EQ.
REFBYPCA75	1	10 nF	
REFBYPCB25	1	10 nF	
REFBYPCB75	1	10 nF	

Appendix B MPC5777C ADC Input Model

In some cases, knowledge of the internal topology of the eQADC model is required for some calculations, including sizing of the external capacitors, external resistors, and for setting the minimum sample time of the ADC. The figures below show a representative model of the eQADC inputs including the input multiplexers, internal node capacitances, and the actual sample capacitor of the ADC itself. The analog inputs that are accessible from both eQADC modules are also shown. For readability, the two eQADC modules (A and B) are shown separately.

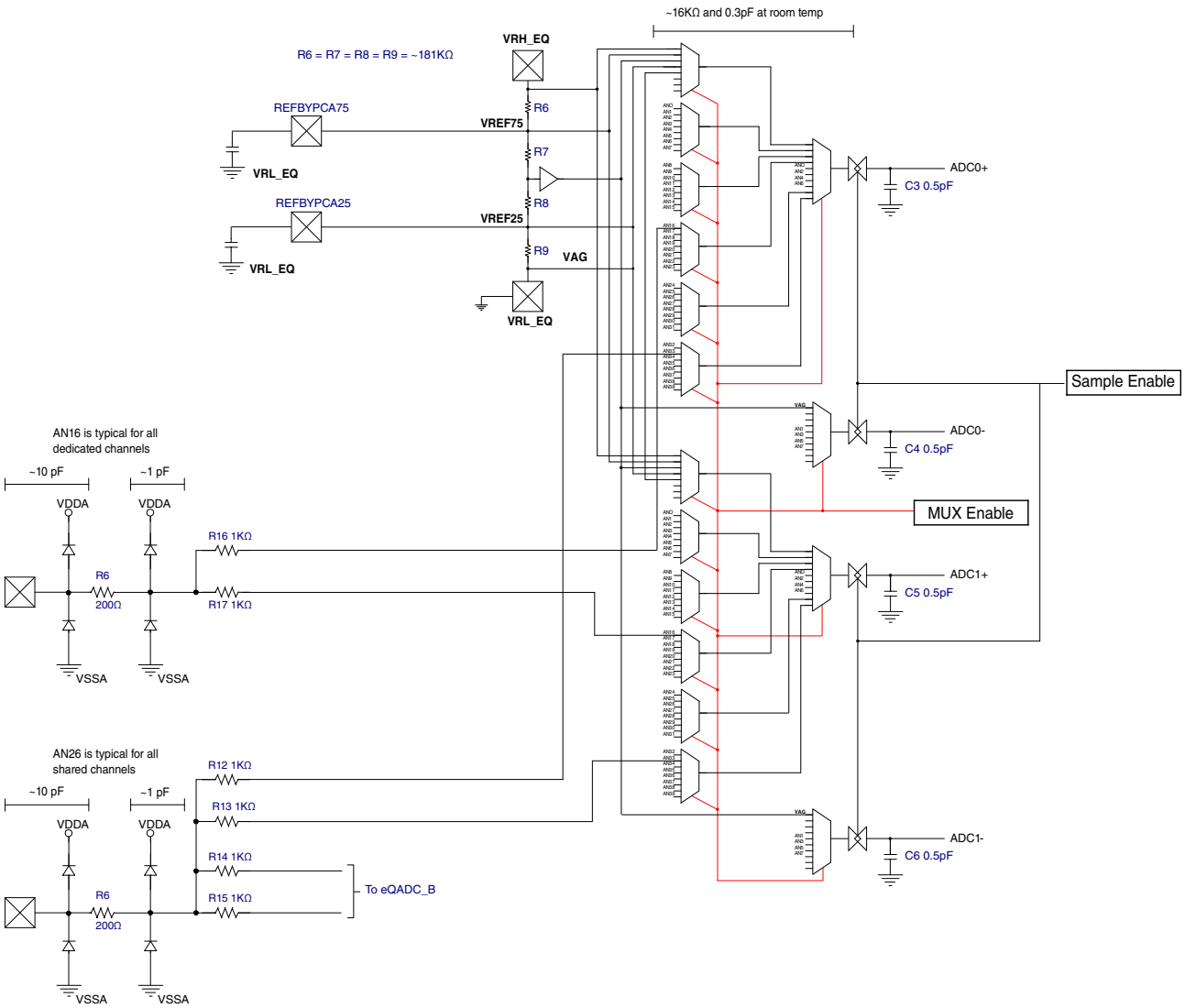

Figure B-1. MPC5777C eQADC_A Input Model

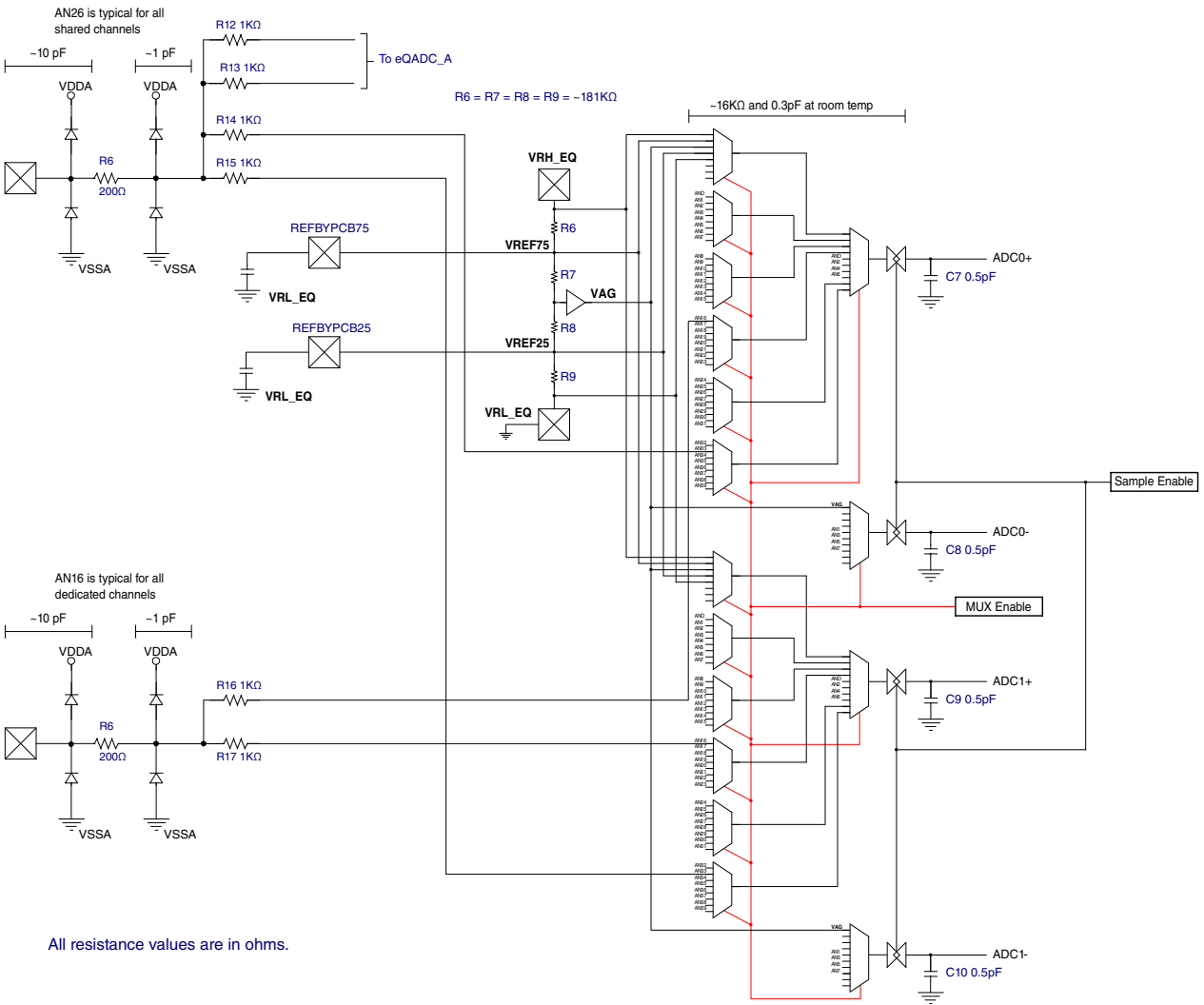

Figure B-2. MPC5777C eQADC_B Input Model

Appendix C References

More information can be found in the documents listed in the table below.

Table C-1. References

Document	Title
MPC5777CRM	MPC5777C Microcontroller Reference Manual
MPC5777C	MPC5777C Data Sheet
e200z759CRM	e200z759n3 Power Architecture Core Reference Manual
AN3968	Nexus Interface Connector for the MPC5674F/MPC5676R
AN2989	Design, Accuracy, and Calibration of Analog to Digital Converters on the MPC5500 Family
AN4731	Understanding Injection Current on NXP Automotive Microcontrollers
AN5134	Introduction to the Zipwire Interface

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