NXP low-power 8051 Flash microcontroller P89V52X2

Low-power Flash microcontroller reduces power consumption by up to 80%

This drop-in, software-compatible replacement for a conventional 80C51 microcontroller reduces power consumption by as much as 80%, delivers improved speeds at all voltage levels, and lowers overall cost.

Key features

- High-performance 8051 CPU with six- or 12-clock operation
- 80% power reduction compared to older 80C51 microcontrollers
- Up to 37-MHz performance at 5 V
- 8 KB of on-chip Flash
- 256 B of Data RAM
- Three 16-bit timers
- Full-duplex enhanced UART
- 32 configurable I/O
- Operating range: 2.7 to 5.5 V
- Backward compatibility
- Power savings, plus power-down and wake-up modes
- Dual Data Pointer (DDP)
- Extended temperature range: -40 to +85 °C
- Six interrupt sources with four priority levels
- Programmable clock-out
- Available in PLCC, LQFP, and DIP packages

The NXP P89V52X2 is a low-power 80C51 microcontroller that operates from 2.7 to 5.5 V and typically consumes only 8 µA at 85 °C. Compared to a conventional 80C51 microcontroller, it uses up to 80% less power, offers higher speeds at all voltage levels, and reduces design cost.

It is a drop-in, software-compatible replacement for NXP P87C52, P87C52X2, P89C52, and P89C52X2 microcontrollers.

The device uses a high-performance 8051 architecture that includes 8 KB of on-chip Flash and 256 B of on-chip Data RAM. Default operation uses six clocks, selectable to 12 clocks.

The low-power, static design supports a wide range of operating frequencies up to 5.5 V. The maximum operating frequency varies according to the number of clocks in operation and the power supply used. During 12-clock operation, the device operates at up to 37 MHz (4.5- to 5.5-V supply) or up to 31 MHz (2.7- to 5.5-V supply). During six-clock operation, the device operates at up to 28 MHz (4.5- to 5.5-V supply) or up to 21 MHz (2.7- to 5.5-V supply).

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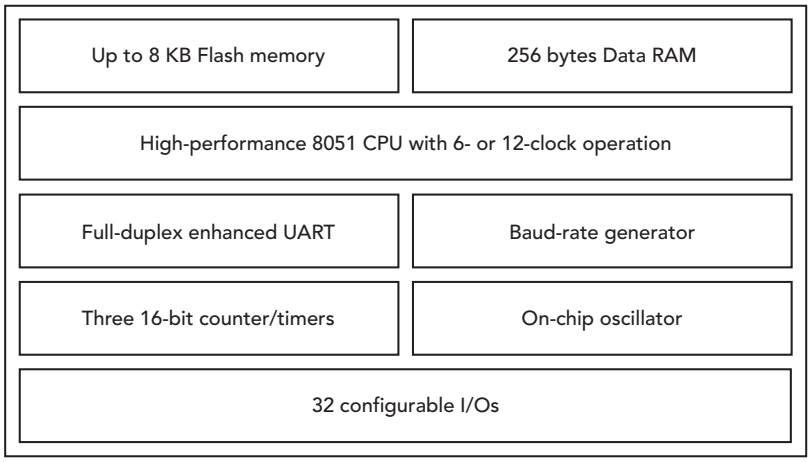
The device integrates three 16-bit counter/timers and uses a nested interrupt structure with six sources and four priority levels. There are 32 configurable I/O ports, plus a serial I/O port that can be used for multiprocessor communications, I/O expansion, or full-duplex UART operation. The device also integrates an on-chip oscillator and clock circuits.

Two software-selectable modes of power reduction, idle and power-down, are available. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions, except response to external interrupts or reset, to be inoperative. Since the design is static, the clock can be stopped without loss of user data and execution can be resumed from the point the clock was stopped.

The device is available in three versions. The –FA version is housed in a 44-pin PLCC, the –FBD version in a 44-pin LQFP, and the –FN in a DIP40.



P89V52X2 block diagram

Third-Party Development Tools

Through third-party suppliers, we offer a range of development and evaluation tools for our microcontrollers. For the most current listing, please visit www.nxp.com/microcontrollers.

P89V52X2 selection guide

Type	Memory		I/O pins	Enhanced UART	Max. operating frequency (6 clocks, MHz)		Max. operating frequency (12 clocks, MHz)		Temperature range (°C)	Package
	Flash	RAM			4.5 – 5.5 V	2.7 – 5.5 V	4.5 – 5.5 V	2.7 – 5.5 V		
P89V52X2FA	8 K	256 B	32	•	28	24	37	31	-40 to +85	PLCC44
P89V52X2FBD	8 K	256 B	32	•	28	24	37	31	-40 to +85	LQFP44
P89V52X2FN	8 K	256 B	32	•	28	24	37	31	-40 to +85	DIP40

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