

NXP low-power DP-to-HDMI active level shifter PTN3363

# Enhanced DP-to-HDMI connectivity for 3G, 3D, and 4K x 2K applications

As part of NXP's industry-leading family of high-performance, robust DisplayPort-to-HDMI interface solutions, this high-speed device provides exceptional signal conditioning with low active and standby power consumption in systems that support HDMI1.4B (3G, 3D, 4K x 2K).

#### **KEY FEATURES**

- ▶ DP++ interface connectivity to host CPU/GPU
- ▶ TMDS signaling/operation up to 3.4 Gbps
- ▶ Configurable receive equalization to compensate for channel attenuation
- ▶ Resistor-adjustable output signal swing
- ▶ Integrated DDC ROM for HDMI dongles
- ▶ Low active power: 72 mW
- Very low standby power: 410 μW
- ▶ Application-friendly HVQFN32 package (5 mm x 5 mm)
- ▶ Industrial temperature range: -40 to 105 °C

### **KEY APPLICATIONS**

- ▶ Notebook, desktop, and tablet PCs for 3G, 3D, and 4K x 2K formats
- ▶ Dongles and adapters
- ▶ Embedded systems
- Video and digital cameras, camcorders, and other portable systems

The NXP PTN3363 is a low-power, high-speed active level shifter that converts four lanes of low-swing AC-coupled differential input signals to DVI v1.0 and HDMI v1.4b compliant open-drain current-steering differential output signals. The device is capable of up to 3.4 Gbps per lane to support 36-bit deep color mode, 4K x 2K video formats, and 3D video data transport.

Each of the four lanes provides a level-shifting differential active buffer, with built-in equalization, to translate from low-swing AC-coupled differential signaling on the source side to TMDS-type DC-coupled differential current-mode signaling, terminated into 50  $\Omega$  to 3.3 V, on the sink side.

Additionally, the PTN3363 provides a single-ended active buffer for voltage translation of the HPD signal, from 5 V on the sink side to 3.3 V on the source side, and provides a channel with active buffering and level shifting of the DDC channel (consisting of a clock and a data line) between the 3.3 V source and 5 V sink. The DDC channel is implemented using active I<sup>2</sup>C-bus buffer technology that provides re-driving and level shifting.



The I<sup>2</sup>C buffer also disables the clock and data lines by isolating between the source and sink.

channel losses to deliver an HDMI output that meets HDMI compliance and achieves good system interoperability.

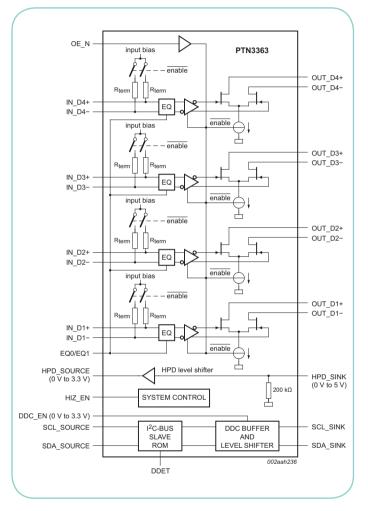
## LOW-POWER ARCHITECTURE

The active level-shifting function used by the PTN3363 offers enhanced capabilities for signal conditioning and, at the same time, optimizes power consumption.

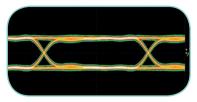
## **CLEAN HDMI OUTPUT**

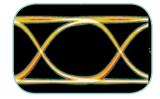
The PTN3363 reduces inter-symbol interference (ISI) and

## PTN3363 block diagram



# PTN3363 eye diagrams at 3 Gbps

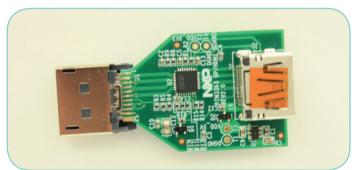




PTN3363 in DP-to-HDMI dongle



## PTN3363 DP-to-HDMI dongle board



# **Ordering information**

For questions, e-mail interface.support@nxp.com

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature (T <sub>amb</sub> )
PTN3363BS	PTN3363BSMP	HVQFN32	Reel 13" Q2/T3 *standard mark SMD dry pack	6000	-40 °C to +105 °C

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