Designer Resource. Accelerate. Simplify.

Issue 5, Version 2
November 2010

Beyond Bits

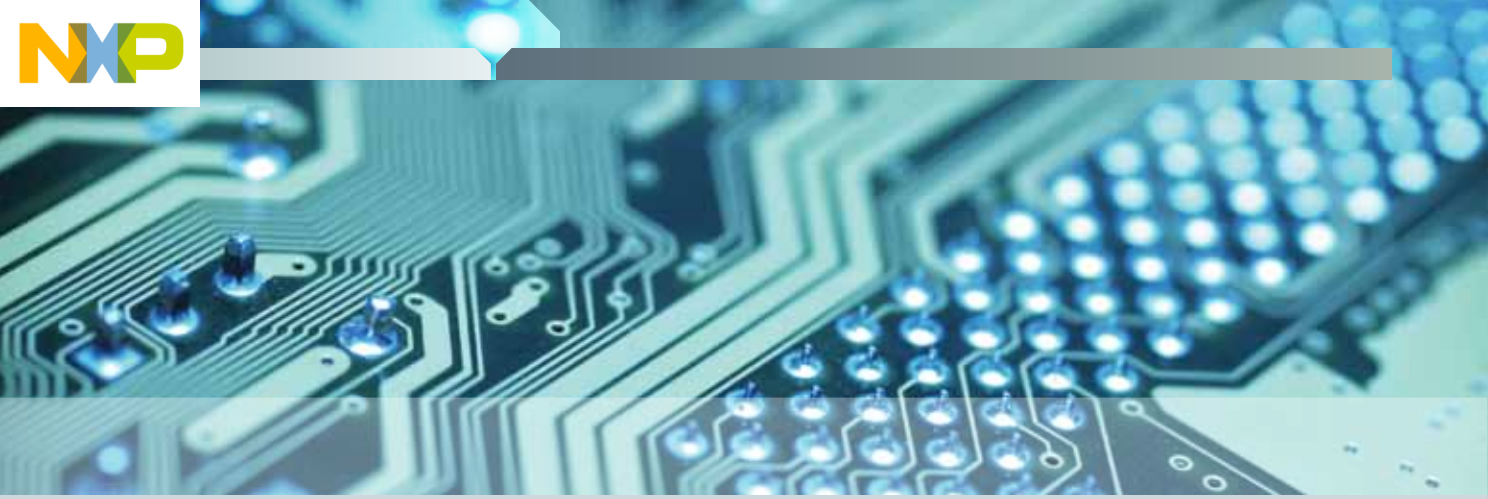
Next-Generation Microcontrollers

INTRODUCING

ColdFire+ Family

Kinetis Family

freescale™ semiconductor



Issue 5

Beyond Bits

Building the industry's most trusted MCUs

Welcome to the exciting fifth edition of *Beyond Bits*. We're introducing two new microcontroller lines to help realize your most innovative ideas.

The Freescale ColdFire+ and Kinetis 32-bit MCU families expand your choices, regardless of core or architecture preference, and help you design more optimized products. Built from 90nm thin-film storage (TFS) flash technology, our new MCUs feature unique FlexMemory capability, a powerful array of mixed-signal analog peripherals and the latest ultra-low-power technology. Bundled with the latest Eclipse-based CodeWarrior Development Studio, MQX™ RTOS and the modular Tower System, we help you design more quickly and easily.

In addition to these two new lines, our extensive range of 8-, 16- and 32-bit MCUs offer MCU solutions you can trust. You can count on us to deliver industry-leading vertical solutions, scalable product lines, intellectual property and process technology roadmaps, outstanding technical support and a broad range of devices available for a minimum period of 10 years. We've worked hard to create a seamless design environment where you can easily scale from 8-bit to 32-bit, between architectures, re-using code and developing with the same tools.

This fifth edition focuses on product family details and key technical highlights of these new MCU families. And you won't want to miss these details—we've packed some exciting new features onto these parts, including the best in low power, connectivity, HMI and security innovation.

Overall, we're adding hundreds of new 32-bit MCUs to help fuel your imagination and inspire your next design.

Enjoy this edition.

Regards,

Reza Kazerounian
Senior Vice President, Microcontroller Solutions Group

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Issue 5

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

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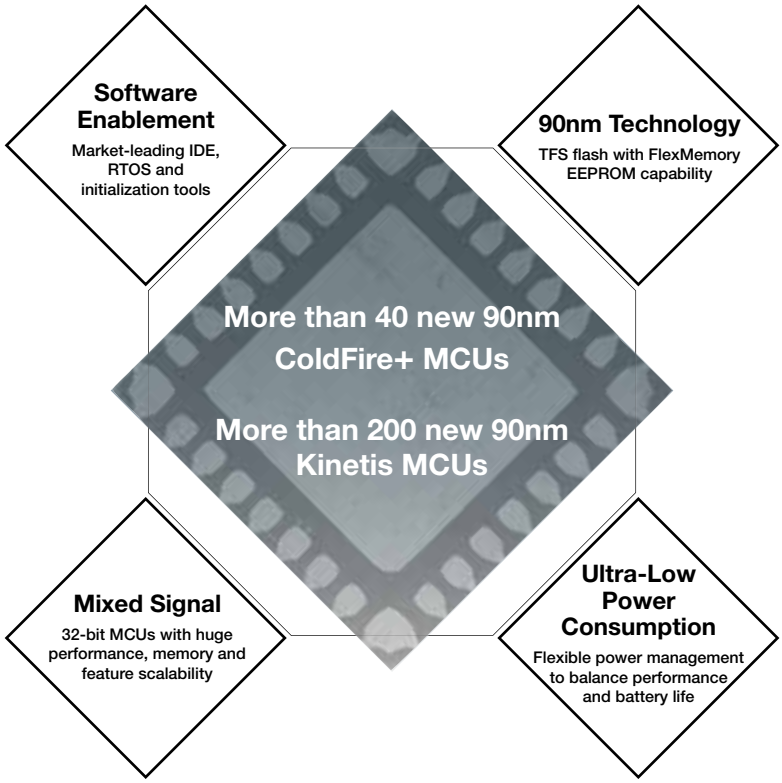
Portfolio Overview

Next-generation 32-bit microcontrollers

Freescale's 32-bit industrial and consumer microcontrollers are evolving into a new era enabled by innovative 90nm thin-film storage (TFS) flash memory technology with FlexMemory. The result? Hundreds of new mixed-signal MCUs with performance, memory and feature scalability, and a market-leading enablement bundle that delivers a one-stop-shop solution for MCUs, development tools and runtime software.

Freescale has combined its innovative IP, flash technology and platform-based design capability into a portfolio of devices that are solutions-focused and core-agnostic. The new 32-bit ColdFire+ MCU families are built using the ColdFire V1 core. The new Kinetis MCU families are built using the ARM® Cortex™-M4 core. Both families share the same software enablement, the same low-power flexibility and offer consistent peripherals—making it simple to pick the best solution for your end application.



ColdFire+ Microcontrollers

Design Innovation. Accelerated.

Application-oriented solutions with increased integration, ultra-low power and optimized cost.

ColdFire+ MCUs build upon the ColdFire architecture's strong heritage and signify the next step in the evolution of ColdFire MCUs. ColdFire+ MCUs add several impressive new features:

- FlexMemory, configurable embedded EEPROM
- Additional application-specific peripherals for consumer goods, appliances and smart metering
- High-precision, high-performance mixed-signal capability
- Incredible low-power features, with run currents down to 150 µA/MHz

The MCF51Qx/Jx families are the first ColdFire+ products that combine cutting-edge low-power performance with a diverse set of analog, connectivity and security peripherals, all packaged in low cost, small footprint packages. These are only the beginning of the next round of investment in the future of ColdFire.

Kinetis Microcontrollers

Design Potential. Realized.

Market-leading mixed-signal integration, scalable performance and ultra-low power.

Complementing Freescale's ARM based i.MX MPU products, Kinetis represents the most scalable portfolio of mixed-signal ARM Cortex-M4 MCUs in the industry. By offering ARM microcontrollers in addition to our existing ColdFire solutions and MCUs built on Power Architecture® technology, Freescale is focused on delivering the best hardware and software solution available in the marketplace—regardless of core architecture preference.

Freescale will deliver over 200 new Kinetis MCUs with scalable performance, memory and feature integration over the course of the next 18 months. The benefits are obvious: designers can select the part they need while knowing they can also quickly adjust to market changes. Pin compatibility, peripheral compatibility and software compatibility allow maximum reuse while minimizing design time and cost.

Built upon the ARM Cortex-M4 core, Kinetis MCUs share the same FlexMemory configurable EEPROM capability, mixed-signal integration and low-power IP strengths as their ColdFire+ cousins, but add additional connectivity, human-machine interface and safety and security functionality. The first phase of the Kinetis portfolio consists of five compatible MCU families that take MCU scalability and integration to the next level. Additional families with application-focused peripheral sets are currently in design and will be available throughout 2011.

Comprehensive Enablement

Time to market in 32-bit MCU design increasingly depends on software development and the expectation that silicon vendors will provide complete enablement solutions. Freescale recognizes this and has enabled ColdFire+ and Kinetis MCUs with a powerful set of common software and hardware development tools. Freescale plans to deliver and support CodeWarrior for Microcontrollers v10.x (Eclipse™) IDE with Processor Expert, the most advanced tool of its kind, along with the complimentary Freescale MQX™ RTOS for both ColdFire+ and ARM Cortex-M4 solutions. Kinetis MCUs also have the full support of the expansive ARM ecosystem, including IAR and Keil™. The Freescale enablement offering, combined with the full support of the ARM ecosystem, provides a pathway for quick design and reduced design headaches. The Freescale Tower rapid prototyping system completes the offering by providing unlimited quick prototyping capabilities, eliminating months of development time.

ColdFire+ Microcontrollers


Design Innovation. Accelerated.



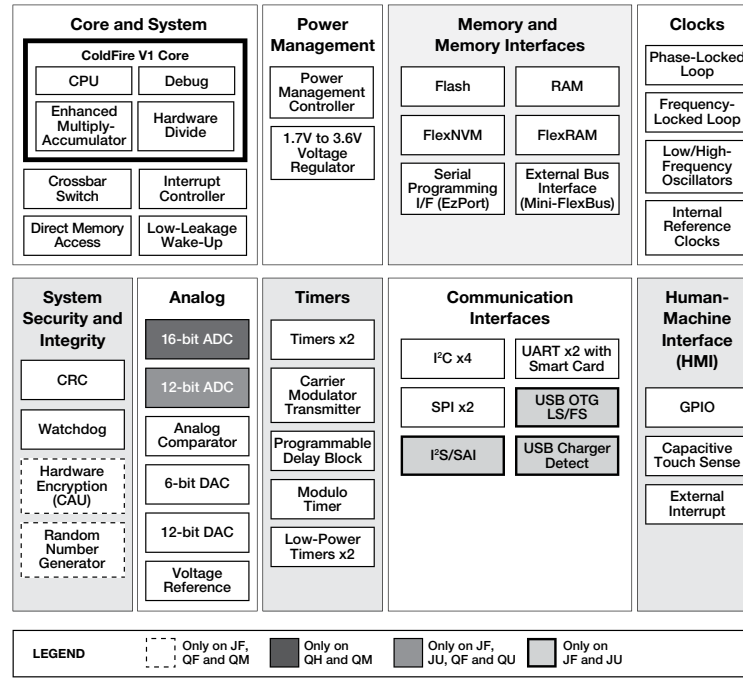
ColdFire+ V1 Microcontrollers

For secure ultra-low-power applications

The ColdFire+ Qx and Jx families combine cutting-edge low-power performance with a diverse set of analog, connectivity and security peripherals, all packaged in cost-effective, small footprint packages. Six families are built from 90nm thin-film storage flash technology with FlexMemory. Features common to all six families include 32 KB–128 KB of flash, up to 32 KB of FlexMemory (2 KB EEPROM), flash programming and peripheral operation from 1.71V to 3.6V, 10 low-power modes, a low-power touch-sensing interface, 12-bit DAC and a range of serial communications interfaces and timers. This rich set of features makes the ColdFire+ Qx/Jx families ideal for cost- and space-constrained consumer and industrial applications ranging from portable hand-held devices to wireless sensing nodes.

The six scalable ColdFire+ families consist of the MCF51QU, MCF51QH, MCF51QF and MCF51QM, and the MCF51JU and MCF51JF devices. All families are software and pin-to-pin compatible, allowing easy migration between devices to take advantage of additional memory and functionality.

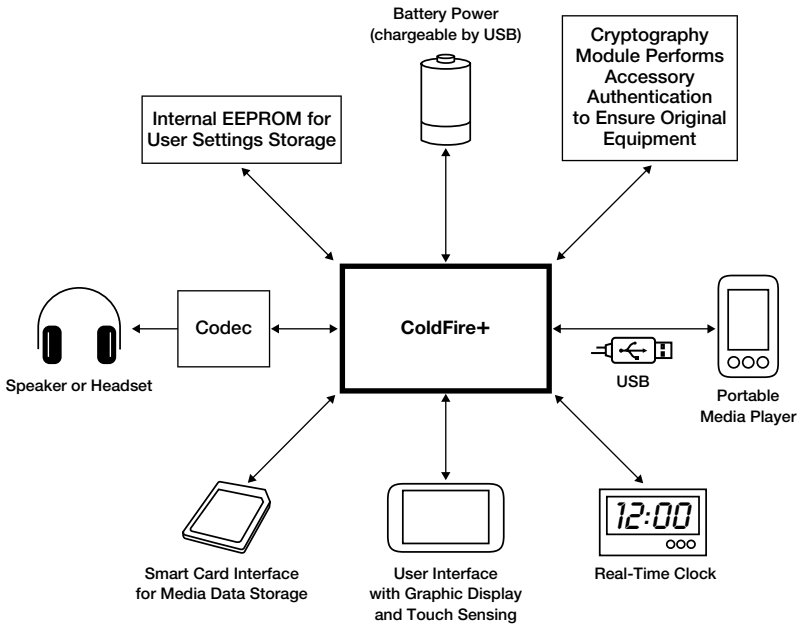
ColdFire+ Jx/Qx Families



Performance

- 50 MHz ColdFire V1 core + eMAC + hardware divide
- 4-channel DMA for peripheral and memory servicing with reduced CPU loading and faster system throughput
- Cross bar switch enables concurrent multi-master bus access, increasing bus bandwidth
- Independent flash banks, allowing concurrent code execution and firmware updating with no performance degradation or complex coding routines

Portable Media Player Device Accessory



Ultra-Low Power

- 10 low-power modes with power and clock gating for optimal peripheral activity and recovery times. Stop currents of <500 nA, run currents of 150 uA/MHz, 4 µs wake-up from stop mode
- Full flash programming and analog operation down to 1.71V for extended battery life
- Low-leakage wake-up unit with up to four internal modules and 16 pins as wake-up sources in low-leakage stop (LLS)/very low-leakage stop (VLLS) modes
- Two low-power timers for continual system operation in reduced power state

Flash SRAM and FlexMemory

- 32 KB to 128 KB flash
- 8 KB to 32 KB of RAM
- FlexMemory: Up to 2 KB of user-segmentable byte write/erase EEPROM for data tables/system data. Over 4.4M write/erase cycles with 100 µsec write time (brownouts without data loss or corruption). No user or system intervention to complete programming and erase functions and full operation down to 1.71V. In addition, FlexNVM up to 32 KB for extra program code, data or EEPROM backup

Continued on next page

ColdFire+ V1 Qx Family

An incredibly cost-effective, ultra-low-power, mixed-signal microcontroller family ideal for secure portable or battery-powered applications.

Target applications

- Wireless sensor nodes
- Security control pads
- Video game accessories

MCF51QH 16-bit ADC	**MCF51QM** Encryption 16-bit ADC
MCF51QU 12-bit ADC	**MCF51QF** Encryption 12-bit ADC

ColdFire+ V1 Jx Family

Ideal for portable consumer devices, the ColdFire+ Jx family adds USB On-The-Go (OTG) capability and a serial audio interface to the ColdFire+ Qx family.

Target applications

- Secure, low-power iPod accessories
- USB audio bridges
- PC peripherals
- High-end remote controls

MCF51JU USB OTG 12-bit ADC	**MCF51JF** USB OTG 12-bit ADC Encryption

Continued from previous page

Mixed-Signal Capability

- High-speed 12/16-bit ADC with configurable resolution. Single or differential output mode operation for improved noise rejection. 500 ns conversion time achievable with programmable delay block triggering
- 12-bit DAC for analog waveform generation for audio applications
- High-speed comparators provide fast and accurate motor over-current protection by driving PWMs to a safe state
- Accurate on-chip voltage reference eliminates need for accurate external voltage reference IC, reducing overall system cost

Connectivity and Communications

- USB 2.0 OTG and device charger detect optimizes charging current/time for portable USB devices, enabling longer battery life. Integrated USB low-voltage regulator supplies up to 120 mA off chip at 3.3V to power external components
- Two UARTs with ISO7816 smart card support. Variety of data size, format and transmission/reception settings supported for multiple industrial communication protocols
- Inter-IC Sound (I²S) interface for audio system interfacing
- Two SPI and up to four I²C

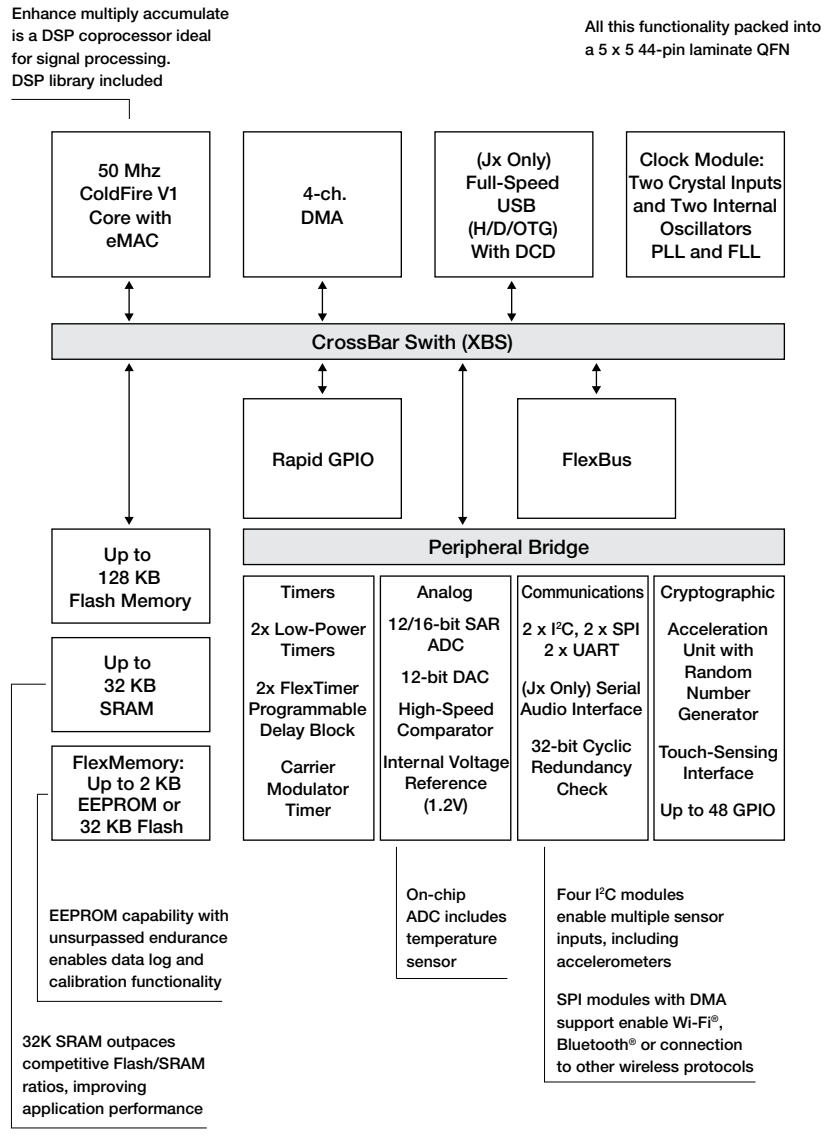
Human-Machine Interface

- Xtrinsic low-power touch-sensing interface with up to 16 inputs. Operates in all low power modes (minimum current adder when enabled). Hardware implementation avoids software polling method. High sensitivity level allows use of overlay surfaces and robust performance in noisy environments

Timing and Control

- Up to two FlexTimers with a total of eight channels. Hardware dead-time insertion and quadrature decoding for motor control
- Carrier modulator timer generates infrared waveforms for remote control applications

Smart Sensor Node



ColdFire+ Features Options

Family	CPU Frequency (MHz)	Memory									Feature Options										Packages				
		Flash (KB)	FlexNVM (KB)	SRAM (KB)	eMAC + HDIV	ADC	DAC	High-Speed Comparator	Touch-Sensing Interface	USB/OTG (LS/FS)	Cryptographic Acceleration Unit	FlexTimer	Low-Power Timer	Carrier Modulator Transmitter	Programmable Delay Block	UART	SPI	I²C	I²S	External Bus Interface	32OFN (5x5mm)	44OFN (5x5mm)	48LOFP (7x7mm)	64OFN (9x9mm)	64LOFP (10x10mm)
Qx	50	32	16	8	√	Up to 16-bit	12-bit	Up to 2	Up to 7		optional	Up to 7 ch	2	√	√	2	2	3		44-pin only	√	√			
		64	32	16	√	Up to 16-bit	12-bit	2	Up to 8		optional	7 ch	2	√	√	2	2	3		√		√	√		
		128	32	8	√	Up to 16-bit	12-bit	Up to 4	16		optional	Up to 8 ch	2	√	√	2	2	44-pin only		√		√		√	√
Jx	50	32	16	16	√	12-bit	12-bit	Up to 2	Up to 7	√	optional	Up to 7 ch	2	√	√	2	2	3	√	44-pin only	√	√			
		64	32	32	√	12-bit	12-bit	2	Up to 8	√	optional	7 ch	2	√	√	2	2	3	√	√		√	√		
		128	32	32	√	12-bit	12-bit	Up to 4	16	√	optional	Up to 8 ch	2	√	√	2	2	44-pin only	√	√		√		√	√

Reliability, Safety and Security

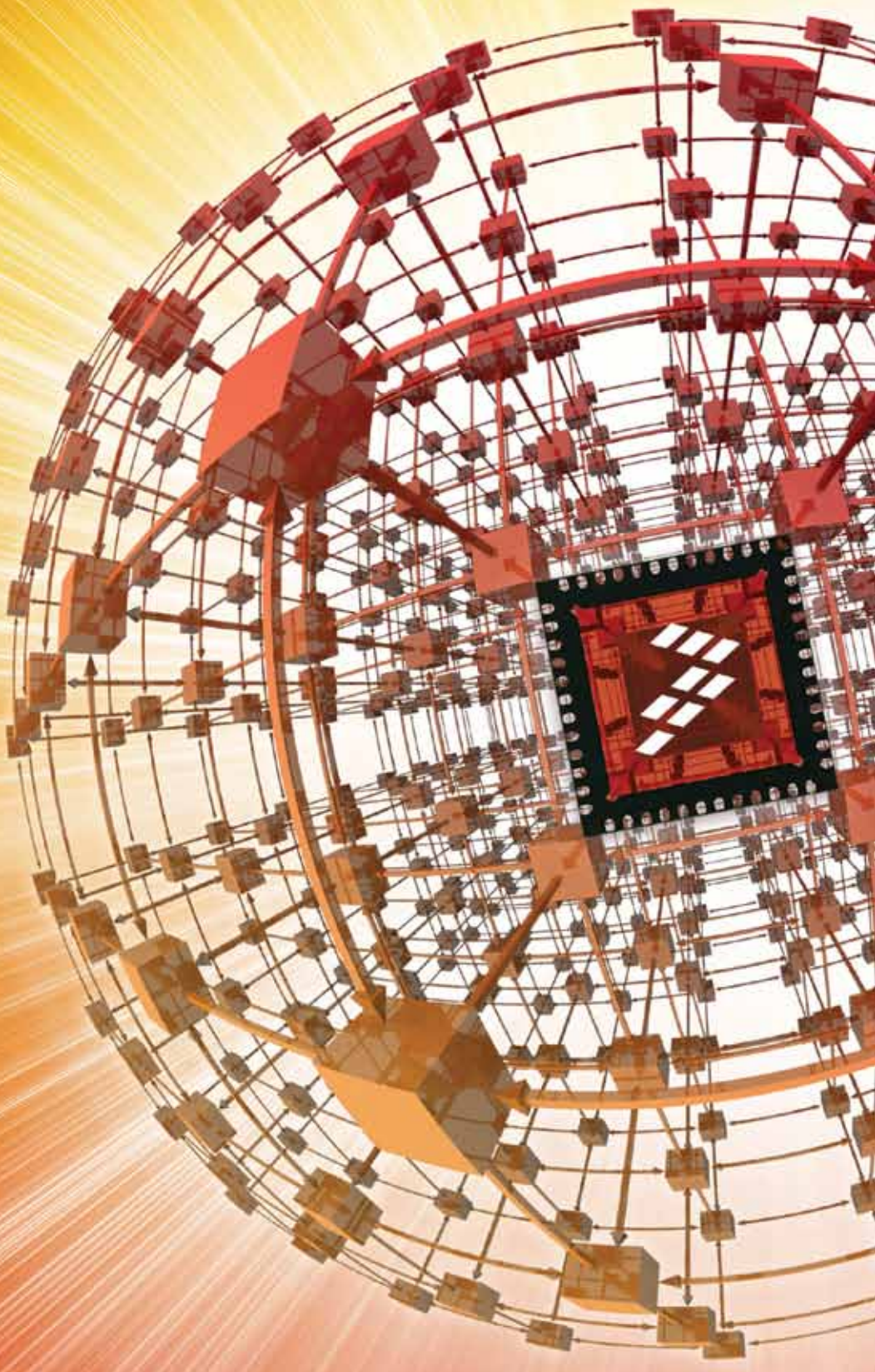
- Encryption coprocessor for secure data transfer and storage. Faster than software implementations with wide algorithm support for DES, 3DES, AES, MD5, SHA-1 and SHA-256
- Cyclic redundancy check engine validates memory contents and communication data, increasing system reliability
- Independent-clocked COP guards against clock skew or code runaway for fail-safe applications

External Peripheral Support

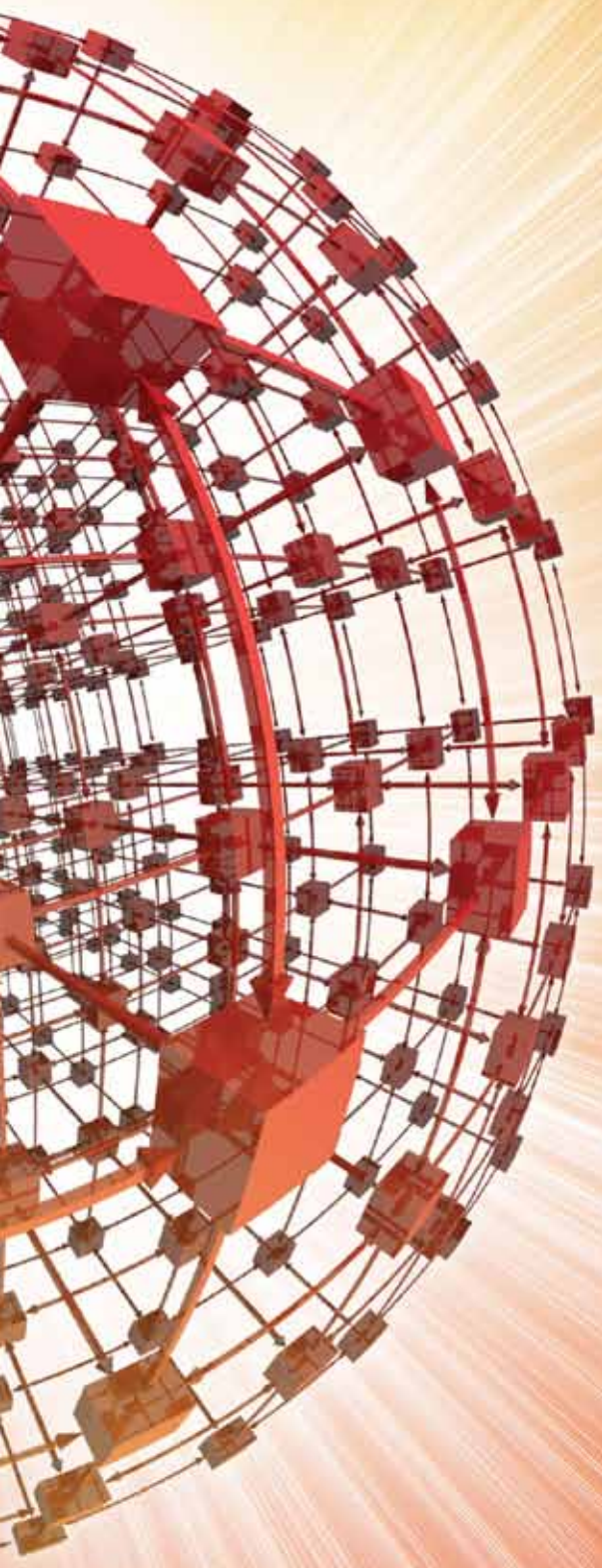
- Mini-FlexBus external bus interface provides interface options to peripherals such as graphics displays. Supports up to two chip selects

Tools and Software

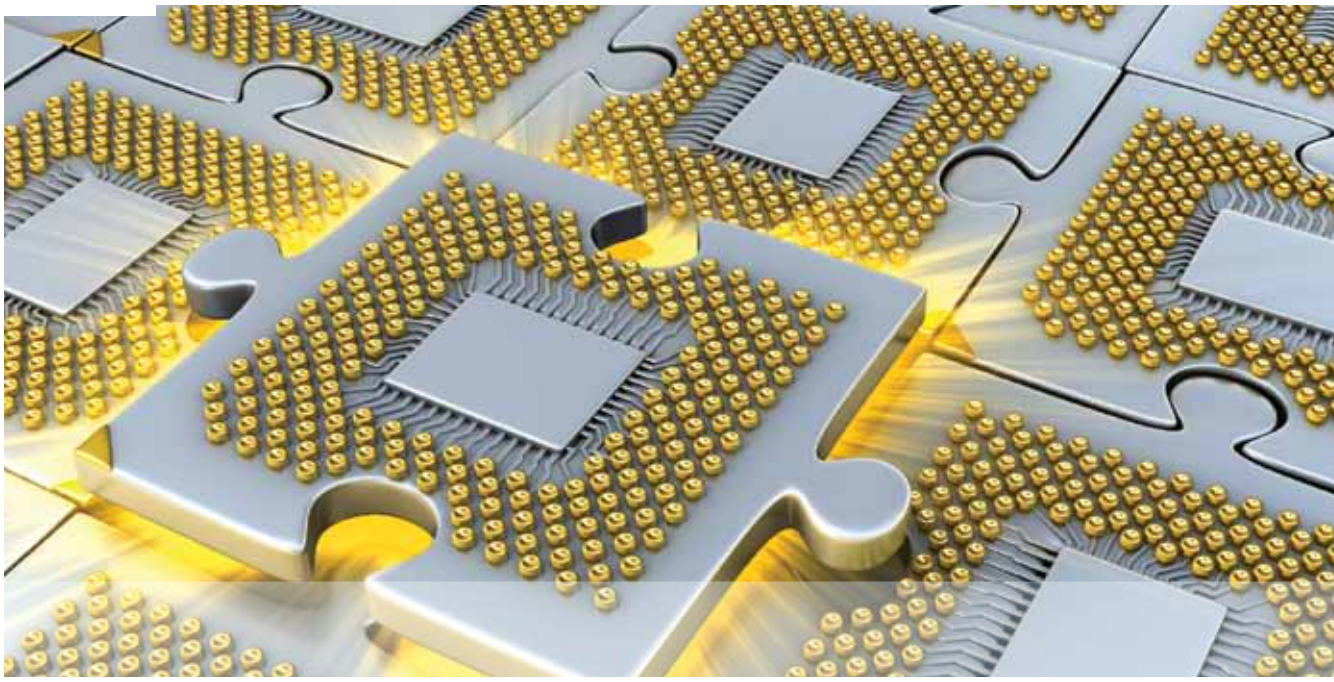
- Freescale Tower System hardware development environment
- Integrated development environments
  - CodeWarrior for Microcontrollers v10.x (Eclipse) IDE with Processor Expert
  - IAR Embedded Workbench
  - CodeSourcery Sourcery G++ (GNU)
- Runtime software and RTOS
  - DSP and encryption libraries
  - Complimentary bare-metal/no OS USB stack with PHDC, MSC, CDC, HID class and more
  - Complimentary Freescale Embedded GUI (eGUI) software driver for graphics LCD panels
  - Complimentary bootloaders (USB, RF, serial)
  - Complimentary Freescale MQX RTOS, USB stack and MFS filesystem
  - Micrium uC/OS-III
  - Express Logic ThreadX
  - SEGGER embOS
  - freeRTOS



Kinetis Microcontrollers



Design Potential. Realized.



Kinetis Microcontrollers

Software-enabled MCU platforms

ARM Cortex microcontrollers are on the move. Kinetis is the first broad-market mixed-signal MCU family based on the new ARM Cortex-M4 core and the most scalable portfolio of mixed-signal ARM Cortex-M4 MCUs in the industry.

The Kinetis portfolio consists of multiple hardware- and software-compatible MCU families with exceptional low-power performance, memory scalability including on-chip FlexMemory/EEPROM, and peripheral integration. Families range from entry-level to highly integrated and include a wide selection of analog, human-machine interface, connectivity, and safety and security functions.

With Kinetis, value isn't confined just to the MCU. A powerful suite of enablement software comes standard from Freescale. Add to this a large and well-established software and tool ecosystem from numerous ARM third parties and the result is a portfolio of MCU platforms that delivers exceptional flexibility and value for designers of industrial and consumer end products.

The platform approach offers a number of benefits for the embedded designer:

Match MCU capabilities to application requirements

Select features as needed while knowing there are paths for future expansion or cost reduction.

Reuse hardware and software across multiple end products

Minimize development costs, learning curves and time to market.

Quickly adjust to market changes in feature requirements

Create super-set or sub-set products with a single MCU portfolio.

Meeting the Needs of the Embedded Designer

Wide Selection of Scalable MCUs from One Supplier

The first phase of the Kinetis MCU portfolio contains five compatible MCU families. Five performance options are available from 50 to 150 MHz with flash memory ranging from 32 KB to 1 MB and high RAM-to-flash ratios throughout. Common peripherals, memory maps and packages both within and across MCU families allow for easy migration to greater/less memory and functionality.

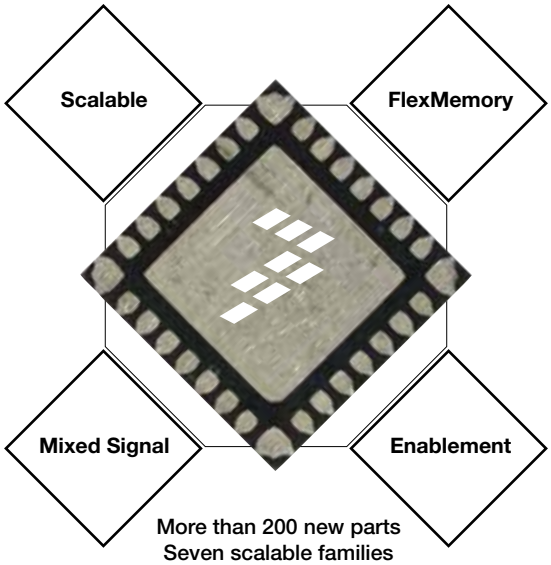
Mixed-Signal Capability for Signal Conditioning, Conversion and Analysis

Kinetis MCUs are rich in mixed-signal capability. Features include multiple high-speed, high-precision 16-bit ADCs, 12-bit DACs, high-speed comparators, and programmable gain amplifiers. With analog integration at this level typically requiring a multi-chip solution, Kinetis MCUs offer the added benefits of reduced system cost and integration effort.

Ultra-Low-Power Performance for Extended Battery Life

Kinetis MCUs feature the best in low-power innovation, including ten flexible low-power operating modes for power profile optimization, power and clock gating, back-biasing, 4µS wake up times, flash programming and analog peripheral operation down to 1.71V and stop and run currents of <500 nA and <200 µA/MHz respectively. A low-power RTC and low-leakage wake-up unit add further flexibility, while a low-power timer enables continual system operation in reduced power states.

Kinetis Family Key Attributes



FlexMemory: Fast, Flexible, High-Endurance On-Chip EEPROM

Freescale's new FlexMemory technology provides an extremely versatile and powerful solution for designers seeking on-chip EEPROM and/or additional program or data flash memory. As easy and as fast as SRAM, it requires no user or system intervention to complete programming and erase functions when used as high endurance byte-write/byte-erase EEPROM. EEPROM array size can also be configured for improved endurance to suit application requirements. FlexMemory can also provide additional flash memory (FlexNVM) for data or program storage in parallel with the main program flash. The user can configure several parameters including EEPROM size, endurance, write size, and the size of additional program/data flash. On larger memory variants, endurance figures of over 10M write/erase cycles can be achieved. In comparison with traditional EEPROM solutions, FlexMemory offers a number of benefits, including greater endurance, faster write/erase times, lower voltage operation and user segmentation. Being on-chip it also eliminates the costs associated with using external EEPROM ICs and the the software headaches and CPU/flash/RAM resource impact encountered with EEPROM emulation schemes.

Fast, Robust Flash Memory

Freescale's 90nm thin-film storage (TFS) flash memory delivers industry-leading reliability and tolerance to charge loss, full flash programming and analog peripheral operation down to 1.71V, significantly reduced run and standby currents, and fast access times. Excellent area efficiency maximizes on-chip feature integration across flash densities, while independent flash banks enable simultaneous code execution and firmware updating without any performance degradation or complex software routines.

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One-Stop Enablement Offering—MCU + IDE + RTOS

Kinetis MCUs come with a complimentary full-featured MQX RTOS and bundled CodeWarrior for Microcontrollers v10.x (Eclipse) IDE with Processor Expert. A selection of connectivity, motor control, LCD and security stacks and drivers are also offered as well as a range of tools from IAR, KEIL and other ARM third-party vendors. Kinetis MCUs are supported by Freescale's Tower System, a rapid prototyping development platform that maximizes hardware reuse and speeds time to market.

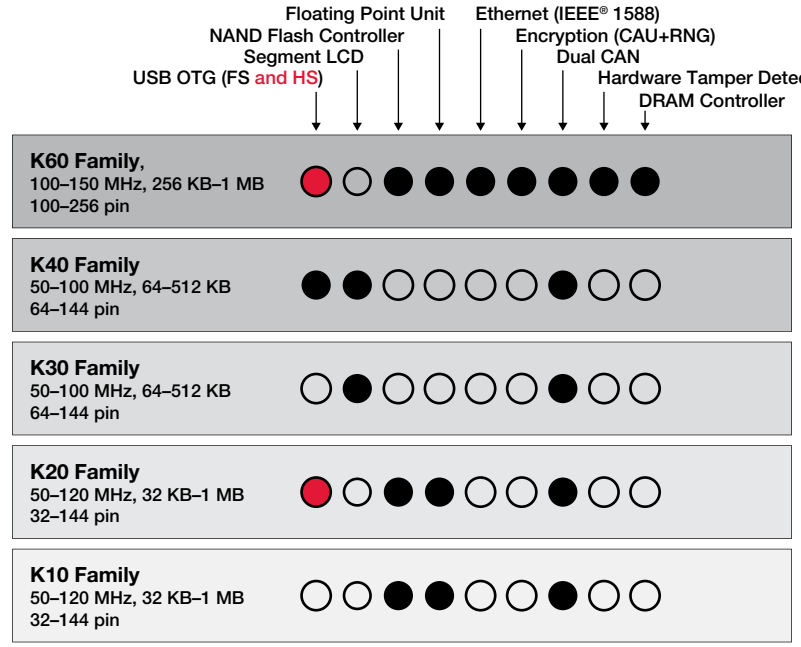
Powerful Processing Capability

Kinetis MCUs feature the new ARM Cortex-M4 core. The ARM Cortex-M4 core retains all the advantages of the ARM Cortex-M3 core and adds new digital signal processing capability in the form of DSP extensions, a single cycle MAC unit and an optional single precision floating point unit. In addition, Freescale has added a direct memory access (DMA) controller, cross bar switch and optional on-chip cache memory which maximize bus bandwidth and flash execution performance, allowing CPU frequencies of up to 150 MHz.

Multiple Timers for Advanced Motor Control

Kinetis MCUs contain multiple FlexTimer modules for a wide range of control applications, including motor control with hardware dead-time insertion and quadrature decoding. A carrier modulator transmitter for generating infrared waveforms for remote control applications is standard on all devices.

Kinetis MCU Families



Common System IP	Common Analog IP	Common Digital IP	Development Tools
32-bit ARM® Cortex™-M4 Core w/DSP Instructions	16-bit ADC	Hardware Cyclic Redundancy Check	Bundled IDE w/Processor Expert
FlexMemory w/ EEPROM Capability	Programmable Gain Amplifiers	I²C	Bundled OS (USB, TCP/IP, Security)
Next-Generation Flash Memory High Reliability, Fast Access	12-bit DAC	I²S	Modular Tower Hardware Development System
Low-Voltage, Low-Power Multiple Operating Modes, Clock Gating (1.71V–3.6V w/5V Tolerant I/0)	High-Speed Comparators	UART/SPI	Application Software Stacks, Peripheral Drivers and App. Libraries (Motor Control, HMI, USB)
Memory Protection Unit	Low-Power Touch Sensing	Programmable Delay Block	Broad Third-Party Ecosystem
DMA		External Bus Interface	
SRAM		Motor Control Timers	
		Secure Digital Host Controller	
		RTC	

Connectivity and Communication Interfaces

Kinetis MCUs feature a number of connectivity peripherals, including USB 2.0 (full- and high-speed) device/host/On-The-Go with device charger detect capability, Ethernet with IEEE® 1588 hardware time stamping for real-time industrial control and a multitude of serial interfaces, including UARTs with support for ISO7816 SIM/smart cards and IrDA interfaces. An Inter-IC Sound (I^2S) serial interface supports the integration of audio processing hardware, while dual CAN modules enable industrial network bridging.

Sophisticated Human-Machine Interfaces

Human-machine interface options start with an Xtrinsic low-power touch-sensing interface (TSI). This provides a modern upgrade from mechanical to touch keypad, rotary and slider user interfaces and operates in all low-power modes. A flexible low-power segment LCD controller is offered on specific families with up to 512 KB flash and includes reduced power operation and segment failure detection capability. At the higher end of the portfolio a graphics LCD controller supports up to QVGA resolution in single-chip configuration, or up to SVGA resolution using external memory. In addition to the graphical user interface options, the DSP capability of the ARM Cortex-M4 core combined with the I^2S interface enable voice and audio user interface options.

Reliability, Safety and Security

Kinetis MCUs include a variety of data integrity and security hardware for safeguarding memory, communication and system data. A cyclic redundancy check module is available for validating memory contents and communication data, while a memory protection unit provides data protection and increased software reliability. For fail-safe applications an independently clocked watchdog offers protection against code runaway. When it comes to security, a hardware encryption unit supports several encryption and hashing algorithms for program validation as well as authentication and securing data for transfer and storage. The system security module included on high-end MCU families includes a unique chip identifier, secure key storage and a hardware tamper detection system. The tamper detection system has integrated sensors for voltage, frequency, temperature and external sensing for physical attack detection.

Support for External Peripherals and Memory

Kinetis MCUs can interface to a variety of external peripherals and memories for system expansion and data storage. A secure digital host controller supports SD, SDIO, MMC or CE-ATA cards for in-application software upgrades, media files, or adding Wi-Fi® support. For interfacing to external peripherals such as graphics displays, a FlexBus external bus interface is provided. NAND flash and DRAM controllers allow the connection of a wide variety of memory types.

Value

Kinetis MCUs offer exceptional value with 10K starting prices from $0.99 for 32 KB flash memory devices in a 32-pin package.

Kinetis Product Families

The first five general-purpose Kinetis MCU families are scheduled to sample in late 2010 with production planned for early 2011. Additional families with application-specific peripherals sets will follow throughout 2011.

All Kinetis families are built around a common set of system, analog and digital IP blocks. The level of peripheral integration within each family increases with flash memory size and pin count. Families are distinguishable by their performance, memory and peripheral capabilities as shown in the figure on page 12.

Kinetis K10 Family

Low-power, mixed-signal MCUs

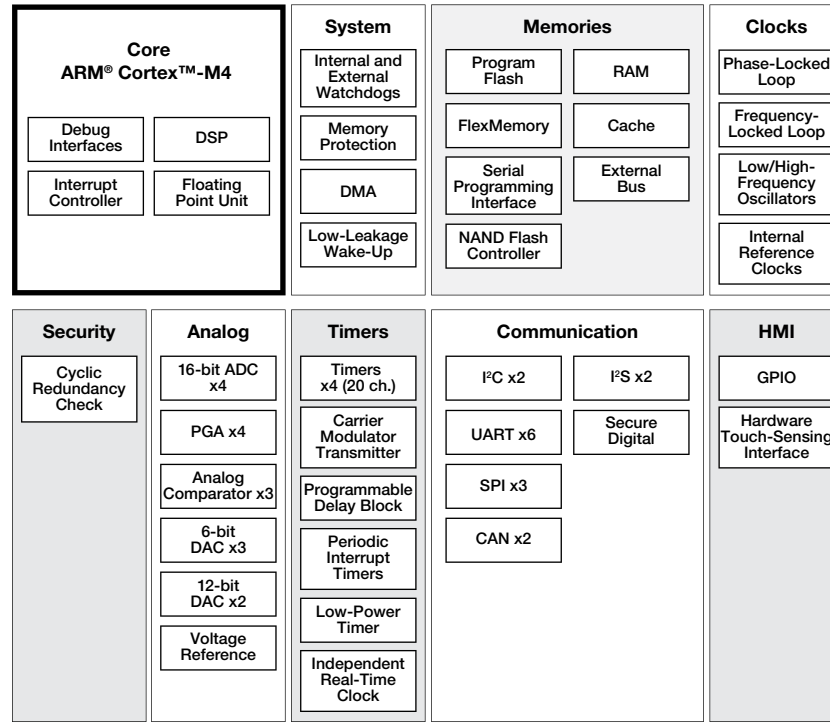
Overview

The K10 MCU family is the entry point into the Kinetis portfolio. Devices start from 32 KB of flash in a small-footprint 5 x 5 mm 32 QFN package extending up to 1 MB in a 144MAPBGA package with a rich suite of analog, communication, timing and control peripherals.Additionally, pin compatibility, flexible low-power capabilities and innovative FlexMemory help to solve many of the major pain points for system implementation.

Ultra-Low Power

- 10 low-power modes with power and clock gating for optimal peripheral activity and recovery times. Stop currents of <500 nA, run currents of <200 uA/MHz, 4 µs wake-up from stop mode
- Full flash programming and analog peripheral operation down to 1.71V for extended battery life
- Low-leakage wake-up unit with up to eight internal modules and sixteen pins as wake-up sources in low-leakage stop (LLS)/very low-leakage stop (VLLS) modes
- Low-power timer for continual system operation in reduced power state

Kinetis K10 Family



K10 Family Summary

Part Numbers	CPU (MHz)	Memory				Feature Options									Packages										
		Flash (KB)	FlexMemory (KB)	SRAM (KB)	Cache (KB)	Single Precision Floating Point Unit	CAN	Memory Protection Unit	Secure Digital Host Controller	NAND Flash Controller	External Bus Interface	12-bit Digital to Analog Converter	Programmable Gain Amplifier	5V Tolerant I/O	32QFN (5x5 mm)	48QFN (7x7 mm)	48LQFP (7x7 mm)	64QFN (9x9 mm)	64LQFP (10x10 mm)	80LQFP (12x12 mm)	81BGA (8x8 mm)	100LQFP (14x14 mm)	104BGA (8x8 mm)	144LQFP (20x20 mm)	144BGA (13x13 mm)
MK10N32Vyy50	50	32	-	8											FM	FT	LF	FX	LH	LK	MB				
MK10N64Vyy50	50	64	-	16											FM	FT	LF	FX	LH	LK	MB				
MK10X32Vyy50	50	32	32	8											FM	FT	LF	FX	LH	LK	MB				
MK10X64Vyy50	50	64	32	16											FM	FT	LF	FX	LH	LK	MB				
MK10X128Vyy50	50	128	32	32			√				√	√	√	√				FX	LH	LK	MB	LL	ML		
MK10X128Vyy72	72	128	32	32			√				√	√	√	√				FX	LH	LK	MB	LL	ML		
MK10X256Vyy72	72	256	32	64			√				√	√	√	√						LK	MB	LL	ML		
MK10X128Vyy100	100	128	128	32			√	√	√		√	√	√	√										LQ	MD
MK10X256Vyy100	100	256	256	64			√	√	√		√	√	√	√										LQ	MD
MK10N512Vyy100	100	512	-	128			√	√	√		√	√	√	√						LK	MB	LL	ML	LQ	MD
MK10X512Vyy120	120	512	512	128	16	√	√	√	√	√	√	√	√	√										LQ	MD
MK10N1M0Vyy120	120	1024	-	128	16	√	√	√	√	√	√	√	√	√										LQ	MD

For details of peripherals offered on specific devices, please refer to the family product brief document at freescale.com.
yy = package designator noted in the "Packages" column

Flash, SRAM and FlexMemory

- 32 KB–1 MB flash. Fast access, high reliability with 4-level security protection
- 8 KB–128 KB of SRAM
- FlexMemory: 32 bytes–16 KB of user-segmentable byte write/erase EEPROM for data tables/system data. EEPROM with over 10M cycles and flash with 100 µsec write time (brownouts without data loss or corruption). No user or system intervention to complete programming and erase functions and full operation down to 1.71V. In addition, FlexNVM from 32 KB–512 KB for extra program code, data or EEPROM backup

Mixed-Signal Capability

- Up to four high-speed 16-bit ADCs with configurable resolution. Single or differential output mode operation for improved noise rejection. 500 ns conversion time achievable with programmable delay block triggering
- Up to two 12-bit DACs for analog waveform generation for audio applications
- Up to three high-speed comparators providing fast and accurate motor over-current protection by driving PWMs to a safe state
- Up to four programmable gain amplifiers with x64 gain for small amplitude signal conversion
- Accurate on-chip voltage reference eliminates need for accurate external voltage reference IC reducing overall system cost

Performance

- ARM Cortex-M4 core + DSP. 50–120 MHz, single cycle MAC, single instruction multiple data (SIMD) extensions, optional single precision floating point unit
- Up to 32-channel DMA for peripheral and memory servicing with reduced CPU loading and faster system throughput
- Cross bar switch enables concurrent multi-master bus accesses, increasing bus bandwidth
- Up to 16 KB of instruction/data cache for optimized bus bandwidth and flash execution performance
- Independent flash banks allowing concurrent code execution and firmware updating with no performance degradation or complex coding routines

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Timing and Control

- Up to four FlexTimers with a total of 20 channels. Hardware dead-time insertion and quadrature decoding for motor control
- Carrier modulator timer for infrared waveform generation in remote control applications
- Four-channel 32-bit periodic interrupt timer provides time base for RTOS task scheduler or trigger source for ADC conversion and programmable delay block

Human-Machine Interface

- Xtrinsic low power touch-sensing interface with up to 16 inputs. Operates in all low-power modes (minimum current adder when enabled). Hardware implementation avoids software polling method. High sensitivity level allows use of overlay surfaces up to 5 mm thick

Connectivity and Communications

- Up to six UARTs, with IrDA support including one UART with ISO7816 smart card support. Variety of data size, format and transmission/reception settings supported for multiple industrial communication protocols
- Up to two Inter-IC Sound (I^2S) serial interfaces for audio system interfacing
- Up to two CAN modules for industrial network bridging
- Up to three DSPI and two I^2C

Reliability, Safety and Security

- Memory protection unit provides memory protection for all masters on the cross bar switch, increasing software reliability
- Cyclic redundancy check engine validates memory contents and communication data, increasing system reliability
- Independent-clocked COP guards against clock skew or code runaway for fail-safe applications such as the IEC 60730 safety standard for household appliances
- External watchdog monitor drives output pin to safe state external components if watchdog event occurs

External Peripheral Support

- FlexBus external bus interface provides interface options to memories and peripherals such as graphics displays. Supports up to six chip selects
- Secure digital host controller supports SD, SDIO, MMC or CE-ATA cards for in-application software upgrades, media files or adding Wi-Fi support
- NAND flash controller supports up to 32-bit ECC current and future NAND types. ECC management handled in hardware, minimizing software overhead

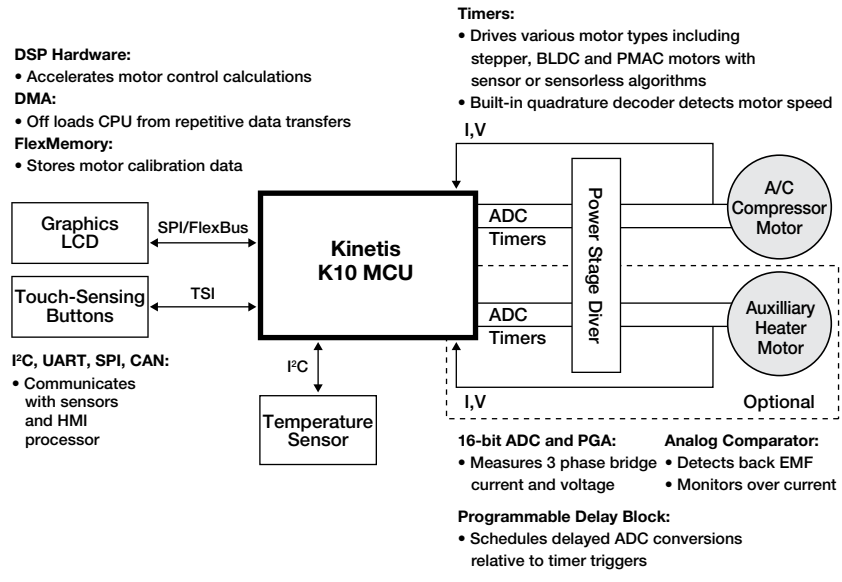
Target Applications

- Remote sensors
- HVAC systems
- Gaming controllers
- Flow meters

Tools and Software

- Freescale Tower System hardware development environment
- Integrated development environments
  - CodeWarrior for Microcontrollers v10.x (Eclipse) IDE with Processor Expert
  - IAR Embedded Workbench
  - Keil MDK
  - CodeSourcery Sourcery G++ (GNU)
- Runtime software and RTOS
  - Math, DSP and encryption libraries
  - Motor control libraries
  - Complimentary bootloaders (USB, Ethernet, RF, serial)
  - Complimentary Freescale embedded GUI (eGUI) software driver for graphics LCD panels
  - Complimentary Freescale MQX
  - Cost-effective Nano™ SSL/Nano™ SSH for Freescale MQX RTOS
  - Micrium uC/OS-III
  - Express Logic ThreadX
  - SEGGER embOS
  - freeRTOS
  - Mocana (security)
- Plus full ARM ecosystem

K10 Family: HVAC System



Kinetis K20 Family

Low-power MCUs with USB On-The-Go

Overview

The K20 MCU family is pin, peripheral and software compatible with the K10 MCU family and adds full and high-speed USB 2.0 On-The-Go with device charger detect capability. Devices start from 32 KB of flash in 5 x 5 mm 32QFN packages extending up to 1 MB in a 144MAPBGA package with a rich suite of analog, communication, timing and control peripherals. High memory density K20 family devices include a single precision floating point unit and NAND flash controller.

Connectivity and Communications

- USB 2.0 On-The-Go and device charger detect optimizes charging current/time for portable USB devices, enabling longer battery life. Integrated USB low-voltage regulator supplies up to 120 mA off chip at 3.3V to power external components from 5V input. Up to 480 Mbps with external ULPI PHY
- Up to six UARTs with IrDA support, including one UART with ISO 7816 smart card support. Variety of data size, format and transmission/reception settings supported for multiple industrial communication protocols

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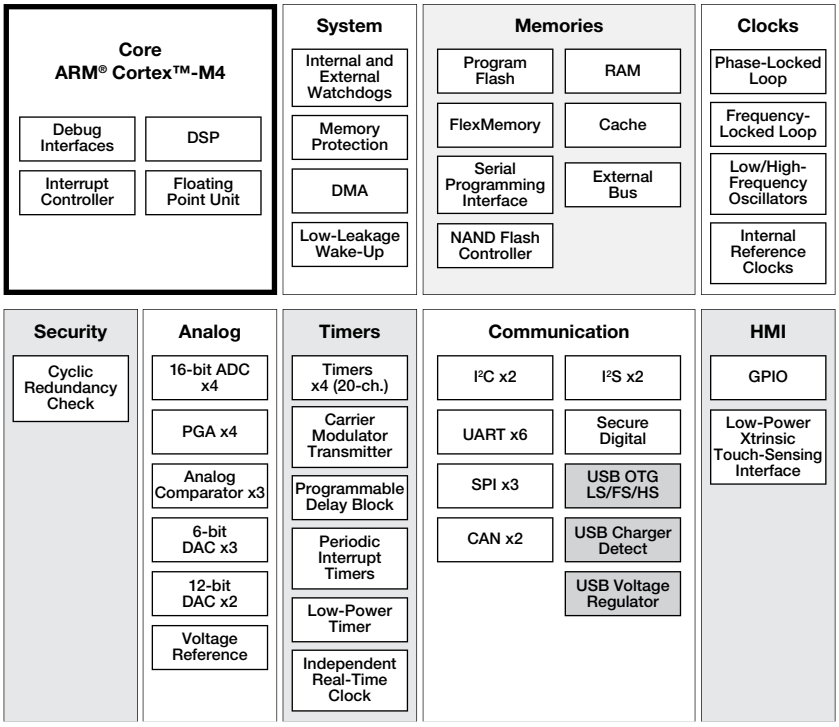
Kinetis K20 Family



K20 Family Summary

Part Numbers	CPU (MHz)	Memory				Feature Options										Packages										
		Flash (KB)	FlexMemory (KB)	SRAM (KB)	Cache (KB)	Single Precision Floating Point Unit	CAN	Memory Protection Unit	Secure Digital Host Controller	NAND Flash Controller	External Bus Interface	12-bit Digital to Analog Converter	Programmable Gain Amplifier	5V Tolerant I/O	Other	32QFN (5x5 mm)	48QFN (7x7 mm)	48LQFP (7x7 mm)	64QFN (9x9 mm)	64LQFP (10x10 mm)	80LQFP (12x12 mm)	81BGA (8x8 mm)	100LQFP (14x14 mm)	104BGA (8x8 mm)	144LQFP (20x20 mm)	144BGA (13x13 mm)
MK20N32Vyy50	50	32	-	8											USB OTG (FS)	FM	FT	LF	FX	LH	LK	MB				
MK20N64Vyy50	50	64	-	16											USB OTG (FS)	FM	FT	LF	FX	LH	LK	MB				
MK20X32Vyy50	50	32	32	8											USB OTG (FS)	FM	FT	LF	FX	LH	LK	MB				
MK20X64Vyy50	50	64	32	16											USB OTG (FS)	FM	FT	LF	FX	LH	LK	MB				
MK20X128Vyy50	50	128	32	32			√				√	√	√	√	USB OTG (FS)				FX	LH	LK	MB	LL	ML		
MK20X128Vyy72	72	128	32	32			√				√	√	√	√	USB OTG (FS)				FX	LH	LK	MB	LL	ML		
MK20X256Vyy72	72	256	32	64			√				√	√	√	√	USB OTG (FS)						LK	MB	LL	ML		
MK20X128Vyy100	100	128	128	32			√	√	√		√	√	√	√	USB OTG (FS)										LQ	MD
MK20X256Vyy100	100	256	256	64			√	√	√		√	√	√	√	USB OTG (FS)										LQ	MD
MK20N512Vyy100	100	512	-	128			√	√	√		√	√	√	√	USB OTG (FS)						LK	MB	LL	ML	LQ	MD
MK20X512Vyy120	120	512	512	128	16	√	√	√	√	√	√	√	√	√	USB OTG (FS & HS)										LQ	MD
MK20N1M0Vyy120	120	1024	-	128	16	√	√	√	√	√	√	√	√	√	USB OTG (FS & HS)										LQ	MD

For details of peripherals offered on specific devices, please refer to the family product brief document at freescale.com.
yy = package designator noted in the "Packages" column

Continued from previous page

- Inter-IC Sound (I^2S) serial interface for audio system interfacing
- Up to two CAN for industrial network bridging
- Up to three DSPI and two I^2C

Flash, SRAM and FlexMemory

- 32 KB–1 MB flash. Fast access, high reliability with four-level security protection
- 8 KB–128 KB of SRAM
- FlexMemory: 32 bytes–16 KB of user-segmentable byte write/erase EEPROM for data tables/system data. EEPROM with over 10M cycles and flash with 100 µsec write time (brown-outs without data loss or corruption). No user or system intervention to complete programming and erase functions and full operation down to 1.71V. In addition, FlexNVM from 32 KB–512 KB for extra program code, data or EEPROM backup

Mixed-Signal Capability

- Up to four high-speed 16-bit ADCs with configurable resolution. Single or differential output mode operation for improved noise rejection. 500 ns conversion time achievable with programmable delay block triggering
- Up to two 12-bit DACs for analog waveform generation for audio applications
- Up to three high-speed comparators providing fast and accurate motor over-current protection by driving PWMs to a safe state
- Up to two programmable gain amplifiers with x64 gain for small amplitude signal conversion
- Accurate on-chip voltage reference eliminates need for accurate external voltage reference IC reducing overall system cost

Performance

- ARM Cortex-M4 core + DSP. 50–120 MHz, single cycle MAC, single instruction multiple data (SIMD) extensions, single precision floating point unit
- Up to 32-channel DMA for peripheral and memory servicing with reduced CPU loading and faster system throughput
- Cross bar switch enables concurrent multi-master bus accesses, increasing bus bandwidth
- Up to 16 KB of instruction/data cache for optimized bus bandwidth and flash execution performance
- Independent flash banks allowing concurrent code execution and firmware updating with no performance degradation or complex coding routines

Human-Machine Interface

- Xtrinsic low-power touch-sensing interface with up to 16 inputs. Operates in all low-power modes (minimal current adder when enabled). Hardware implementation avoids software polling method. High sensitivity level allows use of overlay surfaces up to 5 mm thick

Ultra-Low Power

- 10 low-power modes with power and clock gating for optimal peripheral activity and recovery times. Stop currents of <500 nA and run currents of <200 uA/MHz, 4 µs wake-up from stop mode
- Full flash programming and analog peripheral operation down to 1.71V for extended battery life
- Low-leakage wake-up unit with up to eight internal modules and sixteen pins as wake-up sources in low-leakage stop (LLS)/very low-leakage stop (VLLS) modes
- Low-power timer for continual system operation in reduced power state

Target Applications

- Barcode scanners
- Portable media players
- Printers
- Programmable logic controllers

Timing and Control

- Up to four FlexTimers with a total of 20 channels. Hardware dead-time insertion and quadrature decoding for motor control
- Carrier modulator timer for infrared waveform generation in remote control applications
- Four-channel 32-bit periodic interrupt timer provides time base for RTOS task scheduler or trigger source for ADC conversion and programmable delay block

Reliability, Safety and Security

- Memory protection unit provides memory protection for all masters on cross bar switch, increasing software reliability
- Cyclic redundancy check engine validates memory contents and communication data, increasing system reliability
- Independent-clocked COP guards against clock skew or code runaway for fail-safe applications, e.g. IEC 60730
- External watchdog monitor drives output pin to safe state external components if watchdog event occurs

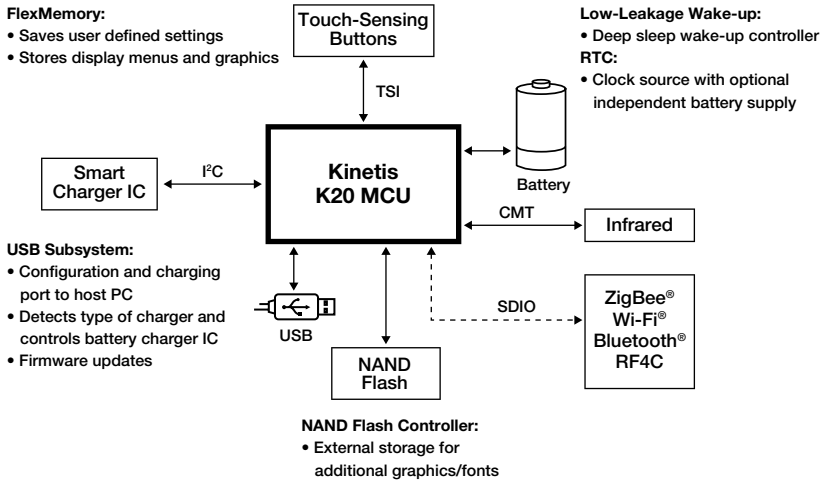
External Peripheral Support

- FlexBus external bus interface provides interface options to memories and peripherals such as graphics displays. Supports up to six chip selects
- Secure digital host controller supports SD, SDIO, MMC or CE-ATA cards for in-application software upgrades, media files or adding Wi-Fi support
- NAND flash controller supports up to 32-bit ECC current and future NAND types. ECC management handled in hardware, minimizing software overhead

Tools and Software

- Freescale Tower System hardware development environment
- Integrated development environments
  - CodeWarrior for Microcontrollers v10.x (Eclipse) IDE with Processor Expert
  - IAR Embedded Workbench
  - Keil MDK
  - CodeSourcery Sourcery G++ (GNU)
- Runtime software and RTOS
  - Math, DSP and encryption libraries
  - Motor control libraries
  - Complimentary bootloaders (USB, Ethernet, RF, serial)
  - Complimentary Freescale embedded GUI (eGUI) software driver for graphics LCD panels
  - Complimentary Freescale MQX
  - Cost-effective Nano SSL/Nano SSH for Freescale MQX RTOS
  - Micrium uC/OS-III
  - Express Logic ThreadX
  - SEGGER embOS
  - freeRTOS
  - Mocana (security)
- Plus full ARM ecosystem

K20 Family: Universal Remote Control





Kinetis K30 Family

Low-power MCUs with segment LCD

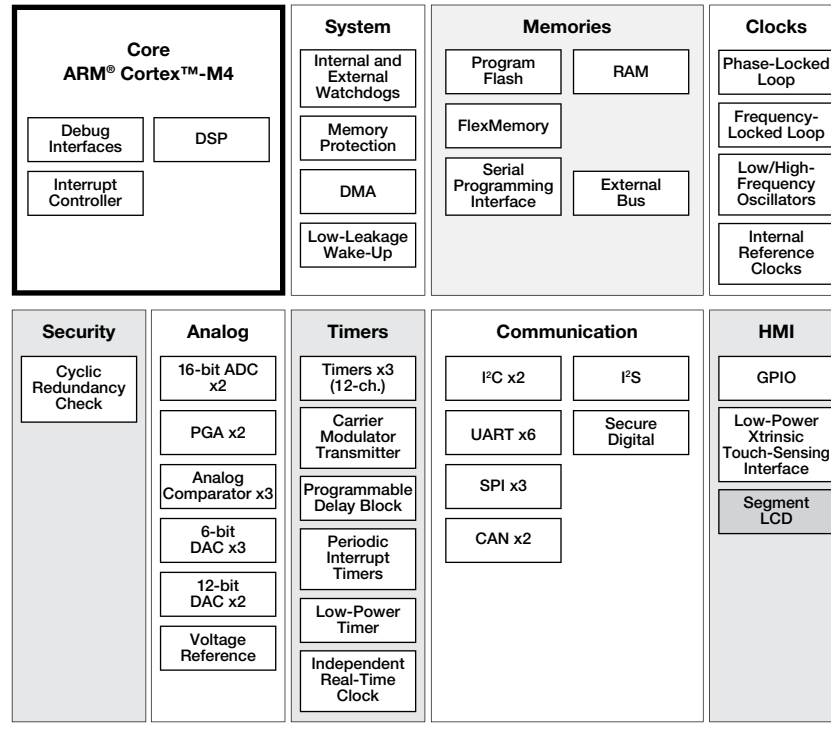
Overview

The K30 MCU family is pin, peripheral and software compatible with the K10 MCU family and adds a flexible low-power segment LCD controller with support for up to 320 segments. Devices start from 64 KB of flash in 64QFN packages extending up to 512 KB in a 144MAPBGA package with a rich suite of analog, communication, timing and control peripherals.

Human-Machine Interface

- Xtrinsic low-power touch-sensing interface with up to 16 inputs. Operates in all low-power modes (minimal current adder when enabled). Hardware implementation avoids software polling method. High sensitivity level allows use of overlay surfaces up to 5 mm thick

Kinetis K30 Family



K30 Family Summary

Part Numbers	CPU (MHz)	Memory			Feature Options								Packages							
		Flash (KB)	FlexMemory (KB)	SRAM (KB)	CAN	Memory Protection Unit	Secure Digital Host Controller	External Bus Interface	12-bit Digital to Analog Converter	Programmable Gain Amplifier	5V Tolerant I/O	Other	64QFN (9x9 mm)	64LQFP (10x10 mm)	80LQFP (12x12 mm)	81BGA (8x8 mm)	100LQFP (14x14 mm)	104BGA (8x8 mm)	144LQFP (20x20 mm)	144BGA (13x13 mm)
MK30X64Vyy50	50	64	32	16	N/A				√	√	√	Segment LCD (up to 25x8/29x4)	FX	LH	LK	MB				
MK30X128Vyy50	50	128	32	32	√				√	√	√	Segment LCD (up to 36x8/40x4)	FX	LH	LK	MB	LL	ML		
MK30X128Vyy72	72	128	32	32	√				√	√	√	Segment LCD (up to 36x8/40x4)	FX	LH	LK	MB	LL	ML		
MK30X256Vyy72	72	256	32	64	√				√	√	√	Segment LCD (up to 36x8/40x4)			LK	MB	LL	ML		
MK30X128Vyy100	100	128	128	32	√	√	√	√	√	√	√	Segment LCD (40x8/44x4)							LQ	MD
MK30X256Vyy100	100	256	256	64	√	√	√	√	√	√	√	Segment LCD (40x8/44x4)							LQ	MD
MK30N512Vyy100	100	512	-	128	√	√	√	√	√	√	√	Segment LCD (up to 40x8/44x4)			LK	MB	LL	ML	LQ	MD

For details of peripherals offered on specific devices, please refer to the family product brief document at freescale.com.
yy = package designator noted in the "Packages" column

- Flexible, low-power LCD controller with up to 320 segments (40x8 or 44x4). LCD blink mode enables low average power while remaining in low-power mode. Segment fail detect alerts the user to failures in the display which helps avoids the possibility of an erroneous readout in medical applications. Frontplane/backplane reassignment provides pin-out flexibility, easing PCB design, and allows LCD configuration changes via firmware with no hardware re-work. Supports multiple 3V and 5V LCD panel sizes with fewer segments (pins) than competitive controllers and no external components. Unused LCD pins can be configured as other GPIO functions

Ultra-Low Power

- 10 low-power modes with power and clock gating for optimal peripheral activity and recovery times. Stop currents of <500 nA and run currents of <200 uA/MHz, 4 µs wake-up from stop mode
- Full flash programming and analog peripheral operation down to 1.71V for extended battery life
- Low-leakage wake-up unit with up to eight internal modules and sixteen pins as wake-up sources in low-leakage stop (LLS)/very low-leakage stop (VLLS) modes
- Low-power timer for continual system operation in reduced power state

Flash, SRAM and FlexMemory

- 64 KB–512 KB flash. Fast access, high reliability with four-level security protection
- 16 KB–128 KB of SRAM
- FlexMemory: 32 bytes–4 KB of user-segmentable byte write/erase EEPROM for data tables/system data. EEPROM with over 10M cycles and flash with 100 µsec write time (brownouts without data loss/corruption). No user or system intervention to complete programming and erase functions and full operation down to 1.71V. In addition, FlexNVM from 32 KB–256 KB for extra program code, data or EEPROM backup

Performance

- ARM Cortex-M4 core + DSP. 50–100MHz, single cycle MAC, single instruction multiple data (SIMD) extensions
- Up to 16-channel DMA for peripheral and memory servicing with reduced CPU loading and faster system throughput
- Cross bar switch enables concurrent multi-master bus accesses, increasing bus bandwidth
- Independent flash banks allows concurrent code execution and firmware updating with no performance degradation or complex coding routines

Mixed-Signal Capability

- Up to two high-speed 16-bit ADCs with configurable resolution. Single or differential output mode operation for improved noise rejection. 500 ns conversion time achievable with programmable delay block triggering
- Up to two 12-bit DACs for analog waveform generation for audio applications
- Up to three high-speed comparators providing fast and accurate motor over-current protection by driving PWMs to a safe state
- Up to two programmable gain amplifiers with x64 gain for small amplitude signal conversion
- Accurate on-chip voltage reference eliminates need for accurate external voltage reference IC reducing overall system cost

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Timing and Control

- Up to three FlexTimers with a total of 12 channels. Hardware dead-time insertion and quadrature decoding for motor control
- Carrier modulator timer for infrared waveform generation in remote control applications
- Four-channel 32-bit periodic interrupt timer provides time base for RTOS task scheduler or trigger source for ADC conversion and programmable delay block

Connectivity and Communications

- Up to six UARTs with IrDA support, including one UART with ISO7816 smart card support. Variety of data size, format and transmission/reception settings supported for multiple industrial communication protocols
- Up to two Inter-IC Sound (I^2S) serial interfaces for audio system interfacing
- Up to two CAN for industrial network bridging
- Up to three DSPI and two I^2C

Target Applications

- Thermostats
- Smart meters
- Heart rate monitors
- Blood gas analyzers

Reliability, Safety and Security

- Memory protection unit provides memory protection for all masters on cross bar switch, increasing software reliability
- Cyclic redundancy check engine validates memory contents and communication data, increasing system reliability
- Independent-clocked COP guards against clock skew or code runaway for fail-safe applications, e.g. IEC60730
- External watchdog monitor drives output pin to safe state external components if watchdog event occurs

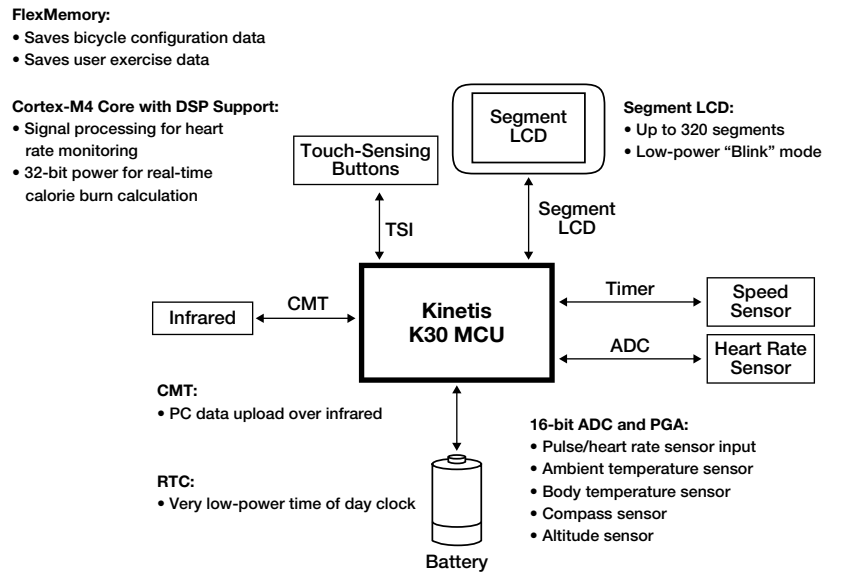
External Peripheral Support

- FlexBus external bus interface provides interface options to memories and peripherals such as graphics displays. Supports up to six chip selects
- Secure digital host controller supports SD, SDIO, MMC or CE-ATA cards for in-application software upgrades, media files or adding Wi-Fi support

Tools and Software

- Freescale Tower System hardware development environment
- Integrated development environments
  - CodeWarrior for Microcontrollers v10.x (Eclipse) IDE with Processor Expert
  - IAR Embedded Workbench
  - Keil MDK
  - CodeSourcery Sourcery G++ (GNU)
- Runtime software and RTOS
  - Math, DSP and encryption libraries
  - Motor control libraries
  - Complimentary bootloaders (USB, Ethernet, RF, serial)
  - Complimentary Freescale embedded GUI (eGUI) software driver for graphics LCD panels
  - Complimentary Freescale MQX
  - Cost-effective Nano SSL/Nano SSH for Freescale MQX RTOS
  - Micrium uC/OS-III
  - Express Logic ThreadX
  - SEGGER embOS
  - freeRTOS
  - Mocana (security)
- Plus full ARM ecosystem

K30 Family: Bicycle Trip Computer



Kinetis K40 Family

Low-power MCUs with USB and LCD

Overview

The K40 MCU family is pin, peripheral and software compatible with the K10 MCU family and adds full-speed USB 2.0 On-The-Go with device charger detect capability and a flexible low-power segment LCD controller with support for up to 320 segments. Devices start from 64 KB of flash in 64QFN packages extending up to 512 KB in a 144MAPBGA package with a rich suite of analog, communication, timing and control peripherals.

Connectivity and Communications

- USB 2.0 On-The-Go + device charger detect optimizes charging current/time for portable USB devices, enabling longer battery life. Integrated USB low-voltage regulator supplies up to 120 mA off chip at 3.3V to power external components from 5V input
- Up to six UARTs with IrDA support including one UART with ISO7816 smart card support. Variety of data size, format and transmission/reception settings supported for multiple industrial communication protocols

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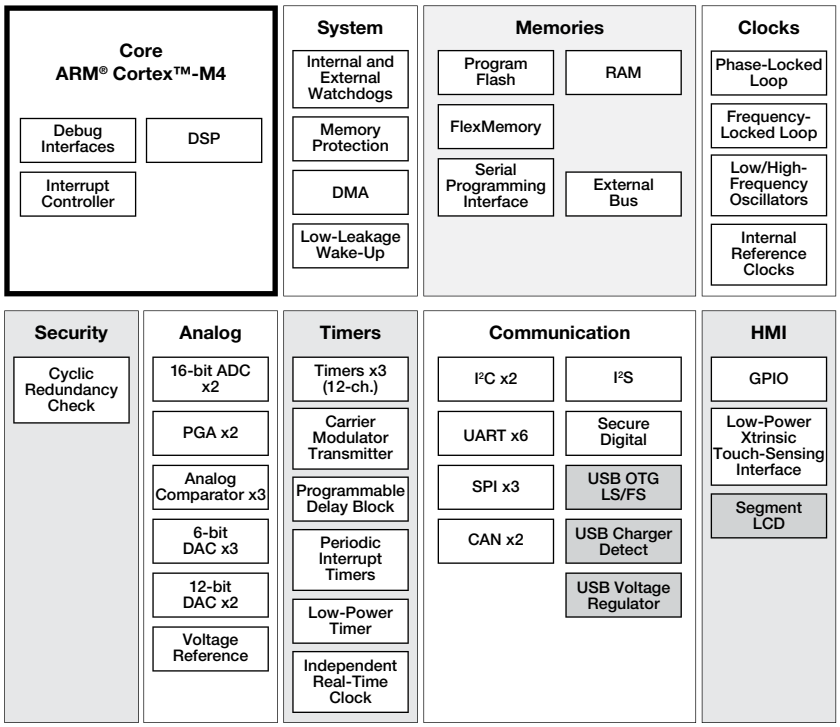
Kinetis K40 Family



K40 Family Summary

Part Numbers	CPU (MHz)	Memory			Feature Options								Packages							
		Flash (KB)	Flex Memory (KB)	SRAM (KB)	CAN	Memory Protection Unit	Secure Digital Host Controller	External Bus Interface	12-bit Digital to Analog Converter	Programmable Gain Amplifier	5V Tolerant I/O	Other	64QFN (9x9 mm)	64LQFP (10x10 mm)	80LQFP (12x12 mm)	81BGA (8x8 mm)	100LQFP (14x14 mm)	104BGA (10x10 mm)	144LQFP (20x20 mm)	144BGA (13x13 mm)
MK40X64Vyy50	50	64	32	16	no 64 pin				√	√	√	USB OTG (FS), Segment LCD (up to 25x8/29x4)	FX	LH	LK	MB				
MK40X128Vyy50	50	128	32	32	√				√	√	√	USB OTG (FS), Segment LCD (up to 36x8/40x4)	FX	LH	LK	MB	LL	ML		
MK40X128Vyy72	72	128	32	32	√				√	√	√	USB OTG (FS), Segment LCD (up to 36x8/40x4)	FX	LH	LK	MB	LL	ML		
MK40X256Vyy72	72	256	32	64	√				√	√	√	USB OTG (FS), Segment LCD (up to 36x8/40x4)			LK	MB	LL	ML		
MK40X128Vyy100	100	128	128	32	√	√	√	√	√	√	√	USB OTG (FS), Segment LCD (up to 40x8/44x4)							LQ	MD
MK40X256Vyy100	100	256	256	64	√	√	√	√	√	√	√	USB OTG (FS), Segment LCD (up to 40x8/44x4)							LQ	MD
MK40N512Vyy100	100	512	-	128	√	√	√	√	√	√	√	USB OTG (FS), Segment LCD (up to 40x8/44x4)			LK	MB	LL	ML	LQ	MD

For details of peripherals offered on specific devices, please refer to the family product brief document at freescale.com.
yy = package designator noted in the "Packages" column

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- Up to two Inter-IC Sound (I²S) serial interfaces for audio system interfacing
- Up to two CAN for industrial network bridging
- Up to three DSPI and two I²C

Human-Machine Interface

- Xtrinsic low-power touch-sensing interface with up to 16 inputs. Operates in all low-power modes (minimal current adder when enabled). Hardware implementation avoids software polling method. High sensitivity level allows use of overlay surfaces up to 5 mm thick
- Flexible, low-power LCD controller with up to 320 segments (40 x 8 or 44 x 4). LCD blink mode enables low average power while remaining in low-power mode. Segment fail detect alerts the user to failures in the display which helps avoids the possibility of an erroneous readout in medical applications. Frontplane/backplane reassignment provides pin-out flexibility, easing PCB design and allows LCD configuration changes via firmware with no hardware re-work. Supports multiple 3V and 5V LCD sizes with fewer segments (pins) than competitive controllers and no external components. Unused LCD pins can be configured as other GPIO functions

Flash, SRAM and FlexMemory

- 64 KB–512 KB flash. Fast access, high reliability with four-level security protection
- 16 KB–128 KB of SRAM
- FlexMemory: 32 bytes–4 KB of user-segmentable byte write/erase EEPROM for data tables/system data. EEPROM with over 10M cycles and flash with 100 µsec write time (brownouts without data loss/corruption). No user or system intervention to complete programming and erase functions and full operation down to 1.71V. In addition, FlexNVM from 32 KB–256 KB for extra program code, data or EEPROM backup

Performance

- ARM Cortex-M4 core + DSP. 50–100 MHz, single cycle MAC, single instruction multiple data (SIMD) extensions
- Up to 16-channel DMA for peripheral and memory servicing with reduced CPU loading and faster system throughput
- Cross bar switch enables concurrent multi-master bus accesses, increasing bus bandwidth
- Independent flash banks allow concurrent code execution and firmware updating with no performance degradation or complex coding routines

Mixed-Signal Capability

- Up to two high-speed 16-bit ADCs with configurable resolution. Single or differential output mode operation for improved noise rejection. 500 ns conversion time achievable with programmable delay block triggering
- Up to two 12-bit DACs for analog waveform generation for audio applications
- Up to three high-speed comparators providing fast and accurate motor over-current protection by driving PWMs to a safe state
- Up to two programmable gain amplifiers with x64 gain for small amplitude signal conversion
- Accurate on-chip voltage reference eliminates need for accurate external voltage reference IC reducing overall system cost

Timing and Control

- Up to three FlexTimers with a total of 12 channels. Hardware dead-time insertion and quadrature decoding for motor control
- Carrier modulator timer for infrared waveform generation in remote control applications
- Four-channel 32-bit periodic interrupt timer provides time base for RTOS task scheduler or trigger source for ADC conversion and programmable delay block

Ultra-Low Power

- 10 low-power modes with power and clock gating for optimal peripheral activity and recovery times. Stop currents of <500 nA and run currents of <200 uA/MHz, 4 µs wake-up from stop mode
- Full flash programming and analog peripheral operation down to 1.71V for extended battery life
- Low-leakage wake-up unit with up to eight internal modules and sixteen pins as wake-up sources in low-leakage stop (LLS)/very low-leakage stop (VLLS) modes
- Low-power timer with continual system operation in reduced power state

Reliability, Safety and Security

- Memory protection unit provides memory protection for all masters on cross bar switch, increasing software reliability
- Cyclic redundancy check engine validates memory contents and communication data, increasing system reliability
- Independent-clocked COP guards against clock skew or code runaway for fail-safe applications, e.g. IEC 60730
- External watchdog monitor drives output pin to safe state external components if watchdog event occurs

External Peripheral Support

- FlexBus external bus interface provides interface options to memories and peripherals such as graphics displays. Supports up to six chip selects
- Secure digital host controller supports SD, SDIO, MMC or CE-ATA cards for in-application software upgrades, media files or adding Wi-Fi support

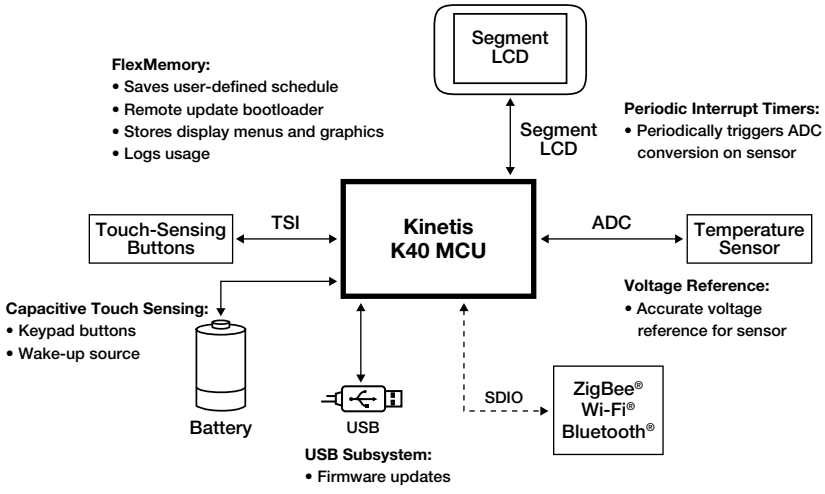
Target Applications

- GPS receivers
- Blood glucose meters
- Bike computers
- Currency counters

Tools and Software

- Freescale Tower System hardware development environment
- Integrated development environments
  - CodeWarrior for Microcontrollers v10.x (Eclipse) IDE with Processor Expert
  - IAR Embedded Workbench
  - Keil MDK
  - CodeSourcery Sourcery G++ (GNU)
- Runtime software and RTOS
  - Math, DSP and encryption libraries
  - Motor control libraries
  - Complimentary bootloaders (USB, Ethernet, RF, serial)
  - Complimentary Freescale embedded GUI (eGUI) software driver for graphics LCD panels
  - Complimentary Freescale MQX
  - Cost-effective Nano SSL/Nano SSH for Freescale MQX RTOS
  - Micrium uC/OS-III
  - Express Logic ThreadX
  - SEGGER embOS
  - freeRTOS
  - Mocana (security)
- Plus full ARM ecosystem

K40 Family: Thermostat





Kinetis K60 Family

Low-power MCUs with Ethernet and security

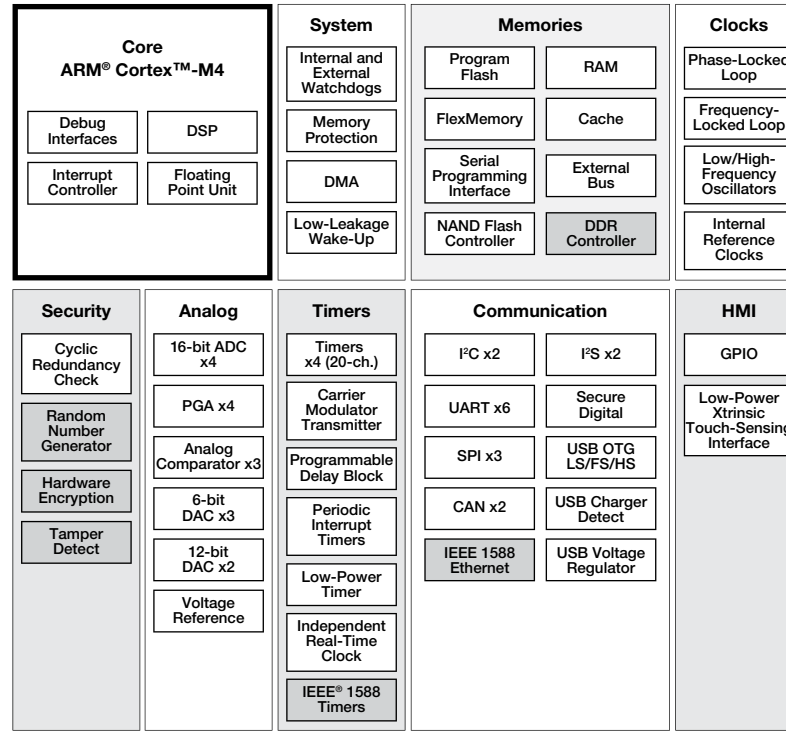
Overview

The K60 MCU family includes IEEE 1588 Ethernet, full- and high-speed USB 2.0 On-The-Go with device charger detect capability, hardware encryption and tamper detection capabilities. Devices start from 256 KB of flash in 100LQFP packages extending up to 1 MB in a 256MAPBGA package with a rich suite of analog, communication, timing and control peripherals. High memory density K60 family devices include an optional single precision floating point unit, NAND flash controller and DRAM controller.

Reliability, Safety and Security

- Hardware Encryption coprocessor for secure data transfer and storage. Faster than software implementations and with minimal CPU loading. Supports a wide variety of algorithms - DES, 3DES, AES, MD5, SHA-1, SHA-256
- System security and tamper detect with secure real-time clock with independent battery supply. Secure key storage with internal/external tamper detect for unsecure flash, temperature, clock, and supply voltage variations and physical attack detection

Kinetis K60 Family



- Memory protection unit provides memory protection for all masters on cross bar switch, increasing software reliability
- Cyclic redundancy check engine validates memory contents and communication data, increasing system reliability

K60 Family Summary

Part Numbers	CPU (MHz)	Memory				Feature Options									Other	100LQFP (14x14 mm)	104BGA (8x8 mm)	144LQFP (20x20 mm)	144BGA (13x13 mm)	196BGA (15x15 mm)	256BGA (17x17 mm)
		Flash (KB)	Flex Memory (KB)	SRAM (KB)	Cache (KB)	Single Precision Floating Point Unit	CAN	Memory Protection Unit	Secure Digital Host Controller	NAND Flash Controller	External Bus Interface	12-bit Digital to Analog Converter	Programmable Gain Amplifier	5V Tolerant I/O							
MK60N256Vyy100	100	256	-	64			√	√	√		√	√	√	√	IEEE 1588 Eth, USB OTG (FS), CAU+RNG	LL	ML	LQ	MD		
MK60N512Vyy100	100	512	-	128			√	√	√		√	√	√	√	IEEE 1588 Eth, USB OTG (FS), CAU+RNG	LL	ML	LQ	MD		
MK60X256Vyy100	100	256	256	64			√	√	√		√	√	√	√	IEEE 1588 Eth, USB OTG (FS), CAU+RNG	LL	ML	LQ	MD		
MK60X512Vyy120	120	512	512	128	16	√	√	√	√	√	√	√	√	√	IEEE 1588 Eth, USB OTG (FS/HS), CAU+RNG, Tamper Detect, *DRAM Ctrlr			LQ	MD	MF	MJ
MK60X512Vyy150	150	512	512	128	16	√	√	√	√	√	√	√	√	√	IEEE 1588 Eth, USB OTG (FS/HS), CAU+RNG, Tamper Detect, *DRAM Ctrlr			LQ	MD	MF	MJ
MK60N1M0Vyy120	120	1024	-	128	16	√	√	√	√	√	√	√	√	√	IEEE 1588 Eth, USB OTG (FS/HS), CAU+RNG, Tamper Detect, *DRAM Ctrlr			LQ	MD	MF	MJ
MK60N1M0Vyy150	150	1024	-	128	16	√	√	√	√	√	√	√	√	√	IEEE 1588 Eth, USB OTG (FS/HS), CAU+RNG, Tamper Detect, *DRAM Ctrlr			LQ	MD	MF	MJ

*256 pin packages only

For details of peripherals offered on specific devices, please refer to the family product brief document at freescale.com.
yy = package designator noted in the "Packages" column

- Independent-clocked COP guards against clock skew or code runaway for fail-safe applications, e.g. IEC 60730
- External watchdog monitor drives output pin to safe state external components if watchdog event occurs

Connectivity and Communications

- IEEE 1588 Ethernet MAC with hardware time stamping provides precision clock synchronization for real-time industrial control
- USB 2.0 On-The-Go + device charger detect optimizes charging current/time for portable USB devices enabling longer battery life. Integrated USB low voltage regulator supplies up to 120 mA off chip at 3.3V to power external components from 5V input. Up to 480 Mbps with external ULPI PHY
- Up to six UARTs with IrDA support, including one UART with ISO 7816 smart card support. Variety of data size, format and transmission/reception settings supported for multiple industrial communication protocols
- Up to two Inter-IC Sound (I^2S) serial interfaces for audio system interfacing
- Two CAN for industrial network bridging
- Up to three DSPI and two I^2C

External Peripheral Support

- FlexBus external bus (bus interface provides interface options) provides interface options to memories and peripherals such as graphics displays. Supports up to six chip selects
- Secure digital host controller supports SD, SDIO, MMC or CE-ATA cards for in-application software upgrades, media files or adding Wi-Fi support
- NAND flash controller supports up to 32-bit ECC current and future NAND types. ECC management handled in hardware, minimizing software overhead
- DRAM controller supports connection of DDR, DDR2 and low-power DDR memories. Max. frequency (clock/data) 125/250 MHz

Flash, SRAM and FlexMemory

- 256 KB–1 MB flash. Fast access, high reliability with four-level security protection
- 64 KB–128 KB of SRAM
- FlexMemory: 32 bytes–16 KB of user-segmentable byte write/erase EEPROM for data tables/system data. EEPROM with over 10M cycles and flash with 100 µsec write time (brownouts without data loss/corruption). No user or system intervention to complete programming and erase functions and full operation down to 1.71V. In addition, FlexNVM from 256 KB–512 KB for extra program code, data or EEPROM backup

Performance

- ARM Cortex-M4 core + DSP. 100–150 MHz, single cycle MAC, single instruction multiple data (SIMD) extensions, single precision floating point unit
- Up to 32-channel DMA for peripheral and memory servicing with reduced CPU loading and faster system throughput
- Cross bar switch enables concurrent multi-master bus accesses, increasing bus bandwidth
- Up to 16 KB of instruction/data cache for optimized bus bandwidth and flash execution performance
- Independent flash banks allow concurrent code execution and firmware updating with no performance degradation or complex coding routines

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Mixed-Signal Capability

- Up to four high-speed 16-bit ADCs with configurable resolution. Single or differential output mode operation for improved noise rejection. 500 ns conversion time achievable with programmable delay block triggering
- Up to two 12-bit DACs for analog waveform generation for audio applications
- Up to three high-speed comparators providing fast and accurate motor over-current protection by driving PWMs to a safe state
- Up to four programmable gain amplifiers with x64 gain for small amplitude signal conversion
- Accurate on-chip voltage reference eliminates need for accurate external voltage reference IC, reducing overall system cost

Human-Machine Interface

- Xtrinsic low power with up to 16 inputs. Operates in all low-power modes (minimal current adder when enabled). Hardware implementation avoids software polling method. High sensitivity level allows use of overlay surfaces up to 5 mm thick

Target Applications

- Building automation controllers
- Elevator control panels
- Instrumentation clusters
- Surveillance cameras

Timing and Control

- Up to four FlexTimers with a total of 20 channels. Hardware dead-time insertion and quadrature decoding for motor control
- Carrier modulator timer for infrared waveform generation in remote control applications
- Four-channel, 32-bit periodic interrupt timer provides time base for RTOS task scheduler or trigger source for ADC conversion and programmable delay block

Ultra-Low Power

- 10 low-power modes with power and clock gating for optimal peripheral activity and recovery times. Stop currents of <500 nA and run currents of <200 uA/MHz, 4 µs wake-up from stop mode
- Full flash programming and analog peripheral operation down to 1.71V for extended battery life
- Low-leakage wake-up unit with up to eight internal modules and sixteen pins as wake-up sources in low-leakage stop (LLS)/very low-leakage stop (VLLS) modes
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Tools and Software

- Freescale Tower System hardware development environment
- Integrated development environments
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  - IAR Embedded Workbench
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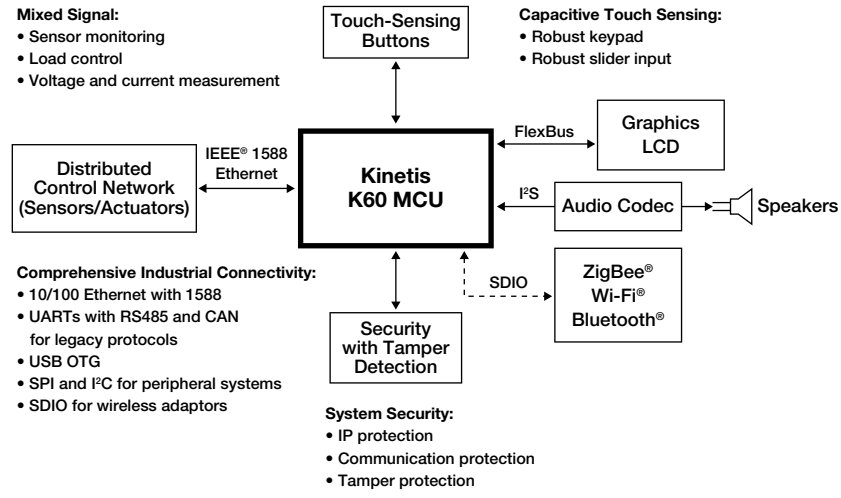
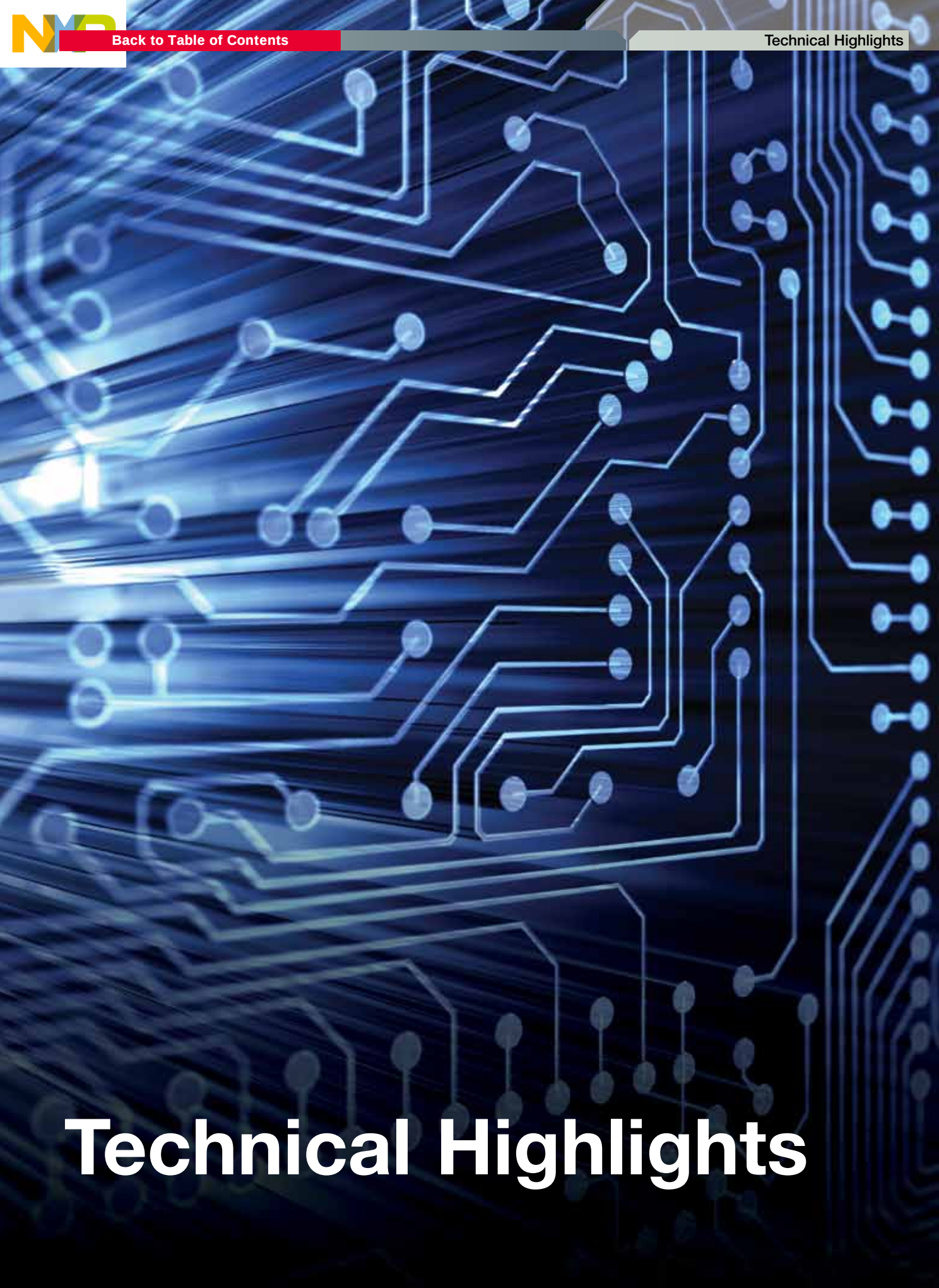
- Runtime software and RTOS
  - Math, DSP and encryption libraries
  - Motor control libraries
  - Complimentary bootloaders (USB, Ethernet, RF, serial)
  - Complimentary Freescale embedded GUI (eGUI) software driver for graphics LCD panels
  - Complimentary Freescale MQX
  - Cost-effective Nano SSL/Nano SSH for Freescale MQX RTOS
  - Micrium uC/OS-III
  - Express Logic ThreadX
  - SEGGER embOS
  - freeRTOS
  - Mocana (security)
- Plus full ARM ecosystem

K60 Family: Factory/Building Automation Controller





Technical Highlights

Core Technology

ColdFire V1 core and ARM Cortex-M4 core

Freescale Semiconductor's new 90nm 32-bit microcontroller families are built using the ColdFire V1 core and the ARM Cortex-M4 core. Each core has attributes that make it the appropriate choice for many embedded application spaces.

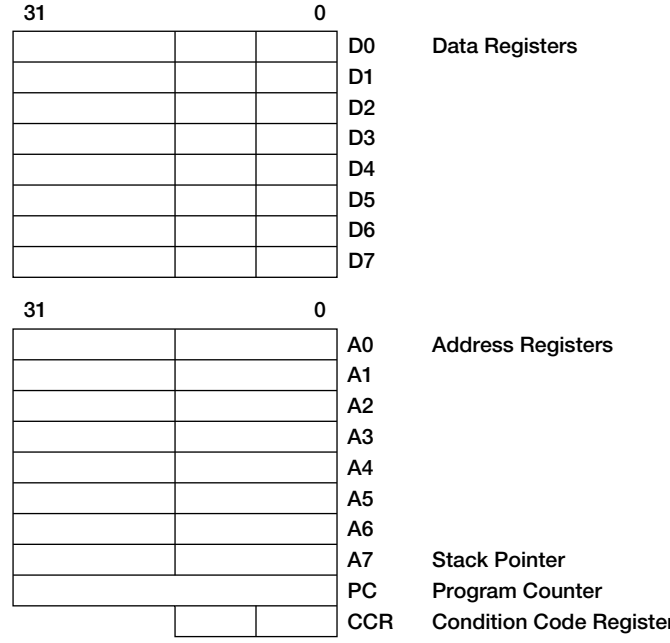
Version 1 ColdFire Core

Designed for 32-bit entry-level applications, the primary focus of the ColdFire V1 core is minimum core size and power dissipation. A simplified version of the V2 ColdFire core, it features improved handling of byte (8-bit) and word (16-bit) operands, while maintaining the same addressing modes and instruction definitions of the ColdFire architecture. The core implements Revision C of the ColdFire instruction set architecture. Figure 1 shows the user programming model, which includes:

- 16 general-purpose 32-bit registers (8 data registers, D[0-7] and 8 address, A[0-7])
- 32-bit program counter (PC)
- 8-bit condition code register (CCR)

The ISA defines variable length operations where instructions can be 16, 32 or 48 bits in length and include a powerful set of data memory addressing modes. Supported data operand types are 1-, 8-, 16- and 32-bit integers. In addition to memory-referencing load and store operations, the ISA supports embedded load instructions and memory-to-memory moves.

Figure 1: ColdFire Family User Integer Programming Model



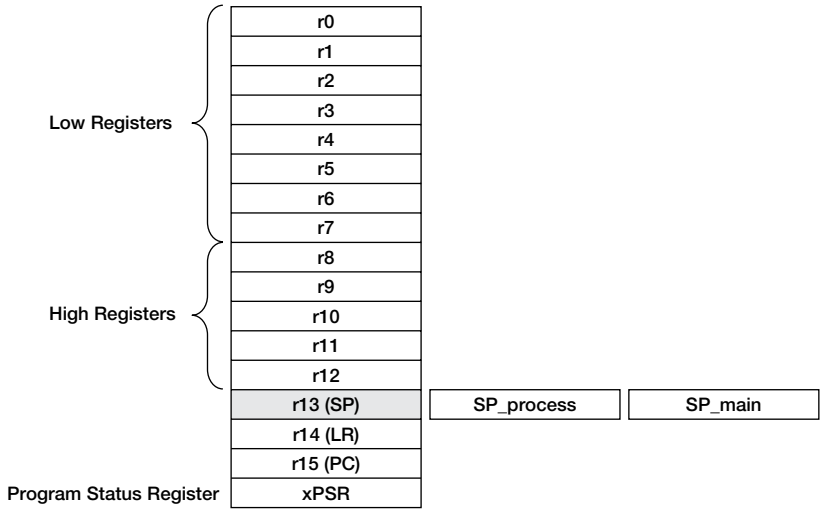
The enhanced multiply-accumulate (EMAC) unit included in the MCF51Qx/Jx families adds support for 16- and 32-bit signed fractional numbers, compound MAC+MOVE instructions, circular memory queue addressing and four 48-bit accumulator registers.

The core architecture includes support for generic coprocessor instructions and a hardware interface to accelerate operations at the instruction or function level. An example is the cryptographic acceleration unity (CAU). The CAU provides a significant performance boost to a number of security algorithms popular today, including DES, AES, SHA1, SHA-256 and MD5 with a small hardware gate cost. The coprocessor interface allows a tightly coupled accelerator where the CPU fetches operands and sends commands to the hardware module.

Like all ColdFire processor implementations, the ColdFire V1 core uses a 2-stage instruction fetch pipeline (IFP) and 2-stage operand execution pipeline (OEP) to provide an appropriate hardware implementation to handle the variable length instruction set. The core interfaces to the SoC via a single 32-bit AMBA™ AHB bus. The IFP and OEP memory interfaces are multiplexed together and map directly into the 2-stage (address phase, data phase) pipelined AHB bus.

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

Figure 2: ARM® Cortex™-Mx Register Programming Model



ARM Cortex-M4 Core

The ARM Cortex-M4 core builds on the legacy of its ARM Cortex™-M3 predecessor and brings an intelligent blend of MCU and DSP features. The ARM Cortex-M4 implements the ARMv7-ME™ instruction set architecture. This is the ARM Thumb2 definition and provides compatibility with ARM Cortex-M3 plus adds significant new capabilities with DSP and SIMD extensions. The basic multiply-accumulate instructions support operations up to 32 x 32 + 64 –> 64. The ARM Cortex-M4 core also supports an optional single-precision floating-point unit (FPU) which includes an extension register file of 32 32-bit floating-point data registers.

Figure 2 shows the basic user programming model, which includes:

- 13 general-purpose registers, r[0-12] stack pointer (r13 = SP), link register (r14 = LR), program counter (r15 = PC)
- Stack pointer, link register, program counter
- Multiple program status registers (xPSR)

The ISA defines variable length operations with 16 and 32-bit instructions. It supports data operand sizes of 8-, 16- and 32-bit integers plus fields of 1–32-bit widths.

ARM Cortex-Mx cores are targeted at application spaces where overall size and deterministic operation are more important than absolute performance. As a result, the ARM Cortex-M4 core features a three-stage pipeline microarchitecure: instruction fetch (Fe), instruction decode (De) and, instruction execute (Ex).

The added DSP and SIMD instruction extensions are executed in a high-speed multiply/accumulate structure; almost all the multiply and optional accumulation instructions have a single-cycle execution time.

ARM Cortex-M4 implements multiple 32-bit bus interfaces that support a Harvard memory architecture. Specifically, the core provides a modified Harvard connection with AHB code and system buses. The code bus is typically used for instruction fetching and data accesses of PC-relative data, while the system bus is typically used for RAM and peripheral accesses. A separate 32-bit private peripheral bus (PPB) connection to several important modules (e.g, the Nested Vectored Interrupt Controller) is accessible to only the core.

Compatibility and Scalability

Simplify design efforts and speed time to market

To simplify your application's hardware and software design, all the Kinetis microcontroller families have unprecedented compatibility and scalability. All families share common characteristics spanning the features below:

- Wide operating voltage range from 1.71V to 3.6V with both flash programming and analog operation down to 1.71V
- Ambient operating temperature ranges from -40°C to +105°C
- Flexible performance levels with devices rated at maximum CPU frequencies from 50 MHz to 150 MHz
- Multiple package options from 32-pin QFN (5 x 5 mm body size) to 256-pin MAPBGA
- Scalable embedded memory densities from 32 KB flash/8 KB SRAM to 1 MB flash/128 KB SRAM with multiple flash arrays allowing read-while-write operations
- High-endurance, byte-writeable, embedded EEPROM from 32 bytes to 16 KB capable of exceeding 10 million read/write cycles
- Identical peripherals and memory maps simplifying code reuse
- Powerful ARM Cortex-M4 core with built-in DSP instructions and optional single-precision FPU
- Industry-standard serial wire debug, IEEE® 1149.1 JTAG, and IEEE 1149.7 compact JTAG debug interfaces along with ARM CoreSight™ architecture trace components
- 10 power modes with power savings across run, wait and stop modes
- Robust 5V-tolerant pin inputs

Figure 1: Compatibility of Kinetis Families

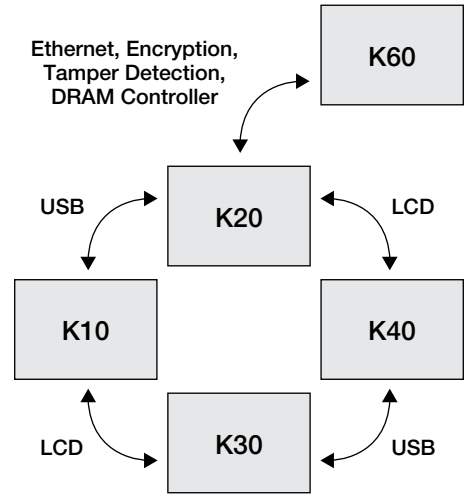


Table 1: Kinetis Family	Differentiating Peripherals
K10	Baseline
K20	Baseline + USB
K30	Baseline + LCD
K40	Baseline + USB + LCD
K60	Baseline + USB + Ethernet + Encryption + Tamper Detect + DRAM Controller

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

Figure 2: Memory Comparison Across Kinetis Families WITHOUT FlexMemory

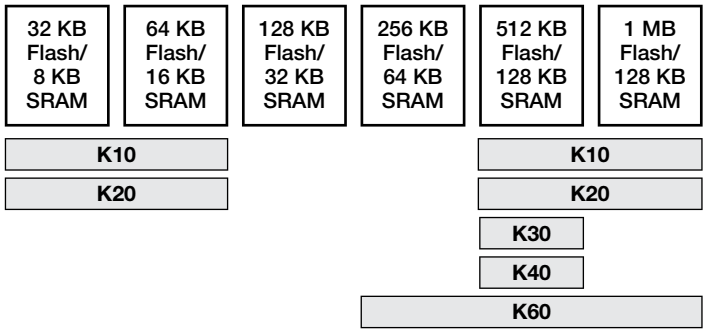


Figure 3: Memory Comparison Across Kinetis Families WITH FlexMemory

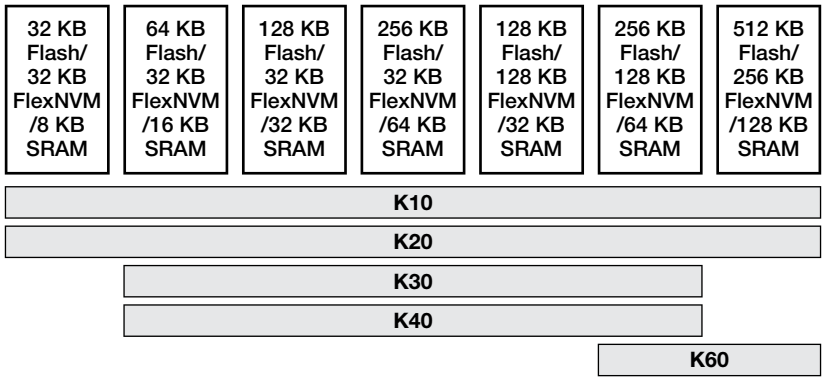
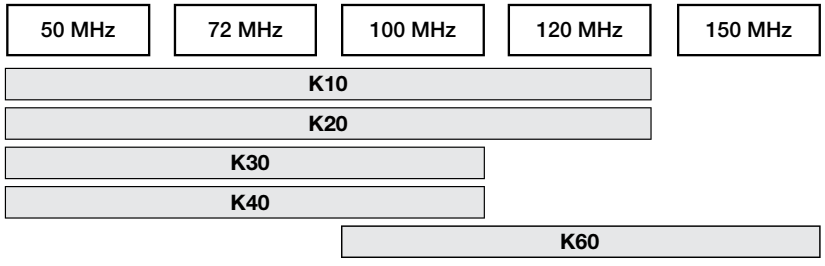


Figure 4: Range of Maximum CPU Frequency Across Kinetis Families



The scalability within these options enables you to upgrade seamlessly or reduce your product costs by migrating among the families without having to redesign common hardware and software.

An upgrade to your product could be as simple as choosing a different derivative with augmented peripherals (see Table 1 and Figure 1).

Another common reason to upgrade is to increase the memory footprint, increase the performance level or add FlexMemory with EEPROM to your final design (see Figures 2, 3 and 4). Likewise, you could reduce costs by removing similar features.

Each family integrates both market-focused and common embedded MCU features. As pin counts increase with larger package options, more features become available. Features can be added while maintaining flexibility in body size, pitch and package types to best fit your board manufacturing process and product dimensions.

Continued on next page

Compatibility and Scalability

Continued from previous page

Packages include LQFP, QFN and MAPBGA options (see Table 2).

To provide exceptional compatibility, all Kinetis families were designed to be scalable yet pin-to-pin compatible or drop-in replacements.

Pin Compatibility within an MCU Family

1. Changing your memory footprint or performance tier within identical package types is a drop-in replacement, e.g. from a K30 family 80-pin device with 128 KB of flash, to a K30 family 80-pin device with 256 KB of flash
2. Changing between identical LQFP and QFN package types has no effect on pin ordering, e.g. from a K10 family 64LQFP device, to a K10 family 64QFN device
3. Features can be added with larger packages with minimal layout impact

Pin Compatibility across MCU Families

1. You can add USB by migrating from a K10 device to a K20 device, or a K30 device to a K40 device, in an identical package with minimal board layout changes by replacing four digital GPIO pins with four USB pins. (see Figure 5)
2. You can add LCD by migrating from a K10 device to a K30 device, or a K20 device to a K40 device, in an identical package with minimal board layout changes by replacing four digital GPIO pins with four LCD power supply pins. The additional LCD signals are multiplexed with other digital GPIO pins. (see Figure 6)

Table 2: Package Types Across Kinetis Families

Package Type	Body Size	Pitch	Families
32-pin QFN	5 X 5 mm	0.5 mm	K10, K20
48-pin QFN	7 X 7 mm	0.5 mm	K10, K20
48-pin LQFP	7 X 7 mm	0.5 mm	K10, K20
64-pin QFN	9 X 9 mm	0.5 mm	K10, K20, K30, K40
64-pin LQFP	10 X 10 mm	0.5 mm	K10, K20, K30, K40
80-pin LQFP	12 X 12 mm	0.5 mm	K10, K20, K30, K40
81-pin MAPBGA	8 X 8 mm	0.65 mm	K10, K20, K30, K40
100-pin LQFP	14 X 14 mm	0.5 mm	K10, K20, K30, K40, K60
104-pin MAPBGA	10 X 10 mm	0.65 mm	K10, K20, K30, K40, K60
144-pin LQFP	20 X 20 mm	0.5 mm	K10, K20, K30, K40, K60
144-pin MAPBGA	13 X 13 mm	1.0 mm	K10, K20, K30, K40, K60
196-pin MAPBGA	15 X 15 mm	1.0 mm	K60
256-pin MAPBGA	17 X 17 mm	1.0 mm	K60

Figure 5: USB

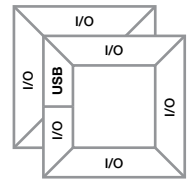


Figure 6: LCD

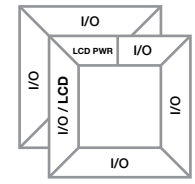
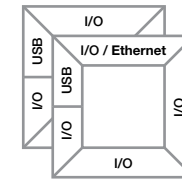


Figure 7: Ethernet



3. You can add Ethernet by migrating from a K20 device to a K60 device in an identical package type. The additional Ethernet signals are multiplexed with other digital GPIO pins, so this migration is a drop-in replacement. (see Figure 7)

ColdFire+ Compatibility

Coldfire+ families share the same compatibility characteristics as the Kinetis families. Within a family, changing your memory footprint is a drop in replacement. For example, MCF51JU32 in a 44-pin package is a drop in replacement for the MCF51JU64 in a 44-pin package. In addition, changing from 64LQFP to 64QFN within a family maintains the same pin ordering. The benefit is that designs can easily implement dual package layouts which utilize QFN and LQFP footprints.

Migrating across families (Jx to Qx) also requires a minimum set of changes. Only a small subset of pins (4 pins) will change when migrating between these devices. The benefit is that when adding or removing USB functionality, only minimal hardware changes are required.

90nm TFS Flash and FlexMemory

Configurable high-endurance embedded EEPROM

Freescale's next-generation microcontrollers will offer exceptional low-power capability, performance and flexibility through 90nm thin film storage (TFS) flash and FlexMemory technology.

TFS Flash Memory

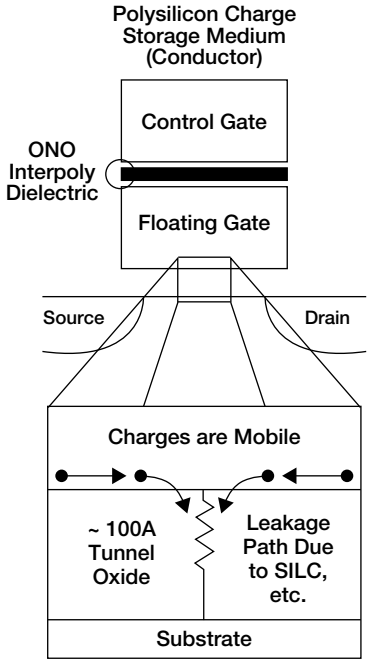
By combining split gate bit cell and TFS technology, Freescale is bringing a powerful combination to the embedded market that offers several key advantages versus competing technologies.

Split Gate Bit Cell

- Flash access times of less than 30 ns. 30 to 50 percent faster than many competing technologies.
- Fast, low-voltage transistors provide flash programming and analog peripheral operation down to 1.71V and significantly reduced run and standby currents. Competing technologies are typically limited to 2.0V or above.
- Excellent area efficiency (only a small positive voltage pump is necessary for programming) enables a high level of memory and peripheral integration across flash densities, while maintaining low MCU cost.

Continued on next page

Conventional Floating Gate Bit Cell



FlexMemory as EEPROM Key Features	Customer Benefits
Programmable trade-off of EEPROM quantity vs. endurance	Flexibility: EEPROM size and endurance can be customized to application needs
Endurance of over 10M write/erase cycles	Longer EEPROM/product life
Erase + write time of 1.5 ms	Fast programming time allows intense EEPROM use with large data sets. Fast write time enables brown-out capability.
No software intervention necessary	As simple as RAM from the user's viewpoint

90nm TFS Flash and FlexMemory

Continued from previous page

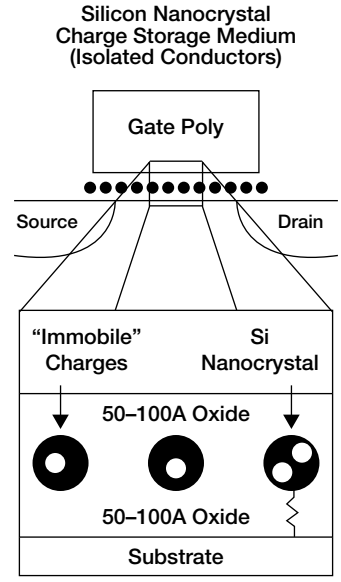
Silicon Nanocrystals

- Inherently robust design: Electrons stored within the bit cell are distributed among an array of silicon nanocrystals which are separated from each other by an insulator.
- Inherently reliable: No single nanocrystal is responsible for maintaining the charge in the cell. If a leakage path develops beneath one nanocrystal, it may lose its stored charge, but the other nanoncrystals retain their charge—and the cell retains its data.

FlexMemory

Freescale's new FlexMemory technology provides an extremely versatile and powerful solution for designers seeking on-chip EEPROM and/or additional program or data flash memory. As easy and as fast as SRAM, it requires no user or system intervention to complete programming and erase functions when used as high endurance byte-write/byte-erase EEPROM. EEPROM array size can also be configured for improved endurance to suit application requirements. FlexMemory can also provide additional flash memory (FlexNVM) for data or program storage in parallel with the main program flash. The user can configure several parameters including EEPROM size, endurance, write size and the size of additional program/data flash. On larger memory variants, endurance figures of over 10M write/erase cycles can be achieved. Additionally, designers can access the FlexRAM to expand system RAM for general application use.

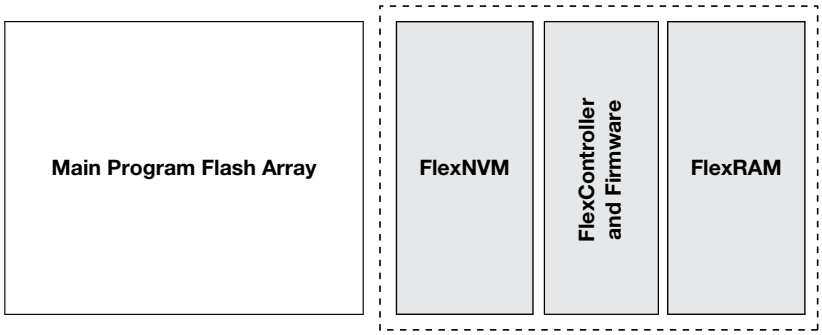
Thin Film Storage Bit Cell



Attribute	Traditional EEPROM	FlexMemory
Read-while-write with program memory	Yes	Yes
Granularity	Byte write/erase	Byte write/erase
Write time	~1–5 msec (byte write only)	~100 µsec (word or byte program, brown-outs without loss or corruption of data)
Erase + write time	~5–10 msec	~1.5 msec
Endurance	50–300K cycles (fixed)	SoC implementation and user configurable, over 10M cycles
Minimum write voltage	> 2.0V	1.71V
Flexibility	Fixed by part number	Programmable trade-off of quantity vs. endurance

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

FlexMemory



FlexMemory

The key features of FlexMemory include:

- Configurability for designer:
  - EEPROM array size and number of write/erase cycles
  - Program or data flash size
- EEPROM endurance of 10M write/erase cycles possible over full voltage and temperature range
- Seamless EEPROM read/write operations: simply write or read a memory address
- High-speed byte, 16-bit, and 32-bit write/erase operations to EEPROM
- Eliminates the costs associated with external EEPROM ICs, and the software headaches and resource (CPU/flash/RAM) impact of EEPROM emulation schemes
- Storage for large data tables or bootloader
- Read-while-write operation with main program flash memory
- Minimum write voltage 1.71V

Programmable Trade-Off

FlexMemory lets the user fully configure the way FlexNVM and FlexRAM blocks are used to provide the best balance of memory resources for their application. The user can configure several parameters, including EEPROM size, EEPROM endurance, byte-write and read-while-write cycles, and the size of additional program/data flash and RAM. In addition to this flexibility, FlexMemory provides superior EEPROM performance, endurance and low-voltage operation when compared to traditional EEPROM solutions.

Enhanced EEPROM

- Combines FlexRAM and FlexNVM to create byte write/erase, high-speed and high-endurance EEPROM

FlexNVM

- Can be used as part of the enhanced EEPROM configuration, or in addition to the main program or data flash
- Can be sub-segmented into two blocks of memory. For example, a portion can be used as flash while the rest is used for enhanced EEPROM backup

FlexRAM

- Can be used as part of the EEPROM configuration

High Endurance

Byte-writeable EEPROM endurance is user configurable by two factors:

- Size of EEPROM
- Size of FlexNVM allocated to EEPROM backup

Use Case Example

MCU has 128 KB program flash, 32 KB SRAM and FlexMemory has 128 KB FlexNVM and 4 KB FlexRAM (maximum EEPROM size). The application requires 8 KB additional program flash for a bootloader and 256 bytes of high-endurance EEPROM. The user would allocate 8 KB of FlexNVM for the additional program flash and the remaining 120 KB for EEPROM backup. The user would define 256 bytes of EEPROM size from the FlexRAM. In this example, the EEPROM endurance would result in a minimum of 2.32M write/erase cycles.

Power Management

Multiple flexible low-power modes for long battery life

The power management controller provides the user with multiple power mode options. Ten modes of operation are supported to allow the user to optimize power consumption for the level of functionality needed.

There are several wake-up sources for the power modes. A low-leakage wake-up unit has up to eight internal peripheral wake-up sources, as well as up to sixteen external pins for wake-ups. In the lowest power mode several wake-up sources are available: low-power timer, real-time clock, analog comparator, DAC, capacitive touch-sensing Interface and several pin interrupts.

Depending on the requirements of the user application, a variety of stop modes are available that provide state retention, partial power down or full power down of certain logic and/or memory. I/O states are held in all modes of operation.

- Normal run mode allows the CPU to execute code with power consumption as low as 200 uA/MHz.
- Low-leakage stop mode reduces the voltage to internal logic, minimizing leakage from unused internal circuits. Keeps fast wake-up time down to 4 uS.
- Very low-leakage stop modes power down the internal logic, and optionally RAM memory, eliminating leakage from unused circuits. This mode keeps 32-byte register file content for critical application data.

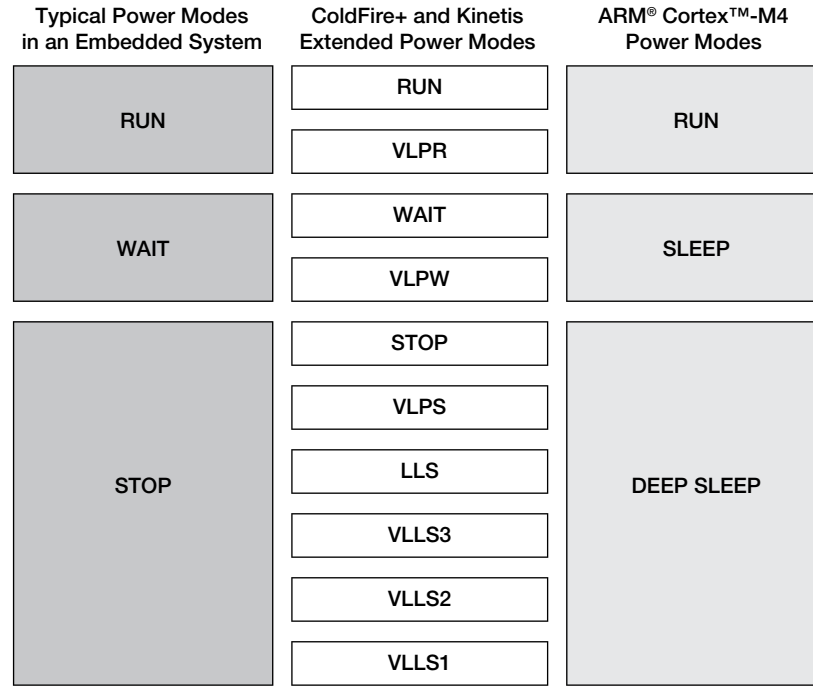
VLPR: Very Low Power Run

VLPW: Very Low Power Wait

VLPS: Very Low Power Stop

VLL: Very Low Leakage

Comparison of Power Modes



Key Features	Customer Benefits
Nano-amp current consumption with RAM retention	Extended battery life
Wake-up time as low as 4 uS	Minimize average power consumption in frequent power mode change applications
Multiple low power modes	Customize peripheral activity and recovery times to suit application power budget
200 uA/MHz normal run mode	Device can be active with minimal power consumption

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

Mode	Brief Description
Run	MCU can be run at full-speed.
Wait	Allows peripherals to function while CPU goes to sleep, reducing power consumption.
VLP Run	CPU and peripheral clock maximum frequency is restricted. CPU/platform clock is restricted to 2 MHz. Flash access is restricted to 1 MHz. LVD is off.
VLP Wait	Similar to VLP Run, with CPU in sleep to further reduce power.
Stop	MCU is in static state. Lowest power mode that retains all registers while maintaining LVD protection.
VLP Stop	MCU is in static state with LVD operation off. Lowest power mode with ADC, LPT, RTC, LCD, HSCMP, DAC and pin interrupts functional.
LL Stop	MCU is in low-leakage state retention power mode. LLWU controls wake-up sources including LPT, RTC, LCD, HSCMP, DAC and select pin interrupts.
VLL Stop3	MCU is placed in a low-leakage mode powering down most internal logic. All system RAM contents are retained and I/O states held. LLWU controls wake-up sources, including LPT, RTC, LCD, HSCMP, DAC and select pin interrupts.
VLL Stop2	Similar to VLL Stop 3, with only partial system RAM retention. FlexRAM contents can optionally be retained.
VLL Stop1	Similar to VLL Stop 3, with only 32 byte register file retention.

Description of Power Modes

Additional features for low-power/battery applications include:

- Low-voltage detection can be configured to generate a reset or interrupt to protect against voltage drops.
  - Supports two low-voltage detection trip points
  - Four low-voltage warning levels per trip point
- Programmable clock gating allows an application to shut down unused peripheral clocks to further minimize power consumption in run and wait modes.

Low-leakage wake-up unit:

- Supports up to sixteen external input pins and up to eight internal modules with individual enable bits.
- Input sources may be external pins or from internal peripherals capable of running in LLS or VLLS modes.
- Each external pin wake-up input is programmable as falling edge, rising edge or any change.
- An optional low-power oscillator (LPO) cycle digital filter provided to qualify an external pin detect and RESET pin detect.

Xtrinsic Low-Power Touch-Sensing Interface

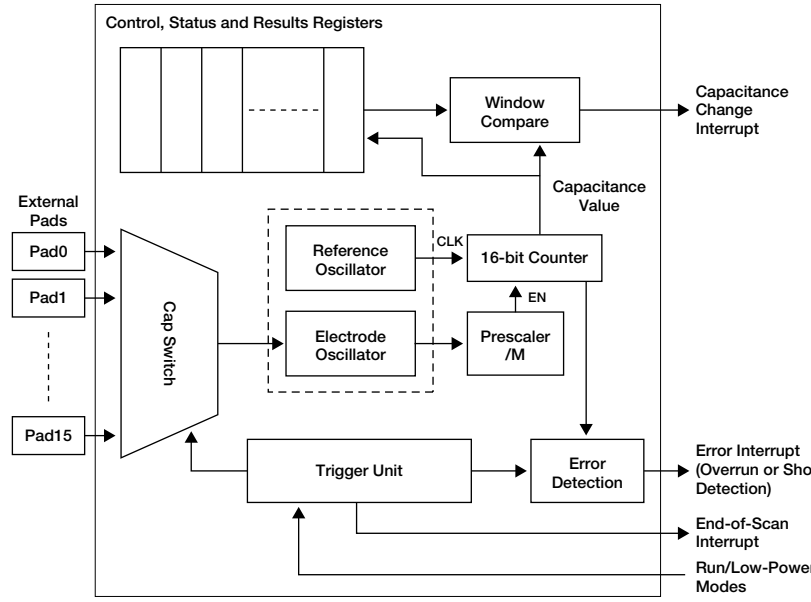
Attractive user interfaces with low power appeal

Touch sensing offers a modern alternative to traditional push-button switches through the creation of touch-activated push-button, slider and rotary user interfaces. Benefits include design flexibility, low maintenance, cleanliness and the ability to support a variety of sensitivity levels and overlay surfaces. The use of touch-sensing interfaces now extends beyond the latest consumer products into domestic appliances, portable medical devices and industrial control panels.

The touch-sensing input (TSI) module provides capacitive touch-sensing detection with high sensitivity, enhanced robustness and extreme low-power performance. The module's key features are:

- Up to 16 electrodes, using a single pin per electrode, with no need for an external component
- Functional in all low-power modes, waking the CPU only in the event of electrode capacitance variations
- Minimal current adder when enabled
- Capacitance measurement resolution down to 0.02fF
- Electrode sampling integration: variable electrode sampling period for increased noise robustness in noisy environments
- Fault detection: detects electrode short circuits and sample time misconfigurations
- Periodic electrode scan mode requires no additional MCU peripheral

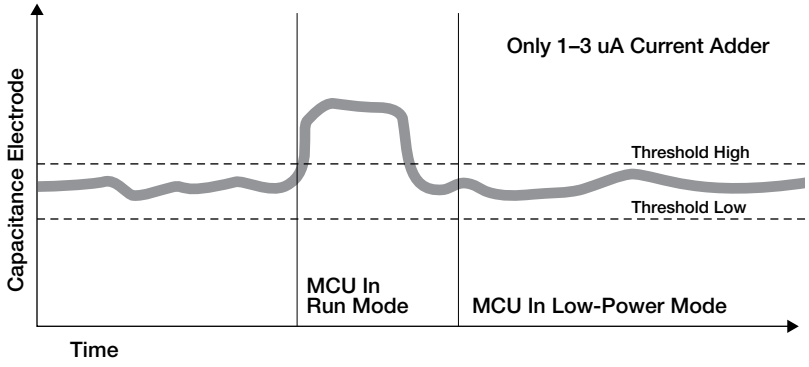
TSI Module Overview



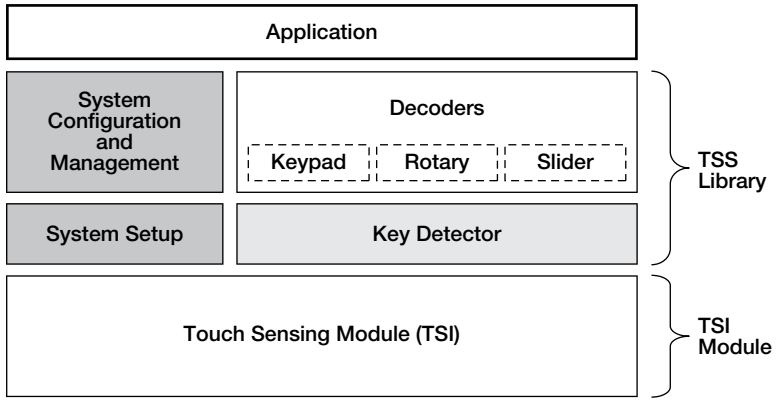
Key Features	Customer Benefits
Operational in all low power modes with only minimal current adder when enabled	Ideal for battery-powered applications
Fault detection capability	Robust performance in noisy environments
High sensitivity capacitance measurement resolution down to 0.02fF	High sensitivity allows use of thick glass, plastic and flexi-glass overlay surfaces
Fully integrated with Freescale's Touch-Sensing Software (TSS) Library	Fully compatible with CodeWarrior IDE. Includes smart auto-calibration mechanisms to prevent environmental issues, noise rejection algorithms, an optimized buffer structure enabling any arrangement of electrodes and a PC GUI application for electrode characterization that includes demos and application examples

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

Low-Power Mode Operation



Touch-Sensing Software Library



Low-Power Mode Operation

The TSI module has programmable high and low thresholds and can be enabled in all low-power modes with minimum current consumption.

An internal periodic scan module is active in all MCU power modes and has separate scan intervals for low-power and run modes. This allows the user to set longer scan intervals for minimizing power consumption. Conversely, in run mode the application can set shorter scan intervals for faster touch response.

The low-power capabilities of the TSI module open up new touch-sensing application spaces for touch sense interfaces. Such devices are now able to be woken up from sleep states via a touch input.

When a touch occurs, the instantaneous electrode capacitance is detected to be out of the threshold-defined range. This issues a TSI interrupt, which in turn wakes up the CPU.

Touch-Sensing Library Integration

Several applications require the implementation of keypad, rotary and slider user interfaces. Operating environment, desired response time and sensitivity to touch detection all need to be considered according to application requirements.

Freescale provides a complete touch solution with a touch-sensing module that is seamlessly integrated with the Freescale Touch Sensing Library.

Visit **freescale.com/touchsensing** for more information on touch-sensing software solutions.

Segment LCD Controller

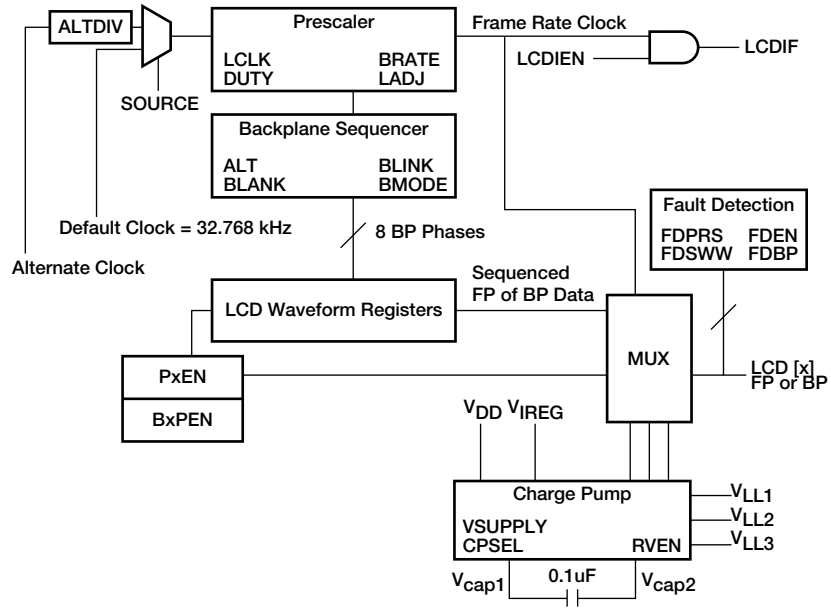
A configurable, low-power display

The Kinetis K30 and K40 MCU families include a flexible segment LCD controller that offer a number of benefits for cost-effective GUI-enabled designs. Features include software-configurable frontplanes and backplanes, low-power blink modes and fault-detection capabilities as well as support for a broad range of 3 and 5V LCD panels.

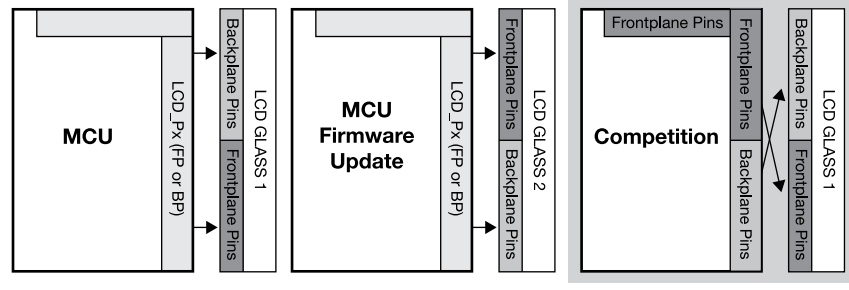
The segment LCD controller is used to drive monochrome LCD displays in all CPU modes of operation, including very low-leakage stop modes. Key features of this peripheral include:

- Fault detection hardware alerts the user to faults in the display, the display connector, and the board connections between the MCU and the display
- Low-power blink mode operation allows segments to be turned on and off at set intervals conserving power in stop modes
- Configurable frame rate and duty cycle up to x8
- Internally regulated voltage to support contrast control
- Drive for 3V or 5V LCD glass
- Multi-purpose LCD pins which support backplane/COM, frontplane/SEG or GPIO functions

LCD Module Overview



Configuration Assignment



Key Features	Customer Benefits
Segment fault detection	Avoids erroneous reading of LCD display by alerting the user to faults in the display, the display connector and the board connections between the MCU and the display. Example: In medical applications, prevents the user from interpreting a potentially unsafe readout and prescribing improper treatment (dosage level)
LCD pins can be configured as frontplane or backplane	Board layout can be optimized to the LCD. Changes to the LCD design can be handled by firmware, avoiding costly hardware changes
Low-power blink mode operation—blink to blank screen or blink to alternate screen at 1/8s, 1/4s, 1/2s, 1s, 2s, 4s and 8s intervals	Lower average power

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
○	○	○	○	●	●	○

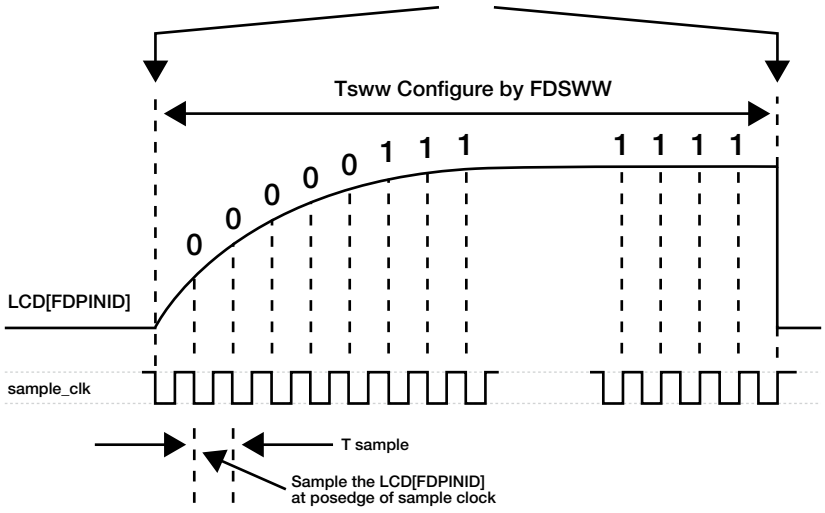
Frontplane and Backplane Reassignment

The segment LCD control registers can configure any LCD pin to be a frontplane or a backplane LCD signal.

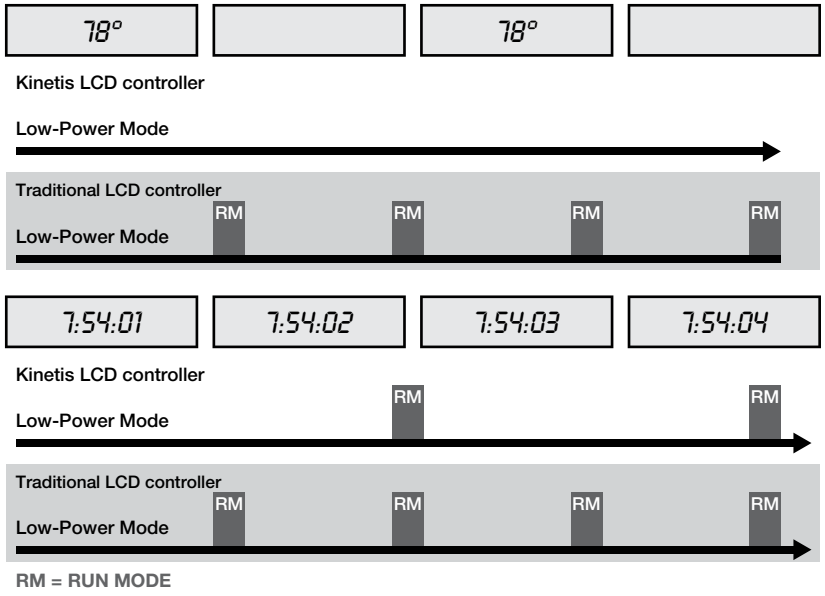
The frontplane or backplane assignment can be optimized to match the layout of the LCD display by software configuration.

Changes to LCD display design can be handled by firmware updates, reducing cycle time and hardware cost.

Fault Detection



Blink Mode Timing



Segment Fault Detection

The segment LCD controller has hardware support for detecting faults on the LCD pins. Failures, where an LCD segment is either unexpectedly on or off, result in erroneous information that can mislead the user.

The LCD display fault-detect circuits can be used to find faults in the LCD display, display connector and board connections between the MCU and the display.

Hardware is used to sample and digitize generated LCD waveforms. The digitized data can be analyzed for changes in LCD capacitances that indicate faults.

Blink in Low-Power Modes

The segment LCD controller supports blink to blank screen or blink to alternate screen while in low-power modes.

Blinking to a blank screen turns all segments off. Blinking to an alternate screen allows different display data to be shown during the configurable blink period.

With this function, the MCU can achieve lower average power consumption by supporting LCD blinking without exiting the low-power mode, as shown in this diagram.

Refer to **freescale.com/LCD** for more information.

Precision Analog and Control

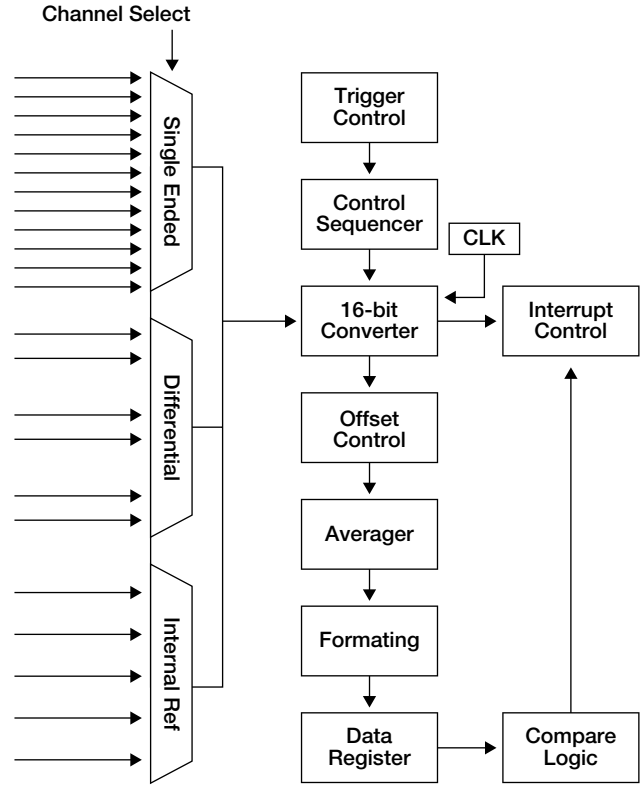
Rich on-chip mixed signal capability

Analog-to-Digital Converter

The 16-bit resolution analog-to-digital converter (ADC) module uses the successive-approximation register (SAR) method, which is faster and consumes less power than the sigma-delta method. It also uses averaging to enhance the resolution. Key features of the ADC module include:

- Support for single-ended or differential inputs
- Averaging by 1, 4, 8, 16 or 32
- Automatic compare function
- Triggering synchronization with DAC
- Configurable for 8-,10-,12- or 16-bit resolution mode to manage trade-offs between speed and accuracy depending on application requirements

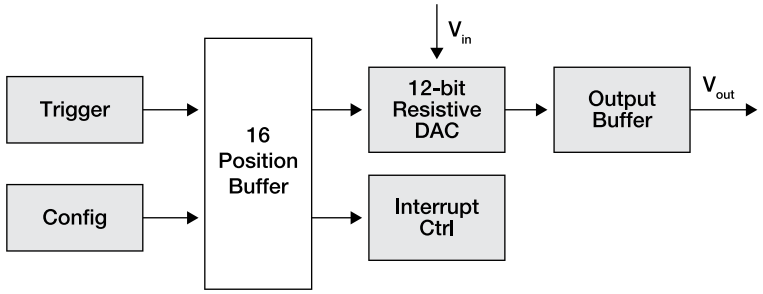
ADC Block Diagram



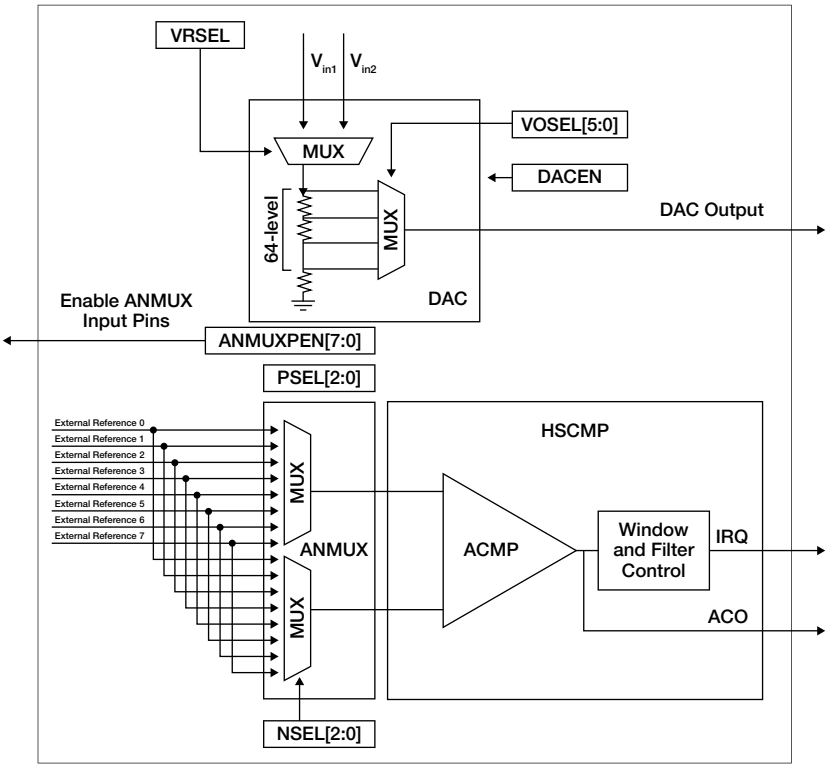
Peripheral	Key Features	Customer Benefits
16-bit analog-to-digital converter (ADC)	• Successive approximation architecture • Averaging • Self-test method • Interleaving	• Significantly faster and lower power than sigma delta (SD) ADC types. Resolution is comparable to SD types when averaging is employed
	• Differential inputs • Offset and gain calibration	• Improved noise rejection, dynamic range and measurement accuracy
12-bit digital-to-analog converter (DAC)	• Operation in low-power modes	• Increased battery life
	• Watermark FIFO	• No CPU intervention required for waveform generation–increased system performance
High-speed comparator (HSCMP)	• Internal DAC	• On-chip configurable voltage reference
	• Analog MUX	• Input signal flexibility for monitoring multiple sources

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

DAC Block Diagram



HSCMP Block Diagram



Digital-to-Analog Converter

The 12-bit digital-to-analog converter (DAC) provides a voltage output from a given digital value. Key features of the DAC module include:

- Output to external pin or internal connection to other peripherals
- Operation in stop modes
- Multiple modes: Swing, one-time scan or normal
- Multiple hardware interrupt request sources: Top or bottom positions or watermark

High-Speed Comparator (HSCMP)

The on-chip high-speed analog comparator modules provide a fast interrupt when monitoring an internal or external signal. The modules main features include:

- Operation over the entire voltage supply range
- Programmable hysteresis control
- Internal 6-bit DAC module with internal connection
- Internal input signal multiplex unit provides flexibility

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Voltage Reference

The voltage reference (VREF) is intended to supply an accurate voltage output that is trimmable by an 8-bit register in 0.5 mV steps.

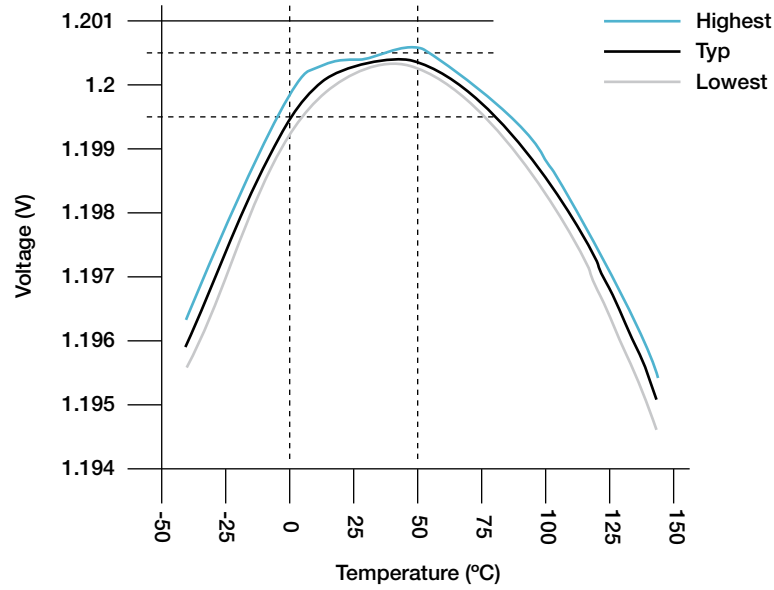
- Peripherals that can use VREF include ADC, DAC and HSCMP
- Off-chip peripherals can access the VREF output signal through the voltage reference output (VREFO) pin
- High-power mode for external use
- Temperature variation less than 33 ppm/C from 0° to 50°C

Programmable Delay Block

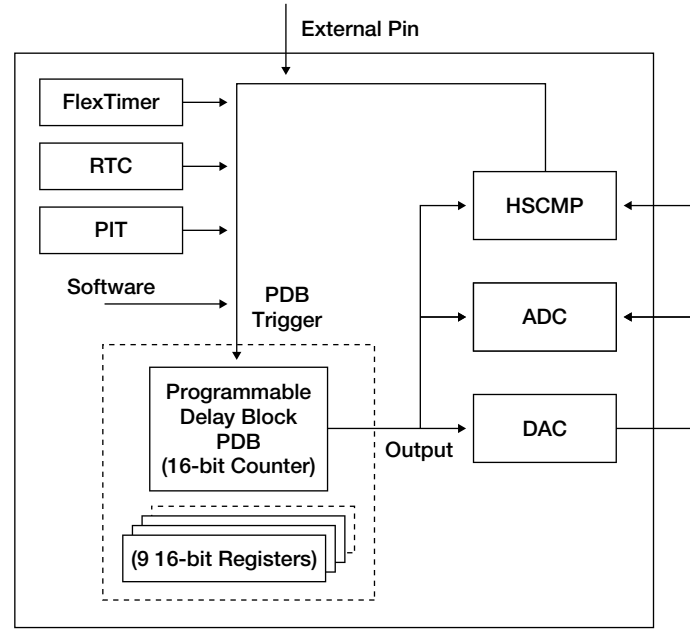
The programmable delay block (PDB) enables timing synchronization between multiple internal or external peripherals. Use case examples include:

- In BLDC motor control applications, to measure the back EMF voltage with the HSCMP, the PDB synchronizes a few microseconds after the FlexTimer pulse width modulation (PWM) rising-edge and creates a sample window mode
- In general motor control applications, the PDB measures voltages and currents for synchronizing the FlexTimer PWM and the ADC module
- In metering applications, the PDB measures both voltage and current with the ADC, synchronized with one of the timer modules
- In medical applications, the PDB provides a hardware trigger for the ADC and at the same time advances the DAC buffer pointer for signal conditioning

Curve: VREF (V) x Temperature (°C)

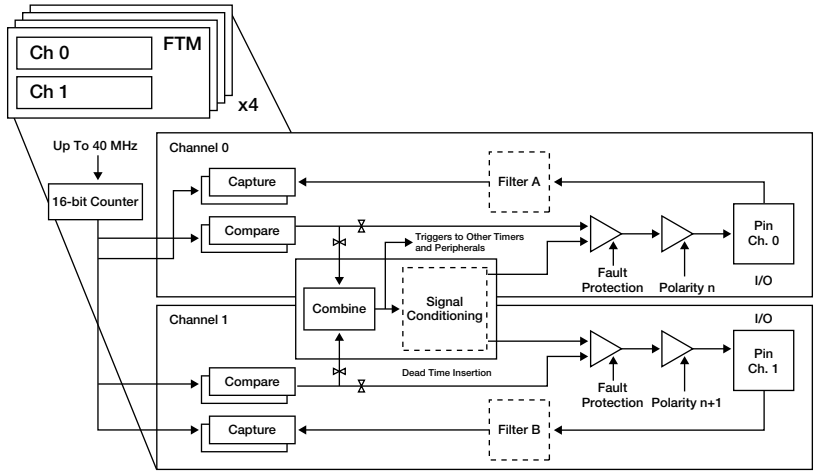


PDB Block Diagram

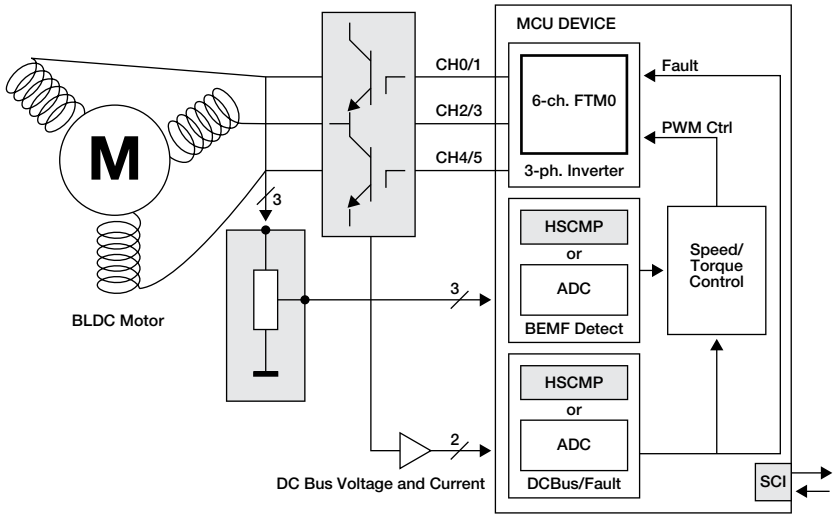


Peripheral	Key Features	Customer Benefits
Voltage reference (VREF)	Trimming: 8-bits register for 0.5 mV step	Higher accuracy, temperature, process and voltage deviation correction. Eliminates need for external voltage reference, reducing overall system cost
Programmable delay block (PDB)	Multiple peripheral integration modes for time-sensitive applications	Single set of peripherals can support a wide range of applications
FlexTimer (FTM)	Hardware dead timer insertion and quadarature decode	Suitable for motor control applications

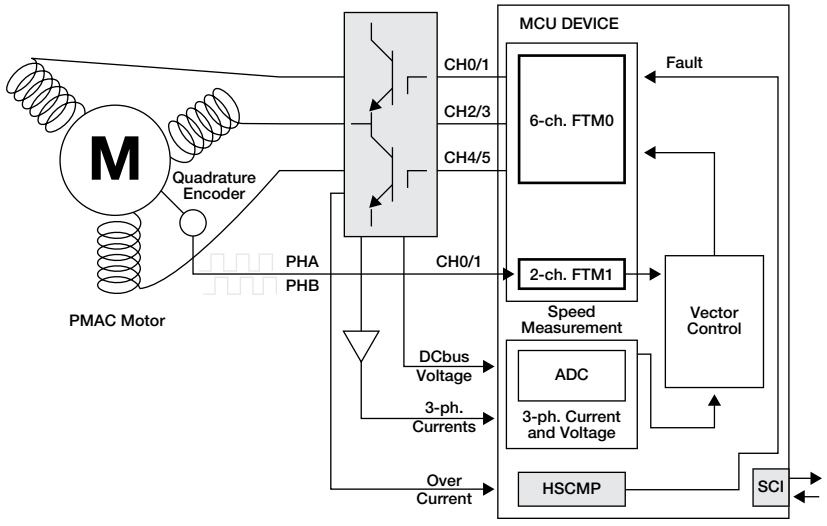
FlexTimer Block Diagram



Application Example: BLDC Motor Control



Application Example: PMAC Motor Control



FlexTimer

The FlexTimer module (FTM) is designed for motor control and power management applications but also retains standard timer features, such as output compare or input capture functions. In motor control environments, the FlexTimer provides complementary signal generation, hardware dead time generation, mask, polarity and fault control capabilities — features typical of dedicated PWM modules. This flexibility makes the FlexTimer suitable for a wide range of applications.

Motor Control Example

The peripheral sets for the ColdFire+ Qx/Jx and Kinetis microcontroller families enable 6-step vector control for brushless DC motor control using a sensorless algorithm. The high-speed comparator is used for back EMF detection, the 16-bit ADC for DC bus measurements and the FlexTimer in PWM mode. This enables a list of differentiating features, including:

- Automatic dead-time insertion
- Automatic duty-cycle load on channel pairs
- Independent control of both edges
- Maskable output
- Hardware input fault pin
- Event trigger inputs and outputs enable time-sensitive tasks

Permanent magnet sinusoidal motors (PMAC) are popular due to their high energy efficiency and precise control. The ColdFire+ Qx/Jx and Kinetis microcontroller families offer several features to enable full three-phase vector control:

- FlexTimer with advanced PWM features
- FlexTimer with quadrature decoder mode for speed detection
- Fast 16-bit SAR ADC for current and voltage measurement
- High-speed comparator for additional fault detection
- DSP instruction capabilities for high-speed calculations

Clocking System

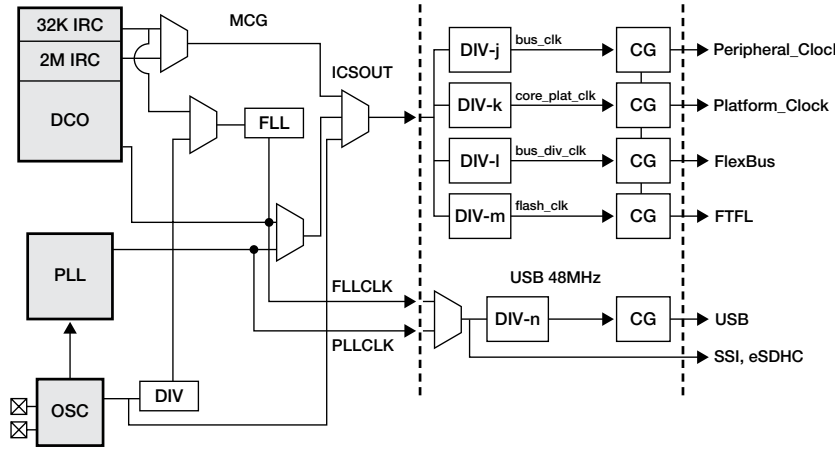
Multi-purpose clock generator

The clocking system generates the clock signals necessary to drive the core, platform peripherals (USB, DMA) and other general-purpose peripherals. The multi-purpose clock generator (MCG) is at the heart of the clocking system and controls how system clocks are generated. Separate clock divider control allows individual clocks to be fractionally divided and optimized for lower power operation.

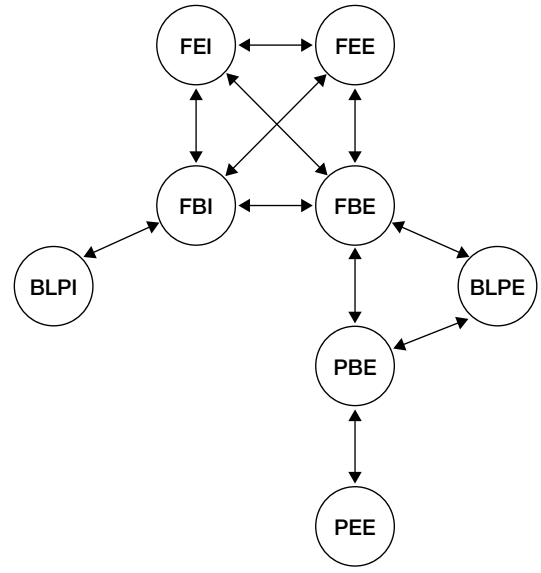
Depending on the input clock source and the system clock speeds required, the MCG can be placed into eight different modes of operation. The state diagram below highlights the different modes. For a full description, see the following table.

Each of the MCG modes can meet a different set of clocking requirements. This allows end applications to be optimized for cost, performance or power consumption. The MCG allows the user to easily change between modes.

Clock Diagram



MCG State Diagram



Key Features	Customer Benefits
Low- and high-frequency internal references for system clock generation	Lower system cost can be met with no crystal configurations to achieve maximum performance
Frequency-locked or phase-locked loop operation	MCG can be used in FLL or PLL modes. PLL modes allow for reduced jitter
Loss-of-lock and loss-of-clock protection circuits	Interrupts or resets can be generated based on the state of the MCG clock source

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

Mode	Description
FLL Engaged Internal (FEI)	In FEI mode, MCGOUT is derived from the FLL clock (DCOCLK), which is controlled by the 32 kHz internal reference clock (32 kHz IRC). The FLL loop will lock the DCO frequency to the FLL factor, as selected by the DRS[1:0] and DMX32 bits, multiplied by the internal reference frequency (32 kHz IRC). In FEI mode the PLL is disabled in a low-power state unless PLLCLKEN is set.
FLL Engaged External (FEE)	In FEE mode, MCGOUT is derived from the FLL clock (DCOCLK), which is controlled by the external reference clock. The FLL loop will lock the DCO frequency to the FLL factor, as selected by the DRS[1:0] and DMX32 bits, multiplied by the external reference frequency, as specified by the MCGC1[FRDIV] and MCGC2[RANGE]. In FEE mode the PLL is disabled in a low-power state unless PLLCLKEN is set.
FLL Bypassed Internal (FBI)	In FBI mode, the MCGOUT clock is derived either from the slow (32 kHz IRC) or fast (2 mHz IRC) internal reference clock, as selected by the IRCS bit. The FLL is operational but its output is not used. This mode is useful to allow the FLL to acquire its target frequency while the MCGOUT clock is driven from the IRCS selected internal reference clock. The FLL clock (DCOCLK) is controlled by the slow (32 kHz IRC) internal reference clock, and the DCO clock frequency locks to a multiplication factor, as selected by the DRS[1:0] and DMX32 bits, multiplied by the 32 kHz internal reference frequency. In FBI mode the PLL is disabled in a low-power state unless PLLCLKEN is set.
FLL Bypassed External (FBE)	In FBE mode, the MCGOUT clock is derived from the external reference clock. The FLL is operational but its output is not used. This mode is useful to allow the FLL to acquire its target frequency while the MCGOUT clock is driven from the external reference clock. The FLL clock (DCOCLK) is controlled by the external reference clock, and the DCO clock frequency locks to a multiplication factor, as selected by the DRS[1:0] and DMX32 bits, multiplied by the internal reference frequency. In FBI mode the PLL is disabled in a low-power state unless PLLCLKEN is set.
PLL Engaged External (PEE)	In PEE mode, the MCGOUT is derived from the PLL clock, which is controlled by the external reference clock. The PLL clock frequency locks to a multiplication factor, as specified by MCGC6[VDIV], multiplied by the external reference frequency, as specified by MCGC5[PRDIV]. The FLL is disabled in a low-power state.
PLL Bypassed External (PBE)	In PBE mode, MCGOUT is derived from the external reference clock. The PLL is operational, but its output clock is not used. This mode is useful to allow the PLL to acquire its target frequency while MCGOUT is driven from the external reference clock. The PLL clock frequency locks to a multiplication factor, as specified by MCGC6[VDIV], multiplied by the external reference frequency, as specified by MCGC5[PRDIV]. The FLL is disabled in a low-power state.
Bypassed Low-Power Internal (BLPI)	In BLPI mode, MCGOUT is derived from the internal reference clock. The FLL is disabled and PLL is disabled even if the PLLCLKEN is set to 1.
Bypassed Low-Power External (BLPE)	In BLPE mode, MCGOUT is derived from the external reference clock. The FLL is disabled and PLL is disabled even if the PLLCLKEN is set to 1.

IEEE® 1588 Ethernet Controller

Real-time networked measurement and control

The Ethernet controller module, in conjunction with an external 10/100 Ethernet PHY, is used to add Ethernet connectivity. Hardware IEEE 1588 time stamping provides precision clock synchronization for real-time control in networked automation, test and measurement applications. Features of the Ethernet controller include:

- Full implementation of the 802.3 specification
- Supports MII and RMII interfaces to external PHY
- Supports Advanced Micro Devices (AMD) Magic Packet detection
- Support for VLAN-tagged frames (IEEE 802.1Q)
- IP protocol performance optimizations
- Hardware time stamping support for IEEE 1588

AMD Magic Packet Detection

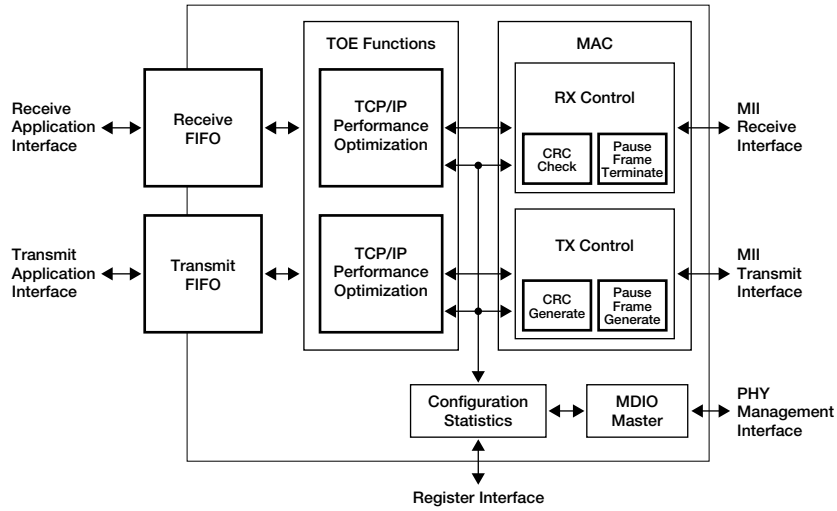
This utility allows an external node to make a remote wake-up request.

When Magic Packet detection is enabled, the Ethernet controller can be put into sleep mode and/or the processor can enter stop mode. In this mode:

- Ethernet transmit logic is disabled
- Ethernet FIFO receive/transmit functions are disabled
- Ethernet receive logic is kept in normal mode, but all incoming traffic except for Magic Packets are ignored

When a Magic Packet is detected, a wake-up request is sent to the core that can be used to exit the processor from stop mode.

Ethernet Controller Block Diagram



Key Features	Customer Benefits
AMD Magic Packet detection	Lower average power consumption
IP protocol performance optimizations	Higher Ethernet throughput
IEEE 1588 hardware time stamping	Reduced latency vs. software implementations–100 nS accuracy (network dependant)

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
○	○	○	○	○	○	●

IPv4 and IPv6 Checksum Calculations

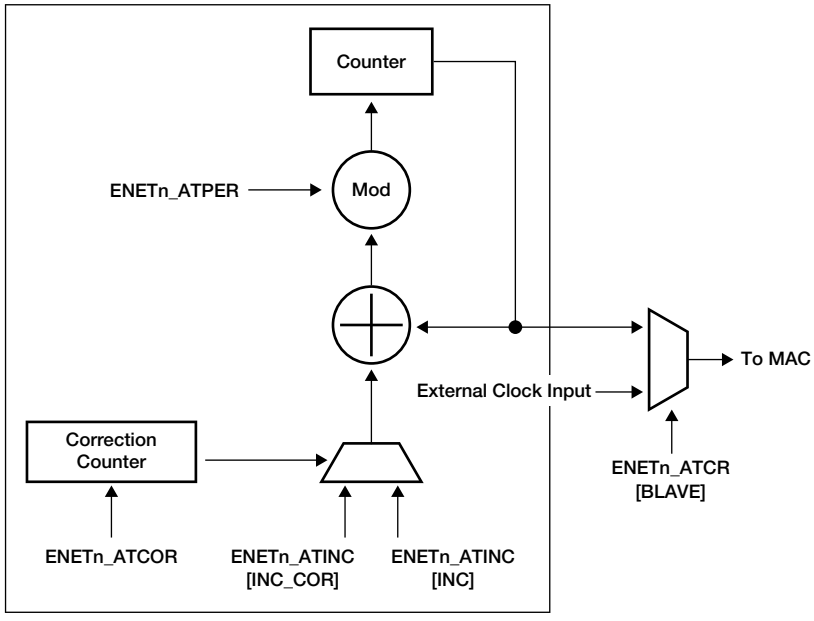
IPv4 Pseudo Header for Checksum Calculation

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Source Address							
Destination Address							
Zero		Protocol		TCP/UDP Length			

IPv6 Pseudo Header for Checksum Calculation

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Source Address							
Destination Address							
TCP/UDP Length							
Zero						Next Header	

Adjustable Timer



IP Protocol Optimization

The Ethernet controller module includes hardware logic that can handle a range of common Ethernet protocol functions. This helps to decrease the software overhead required for Ethernet stacks and can increase overall Ethernet throughput.

Features include:

- Support for TCP/IP, UDP/IP, ICMP/IP and IP header-only protocols in IPv4 and IPv6 formats
- Automatic IP header and payload (protocol specific) checksum generation and calculation
- Transparent passing of frames of other types and protocols

For TCP and UDP, the checksum is calculated over the header and data sections along with some values from the IP header. The diagram below shows the IP header fields that are used for TCP and UDP checksum calculations.

IEEE 1588 Support

The Ethernet controller includes a hardware time-stamping module to support IEEE 1588 or similar time synchronization protocol implementations.

The adjustable timer module is used to synchronize the Ethernet controller's local clock to a remote master. There is a free running 32-bit counter and a second correction counter. The correction counter increases or decreases the rate of the free running counter, enabling very fine granular changes of the timer for synchronization.

Universal Asynchronous Receiver/Transmitter

A flexible approach to full-duplex serial communication

The universal asynchronous receiver/transmitter (UART) module allows for asynchronous, full-duplex serial communication in a variety of formats. Features of the UART include:

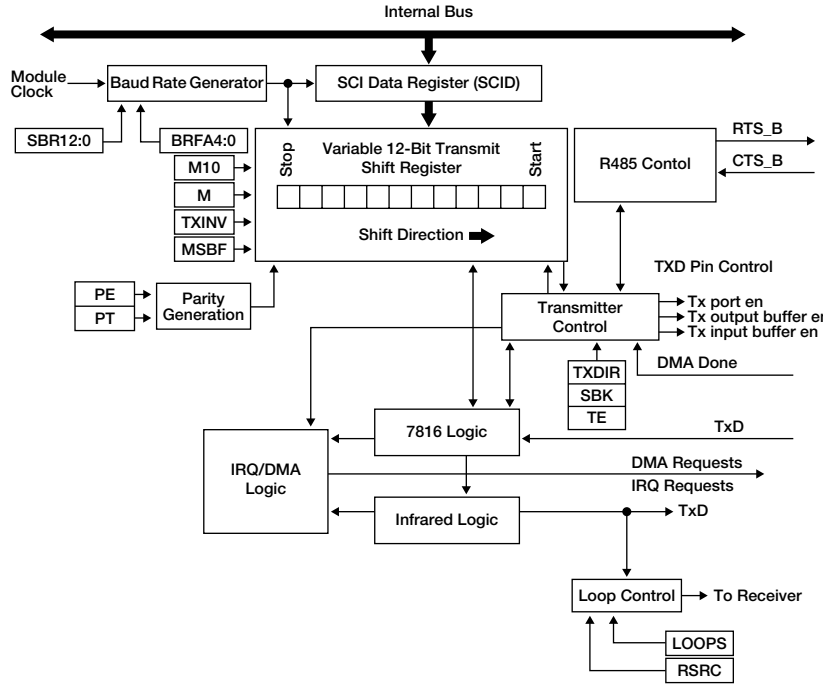
- Standard mark/space non-return-to-zero format (NRZ)
- Supports IrDA 1.4 return-to-zero-inverted (RZI) format
- Supports ISO 7816 protocol for interfacing with SIM cards and smartcards (feature supported on one UART module only)
- 13-bit baud rate selection with by-32 fractional divide
- Programmable eight- or nine-bit data formats
- Ability to select MSB or LSB to be first on the wire
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Separate transmit and receive (feature supported on two UART modules only) FIFOs with DMA request capability

ISO 7816 Support

One of the UART modules supports the ISO 7816 standard, allowing communication with SIM cards and smartcards. This feature has the following characteristics:

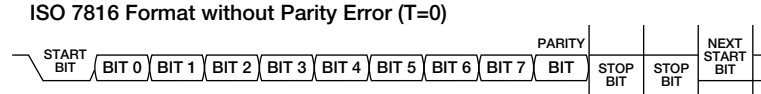
- Supports T=0 and T=1 protocols
- Automatic retransmission of NACKed packets with programmable retry threshold
- Supports 11 and 12 ETU transfers
- Detects initial packet and automated transfer parameter programming
- Interrupt-driven operation with seven ISO-7816 specific interrupts:

UART Transmit Logic



ISO 7816 Timing Diagrams

ISO 7816 Format without Parity Error (T=0)



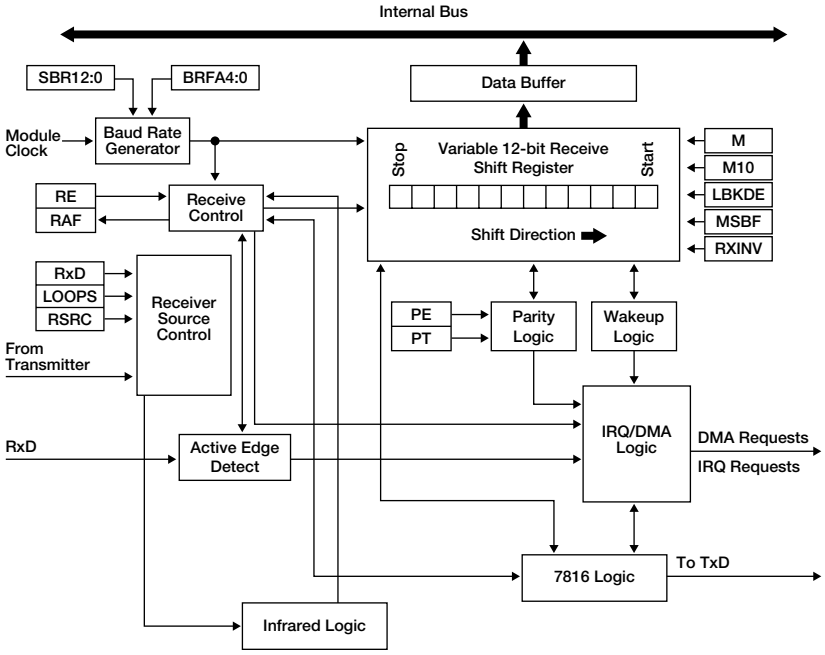
ISO 7816 Format with Parity Error (T=0)

ISO 7816 Format (T=1)

Key Features	Customer Benefits
ISO 7816 protocol support	Support for SIM and smart cards
Large number of communication formats available	Flexibility to implement a variety of serial communication protocols
FIFOs with DMA request capability	Decreased CPU loading

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

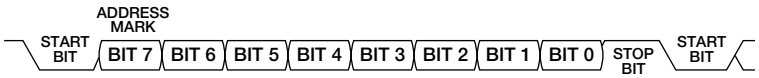
UART Receive Logic



UART Data Formats

Eight Bits of Data with LSB First

Eight Bits of Data with MSB First



Nine Bits of Data with LSB First

Nine Bits of Data with MSB First

- Wait time violated
- Character wait time violated
- Block wait time violated
- Initial character detected
- Transmit error threshold exceeded
- Receive error threshold exceeded
- Guard time violated

Variety of Communications Formats Available

The UART offers a number of options for data size, format and transmission/reception settings. The variety of available options makes the UART capable of implementing a wide variety of serial communications protocols.

Features include:

- Eight- and nine-bit data formats supporting parity over all nine bits
- MSB or LSB first on wire
- Programmable transmitter output polarity
- Programmable receiver input polarity

FIFOs with DMA Request Capability

The UART FIFOs reduce the frequency of CPU processing required by the UART.

The DMA can be configured to transfer an entire packet of data and then interrupt the CPU when all bytes are received. This means the CPU can process the entire packet all at once instead of needing to stop the current program flow to move data bytes as they are received.

The size of the FIFOs vary depending on the particular device and the specific UART. Most devices will implement an 8-byte receive and 8-byte transmit FIFO on UART0 and UART1, and no FIFOs on the remaining UARTs.

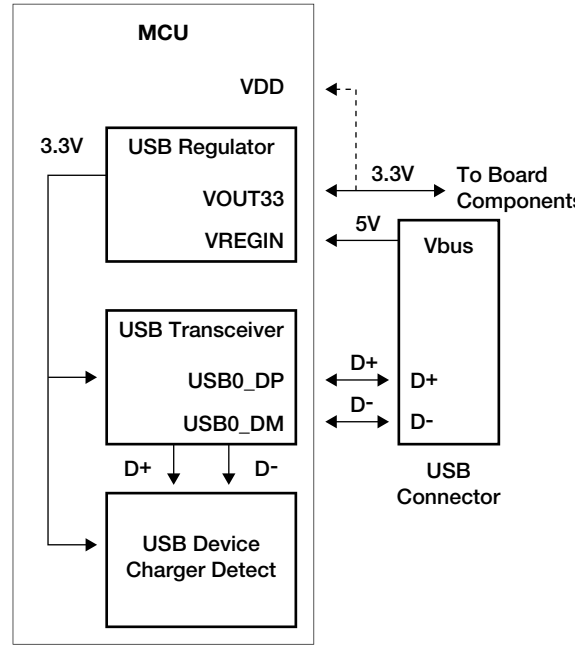
USB Subsystem

Flexible USB connectivity

The USB subsystem is comprised of several blocks that, together, provide full, flexible USB functionality. The USB subsystem includes:

- USB On-The-Go (OTG) 2.0 compliant controller (specific controller depends on the device). Options are:
  - Full-speed (FS)/low-speed (LS) USB controller
  - High-speed (HS)-capable controller (Kinetis K20 and K60 families only). HS option supported using external ULPI PHY
  - On-chip FS/LS USB transceiver
  - USB regulator
  - USB device charger detect (DCD)

USB Regulator



FS/LS Controller

The USB FS/LS controller provides USB host and device communications along with support for OTG operation. The FS/LS controller is USB 2.0 compliant and supports full-speed (12 Mbps) and low-speed (1.5 Mbps) data transfer rates.

The FS/LS controller is always used with the on-chip FS/LS transceiver block. The on-chip transceiver includes internal pulldown resistors on the D+ and D- lines and an internal pullup resistor on the D+ line. This helps to reduce the number of external components needed for USB connectivity.

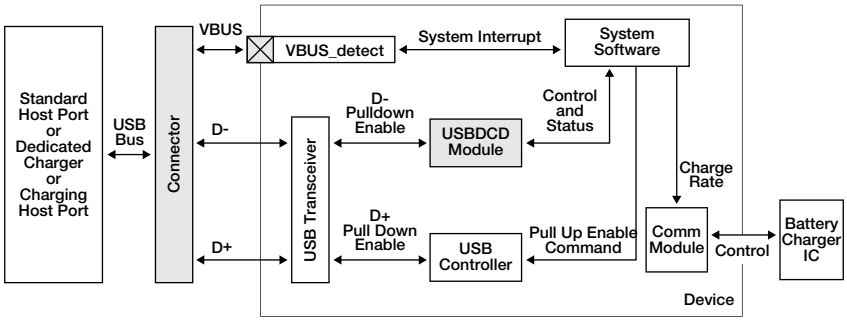
HS-Capable Controller

The USB HS-capable controller provides USB host and device communications along with support for OTG operation. The HS-capable controller is USB 2.0 compliant. The controller supports HS (480 Mbps), FS (12 Mbps) device and OTG operation; the controller supports HS/FS/LS host operation.

The HS-capable controller can be used with an optional external UTMI+ low pin interface (ULPI) PHY to support HS mode. If HS operation is not needed, the on-chip FS/LS transceiver can be used instead.

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
○	●	○	●	○	●	●

USB Device Charger Detect



USB Regulator

The USB regulator generates a 3.3V supply from the USB VBUS or a rechargeable battery supply.

The USB regulator is an LDO linear voltage regulator module that provides 3.3V from an input power supply varying from 2.7 to 5.5V. The 3.3V output from the regulator is used to power the on-chip USB transceiver and device charger detect. The output pin (VOUT33), capable of sourcing up to 120 mA, can be used to power external board components and/or the MCU main power supply. This eliminates the cost of external LDO.

USB Device Charger Detect

The USB device charger detect (USBDCD) module works with the USB transceiver to detect if the USB device is attached to a charging port (either a dedicated charging port or a charging host). By properly identifying the type of charging port, the MCU can now control the battery charging IC requesting higher current draw from USB VBUS, making the product a smart charging device. Traditionally, a USB subsystem without USBDCD hardware would only receive the minimal current draw for charging from USB VBUS. The advantage is that the charging current/time is optimized.

Features include:

- Complies with the latest industry-standard specification, USB Battery Charging Specification, Revision 1.1
- Programmable timing parameters default to values required by industry standards:
  - Standard default values allow minimal configuration
  - Programmability allows the flexibility to meet future standards updates
- Compatible with systems powered from:
  - Rechargeable battery
  - Non-rechargeable battery
  - External 3.3V LDO regulator powered from USB or directly from USB using internal regulator

External Interfaces

System expansion and off-chip data storage

The Kinetis MCU families support a wide variety of external interfaces, including a DRAM controller, FlexBus external bus interface and NAND flash controller. ColdFire+ Qx and Jx families include a Mini FlexBus external bus interface.

DRAM Controller

The DRAM controller enables users to connect large amounts of DRAM to the MCU. This means that applications are not limited to internal SRAM, opening the doors for new use cases. The main features of this block are:

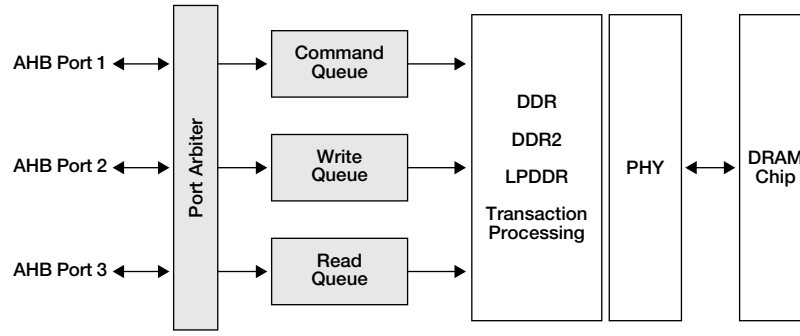
- Enables the MCU family to be used in applications that require access to large amounts of memory—supports up to 512 MB of external memory
- 8- and 16-bit external data bus interfaces
- Maximum frequency (clock/data) 150/300 MHz
- Supports DDR, DDR2 and LPDDR memory types
- Fully asynchronous operation with an independent PLL
- Supports dynamic on-die termination both in the host device and in the DRAM
- Supports one chip select and up to eight bank devices
- Supports bursts of 16 and 32 bytes, independent byte lane timing and very robust timing recovery for simplified board routing
- Supports low-power modes

Mini FlexBus/FlexBus

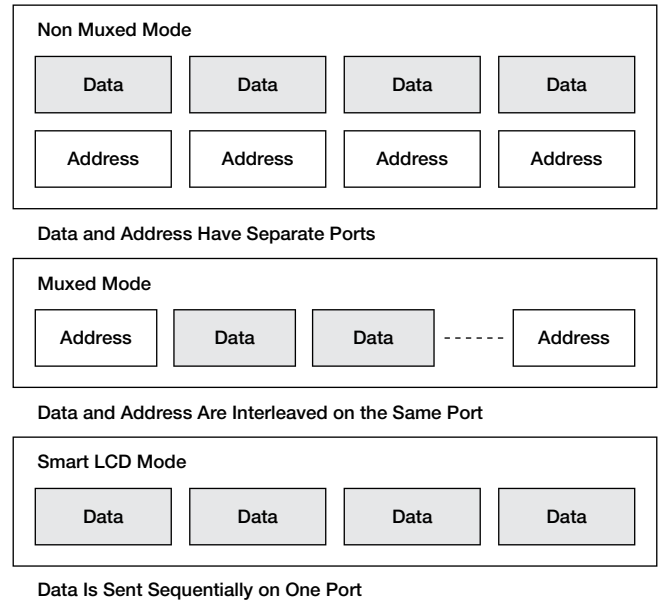
The Mini FlexBus interface on the ColdFire+ family devices is designed to connect with up to two external devices. The FlexBus interface on the Kinetis family devices is designed to connect with up to six external devices. Each version has 8-, 16- and 32-bit port sizes with configuration for multiplexed or non-multiplexed addresses and data buses. Features include:

- Byte-, word-, longword- and 16-byte line-sized transfers
- Programmable burst and burst-inhibited transfers selectable for each chip select and transfer direction
- Auto-acknowledge feature
  - Primary wait state counter up to 63 clocks
  - Optional secondary wait state counter
  - Useful for interfacing to burst memories that have a long access time for the first chunk of data, but can deliver subsequent data faster
- Programmable address setup time with respect to the assertion of chip select
- Programmable address hold time with respect to the negation of chip select and transfer direction

DRAM Controller



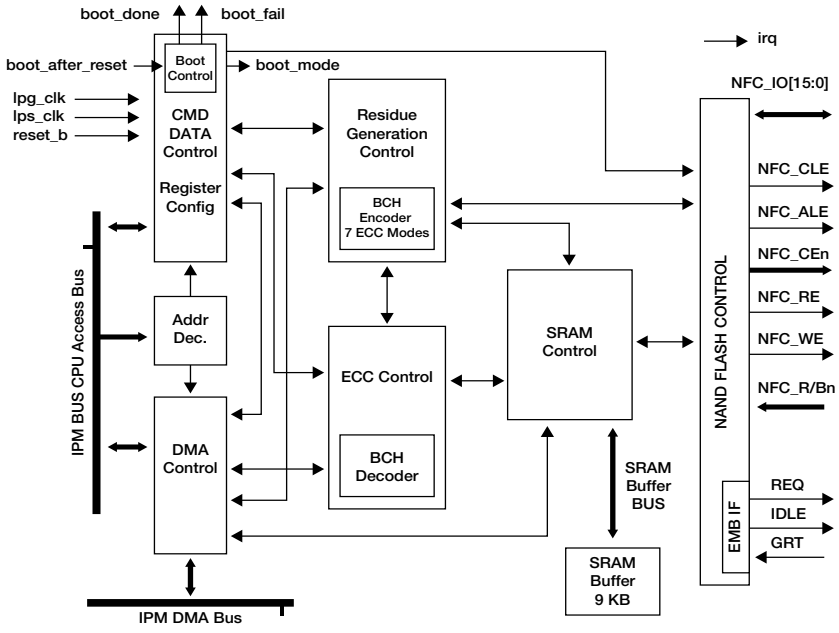
FlexBus Modes of Operation



ColdFire+		Kinetis*				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

Peripheral	Key Features	Customer Benefits
FlexBus	8-, 16-, 32- and 128-bit line sized transfers	Maximize throughput according to the specific application
	Programmable burst and burst-inhibited transfers selectable for each chip select and transfer direction	Optimized traffic patterns for each client in the bus
	Auto-acknowledge feature	Increased flexibility and lower BOM costs in glueless external device connections
	Programmable address-setup time	
	Programmable address-hold time	
DRAM Controller	Supports DDR, DDR2 and LPDDR memory types	The power vs performance trade-off can be optimized for the application
	Fully asynchronous operation with an independent PLL	DRAM operating frequecy can be set independently of the system frequency
	Supports bursts of 16 and 32 bytes with independent byte lane timing and very robust timing recovery	Reduced complexity in board routing and component selection
	Supports low-power modes	Minimizes overall system power consumption

NAND Flash Controller Block Diagram



*External interfaces are offered on the following families:
DRAM Controller: Kinetis K60
Mini FlexBus: ColdFire+ Qx/Jx
FlexBus: Kinetis K10/K20/K30/K40/K60
NAND Flash Controller: Kinetis K10/K20/K60

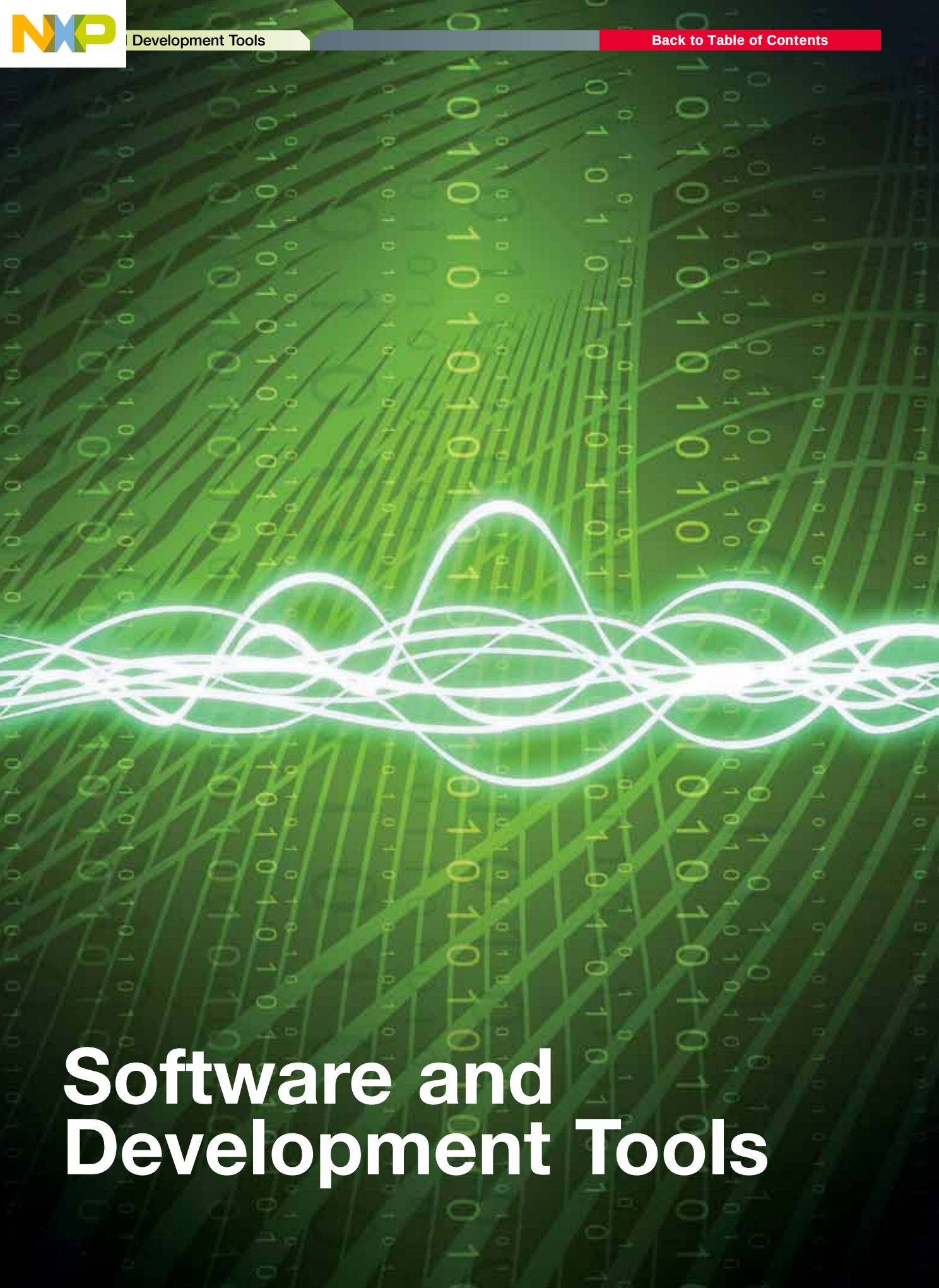
FlexBus supports the connection to:

- Flash
- Smart LCDs
- FPGAs
- SRAM
- PROM
- EPROM
- EEPROM

NAND Flash Controller

The NAND flash controller (NFC) enables a glueless connection to MLC NAND memories. The heavy load of error correction code (ECC) calculations are handled in hardware and up to 32-bit ECC helps ensure that current and foreseeable generations of MLC NAND memories are supported. The main features of this block are:

- 8-/16-bit NAND flash interface
- Memory mapped registers and SRAM buffer
- Supports all NAND flash products regardless of density/organization (with page sizes of 512+16B/2 KB+ 64B/4 KB+128B/4 KB+218B/8 KB)
- Supports flash device commands such as page read, page program, reset, block erase, read status, read ID, copy-back, multiplane read/program, interleaved read/program, random input/output and read in EDO mode
- In bypassable ECC mode, the NFC supports 4-, 6-, 8-, 12-, 16-, 24- and 32-bit error correction
- Two configurable DMA channels: Use DMA channel 1 to read/write the main area of a page, and DMA channel 2 for the spare area. Use DMA channel 1 only to read/write a page for both main and spare areas of a page



Software and Development Tools

Freescale MQX™ Software Solutions

Complimentary full-featured RTOS

Freescale streamlines embedded design with a complimentary real-time operating system and software stacks

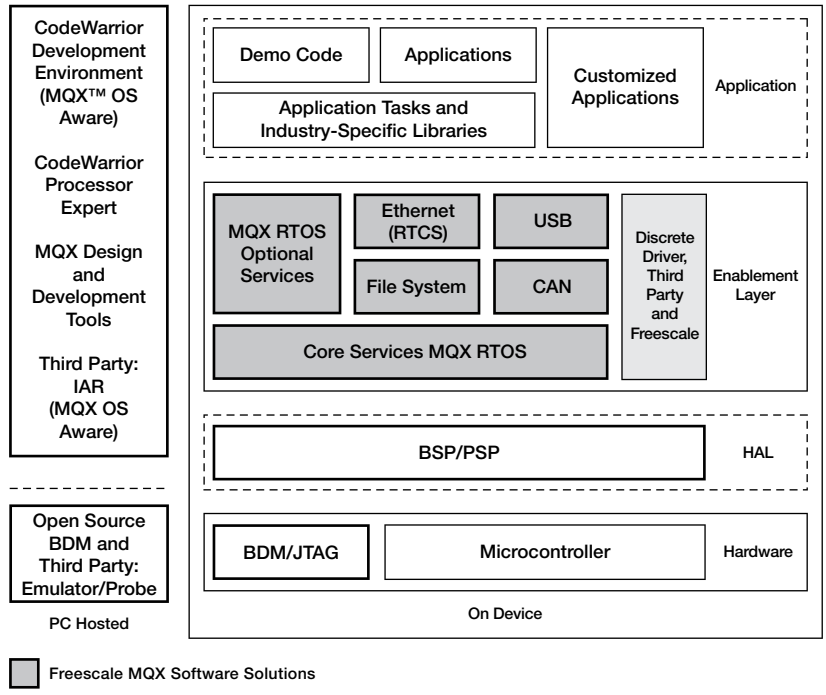
The increasing complexity of industrial applications and expanding functionality of semiconductors are driving embedded developers toward solutions that combine proven hardware and software platforms. To help accelerate time to market and improve application development success, Freescale is offering the MQX real-time operating system (RTOS) with TCP/IP and USB software stacks and peripheral drivers to ColdFire, ColdFire+ and Kinetis MCU customers at no additional charge. The combination of Freescale MQX software solutions and our silicon portfolio creates a comprehensive source for hardware, software, tools and services.

Reducing Cost, Accelerating Success

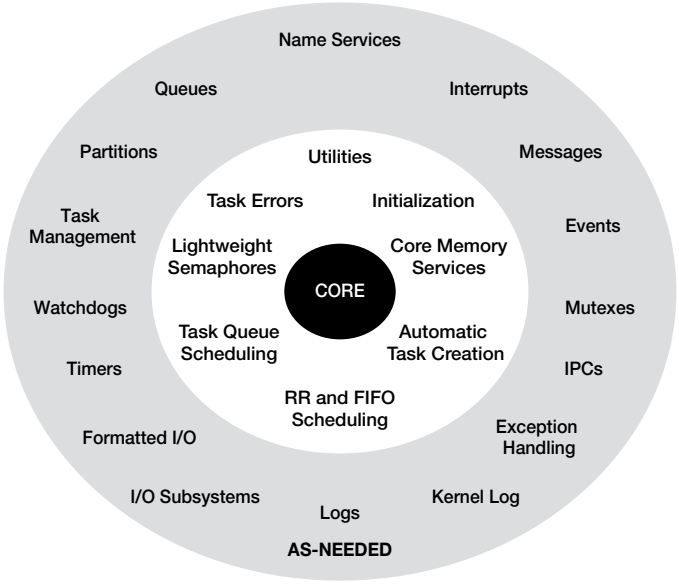
By providing complimentary Freescale MQX software solutions with its silicon products, Freescale helps alleviate much of the initial software investment hurdle faced by embedded developers. Comparable full-featured software offerings may cost developers as much as $95,000 (USD) in licensing fees.

Continued on next page

Freescale Comprehensive Solution



MQX RTOS: Customizable Component Set



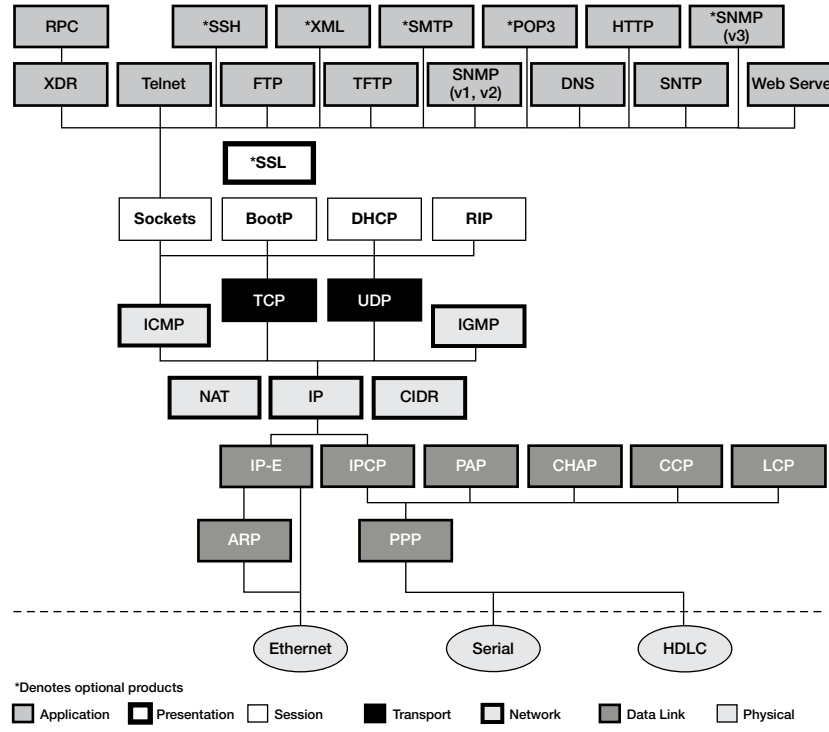
Freescale MQX Software Solutions

Continued from previous page

According to recent research, development teams spend approximately 60 percent of their resources on software. Embedded projects based on 32-bit devices have a greater need for software reuse to manage development costs. The Freescale MQX RTOS and software stacks address these developer needs by providing a scalable, reusable platform that works across a wide range of Freescale processor architectures, development tools and third-party software environments.

Freescale MQX is deployed as production-ready source code, including communications software stacks and peripheral drivers, at no additional cost. Freescale MQX is provided with a commercial-friendly software licensing model, enabling developers to keep their source modifications while being able to distribute the required binary code.

RTCS TCP/IP Stack



Full Featured, Proven and Scalable

The MQX RTOS has been the backbone of embedded products based on Freescale silicon for more than 15 years. MQX software deployment spans a broad range of market segments and leading manufacturers worldwide.

The Freescale MQX RTOS offers powerful, preemptive real-time performance with optimized context switch and interrupt time, enabling fast, highly predictable response times. Its small, configurable size conserves memory space for embedded applications and it can be configured to take as little as 6 KB of ROM, including kernel, interrupts, semaphores, queues and memory manager.

The Freescale MQX RTOS offers a straightforward application programming interface (API) with a modular, component-based architecture that makes it very scalable. Components are linked in only if needed, preventing unused functions from bloating the memory footprint. Plug-ins, such as security, industrial protocols and graphical interfaces from Freescale's strong network of partners, can also be added.

Certifiable to Medical and Aerospace Standards

Even if your application does not require formal certification, the robustness of MQX provides a trusted platform that has been proven in thousands of time-critical, sophisticated applications. For designs that do have a formal certification process to follow, MQX is an excellent choice. Past licensees have certified MQX-based applications to medical specifications (CFR 820.30 Part 21, IEC 60601-1) and the aerospace requirements listed under DO-178b. Safety critical applications based on MQX include eye surgery equipment, drug injection equipment, radiation dose monitoring equipment, aircraft braking systems and aircraft navigation equipment.

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

Freescale MQX Add-on Software	
Real-Time TCP/ IP Communication Suite (RTCS) Optional Components Available from Embedded Access Inc.	• Network management: Support for SNMP version 1 and 2 is built into RTCS. EAI offers MQX SNMPv3 • XML parsing and framing: The MQX XML component enables your device to accept data in XML, as well as send data packaged in XML • e-Mail communication: The MQX SMTP module provides your device with outbound e-mail communication and MQX POP3 provides the capability to accept incoming e-mail communication
NanoSSL™ and NanoSSH™ software by Mocana available from Freescale Semiconductor	• NanoSSH: Provides privacy, authentication and ensures data integrity between a secure server and its clients • NanoSSL: Cyptographic protocols that provide security for communications over networks such as the Internet
PEG + Graphics Library Available from Embedded Access Inc.	• Portable embedded GUI library designed to provide a professional-quality GUI for embedded systems applications • Small, fast and easily ported to virtually any hardware configuration capable of supporting graphical output
SEGGER emWin Graphics Library/GUI Available from SEGGER Microcontroller	• emWin is designed to provide an efficient, LCD controller-independent GUI for any application that operates with a graphical LCD
CANOpen Master/Slave for Embedded Devices Available from IXXAT, Inc.	• CANopen is a CAN-based higher layer protocol • Developed as a standardized embedded network with highly flexible configuration capabilities • Unburdens the developer from dealing with CAN-specific details such as bit-timing and implementation-specific functions
Industrial Network and Field Bus Protocols Available from IXXAT, Inc.	• Profinet RT for I/O device • EtherNet/IP for adapter and scanner • Ethernet powerlink for managing and controlled nodes • EtherCAT for slave nodes • SERCOS III for slave devices • Precision time protocol IEEE 1588-2008 (v2)
SFFS Flash File System Available from Embedded Access Inc.	• SFFS is a safe flash file system that can support almost any NOR or NAND flash device • Provides a high degree of reliability and complete protection against unexpected power failure or reset events • Provides wear leveling, bad block handling and ECC K30C algorithms to ensure you get optimal use out of a flash device • Pre-integrated with the MQX RTOS: allows you to create a robust file system quickly for an embedded device using on-chip or on-board flash devices

Freescale MQX Real-Time TCP/IP Communication Suite

The Freescale MQX real-time communication suite (RTCS) is a fast, efficient and low-footprint embedded Internet stack that supports a rich set of standard TCP/IP protocols. It comes complete with a number of application layer protocols such as Telnet, FTP, SNMP v1 and SNMP v2. A number of optional, pre-integrated protocols and products are also available from third parties.

The Freescale MQX RTCS is scalable, allowing you to easily define the feature set you want to accommodate your ROM and RAM memory budgets.

For more information about the Freescale MQX platform, please visit **freescale.com/MQX**.

Freescale Tower System

A modular development platform

Overview

The Freescale Tower System is a modular development platform for 8-, 16- and 32-bit microcontrollers that enables advanced development through rapid prototyping. Featuring multiple development boards or modules, the Tower System provides designers with building blocks for entry-level to advanced microcontroller development.

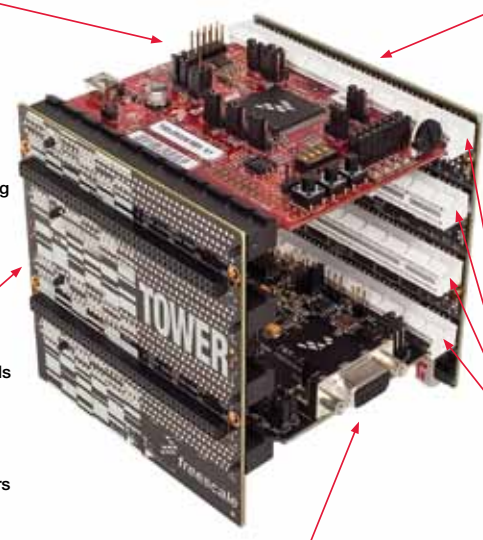
Modular and Expandable

- Controller modules provide easy-to-use, reconfigurable hardware
- Interchangeable peripheral modules—serial, memory and graphical LCD—make customization easy
- Open-source hardware and standardized specifications promote the development of additional modules for added functionality and customization

Speeds Development Time

- Open source hardware and software allows quick development with proven designs
- On-board debug hardware for easy programming and debugging using only a standard USB cable

The Freescale Tower System



Controller Module

- Tower MCU/MPU board
- Works stand-alone or in Tower System
- Features integrated debugging interface for easy programming and run-control via standard USB cable

Secondary Elevator

- Additional and secondary serial and expansion bus signals
- Standardized signal assignments
- Mounting holes and expansion connectors for side-mounting peripheral boards

Size

- Tower is approx. 3.5” H x 3.5” W x 3.5” D when fully assembled

Peripheral Module

- Examples include serial interface module, memory expansion module and Wi-Fi®

Primary Elevator

- Common serial and expansion bus signals
- Two 2x80 connectors on backside for easy signal access and side-mounting board (LCD module)
- Power regulation circuitry
- Standardized signal assignments
- Mounting holes

Board Connectors

- Four card-edge connectors
- Uses PCI Express® connectors (x16, 90 mm/ 3.5” long, 164 pins)

Controller Modules	Features
Kinetis K40 Family: **TWR-K40X256** (K40 MCU module) **TWR-K40X256-KIT** (K40 MCU module + elevator modules + serial module)	• 256 KB flash MCU, 256 KB FlexMemory in 144 MAPBGA package • On-board JTAG debug interface • Access to all features, including segment LCD and USB
Kinetis K60 Family: **TWR-K60N512** (K60 MCU module) **TWR-K60N512-KIT** (K60 MCU module + elevator modules + serial module)	• 512 KB flash MCU, non FlexMemory in 144 MAPBGA package • On-board JTAG debug interface • Access to all features, including Ethernet and USB
ColdFire+ JF Family MCU Module	• 128 KB flash MCU in \64 LQFP package • On-board BDM debug interface • Access to all features, including USB
ColdFire+ QM Family MCU Module	• 128 KB flash MCU in 64 LQFP package • On-board BDM debug interface • Access to all features, including 16-bit ADC

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

Tower System Modules	
Features	**Benefits**
Controller Modules (8-, 16-, 32-bit)	
Works stand-alone or as part of Tower System	Allows rapid prototyping
Features on-board debug interface	Provides easy programming and debugging via mini-B USB cable
Peripheral Modules	
Can be re-used with all Tower System MCU/MPU modules	Eliminates the need to buy/develop redundant hardware
Interchangeable peripheral modules—serial, memory, graphical LCD, prototyping and more	Enables advanced development and broad functionality
Elevator Boards	
Two 2x80 connectors	Provides easy signal access and enables side-mounting modules (i.e. LCD module)
Power regulation circuitry	Provides power to all boards
Standardized signal assignments	Allows for customized peripheral module development
Four card-edge connectors available	Allows easy expansion using PCI Express connectors (x16, 90 mm/3.5" long, 164 pins)

Available Tower System Modules		
Controller Modules	**Price**	**Features**
TWR-MCF51CN	$39	MCF51CN ColdFire V1 Ethernet module
TWR-MCF5225X	$49	MCF5225X ColdFire V2connectivity module
TWR-S08LL64	$69	MC9S08LL64 8-bit segment LCD module
TWR-S08LH64	$69	MC9S08LH64 8-bit segment LCD module with integrated 16-bit ADC
TWR-MPC5125	$119	MPC5125 e300c4 Power Architecture® module
TWR-MCF51MM	$59	MCF51MM ColdFire V1microcontroller module designed for medical applications
TWR-S08MM128	$59	MC9S08MM128 8-bit microcontroller module designed for medical applications
TWR-MCF51JE	$69	MCF51JE ColdFire V1 USB microcontroller module
Peripheral Modules	**Price**	**Features**
TWR-SER	$49	Serial module with RS232/RS485, Ethernet, CAN, USB
TWR-ELEV	$29	Elevator modules: Primary and Secondary
TWR-PROTO	$14.99	Prototyping module
TWR-LCD	$99	Graphical LCD module with 3.2" QVGA display
TWR-MEM	$89	Memory module with serial flash, MRAM, SD card and compact flash interfaces
TWR-SENSOR-PAK	$149	Swappable sensor module with accelerometer, barometer and touch-sensing controller
Complete Kits	**Price**	**Includes**
TWR-MCF51CN-KIT	$99	TWR-MCF51CN, TWR-SER and TWR-ELEV modules
TWR-MCF5225X-KIT	$119	TWR-MCF5225X, TWR-SER and TWR-ELEV modules
TWR-S08LL64-KIT	$99	TWR-S08LL64, TWR-PROTO and TWR-ELEV modules
TWR-S08LH64-KIT	$99	TWR-S08LH64, TWR-PROTO and TWR-ELEV modules
TWR-MPC5125-KIT	$169	TWR-MPC5125, TWR-SER and TWR-ELEV modules
TWR-MCF51MM-KIT	$149	TWR-MCF51MM, TWR-SER, TWR-ELEV and MED-EKG modules
TWR-S08MM128-KIT	$149	TWR-S08MM128, TWR-SER, TWR-ELEV and MED-EKG modules
TWR-MCF51JE-KIT	$119	TWR-MCF51JE-KIT, TWR-SER and TWR-ELEV modules

Cost Effective

- Peripheral modules can be re-used with all Tower System controller modules, eliminating the need to purchase redundant hardware for future designs
- Enabling technologies like LCD, serial and memory interfacing are offered off-the-shelf at a low cost to provide a customized enablement solution

Software Enablement and Support

The increasing complexity of industrial applications and expanding functionality of semiconductors are driving embedded developers toward solutions that require the integration of proven hardware and software platforms. Freescale, along with a strong alliance network, offers comprehensive solutions including development tools, debuggers, programmers and software.

Take Your Design to the Next Level

For a complete list of development kits and modules offered as part of the Freescale Tower System, please visit **freescale.com/Tower**.

Join the online community of Tower Geeks. Interact. Explore. Create. **towergeeks.org**

CodeWarrior Development Studio

Based on the Eclipse open development platform

Freescale's CodeWarrior Development Studio for Microcontrollers v10.x integrates the development tools for the RS08, HCS08, ColdFire, ColdFire+ and Kinetis architectures into a single product based on the Eclipse open development platform. Eclipse offers an excellent framework for building software development environments and is becoming a standard framework used by many embedded software vendors.

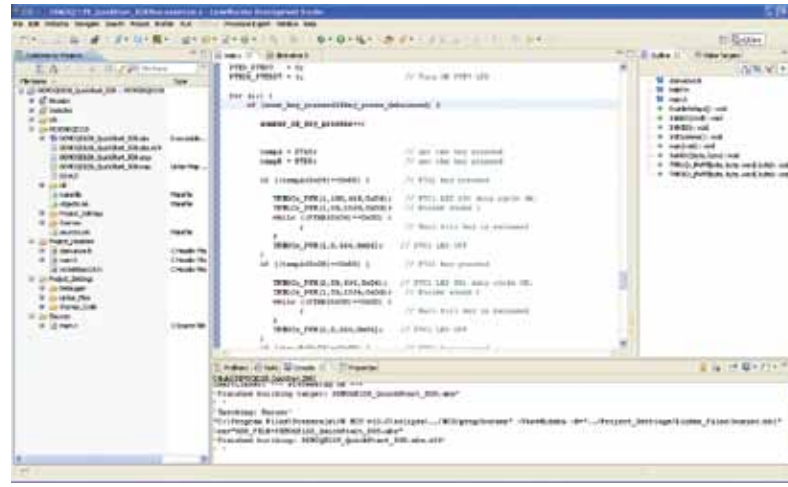
- Eclipse IDE 3.4
- Build system with optimizing C/C++ compilers for HCS08, RS08, ColdFire, ColdFire+ and Kinetis processors
- Extensions to Eclipse C/C++ development tools (CDT) to provide sophisticated features to troubleshoot and repair embedded applications

MCU Change Wizard

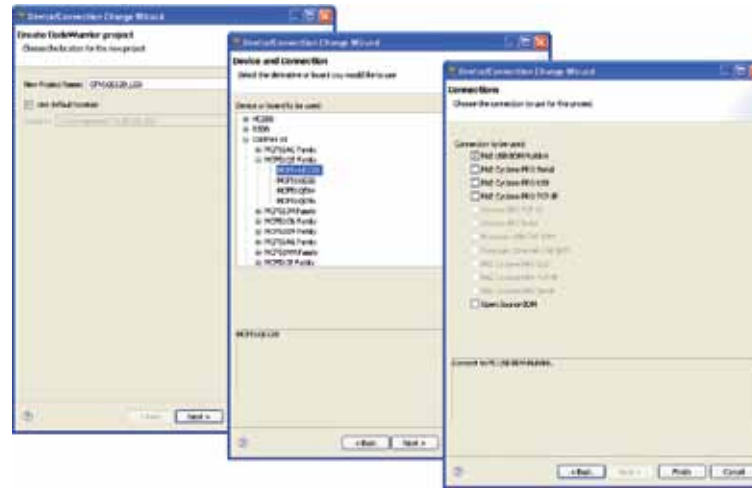
The MCU Change Wizard allows a project to be re-targeted to a new processor in as few as six mouse clicks. Simply select a new device (from the same or a different architecture—RS08, HCS08, ARM or ColdFire), select the default connection and the CodeWarrior tool suite will automatically reconfigure the project for the new device with the correct build tools and support files.

- Compiler
- Assembler
- Linker
- Header files
- Vector tables
- Libraries
- Linker configuration files

C/C++ Perspective



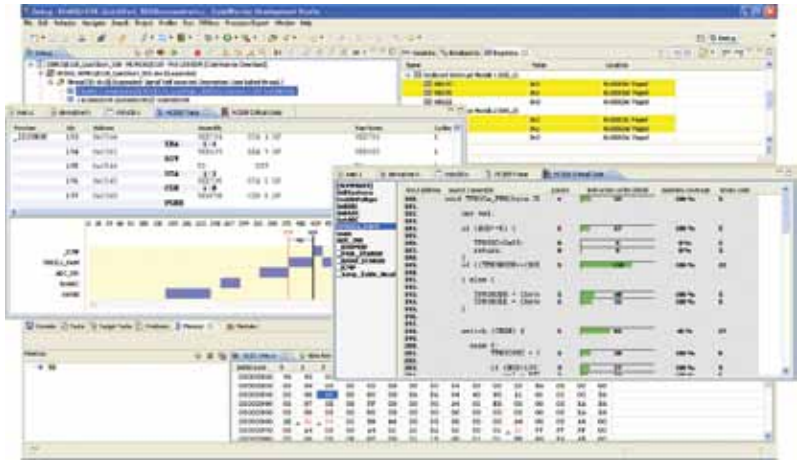
MCU Change Wizard



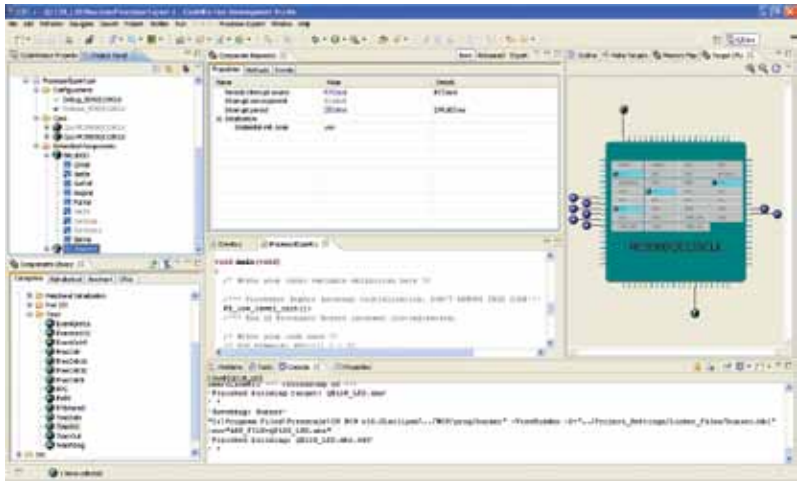
CodeWarrior Key Features	Key Benefits
MCU Change Wizard	Ability to easily retarget project to a new processor
Trace and profile support for on-chip trace buffers	Sophisticated emulator-like debug capability without additional hardware
LiveView	Ability to monitor registers, memory and global variables without stopping the processor
Freescale Processor Expert	Problems in hardware layer can be resolved during initial design phase

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

Debug Perspective



Processor Expert



Processor Expert Key Features	Key Benefits
Graphical user interface	Allows an application to be specified by the functionality needed
Automatic code generator	Creates tested, optimized C code tuned to application needs and the selected Freescale device
Built-in knowledge base	Immediately flags resource conflicts and incorrect settings so errors are caught early in the design cycle
Component wizard	Allows for the creation of user-specific hardware-independent embedded components

Profiling and Analysis

The CodeWarrior profiling and analysis tools provide visibility into an application as it runs on the processor to identify operational problems.

- Supports architectures with on-chip trace buffers (HCS08, ColdFire V1, ColdFire+ and Kinetis)
- Allows tracepoints to be set to enable and disable trace output
- Able to step through trace data and the corresponding source code simultaneously
- Allows trace data to be exported into a Microsoft® Excel® file

Processor Expert

Freescale's Processor Expert is a rapid application design tool that combines easy-to-use component-based application creation with an expert knowledge system.

- CPU, on-chip peripherals, external peripherals and software functionality are encapsulated into embedded components
- Each component's functionality can be tailored to fit application requirements by modifying the component's properties, methods and events
- When the project is built, Processor Expert automatically generates highly optimized embedded C-code and places the source files into the project

IAR Embedded Workbench

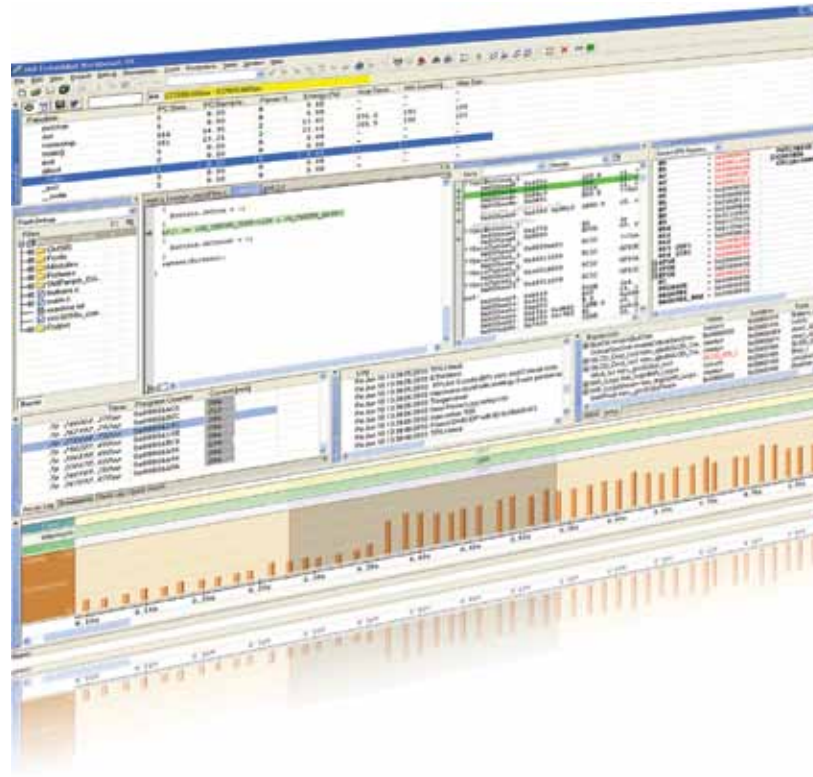
Powerful, reliable development tools

IAR Embedded Workbench is a set of development tools for building and debugging embedded applications using assembler, C and C++. It is available for various Freescale MCU and MPU families, including ColdFire+ and Kinetis.

IAR Embedded Workbench provides a completely integrated development environment, including project manager, editor, build tools and debugger. In a continuous workflow, you can create source files and projects, build applications and debug them in a simulator or on hardware.

Regardless of which Freescale device you have chosen to work with, you will experience the same intuitive user interface coupled with target-specific support for each device. Reuse of code and migration to new microcontroller architectures is made easy as each IAR C/C++ Compiler uses the same naming convention.

IAR Embedded Workbench IDE

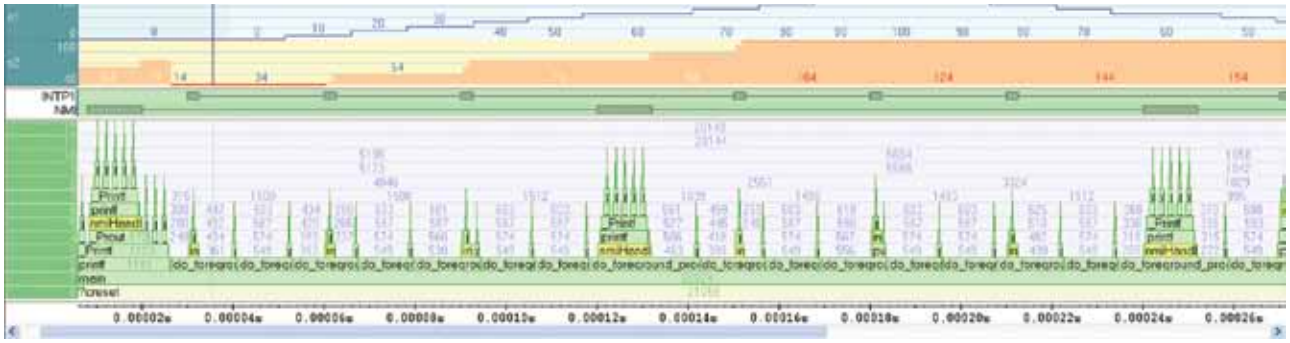


Key Components

- Integrated development environment with project management tools and editor
- Highly optimizing C and C++ compiler
- C-SPY® simulator and hardware debugger systems
- IAR J-Trace and IAR J-Link debug probes
- Timeline window visualizes call stack, interrupts and variable values over time
- Power debugging
- Code coverage and function profiling analysis utilities
- Support for RTOS-aware debugging on hardware
- Freescale MQX Software Solutions integration
- Information Center provides quick access to user guides, examples and other useful information
- Configuration files for all supported devices
- Ready-made code and project examples for supported evaluation boards
- User and reference guides in PDF format
- Context-sensitive online help

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

IAR Embedded Workbench Timeline Window



Timeline

IAR Embedded Workbench provides you with advanced features for powerful trace debugging. The timeline window graphically displays correlated information about various properties on a single timeline.

- Visualization of the call stack provides information about depth of stack and length of each function call
- Interrupt graph displays events taking place in the application
- Variable values are plotted over time

Power Debugging

IAR Embedded Workbench supports power debugging on Kinetis microcontrollers. Power debugging allows you to optimize your system for lower power consumption.

- Visualization of the power consumption over time in the timeline window
- Simultaneous visualization of the call stack, interrupts and variable values gives you a high-level view of the system's power consumption
- Power log provides high-resolution power data
- Power consumption is correlated to the source code. Click in the power graph and the corresponding source code is highlighted
- Power profiling utility

MQX Integration

Freescale MQX Software Solutions has been integrated with IAR Embedded Workbench. A ready-made port which can be compiled and linked using IAR Embedded Workbench is available and ready for use. There are also project templates that make it easy to create an MQX-based project.

IAR C-SPY Debugger provides kernel awareness for the MQX RTOS, as well as other operating systems. Kernel awareness in the debugger allows the user to examine operating system properties during a debug session.

- Operating system properties such as tasks, semaphores and mailboxes can be monitored
- Execution control can be kernel dependent. For instance, it is possible to set breakpoints on conditions for specific operating system properties

For more information, visit **IAR.com**.

IAR SYSTEMS

Keil Microcontroller Development Kit

ARM MCU development environment

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
○	○	●	●	●	●	●

The Keil micocontroller development kit MDK supports all ARM and Cortex-M processor-based MCUs, including Freescale's new Kinetis family. It combines the µVision™ 4 IDE/debugger with ARM compilation tools to provide developers with an easy to use, feature-rich environment.

MDK provides many unique features designed to help you quickly develop your project.

- Device database: Automatically configures device and project parameters
- Trace and analysis tools: Optimizes and verifies the application by measuring performance and code coverage
- Fully functional RTX™ real-time operating system: Add resource management to the application

The MDK consists of the several powerful components for debugging and analysis:

- ARM compilation tools: Deliver optimized, high-performance code for all ARM-powered devices. Further code size savings can be gained by selecting the MicroLib library.
- Debugger: Can be configured as a simulator or target debugger and provides a single environment for application testing.
- System viewer: Provides an advanced method of viewing and modifying peripheral registers.
- Analysis tools: Work with the simulator or with target hardware via the ULINK™ pro streaming trace adapter.
- Configurable logic analyzer: Provides a graphical display of signals and variables. Users can display the specific instructions that caused variable changes.

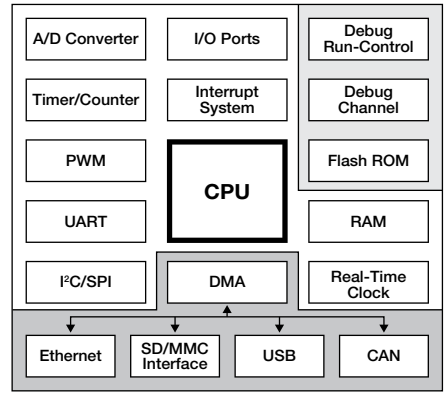
Microcontroller Development Kit (MDK)

Microcontroller Development Kit (MDK)
- Best-in-class ARM C/C++ Compilation Tools
- Genuine Keil µVision®4 IDE/Debugger/Simulator
- Royalty-free RTX Real-Time Operating System
- Easy device configuration with Device Database support for more than 700 ARM-Powered devices

ULINK® USB Adapters
- JTAG and Serial Wire Interface
- Flash Programming
- On-the-fly Target Debugging
- Real-Time Data Trace
- ETM Instruction Trace (ULINKpro)

Evaluation Boards
- Keil provides a wide range of evaluation boards for ARM and Cortex-M devices

RTOS and Middleware
- RTX Real-Time OS with Source Code
- TCP/IP Suite with Server Applications
- File System for ROM and Memory Cards
- Direct support for USB and CAN interfaces



- Debugger: Provides code coverage statistics to verify applications that require certification testing and validation.
- Performance analyzer: Displays the execution time recorded for functions including the time spent in a function and the number of calls to it.
- Execution profiler: Records execution statistics for each CPU instruction, including the execution count and execution time for each instruction.

All Cortex-M-based devices feature ARM CoreSight technology with advanced debug and trace capabilities. Together with a ULINK adapter it allows the user to control the CPU, single step one source or assembler line, set breakpoints while the processor is running, and read/write memory and peripheral registers on the fly.

All Cortex-M3 and Cortex-M4 devices provide data and event trace. MDK provides a number of ways to analyze this information while your system is running, including a trace window, debug viewer, exceptions window, event counters and a logic analyzer.

All Cortex-M devices with ETM provide instruction trace. The Keil ULINKpro is the only trace adapter which streams instruction trace directly to your PC. This enables debugging of historical sequences, execution profiling and code coverage analysis.

The virtually unlimited stream of trace information enables MDK to provide complete code coverage of your program. Code coverage identifies every instruction that has been executed, ensuring thorough testing of your application. This is an essential requirement for complete software verification and certification. For more information, visit **keil.com**.

KEIL Tools by ARM

Development Tools, RTOS and Middleware

ARM Embedded Software Solutions

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

Green Hills Software offers solutions for Kinetis MCUs based on ARM Cortex-M4 technology.

Real-Time Operating System

- µ-velOSity™ royalty-free RTOS is a small, fast, easy-to-learn operating system for the most cost-sensitive and resource-constrained devices

Software Development Tool

- MULTI® and AdaMULTI™ development environments allow to quickly develop, debug, test and optimize embedded and real-time applications
- TimeMachine™ debugging suite allows the user to find the most outrageously difficult bugs—in minutes
- DoubleCheck™ integrated static analyzer easily pinpoint bugs early in development
- Green Hills optimizing compilers generate the smallest and fastest code from C, C++, Ada 95 and Fortran

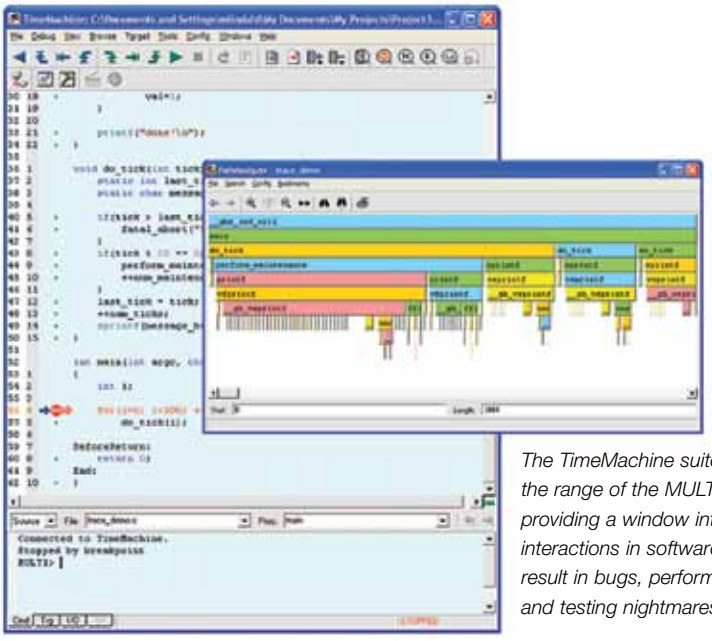
Processor Probes

- SuperTrace™ Probe allows for fast trace, download and debug
- Green Hills Probe for high-performance real-time debugging

ARM Optimizing Compilers

The Green Hills Compiler for ARM generates architecture-specific and even processor-specific optimizations to use the pipeline and instruction set characteristics of each supported ARM processor model. Green Hills offers further optimization through CodeFactor, a link-time optimization which reduces overall program size by identifying and removing redundant segments of code from object files.

TimeMachine™ Debugging Suite



The TimeMachine suite extends the range of the MULTI IDE by providing a window into the complex interactions in software that can result in bugs, performance problems and testing nightmares.

Green Hills C/C++ Compilers fully conform to ANSI/ISO industry standards, and include optional enforcement of MISRA C programming guidelines.

MULTI Development Environment

MULTI provides a host-based (Windows, Linux or UNIX workstation) graphical environment for ARM target development. Host-target connectivity is provided through a variety of means, depending on the target environment. MULTI supports many ARM targets.

The DoubleCheck integrated static analyzer finds code sequences that may result in buffer overflows, resource leaks and many other security and reliability problems. It is effective at locating a significant class of defects that are not detected by compilers during standard builds and often go undetected during run-time testing or typical field operation.

The MULTI TimeMachine debugging suite offers a wide variety of trace analysis tools that enable embedded software developers to find and fix bugs faster, optimize with ease and test with confidence. By presenting the information in easy-to-understand displays, TimeMachine enables developers to quickly navigate through trace data and produce better code in less time.

Learn more at **ghs.com/products/arm_development.html**.

Green Hills SOFTWARE

CodeSourcery: Sourcery G++

Tools for professional ColdFire and Kinetis developers

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
●	●	●	●	●	●	●

Sourcery G++ is CodeSourcery's comprehensive tools solution for professional embedded C and C++ developers. Sourcery G++ has all the tools a developer needs to build and debug embedded applications, including an IDE, optimizing C/C++ compilers, runtime libraries, source-and assembly-level debugger with hardware debug support, simulator, BSPs and utilities for Linux developers.

Sourcery G++ supports Freescale's ColdFire, Kinetis, i.MX and Power Architecture-based processor families.

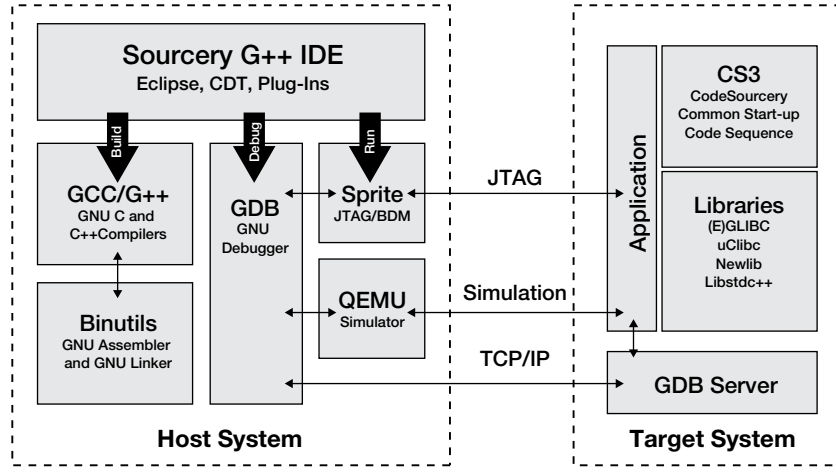
Sourcery G++ runs on Linux and Windows host systems and targets Linux, uClinux, RTOS or bare metal systems. Support for the MQX RTOS is coming soon.

Sourcery G++ is based on the GNU Toolchain and the Eclipse IDE, so it comes with all of the advantages of these powerful open-source tools with additional features available only from CodeSourcery.

Bare Metal and RTOS Development

Developers working with a bare metal system can take advantage of the Sourcery G++ Debug Sprite for running and debugging applications on target hardware via a JTAG or BDM probe. Supported probes include P&E, Axiom BDM, Abatron, Freescale CCS devices, Macraigor, RealView ICE, SEGGER J-Link and ULINK2. Sourcery G++ also includes an instruction set simulator for ColdFire and Kinetis systems.

Sourcery G++ Components



Sourcery G++ offers peripheral register browsing and integrated flash programming.

Sourcery G++ includes the CodeSourcery Common Start-up Code Sequence (CS3), which provides a basic board support package for many popular boards with linker scripts, start-up code and debugger interface files. And for new boards, the Sourcery G++ Board Builder allows developers to create a custom board definition file.

Linux Application and Kernel Development

Sourcery G++ offers a complete Linux build and debug environment for Linux applications, Linux kernel or Linux kernel modules. The Sysroot Utilities and the Remote System Explorer make it easy to get an application running on the target system. Sourcery G++ supports debugging on the target hardware or in the simulator with a debugger that displays multiple threads, and even multiple processes, at once. At the deployment stage, the Prelinker can reduce application startup time and the Library Optimizer can reduce library footprint.

Availability

Sourcery G++ is available in Professional, Standard and Personal Editions. Sourcery G++ Professional and Standard Editions include direct access to CodeSourcery's engineering team—the same team responsible for contributing over 10,000 changes to the official versions of the GNU Toolchain. All Sourcery G++ customers also receive access to regular semi-annual Sourcery G++ updates, as well as any intermediate updates produced for Professional Edition customers. Download a free 30-day evaluation.

For more information, visit **codesourcery.com/sgpp**.

CodeSourcery

Multilink Universal

A single interface for Freescale development

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
•	•	•	•	•	•	•

The Multilink Universal represents the next step forward for P&E's successful line of Multilink hardware interfaces. It combines support, in a single interface, for many Freescale architectures, including HCS08, RS08, HC(S)12, ColdFire/ColdFire+ V1, ColdFire V2–V4, Power Architecture MPC55xx/56xx and Kinetis MCUs based on ARM. It will be available in November 2010, and will be followed by a high-speed version in early 2011.

P&E's Multilinks are affordable, development-oriented interfaces that allow access to BDM/JTAG on a target microcontroller from the user's PC. The Multilink Universal offers this same reliability and affordability while combining support, in a single interface, for many Freescale architectures. It includes several ribbon cables to allow connections to the proper header for each architecture, and is designed to make its broad support of Freescale architectures simple to implement. The user can simply flip open the Multilink case and install the appropriate ribbon cable.

Universal Multilink Features

- Draws power from USB interface—no separate power supply required
- Target voltage of 1.6V–5.25V
- Includes a ribbon cable for each supported architecture

Multilink Universal Supported Architectures

Supported Architectures

- HCS08
- RS08
- HC(S)12
- ColdFire/ColdFire+ V1
- ColdFire V2–V4
- Power Architecture MPC55xx/56xx
- Kinetis ARM

Software Support

- Freescale's CodeWarrior
- P&E Software (including programmers and debuggers)
- Third-party software

Cyclone Production Programmers

P&E has added support for Freescale's ColdFire+ V1 to its Cyclone PRO stand-alone programmer, and support for the Kinetis ARM to the Cyclone MAX stand-alone programmer. These Cyclone products are geared towards production programming, including automated and high-volume programming. P&E is also developing a Cyclone stand-alone programmer that will include support for many Freescale architectures in a single, production-oriented interface.

For more information, visit **pemicro.com/universal**.

SEGGER: J-Link and Flasher

Convenient development and production programming

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
○	○	●	●	●	●	●

Designed using SEGGER's industry-leading embedded software, J-Link debug probes offer a wide array of advanced features and boast support for a broad spectrum of microcontrollers and microprocessors, including Freescale's complete i.MX, Kinetis and ColdFire V2–V4 lines. Many popular IDEs, such as CodeWarrior, IAR, Keil, Code Sourcery V2–V4 and more have built-in support for the J-Link.

The J-Link debug line offers high download speed into RAM* and flash memory. Each hardware model of these JTAG debuggers has its own unique attributes to offer and there are a number of available software add-on modules which enhance the J-Link's functionality. For more details, please see **segger.com/jlink.html**. J-Flash is a comprehensive user interface for flash programming. The flash breakpoint add-on allows for an unlimited number of breakpoints while debugging in flash memory. The J-Link SDK is a standard Windows DLL typically used from C. It makes the entire functionality of the J-Link available through the exported functions and allows to write your own program using J-Link.

Hardware Models

J-Link Pro for connectivity

J-Link Pro is an enhanced version of the J-Link. It incorporates an on-board Ethernet interface in addition to the USB, as well as two LED hardware status indicators. It comes with licenses for all J-Link related SEGGER software products, including flash breakpoints, RDI, J-Flash and GDB Server, providing the optimum debugging solution for the professional developer.

*The regular J-Link performs with an already high 750 KBps, J-Link Ultra allows an even faster peak download speed of 1.5 MBps

SEGGER Debug Probes and Production Flash Programmers

J-Link™ Intelligent Debugging via JTAG/SWD

- Robust communication
- Very high performance (download speed up to 1.5 MB)*
- Unlimited flash breakpoints (license required)

J-Link ULTRA for high performance

J-Link ULTRA is based on the highly optimized and proven J-Link, it offers even higher speed as well as target power measurement capabilities due to the faster CPU, built-in FPGA and High-Speed USB interface. This permits you to take full advantage of the low power features offered by today's modern cores. J-Link Ultra raises the bar, aiming to be the fastest emulator available.

J-Trace for Cortex-M for post-mortem-analysis

J-Trace for Cortex-M is a JTAG probe which includes trace (ETM) support. J-Trace assists the developer in analyzing his target system's behavior. The 4 MB trace memory provides plenty of space to store the last executed functions. This allows to find out how the program arrived at a certain position in code which is either not expected or wanted.

Flasher for production flash programming and in the field services

Our in-circuit programmer (Flasher ARM) is a superset of our J-Link DDL. It contains all of the debug probe features, while being designed for use in a production environment. Different interfaces, like the command line interface or the optionally available SDK allow an easy integration into any production environment.

The Flasher ARM has on-board memory to store your binary image permitting simple stand-alone flash programming. This is particularly useful for support teams which have to upgrade devices out in the field. They only need to carry a small box which is readily configured to perform the update, once it is connected to the target system. For more details, please visit **segger.com/flasherarm.html**.

SEGGER
www.segger.com

Swell PEG Product Line

Any LCD. Anywhere. PEG software.

ColdFire+		Kinetis				
Qx	Jx	K10	K20	K30	K40	K60
•	•	•	•	•	•	•

Swell Software provides graphical user interface (GUI) solutions for embedded devices. Swell's PEG Pro, PEG+ and C/PEG product offering includes a GUI library for embedded development that works tightly with real-time operating systems. The development tool allows developers to layout user interface screens and controls using the PEG library and external resources to generate C/C++ code.

PEG software accelerates GUI design for embedded devices by allowing developers to create prototypes on a Windows® or Linux® based PC by providing a complete visual layout and design tool to enable GUI design to take place in parallel to the embedded software/hardware development.

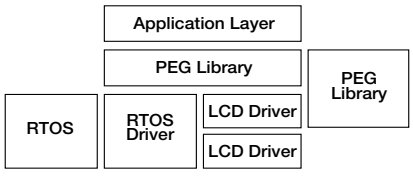
The PEG WindowBuilder automatically generates C++ source code that is ready to be compiled and linked into any application, further accelerating the deployment of the final product.

Swell's GUI software products work hand in hand with Freescale customers' real-time operating systems to incorporate LCD screens and display interfaces into future products.

PEG Pro™	PEG+™	C/PEG™
• Screen transitions • Multiple alpha-blended windows • True anti-aliasing • Gradient manager • Open GL support • Written in C++	• Multiple window updates • Alpha-blended images • Run-time image decoders and language resources • Custom widget integration • Dynamic themes • Written in C++	• Designed for small LCDs (QVGA) • Low color-depth • Very small footprint • Single window update • Multi-language capable • Written in ANSI C
One of the smallest footprints and most efficient code bases available.		
Starting 225 KB Typical 225–250 KB	Starting at 160 KB Typical 160–175 KB	Starting at 90 KB Typical 90–110 KB

Pricing starts as low as $4995 for a developer project license with three seats.

GUI Interface Technology



GUI Interface Technology

PEG's modular form enables a rapid development process.

- The core library interfaces to different RTOSs, input devices and LCD controllers by replacing the underlining driver

Window Builder Technology

PEG WindowBuilder for Rapid Development

WindowBuilder allows a designer to layout each of the screens for a project through a simple-to-use interface, providing a "What You See Is What You Get" display.

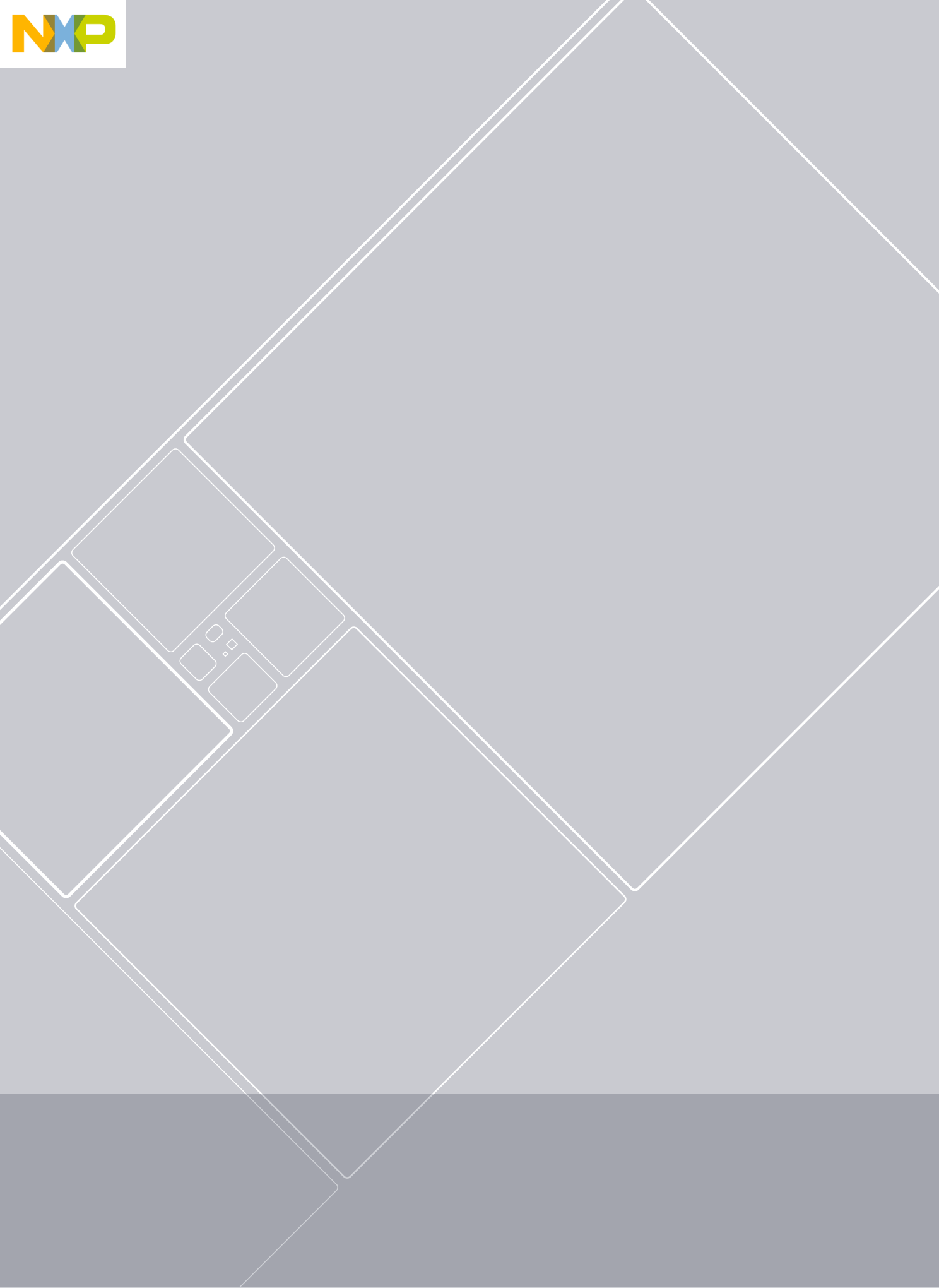
- Full WYSIWYG development
  - Simulation environment for PEG+ and PEG Pro
  - Runs on PC/Linux/X11 to allow proof of concept development
  - Enables hardware/software development to happen in parallel
  - Made available for free evaluation

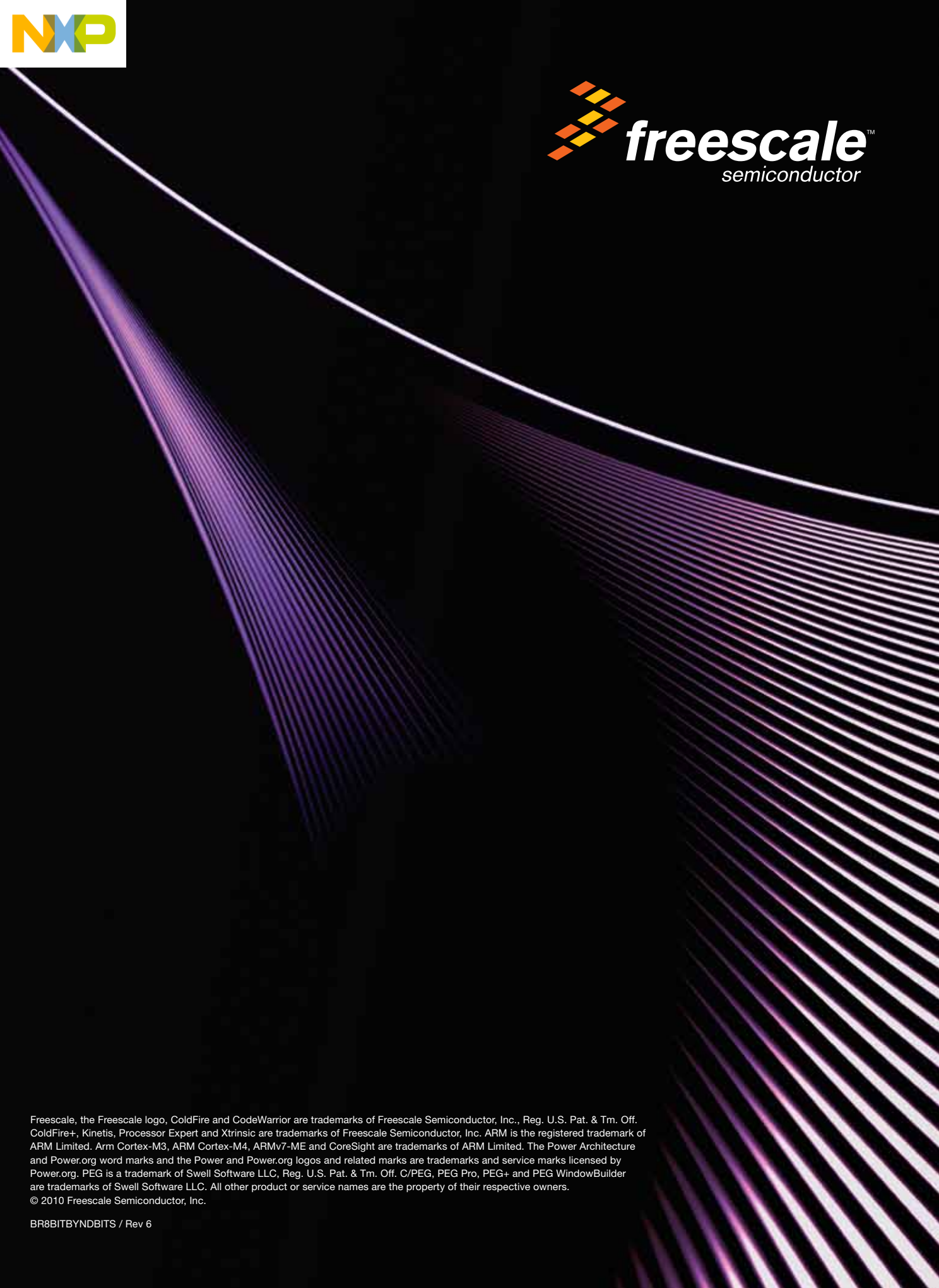
SWELL software

Quick Reference

List of Next-Generation, 32-bit MCU Resources

Resource	URL
ColdFire+ Microcontrollers	**freescale.com/ColdFire+**
Kinetis Microcontrollers	**freescale.com/Kinetis**
Thin Film Storage (TFS) with FlexMemory Technology	**freescale.com/TFS**
Xtrinsic Sensing Solutions	**freescale.com/sensors**
Freescale Tower System	**freescale.com/Tower**
Tower Geeks Community	**towergeeks.org**
MQX Software Solutions	**freescale.com/MQX**
CodeWarrior Development Tools	**freescale.com/CodeWarrior**
Processor Expert	**freescale.com/ProcessorExpert**
IAR Embedded Workbench	**iar.com/Freescale**
Keil Microcontroller Development Kit	**keil.com**
Green Hills Software	**ghs.com/products/arm_development.html**
CodeSourcery: Sourcery G++	**codesourcery.com/sgpp**
Multilink Universal	**pemicro.com/universal**
SEGGER: J-Link and Flasher	**segger.com**





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