

# A5G38H045N

## Airfast RF Power GaN Amplifier

Rev. 2 — 18 October 2023

Product data sheet



## 1 General description

This 5.4 W asymmetrical Doherty RF power GaN amplifier is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 3400 to 4000 MHz.

This part is characterized and performance is guaranteed for applications operating in the 3400 to 4000 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

## 2 Features and benefits

- High terminal impedances for optimal broadband performance
- Improved linearized error vector magnitude with next generation signal
- Able to withstand extremely high output VSWR and broadband operating conditions
- Designed for low complexity linearization systems
- Optimized for massive MIMO active antenna systems for 5G base stations

## 3 Typical performance

Table 1. 3700–3980 MHz — Typical Doherty single-carrier W-CDMA reference circuit performance

$V_{DD} = 48 \text{ Vdc}$ ,  $I_{DQA} = 35 \text{ mA}$ ,  $V_{GSB} = -4.2 \text{ Vdc}$ ,  $P_{out} = 5.4 \text{ W Avg.}$ , Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.<sup>[1]</sup>

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)
3700 MHz	15.5	52.0	8.0	-29.1
3840 MHz	14.9	50.8	8.4	-30.7
3980 MHz	14.2	50.3	8.7	-32.3

[1] All data measured with device soldered to NXP reference circuit.



## 4 Pinning information

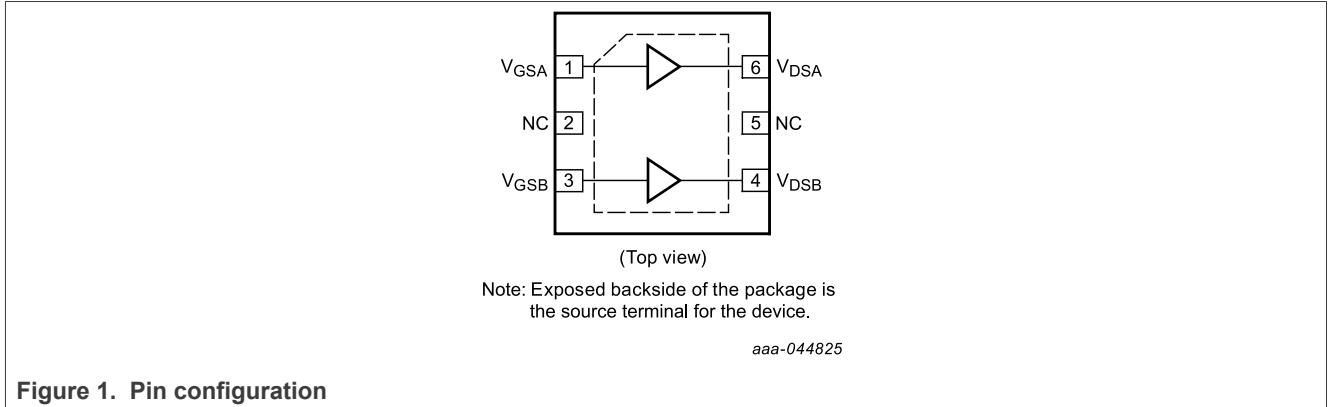


Figure 1. Pin configuration

## 5 Ordering information

Table 2. Ordering information

Device	Tape and Reel Information	Package
A5G38H045NT4	T4 Suffix = 2,500 Units, 16 mm Tape Width, 13-inch Reel	DFN 7 × 6.5

## 6 Product marking



Figure 2. Product marking

Table 3. Product marking trace code

Identifier	Description
A	Assembly location
WL	Wafer lot indicator
YYWW	Date code
Z	Assembly lot

## 7 Limiting values

Table 4. Limiting values

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	125	Vdc
Gate-Source Voltage	$V_{GS}$	-16, 0	Vdc
Operating Voltage	$V_{DD}$	55	Vdc
Maximum Forward Gate Current, $I_{G(A+B)}$ , @ $T_C = 25^\circ\text{C}$	$I_{GMAX}$	6.9	mA
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Case Operating Temperature Range	$T_C$	-55 to +150	$^\circ\text{C}$
Maximum Channel Temperature	$T_{CH}$	225	$^\circ\text{C}$

## 8 Recommended operating conditions

Table 5. Recommended operating conditions

Characteristic	Symbol	Value	Unit
Operating Voltage	$V_{DD}$	48	Vdc

## 9 Thermal characteristics

Table 6. Thermal characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface-to-Case Case Temperature $116^\circ\text{C}$ , $P_D = 6.3\text{ W}$	$R_{\theta JC}$ (IR)	5.1 <sup>[1]</sup>	$^\circ\text{C/W}$
Thermal Resistance by Finite Element Analysis, Channel-to-Case Case Temperature $116^\circ\text{C}$ , $P_D = 6.4\text{ W}$	$R_{\theta CHC}$ (FEA)	11.0 <sup>[2]</sup>	$^\circ\text{C/W}$

[1] Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.

[2]  $R_{\theta CHC}$  (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression  $MTTF$  (hours) =  $10^{[A + B/(T + 273)]}$ , where  $T$  is the channel temperature in degrees Celsius,  $A = -11.6$  and  $B = 9129$ .

## 10 ESD protection characteristics

Table 7. ESD protection characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	1A
Charge Device Model (per JS-002-2014)	C3

## 11 Moisture sensitivity level

Table 8. Moisture sensitivity level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	$^\circ\text{C}$

## 12 Electrical characteristics

### 12.1 DC characteristics

#### 12.1.1 DC characteristics — off characteristics

**Table 9. DC characteristics — off characteristics**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Off characteristics<sup>[1]</sup></b>					
Off-State Drain Leakage ( $V_{DS} = 150\text{ Vdc}$ , $V_{GS} = -8\text{ Vdc}$ ) Carrier ( $V_{DS} = 150\text{ Vdc}$ , $V_{GS} = -8\text{ Vdc}$ ) Peaking	$I_{D(BR)}$	—	—	1.1 2.1	mAdc
Off-State Gate Leakage ( $V_{DS} = 48\text{ Vdc}$ , $V_{GS} = -8\text{ Vdc}$ ) Carrier ( $V_{DS} = 48\text{ Vdc}$ , $V_{GS} = -8\text{ Vdc}$ ) Peaking	$I_{GLK}$	-1.0 -1.0	— —	— —	mAdc

[1] Each side of device measured separately.

#### 12.1.2 DC characteristics — on characteristics

**Table 10. DC characteristics — on characteristics**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>On characteristics — Side A, carrier</b>					
Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 2.3\text{ mAdc}$ )	$V_{GS(th)}$	-4.6	-2.4	-1.8	Vdc
Gate Quiescent Voltage ( $V_{DD} = 48\text{ Vdc}$ , $I_{DA} = 35\text{ mAdc}$ , Measured in Functional Test)	$V_{GSA(Q)}$	-2.9	-2.4	-1.9	Vdc
Gate-Source Leakage Current ( $V_{DS} = 150\text{ Vdc}$ , $V_{GS} = -8\text{ Vdc}$ )	$I_{GSS}$	-0.3	—	—	mAdc
<b>On characteristics — Side B, peaking</b>					
Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 4.6\text{ mAdc}$ )	$V_{GS(th)}$	-4.6	-2.6	-1.9	Vdc
Gate-Source Leakage Current ( $V_{DS} = 150\text{ Vdc}$ , $V_{GS} = -8\text{ Vdc}$ )	$I_{GSS}$	-1.1	—	—	mAdc

**12.2 Functional tests**

**Table 11. Functional tests**

(In NXP Doherty Production ATE<sup>[1]</sup> Test Fixture,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)<sup>[2]</sup>  $V_{DD} = 48\text{ Vdc}$ ,  $I_{DQA} = 35\text{ mA}$ ,  $V_{GSB} = (V_t - 1.55)\text{ Vdc}$ ,  $P_{out} = 5.4\text{ W Avg.}$ ,  $f = 3980\text{ MHz}$ , 1-tone CW.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	$G_{ps}$	12.8	15.1	18.0	dB
Drain Efficiency	$\eta_D$	35.8	42.2	—	%
Saturated Power (Pulsed CW, 5% Duty Cycle)	$P_{sat}$	43.5	44.9	—	dBm

[1] ATE is a socketed test environment.  
 [2] Internally matched part.

**12.3 Wideband ruggedness**

**Table 12. Wideband ruggedness**

(In NXP Doherty Reference Circuit,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)<sup>[1]</sup>  $I_{DQA} = 35\text{ mA}$ ,  $V_{GSB} = -4.2\text{ Vdc}$ ,  $f = 3840\text{ MHz}$ , Additive White Gaussian Noise (AWGN) with 10 dB PAR.

Characteristic	Symbol	Min	Typ	Max	Unit
ISBW of 400 MHz at 55 Vdc, 12 W Avg. Modulated Output Power (3 dB Input Overdrive from 5.4 W Avg. Modulated Output Power)		No Device Degradation			

[1] All data measured with device soldered to NXP reference circuit.

**12.4 Typical performance**

**Table 13. Typical performance**

(In NXP Doherty Reference Circuit,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)<sup>[1]</sup>  $V_{DD} = 48\text{ Vdc}$ ,  $I_{DQA} = 35\text{ mA}$ ,  $V_{GSB} = -4.2\text{ Vdc}$ , 3700–3980 MHz Bandwidth.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Fast CW, 27 ms sweep</b>					
Saturated Power	$P_{sat}$	—	48	—	W
AM/PM (Maximum value measured at saturated power across the 3700–3980 MHz bandwidth)	$\phi$	—	-12	—	°
Gain Variation @ Avg. Power over Temperature (-40°C to +85°C)	$\Delta G$	—	0.035	—	dB/°C
Output Power Variation @ Saturated Power over Temperature (-40°C to +85°C)	$\Delta P_{sat}$	—	0.002	—	dB/°C
<b>Single-carrier W-CDMA, unclipped</b>					
Gain Flatness in 280 MHz Bandwidth @ $P_{out} = 5.4\text{ W Avg.}$	$G_F$	—	1.4	—	dB
<b>2-tone CW</b>					
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	$VBW_{res}$	—	300	—	MHz

[1] All data measured with device soldered to NXP reference circuit.

**Correct biasing sequence for GaN depletion mode amplifiers in a Doherty configuration****Bias ON the device**

1. Set gate voltage  $V_{GSA}$  and  $V_{GSB}$  to  $-5$  V.
2. Set drain voltage  $V_{DSA}$  and  $V_{DSB}$  to nominal supply voltage ( $+48$  V).
3. Increase  $V_{GSA}$  (carrier side) until  $I_{DQA}$  current is attained.
4. Increase  $V_{GSB}$  (peaking side) to target bias voltage.
5. Apply RF input power to desired level.

**Bias OFF the device**

1. Disable RF input power.
2. Adjust gate voltage  $V_{GSA}$  and  $V_{GSB}$  to  $-5$  V.
3. Adjust drain voltage  $V_{DSA}$  and  $V_{DSB}$  to  $0$  V. Allow adequate time for drain voltage to reduce to  $0$  V from external drain capacitors.
4. Disable  $V_{GSA}$  and  $V_{GSB}$ .

13 Package information

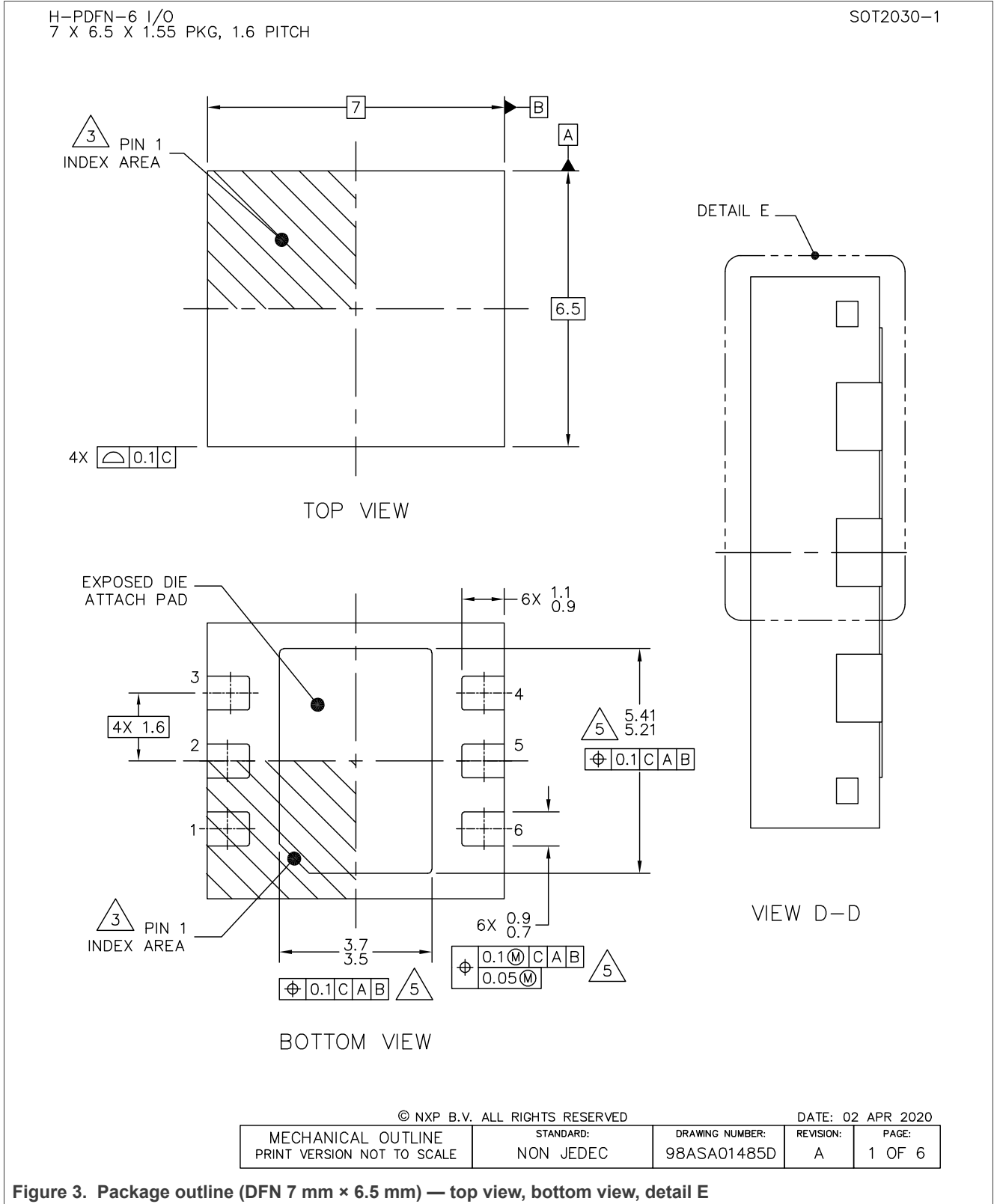
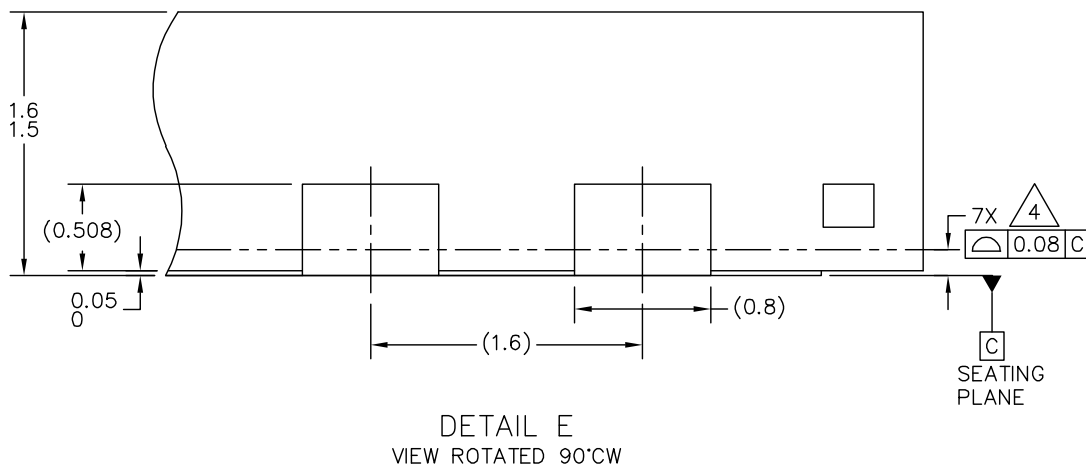


Figure 3. Package outline (DFN 7 mm × 6.5 mm) — top view, bottom view, detail E

H-PDFN-6 I/O  
7 X 6.5 X 1.55 PKG, 1.6 PITCH

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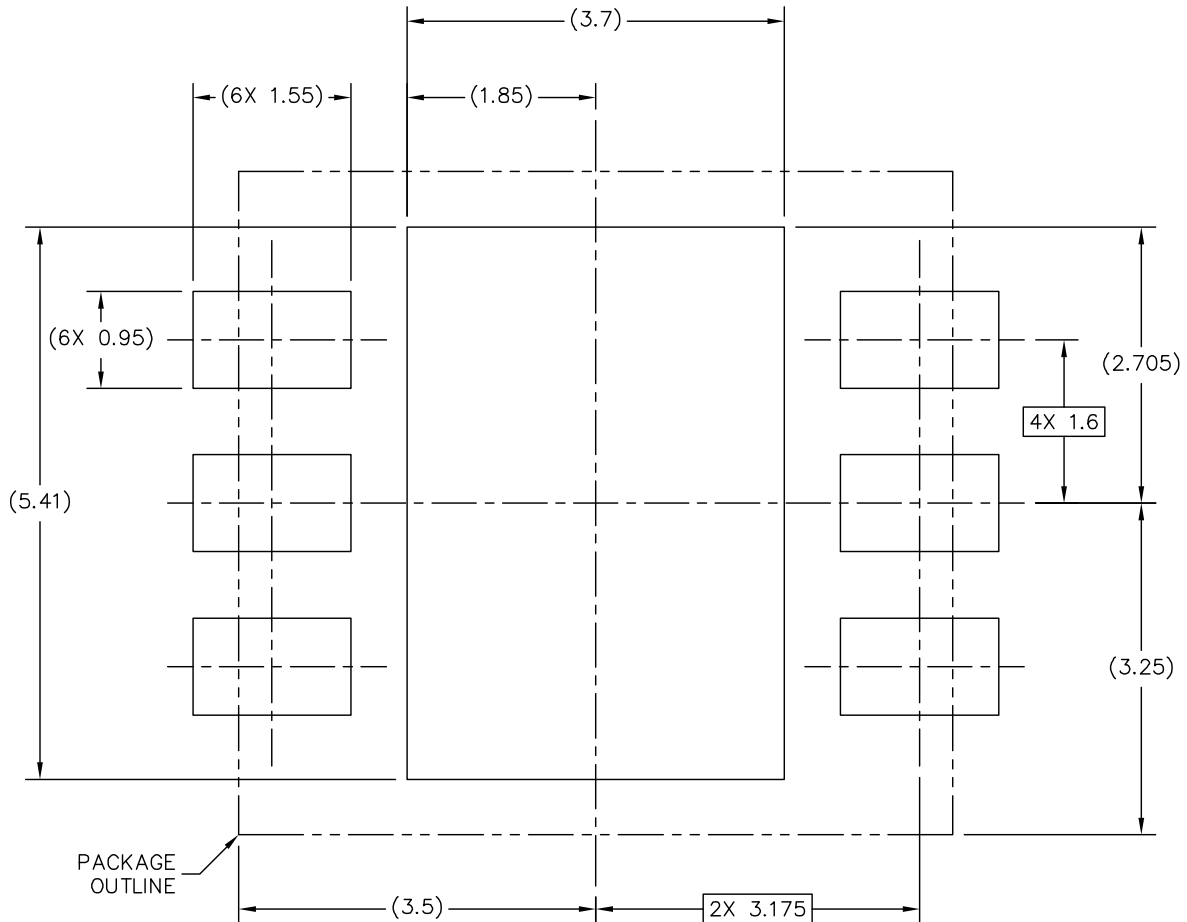
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01485D	REVISION: A	PAGE: 2
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Figure 4. Package outline (DFN 7 mm × 6.5 mm) — detail E, rotated



H-PDFN-6 I/O  
7 X 6.5 X 1.55 PKG, 1.6 PITCH

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PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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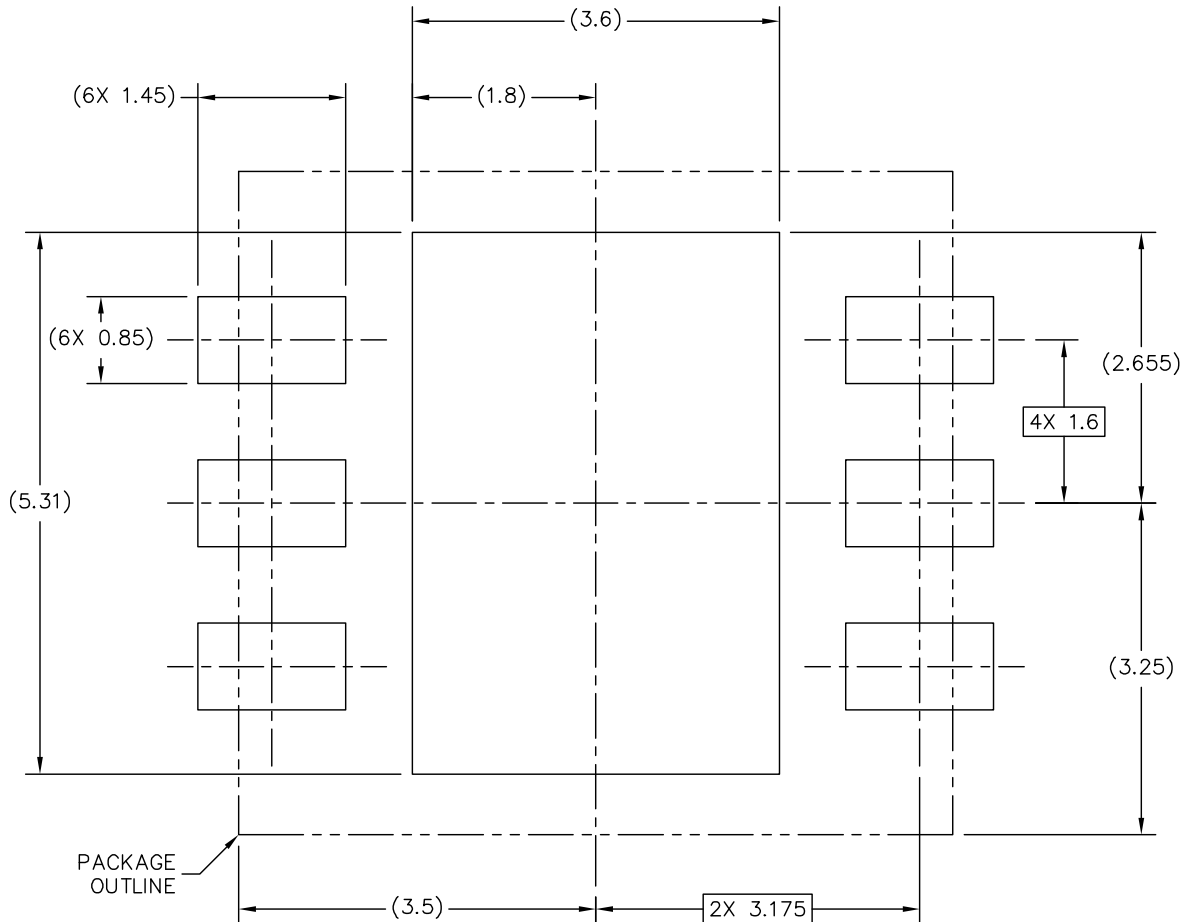
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Figure 5. Package outline (DFN 7 mm × 6.5 mm) — PCB design guidelines: solder mask opening pattern

H-PDFN-6 I/O  
7 X 6.5 X 1.55 PKG, 1.6 PITCH

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PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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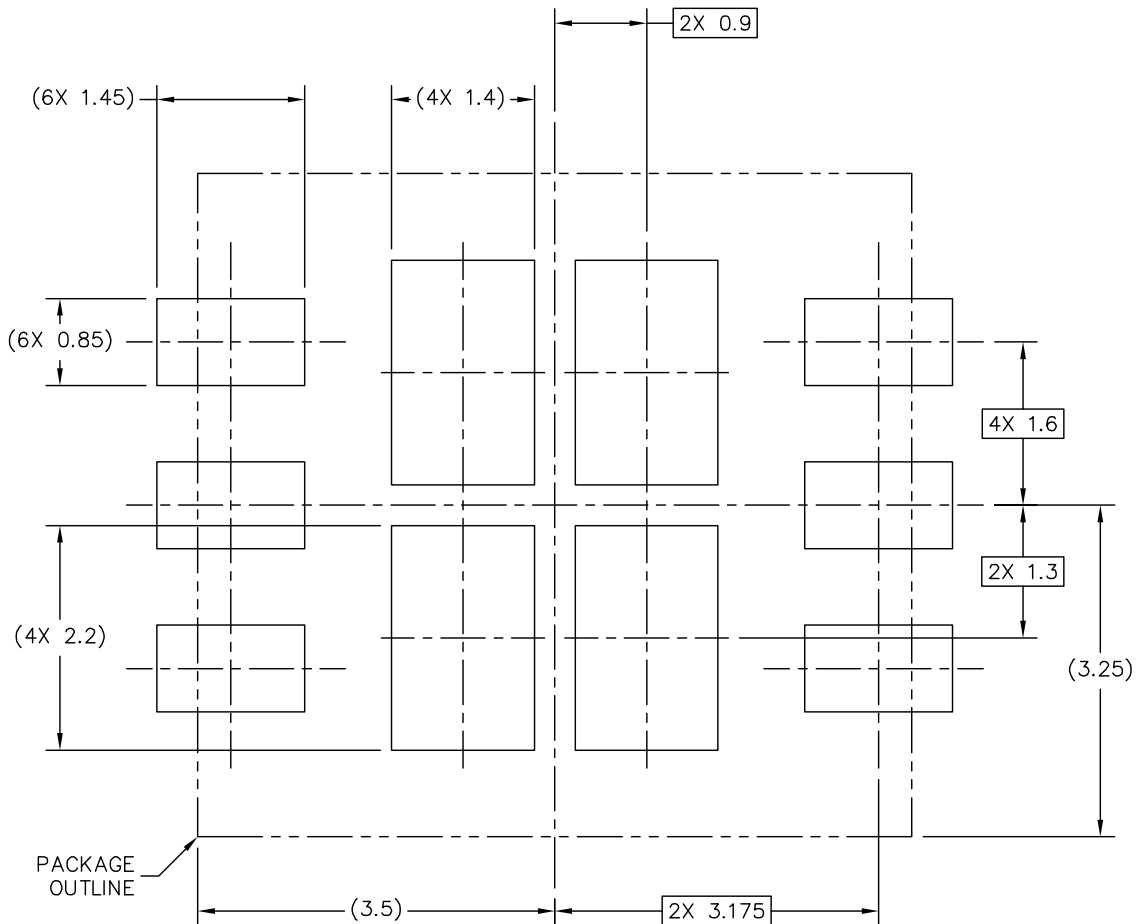
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Figure 6. Package outline (DFN 7 mm × 6.5 mm) — PCB design guidelines: I/O pads and solderable area

H-PDFN-6 I/O  
7 X 6.5 X 1.55 PKG, 1.6 PITCH

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STENCIL THICKNESS 0.125 OR 0.15

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 7. Package outline (DFN 7 mm × 6.5 mm) — PCB design guidelines: solder paste stencil

H-PDFN-6 I/O  
7 X 6.5 X 1.55 PKG, 1.6 PITCH

SOT2030-1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.

5. RADIUS ON LEAD AND DIE ATTACH FLAG IS OPTIONAL.

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**Figure 8. Package outline (DFN 7 mm × 6.5 mm) — notes**

## 14 Product documentation and software

Refer to the following resources to aid your design process.

### Application notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Software

- .s2p File

## 15 Revision history

The following table summarizes revisions to this document.

Table 14. Revision history

Revision	Date	Description
0	22 June 2022	<ul style="list-style-type: none"> <li>• Initial release of data sheet</li> </ul>
1	30 November 2022	<ul style="list-style-type: none"> <li>• Table 1, Maximum Ratings: Gate–Source Voltage: updated –8, 0 to –16, 0 Vdc, p. 2</li> <li>• Table 4, ESD Protection Characteristics, Human Body Model: updated to reflect test data, p. 2</li> <li>• General updates made to align data sheet to current standard</li> <li>• Revision date updated to Nov. 2022</li> </ul>
2	18 October 2023	<ul style="list-style-type: none"> <li>• Figure 2, Product Marking: added, p. 2</li> <li>• Table 3, Product Marking Trace Code: added, p. 2</li> <li>• Table 11, Functional Tests: updated output power test condition, p. 5</li> <li>• General updates made to align data sheet to current standard</li> </ul>

## 16 Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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