A5M36TG140

Airfast Power Amplifier Module

Rev. 1 — January 2023

Data Sheet: Technical Data

The A5M36TG140 is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells and low power remote radio heads. The field−proven LDMOS and GaN−on−SiC power amplifiers are designed for TDD LTE and 5G systems.

3300–3800 MHz

- Typical LTE Performance: P_{out} = 9 W Avg., V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc, 1 × 20 MHz LTE, Input Signal PAR = 8 dB @ 0.01% Probability on CCDF. (1)

Carrier Center Frequency	Gain (dB)	ACPR (dBc)	PAE (%)
3310 MHz	30.5	–28.8	42.9
3410 MHz	31.0	–30.1	45.4
3500 MHz	31.3	–31.8	46.2
3600 MHz	31.8	–33.7	46.1
3700 MHz	32.2	–36.0	45.8
3790 MHz	32.3	–34.8	45.4

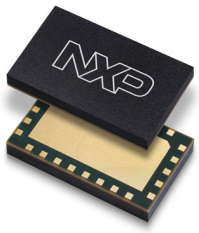
1. All data measured with device soldered in NXP reference circuit.

Features

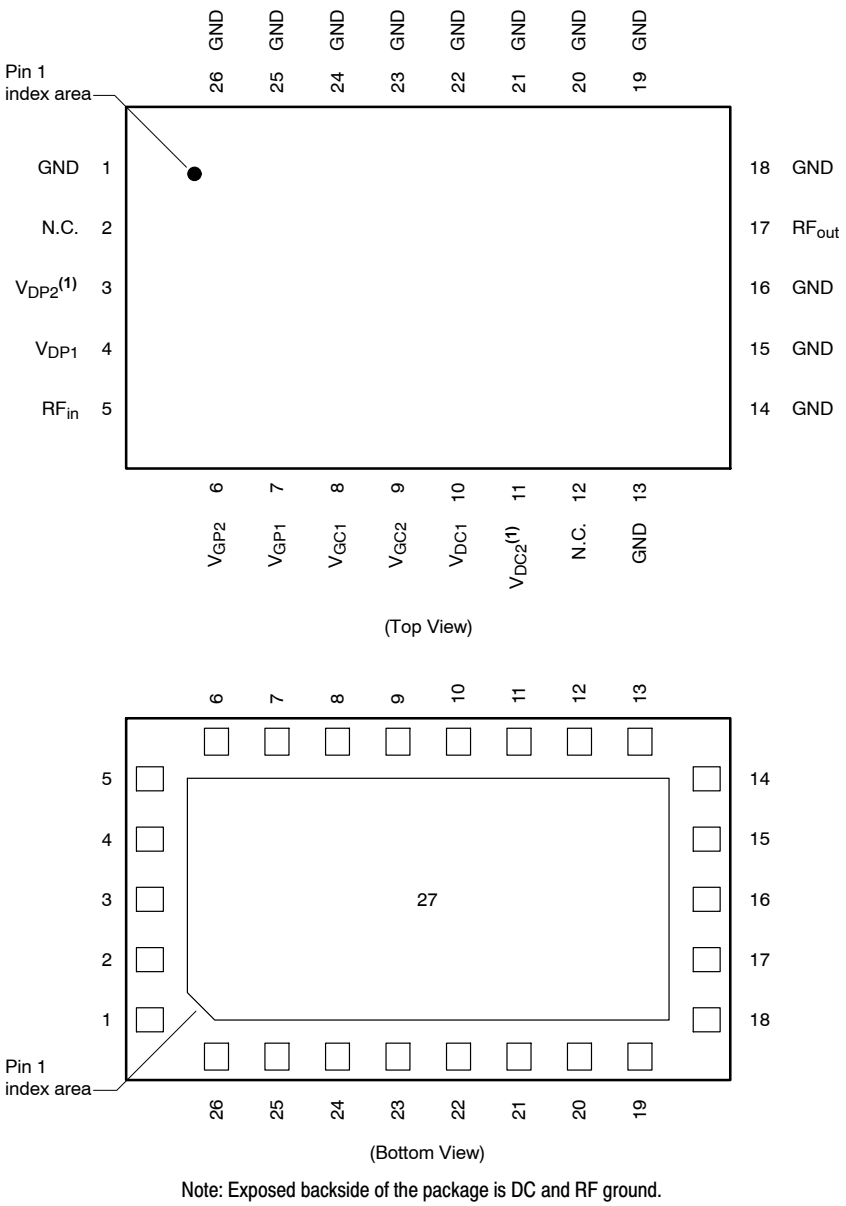
- 2−stage module solution that includes an LDMOS integrated circuit as a driver and a GaN final stage amplifier
- Advanced high performance in−package Doherty
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity digital linearization systems
- Reduced memory effects for improved linearized error vector magnitude

A5M36TG140

3300–3800 MHz, 32 dB, 9 W Avg. AIRFAST POWER AMPLIFIER MODULE



10 mm × 6 mm Module



Note: Exposed backside of the package is DC and RF ground.

Figure 1. Pin Connections

1. V_{DP2} and V_{DC2} are DC coupled internal to the package and must be powered by a single DC power supply.

Table 1. Functional Pin Description

Pin Number	Pin Function	Pin Description
1, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27	GND	Ground
2, 12	N.C.	No Connection
3	V_{DP2}	Peaking Drain Supply, Stage 2
4	V_{DP1}	Peaking Drain Supply, Stage 1
5	RF_{in}	RF Input
6	V_{GP2}	Peaking Gate Supply, Stage 2
7	V_{GP1}	Peaking Gate Supply, Stage 1
8	V_{GC1}	Carrier Gate Supply, Stage 1
9	V_{GC2}	Carrier Gate Supply, Stage 2
10	V_{DC1}	Carrier Drain Supply, Stage 1
11	V_{DC2}	Carrier Drain Supply, Stage 2
17	RF_{out}	RF Output

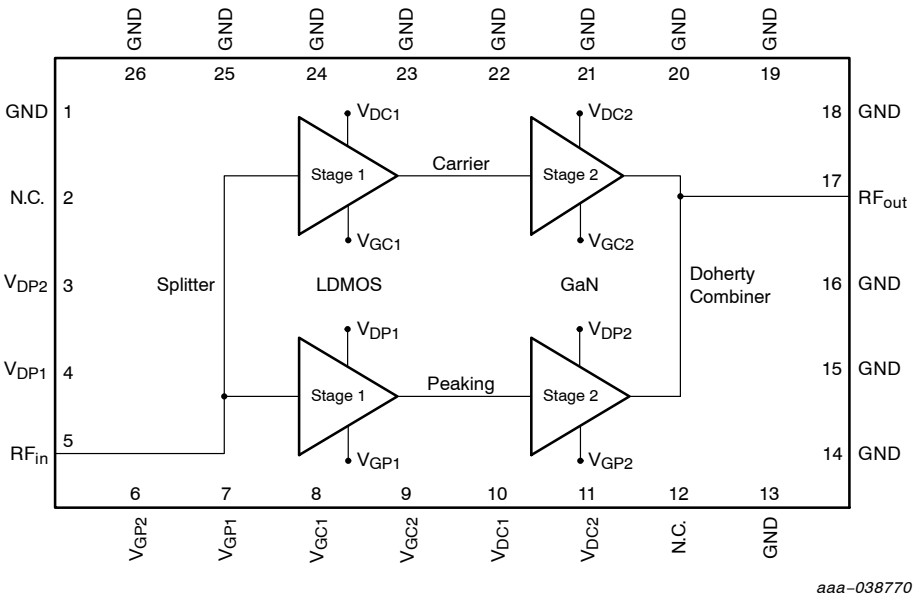


Figure 2. Functional Electrical Routing Diagram

Table 2. Maximum Ratings

Rating	Symbol	Value	Unit
Gate−Bias Voltage Range	V_{G1} V_{G2}	−0.5 to +10 −8, 0	Vdc
Operating Voltage Range	V_{DD1} V_{DD2}	4.75 to 5.25 +38 to +55	Vdc
Maximum Forward Gate Current, $I_{G\ (A+B)}$, @ T_C = 25°C	I_{GMAX}	8.1	mA
Storage Temperature Range	T_{stg}	−65 to +150	°C
Case Operating Temperature	T_C	125	°C
Maximum Channel Temperature	T_{CH}	225	°C
Peak Input Power (3600 MHz, Pulsed CW, 10 μsec(on), 10% Duty Cycle, V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc)	P_{in}	28	dBm

Table 3. Lifetime

Characteristic	Symbol	Value	Unit
Mean Time to Failure Case Temperature 125°C, 75% Duty Cycle, 9 W Avg., V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc	MTTF	> 10	Years

Table 4. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface−to−Case Case Temperature 125°C, P_D = 11.0 W	$R_{\theta JC}$ (IR)	5.6 (1)	°C/W
Thermal Resistance by Finite Element Analysis, Channel−to−Case (2,3) Case Temperature 125°C, P_D = 10.8 W	$R_{\theta CHC}$ (FEA)	9.3 (Typical)	°C/W

Table 5. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS−001−2017)	2
Charge Device Model (per JS−002−2014)	C3

Table 6. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22−A113, IPC/JEDEC J−STD−020	3	260	°C

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
2. $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where *T* is the channel temperature in degrees Celsius, *A* = −11.6 and *B* = 9129.
3. Simulated maximum FEA channel−to−case thermal resistance: 10.7°C/W, P_D = 9.4 W.

Table 7. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Carrier + Peaking Stage 2, GaN — Off Characteristics					
Off−State Drain Leakage (1) (V_{DS} = 150 Vdc, V_{GS} = −8 Vdc)	$I_{D(BR)}$	—	—	5.0	mAdc
Off−State Gate Leakage (V_{DS} = 48 Vdc, V_{GS} = −7 Vdc)	I_{GLK}	−4.0	—	—	mAdc

Characteristic	Symbol	Typ	Range	Unit
Carrier Stage 1, LDMOS — On Characteristics				
Gate Threshold Voltage (V_{DS} = 5 Vdc, I_{DC1} = 120 μAdc)	$V_{GS(th)}$	1.33	±0.4	Vdc
Gate Quiescent Voltage (V_{DS} = 5 Vdc, I_{DQC1} = 80 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.90	±0.4	Vdc
Carrier Stage 2, GaN — On Characteristics				
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 8.1 mAdc)	$V_{GS(th)}$	−2.72	±1.0	Vdc
Gate Quiescent Voltage (V_{DS} = 48 Vdc, I_{DQC2} = 10 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	−2.75	±1.0	Vdc
Peaking Stage 1, LDMOS — On Characteristics				
Gate Threshold Voltage (V_{DS} = 5 Vdc, I_{DP1} = 120 μAdc)	$V_{GS(th)}$	1.36	±0.4	Vdc
Gate Quiescent Voltage (V_{DS} = 5 Vdc, I_{DQP1} = 40 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.85	±0.4	Vdc
Peaking Stage 2, GaN — On Characteristics				
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 8.1 mAdc)	$V_{GS(th)}$	−2.72	±1.0	Vdc
Gate Quiescent Voltage (V_{DS} = 48 Vdc, I_{DQP2} = 0 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	−3.90	±1.0	Vdc

1. Carrier side and Peaking side are tied together for these measurements.

(continued)

Table 7. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests — 3400 MHz (1) (In NXP Doherty Production ATE (2) Test Fixture, 50 ohm system) V_{DD1} = 5 Vdc, V_{DD2} = 48 Vdc, I_{DQC1} = 80 mA, I_{DQC2} = 10 mA, I_{DQP1} = 40 mA, V_{GP2} = (V_{BIAS} − 1.3) (3) Vdc, P_{out} = 9 W Avg., 1−tone CW, f = 3400 MHz					
Gain	G	28.0	30.3	—	dB
Drain Efficiency	η_D	38.0	45.3	—	%
P_{out} @ 3 dB Compression Point	P3dB	48.0	49.0	—	dBm
Functional Tests — 3800 MHz (1) (In NXP Doherty Production ATE (2) Test Fixture, 50 ohm system) V_{DD1} = 5 Vdc, V_{DD2} = 48 Vdc, I_{DQC1} = 80 mA, I_{DQC2} = 10 mA, I_{DQP1} = 40 mA, V_{GP2} = (V_{BIAS} − 1.3) (3) Vdc, P_{out} = 9 W Avg., 1−tone CW, f = 3800 MHz					
Gain	G	28.0	30.2	—	dB
Drain Efficiency	η_D	35.0	42.4	—	%
P_{out} @ 3 dB Compression Point	P3dB	47.6	48.6	—	dBm
Wideband Ruggedness (4) (In NXP Doherty Power Amplifier Module Reference Circuit, 50 ohm system) I_{DQC1} = 80 mA, I_{DQC2} = 10 mA, I_{DQP1} = 40 mA, V_{GP2} = (V_{BIAS} − 1.0) (5) Vdc, f = 3600 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR					
ISBW of 400 MHz at 55 Vdc, 3 dB Input Overdrive from 9 W Avg. Modulated Output Power	No Device Degradation				
Typical Performance (4) (In NXP Doherty Power Amplifier Module Reference Circuit, 50 ohm system) V_{DD1} = 5 Vdc, V_{DD2} = 48 Vdc, I_{DQC1} = 80 mA, I_{DQC2} = 10 mA, I_{DQP1} = 40 mA, V_{GP2} = (V_{BIAS} − 1.0) (5) Vdc, 3600 MHz					
VBW Resonance Point, 2−tone, 1 MHz Tone Spacing (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	300	—	MHz
1−carrier 20 MHz LTE, 8 dB Input Signal PAR					
Gain	G	—	31.8	—	dB
Power Added Efficiency	PAE	—	46.1	—	%
Adjacent Channel Power Ratio	ACPR	—	–33.7	—	dBc
Adjacent Channel Power Ratio	ALT1	—	–46.9	—	dBc
Adjacent Channel Power Ratio	ALT2	—	–54.1	—	dBc
Gain Flatness (6)	G_F	—	1.3	—	dB
Pulsed CW, 10% Duty Cycle					
P_{out} @ 3 dB Compression Point	P3dB	—	48.3	—	dBm
AM/PM @ P3dB	Φ	—	–24	—	°
Gain Variation @ Avg. Power over Temperature (–40°C to +105°C)	ΔG	—	0.051	—	dB/°C
P3dB Variation over Temperature (–40°C to +105°C)	ΔP3dB	—	0.007	—	dB/°C

Table 8. Ordering Information

Device	Tape and Reel Information	Package
A5M36TG140T2	T2 Suffix = 2,000 Units, 24 mm Tape Width, 13−inch Reel	10 mm × 6 mm Module

1. Part input and output matched to 50 ohms.
2. ATE is a socketed test environment.
3. Increase V_{GP2} (peaking side) until I_{DQP2} = 35 mA current is attained, and then subtract 1.3 V for final V_{GP2} bias voltage.
4. All data measured in fixture with device soldered in NXP reference circuit.
5. Increase V_{GP2} (peaking side) until I_{DQP2} = 35 mA current is attained, and then subtract 1.0 V for final V_{GP2} bias voltage.
6. Gain flatness = Max(G(f_{Low} to f_{High})) − Min(G(f_{Low} to f_{High}))

Correct Biasing Sequence

Turn ON:

Bias ON the GaN final stage first

1. Set gate voltage V_{GC2} and V_{GP2} to –5 V.
2. Set drain voltage V_{DC2} and V_{DP2} to nominal supply voltage (+48 V).
3. Increase V_{GP2} (peaking side) until I_{DQP2} = 35 mA current is attained, and then subtract 1.0 V for final V_{GP2} bias voltage.
4. Increase V_{GC2} (carrier side) until I_{DQC2} current is attained.

Bias ON the LDMOS driver stage second

5. Set drain voltage V_{DC1} and V_{DP1} to nominal supply voltage (+5 V).
6. Increase V_{GC1} (carrier side) until I_{DQC1} current is attained.
7. Increase V_{GP1} (peaking side) until I_{DQP1} current is attained.
8. Apply RF input power to desired level.

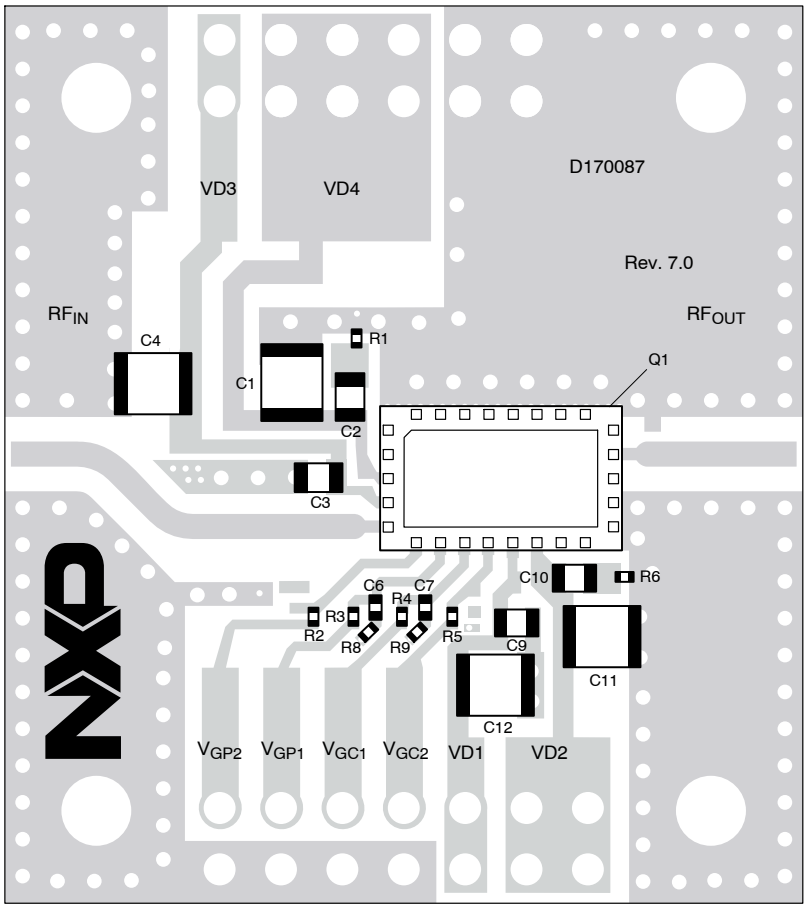
Turn OFF:

Bias OFF the GaN final stage first

1. Disable RF input power.
2. Adjust gate voltage V_{GC2} and V_{GP2} to –5 V.
3. Adjust drain voltage V_{DC2} and V_{DP2} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Disable V_{GC2} and V_{GP2}.

Bias OFF the LDMOS driver stage second

5. Adjust gate voltage V_{GC1} and V_{GP1} to 0 V.
6. Adjust drain voltage V_{DC1} and V_{DP1} to 0 V.



Board Label	Pin Description	Pin Function
VD1	Carrier Drain Supply, Stage 1	V_{DC1}
VD2	Carrier Drain Supply, Stage 2	V_{DC2}
VD3	Peaking Drain Supply, Stage 1	V_{DP1}
VD4	Peaking Drain Supply, Stage 2	V_{DP2}

Figure 3. A5M36TG140 Reference Circuit Component Layout

Table 9. A5M36TG140 Reference Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C4, C11, C12	10 μF Chip Capacitor	GRM32EC72A106KE05L	Murata
C2, C3, C9, C10	1 μF Chip Capacitor	GRM21BC72A105KE01L	Murata
C6, C7	1000 pF Chip Capacitor	GRM155R72A102KA01D	Murata
Q1	Power Amplifier Module	A5M36TG140	NXP
R1, R2, R5, R6, R8, R9	0 Ω, 1/20 W Chip Resistor	RC0201JR-070RL	Yageo
R3, R4	10 Ω, 1/20 W Chip Resistor	RC0201FR-0710RL	Yageo
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D170087	MTL

Note: Component numbers C5, C8 and R7 are intentionally omitted.

Figure 4. Product Marking

Package Information

H–PLGA–27 I/O
10 X 6 X 1.365 PKG, 1 PITCH

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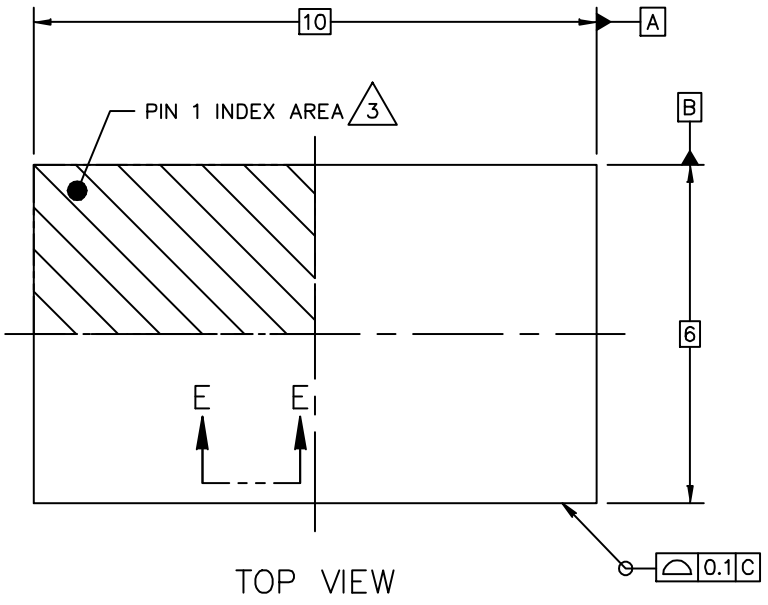
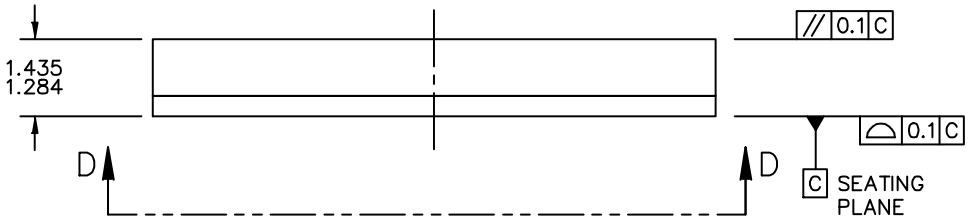


TOP VIEW



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H-PLGA-27 I/O
10 X 6 X 1.365 PKG, 1 PITCH

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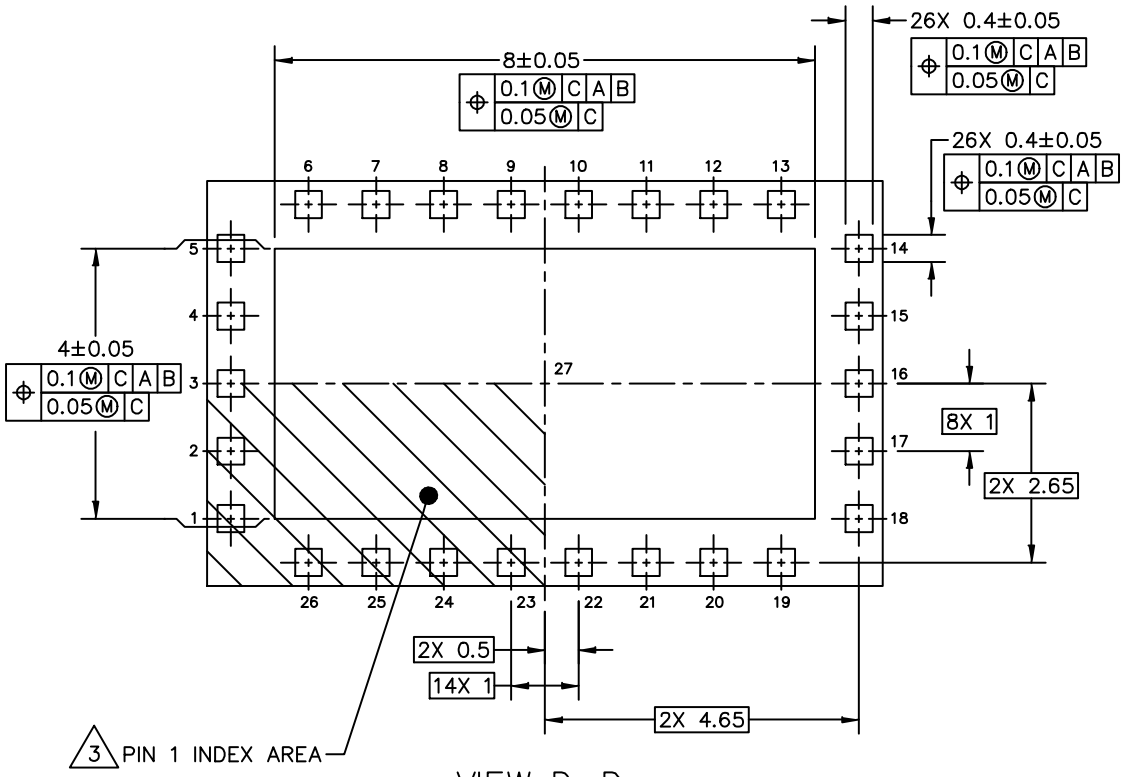
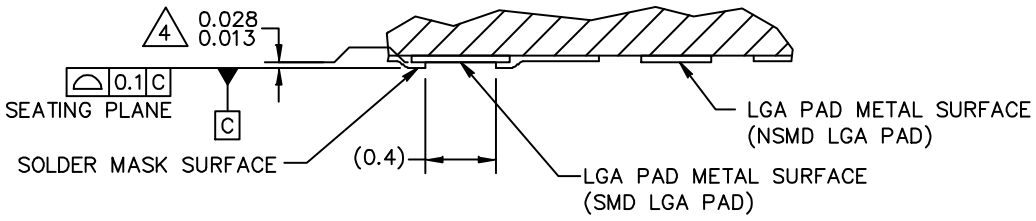


VIEW D-D
(BOTTOM VIEW)



SECTION E-E 5

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10 X 6 X 1.365 PKG, 1 PITCH

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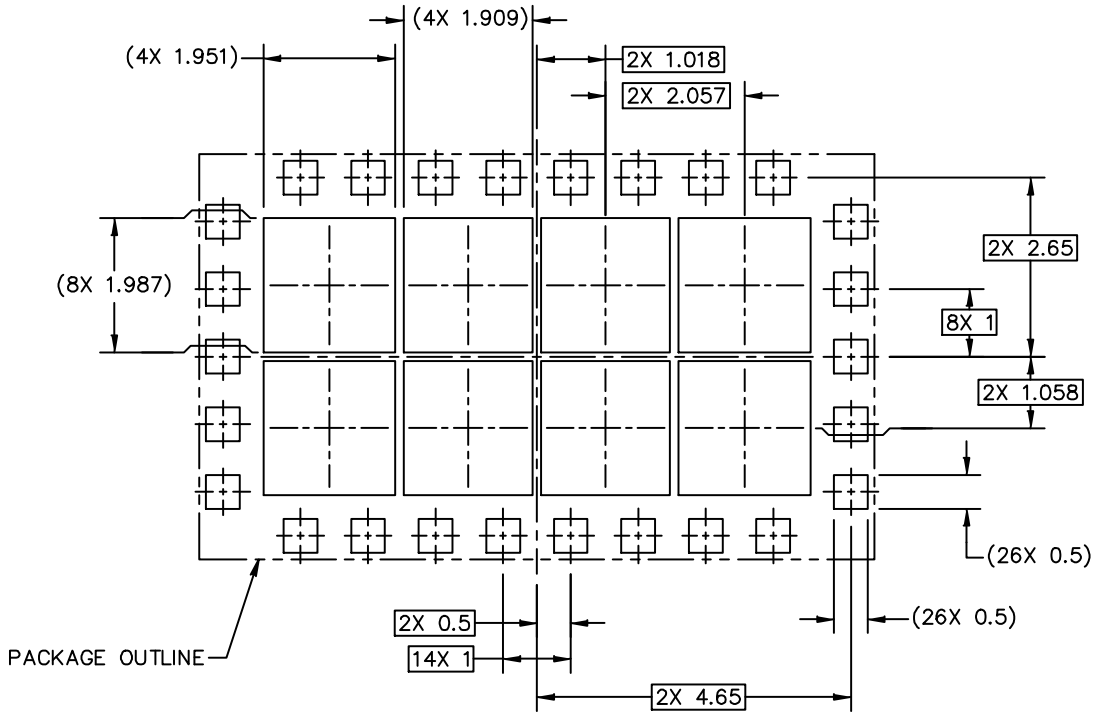

PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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10 X 6 X 1.365 PKG, 1 PITCH

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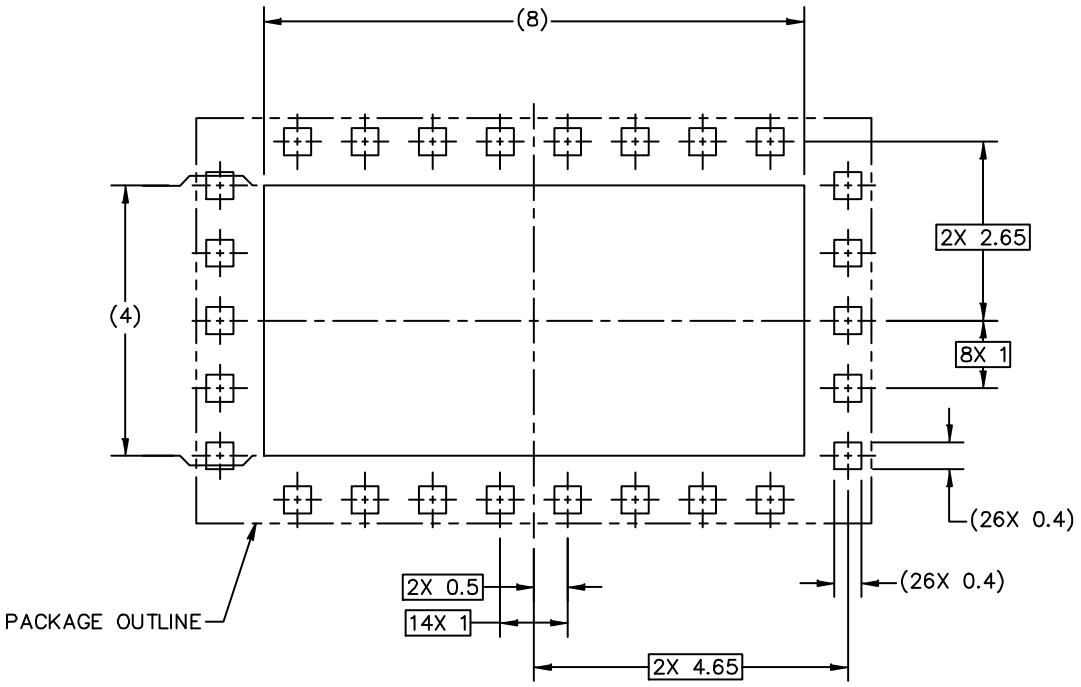

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10 X 6 X 1.365 PKG, 1 PITCH

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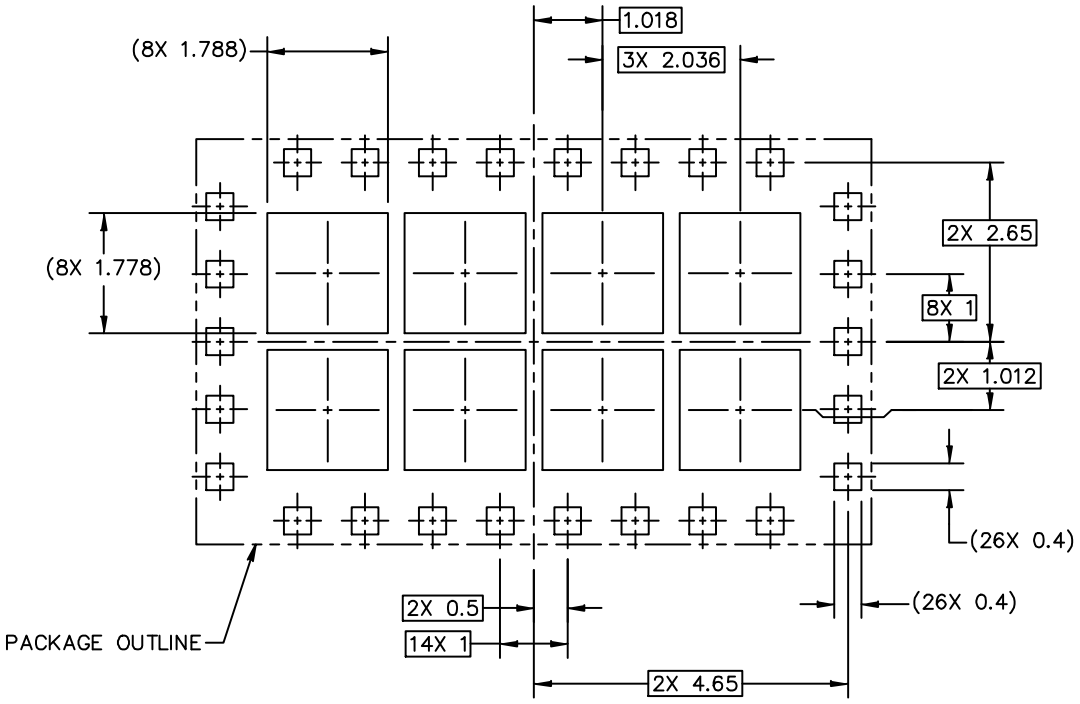

RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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H-PLGA-27 I/O
10 X 6 X 1.365 PKG, 1 PITCH

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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. DIMENSION APPLIES TO ALL LEADS AND FLAG.
5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PIN 27) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON-SOLDERMASK DEFINED (NSMD).

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Product Documentation and Tools

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Development Tools

- Printed Circuit Boards

Failure Analysis

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

Revision History

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2022	• Initial release of data sheet
1	Jan. 2023	• Maximum Ratings table, Maximum Forward Gate Current value: updated to reflect device periphery, p. 4 • Thermal Characteristics table, Thermal Resistance Channel–to–Case: updated to include both typical and maximum FEA simulated values, p. 4 • Typical Performance table, 1–carrier 20 MHz LTE, ALT2: updated Typ value to reflect test data, p. 6 • Typical Performance table, Pulsed CW, 10% Duty Cycle Typ values: updated to reflect test data, p. 6

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