PN7642

Single-chip solution with high-performance NFC reader, customizable MCU, and security toolbox

Rev. 3.2 — 6 May 2024 Product data sheet

1 General description

This document describes the functionality and electrical specification of the NFC open controller PN7642.

Additional documents supporting a design-in of the PN7642 are available from NXP, this additional design-in information is not part of this document.

The PN7642 supports highly innovative and unique features which do not require any host controller interaction. These features include dynamic power control (DPC), adaptive waveform control (AWC), and fully automatic EMD error handling.

The PN7642 is a Cortex M33 microcontroller with integrated NFC interface and security subsystem.

In this document, the term "MIFARE card“ refers to a contactless card using an IC out of the MIFARE Classic, MIFARE Plus, MIFARE Ultralight or MIFARE DESFire product family.

2 Features and benefits

Arm Cortex-M33 microcontroller

- Running at a frequency of up to 90 MHz
- Arm Cortex M33 built-in nested vectored interrupt controller (NVIC)
- Non-maskable interrupt (NMI) input with a selection of sources
- Serial wire debug with breakpoints and watch points. Includes serial wire output for enhanced debug capabilities.
- System tick timer
- up to 21 GPIOs (6 dedicated GPIOs)
- On-chip memory
  - 256 kB flash memory (180 kB available to the user)
  - 32 kB RAM (20 kB available to the user)
- Security
  - Symmetric crypto accelerator
  - Asymmetric crypto accelerator
  - Secure key storage for symmetric keys
    - Refer to Section 9.12.3 for information about how to replace the factory default keys with custom keys
  - Secure boot support
  - Key transfer unit to transfer symmetric keys between key store and crypto engine, without involvement of the CPU
- Serial interfaces
  - I^2C controller [1]
  - SPI controller

1 Updated the terms "master/slave" to "controller/target" to align with the recommendation of the NXP - I^2C and JEDEC SPI standards organizations.

- USB 2.0 Full-speed device controller
- I^2C target up to 3.4 Mbit/s (High-speed mode)
- I^3C target
- SPI target up to 15 Mbit/s
- UART
- CT auxiliary interface
- Host interface supply voltage of 1.8 V and 3.3 V is supported for maximum interoperability with existing micro-controllers

NFC functionality

- The following 13.56 MHz reader/writer modes (PCD) are supported
  - ISO14443-3/4 A/B
  - ISO15693 / ISO18000-3 mode 1
  - FeliCa
  - ISO18000-3 mode 3
- The following 13.56 MHz card modes (PICC) are supported
  - ISO14443-3/4A
- Supports ECP 2.0 (ref. [1])
- All relevant 13.56 MHz reader/writer modes (PCD) are supported
- High data rates for communication with NTAG 5 (based on ISO/IEC15693) up to 212 kbit/s
- Fast hardware and firmware-based EMD error handling without host controller interaction

Transmitter

- 2.0 W transmitter output power
- Dynamic power control (DPC 2.0) works with true current measurement
- DPC 2.0 regulates the transmitter current with lowest latency and without any host controller interaction
- Fine granularity of DPC 2.0 transmitter output voltage settings, step-width is 100 mV
- Adaptive waveform control (AWC) reduces the effort to achieve the standard compliance for various data rates and protocols

Receiver

- Innovative receiver signal processing implemented for advanced robustness against external noise sources (e.g. TFT display and external DC-DC noise)
- True automatic gain control (AGC) and internal voltage divider adjust signal levels automatically for optimized signal to noise ratio
- 10-bit ADC - together with the innovative signal processing delivers high receiver sensitivity and wide communication range
- Receiver signal strength indicator (RSSI) allows configuring receiver settings automatically dependent on the actual antenna signal reception condition.

Power-saving support

- Comprehensive power-saving configurations allow for minimizing the power consumption including standby, OFF mode and hard power down (HPD) mode.
- Software-based low-power card detection (LPCD) for highest detection sensitivity
- Hardware-based ultra low-power card detection (ULPCD) for lowest current consumption

Special features

- Integrated low noise DC-DC allows supplying the transmitter with up to 6.0 V while the system supply is 3.3 V (e.g. battery supply).

- Internal temperature sensor protects against overheating, warning levels are configurable, emergency shutdown at temperature level which might impact product lifetime.
- Overcurrent protection (configurable) protects the chip in case of short on the transmitter outputs
- Two DAC outputs allow the connection of variable capacitors for automatic antenna tuning
- Firmware upgrade is possible "in the field"
- Operating ambient temperature range -40 °C to +85 °C with full RF output power
- Operating ambient temperature from +85 °C to +105 °C is possible with reduced RF output power

2.1 RF functionality

- As a highly integrated high performance full NFC Forum-compliant frontend IC for contactless communication at 13.56 MHz, this NFC frontend IC utilizes an outstanding modulation and demodulation concept completely integrated for relevant 13.56 MHz based contactless communication methods and protocols.
  PN7642 supports communication with all products of the MIFARE product-based card family including MIFARE Ultralight, MIFARE Classic 1K/4K, MIFARE DESFire EV1/EV2 and MIFARE Plus cards CRYPTO implemented in hardware for R/W of all NXP MIFARE product-based cards (includes intellectual-property licensing rights for NXP ISO/IEC 14443-A, Innovatron ISO/IEC 14443-B, and NXP MIFARE products).
  The PN7642 frontend IC supports the following RF operating modes:

2.1.1 ISO/IEC14443-A

- Reader/writer mode supporting ISO/IEC 14443-A R/W up to 848 kbit/s

2.1.2 ISO/IEC14443-B

- Reader/writer mode supporting ISO/IEC 14443-B up to 848 kBit/s

2.1.3 FeliCa

- Reader/writer mode supporting FeliCa 212 kBit/s and 424 kBit/s (without crypto)

2.1.4 Tag type reading

- Supports reading of all NFC tag types (type 1, type 2, type 3, type 4A and type 4B, type 5)

2.1.5 MIFARE card reading

- Reader/writer communication mode for the MIFARE card family including MIFARE Classic

2.1.6 ISO/IEC 15693

- Reader/writer mode supporting ISO/IEC 15693 (ICODE)
- Proprietary data rates based on ISO/IEC15693 with 106 kbit and 212 kbit/s (for NXP NTAG 5 communication)

2.1.7 ISO/IEC 18000-3 Mode 3

- Reader/writer mode supporting ISO/IEC 18000-3 Mode 3

2.1.8 Card emulation

- ISO/IEC4443-A card mode from 106 Kbit/s up to 848 Kbit/s (PICC) with active load modulation for increased communication range.

2.2 Product comparison

The PN76 family consists of two derivatives. Find a comparison in the following table.

Table 1. Comparison of the PN76 family members

	PN7640EV	PN7642EV
Contactless interface features PCD (reader/writer)	• ISO14443-3/4 A/B • ISO15693 / ISO18000-3 mode 1 • MIFARE	• ISO14443-3/4 A/B • ISO15693 / ISO18000-3 mode 1 • FeliCa • ISO18000-3 mode 3 • MIFARE
Contactless interface features PICC (card mode)	• ISO14443-4A	• ISO14443-4A
Available flash memory	120 kB	180 kB
General-purpose I/O	6	Up to 21
Host interfaces	SPI, I^2C, UART, USB device	SPI, I^2C (with SMBUS support), I^2C, HSUART, USB device
Controller interfaces	-	SPI, I^2C (with SMBUS support), ISO7816 UART
Firmware update in the field	I^2C and SPI	USB, SPI, I^2C, I^3C, UART, NFC, from user app
High data rates for NTAG 5 support	-	Yes, up to 212 kbit/s
PWM / ADC interface	-	3 PWM outputs / 1 ADC input
Certification	-	SESIP L2, NFC Forum (reader device and card emulation)
Compliance	-	USB, CT ISO
Cryptographic features	• Hardware Key store for symmetric AES keys (128 or 256 bit) • Key store software extension for symmetric keys • mbedTLS library	• Hardware Key store for symmetric AES keys (128 bit or 256 bit) • Key store software extension for symmetric and asymmetric keys • mbedTLS library
Cryptographic features symmetric	• Fast AES-128 or AES-256 en/decryption • Support for chaining modes: CBC, CTR • SHA256 coprocessor • AES en/decryption via DMA • SHA256 hashing via DMA • Random number generator (RNG) • Countermeasures against side channel information leakage • Supported algorithms – AES-CCM – AES-CBC – AES-ECB – AES-CTR – AES-GCM (in software) – AES-GMAC	• Fast AES-128 or AES-256 en/decryption • Support for chaining modes: CBC, CTR • SHA256 coprocessor • AES en/decryption via DMA • SHA256 hashing via DMA • Random number generator (RNG) • Countermeasures against side channel information leakage • Supported algorithms – AES-CCM – AES-CBC – AES-ECB – AES-CTR – AES-GCM (in software) – AES-GMAC – AES-EAX

Table 1. Comparison of the PN76 family members*...continued*

	PN7640EV	PN7642EV
	– SHA-256	– SHA-256 – SHA-384 / 512 (in software) – 3DES
Cryptographic features asymmetric	• HKDF • HMAC • Elliptic Curve algorithms – ECKA – ECC key generation – ECDSA signing and verification – EdDSA signature verification for Edward curve – Curves – Brainpool P256r1 – Brainpool P384r1 – SECP256 – SECP384 – Ed25519 signature verification – Additional curves on Weierstrass and Prime are supported by feeding the specific domain parameters	• HKDF • HMAC • RSA • Elliptic Curve algorithms – ECKA – ECC key generation – ECDSA signing and verification – EdDSA signing and verification for Edward curve – Curves – Brainpool P256r1 – Brainpool P384r1 – SECP256 – SECP384 – Ed25519 (signature generation and verification) – Additional curves on Weierstrass and Prime are supported by feeding the specific domain parameters

3 Applications

- Physical access
- eGov
- Closed loop payment
- Secure authentication
- Enhanced Contactless Polling (ECP)

4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$VDD_{(VBAT)}$	supply voltage on pin VBAT (analog and digital supply)	VBAT ≥ VDDIO	2.4	-	5.5	V
$VDD_{(VDDIO)}$	supply voltage on pin VDDIO (supply for host interface and GPIOs)	1.8 V supply	1.62	-	1.98	V
		3.3 V supply	2.4	-	3.6	V
$VDD_{(VDDPA)}$	supply voltage on pin VDDPA (input of the transmitter power amplifier)	supply with VDDPA from internal VDDPALDO with DC-DC	1.5	-	5.7	V
I_{pd}	power down current	$VDD_{(VDDPA)}$ = $VDD_{(VDDIO)}$ =$VDD_{(VDD)}$ 3.0 V; hard power down state; pin VEN set LOW,	-	40	105	µA

Table 2. Quick reference data*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		T_{amb} = 25 °C, External supply by VDDIO				
I_{stb}	standby current	T_{amb} = 25 °C	-	45	110	µA
I_{ULPCD}	average ultra-low-power card detection current	T_{amb} = 25 °C, VDD(VDDPA) = VDD(VDDIO) =VDD(VDD) 3.0 V, 330 ms Polling interval, 50 R antenna matching	-	22	-	µA
$IDD_{(VDDPA)}$	supply current on pin VDDPA	supplied via VUP_TX (TX_LDO active)	-	-	350	mA
		supplied without DC-DC and TXLDO active	-	-	400	mA
$P_{(PA)}$	Transmitter output power	supplied via VUP_TX (TX_LDO active)	-	-	2.0	W
		supplied without DC-DC and TXLDO active	-	-	2.3	W
T_{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB,	-40	-	+85	°C
T_{stg}	storage temperature	no supply voltage applied	-55	-	+150	°C
T_{j_max}	maximum junction temperature	-	-	-	+125	°C

5 Ordering information

Table 3. Ordering information

Type number	Package			Packing	12NC
	Name	Description	Version		
PN7642EV/C100	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm. MSL = 3. The firmware download mode is activated by asserting the DWL_REQ pin. Firmware: FW 1.00	SOT1307-2	Tape and Reel packing. Minimum order quantity = 4000 pcs	9354 378 87518
PN7642EV/C100	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm. MSL = 3. The firmware download mode is activated by asserting the DWL_REQ pin. Firmware: FW 1.00	SOT1307-2	Multiple Tray packing (5 trays). Minimum order quantity = 2450 pcs	9354 378 87557
PN7642EV/C101	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm. MSL = 3.	SOT1307-2	Tape and Reel packing. Minimum order quantity = 4000 pcs	9354 563 02518

Table 3. Ordering information*...continued*

Type number	Package			Packing	12NC
	Name	Description	Version		
		The firmware download mode is entered by setting a register in non-volatile memory. Firmware: FW 2.00			
PN7642EV/C101	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm. MSL = 3. The firmware download mode is entered by setting a register in non-volatile memory. Firmware: FW 2.00	SOT1307-2	Multiple Tray packing (5 trays). Minimum order quantity = 2450 pcs	9354 56302557

Table 4. Factory default transport key

Type number	12NC	Factory default transport key
PN7642EV/C100	9354 378 87518 9354 378 87557	**128-bit:** 4B3CEAED37CB6C03DB322BB483888474 **256-bit:** 7B986646E11B4DC55BBF1D35F2B00CAC BA0AE0E822D70E89EAB95825BA843B82
PN7642EV/C101	9354 563 02518 9354 56302557	**128-bit:** A666B9710B9A7AD0831B32C7D33DBF72 **256-bit:** E05B44F8F3C25A716ED8AE847529DAF317E092E5FC643D946 C732D62F42F7229

6 Firmware versions

Firmware versions covered by this data sheet:

PN7642EV/C100

Initialized with firmware 01.00

PN7642EV/C101

Initialized with firmware 02.00 with pinless-download mode enabled by default.

7 Block diagram

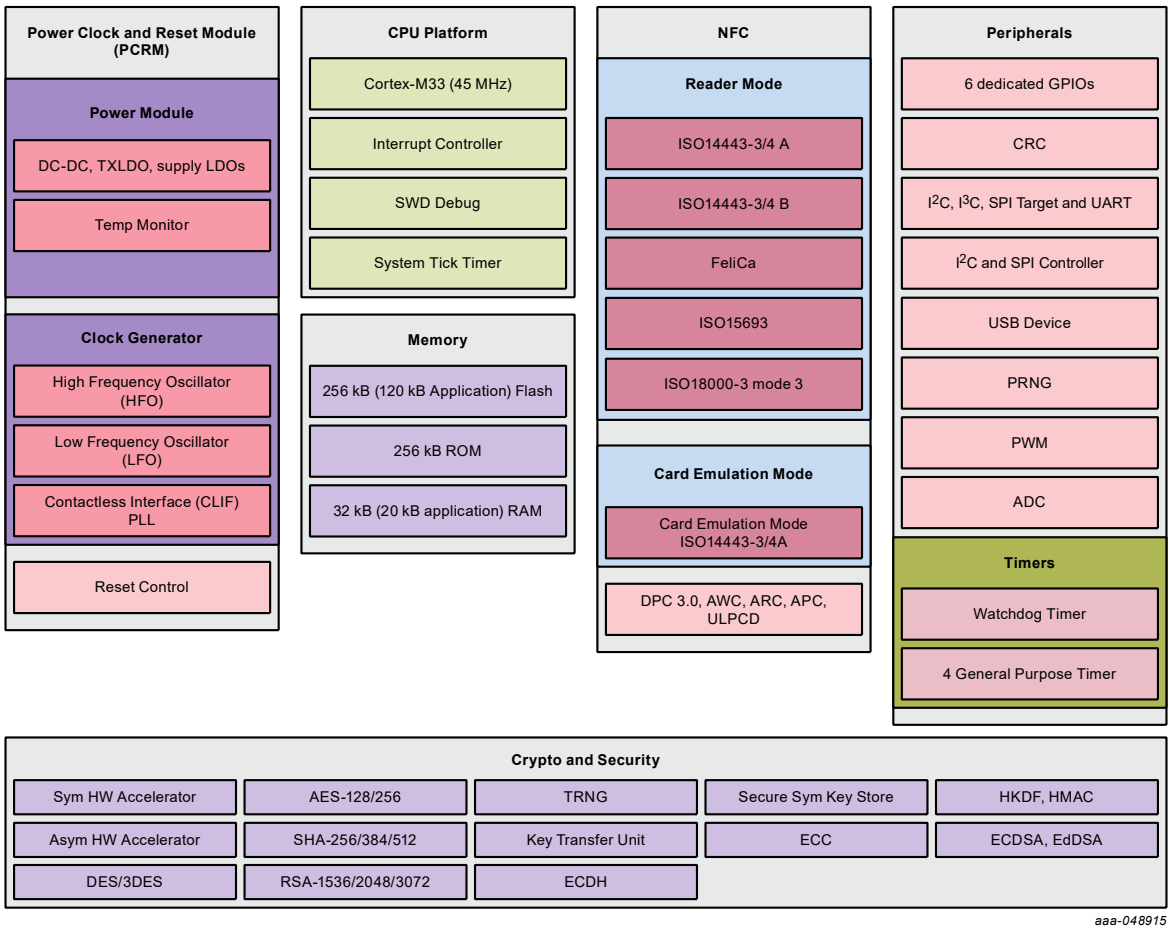


Figure 1. Block diagram PN7642

8 Pinning information

8.1 Pin description VFBGA64

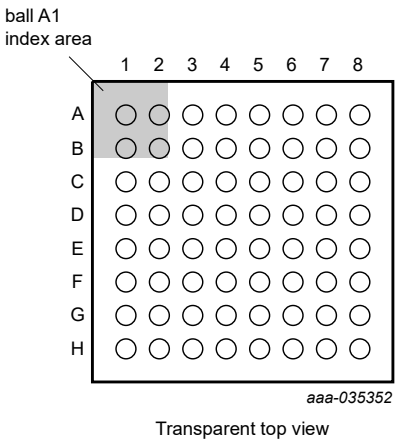


Figure 2. Pin configuration for VFBGA64

Table 5. Pin description VFBGA64

Pin Number	Symbol	Type	Description PN5190	Description PN7642
Host Interface				
E6	ATX_A	Output	SPI target [1] data output	UART RX / I^3C SDA / SPI MISO / I^2C SDA
E5	ATX_B	Input	SPI clock input	UART CTS / I^3C SCL / SPI SCK / I^2C SCL
D6	ATX_C	Input	SPI target select input	UART RTS / I^3C Adr Bit 0 / SPI NSS / I^2C Adr Bit 0 / USB D+
D5	ATX_D	Input	SPI target data input	UART TX / I^3C Adr Bit 1 / SPI MOSI / I^2C Adr Bit 1 / USB D-
B7	IRQ	Output	Host communication/ event interrupt signal	Host communication / event interrupt signal
F8	XTAL1	Input	Crystal / system clock input	Crystal / system clock input
G8	XTAL2	Output	Clock output (amplifier-inverted signal output) for crystal	Clock output (amplifier-inverted signal output) for crystal
B3	VEN	Input	Hardware reset, low active (independent from V_{VDDIO}) Avoid a floating or unexpected toggling of the pin.	Hardware reset, low active (independent from V_{VDDIO}) Avoid a floating or unexpected toggling of the pin.
Supply pins				
H2	VSS_PA	Supply GND	Transmitter ground	Transmitter ground
G3	VSS_PLL	Supply GND	PLL ground (low noise)	PLL ground (low noise)

Table 5. Pin description VFBGA64*...continued*

Pin Number	Symbol	Type	Description PN5190	Description PN7642
A2	VSS_PWR	Supply GND	DC-DC boost ground	DC-DC boost ground
D3	VSS_REF	Supply GND	PMU ground	PMU ground
B2, E3	VSS_SUB	Supply GND	Substrate ground	Substrate ground
C3	VSS_PMU	Supply GND	PMU ground	PMU ground
F4	VSS_DIG	Supply GND	Digital ground	Digital ground
F3	VSS_NFC	Supply GND	NFC ground	NFC ground
E1	VBAT	Supply	System supply, used to supply the analog and digital blocks, memory and internal voltage references	System supply, used to supply the analog and digital blocks, memory and internal voltage references
A8	VDDIO	Supply	I/O pads power supply	I/O pads power supply
G1	VDDPA	Supply	Transmitter supply	Transmitter supply
F1	VUP_TX	Supply	Input supply voltage for transmitter LDO	Input supply voltage for transmitter LDO
B1	VDD BOOST	Supply	DC-DC boost supply	DC-DC boost supply
A1	BOOST_ LX	Output	Boost inductance loopback, to be connected to boost inductor	Boost inductance loopback, to be connected to boost inductor
A3	VBATPWR	Supply	To be connected to boost inductor and transmitter power supply	To be connected to boost inductor and transmitter power supply
Outputs for stabilizing cap				
A4	VDDNV	Output	Non-volatile memory power supply, to be connected to ground via 220 nF blocking cap	Non-volatile memory power supply, to be connected to ground via 220 nF blocking cap
D2	VREF	Output	High quiescent reference voltage, to be connected to ground via 100 nF blocking cap	High quiescent reference voltage, to be connected to ground via 100 nF blocking cap
C1	VDDC	Output	Power supply for Digital Core, to be connected to ground via 220 nF blocking cap	Power supply for Digital Core, to be connected to ground via 220 nF blocking cap
G2	TXVCM	Output	Transmitter voltage common mode, to be connected to ground via 220 nF blocking cap	Transmitter voltage common mode, to be connected to ground via 220 nF blocking cap
F2	TXVCASC	Output	TX decoupling cap, to be connected to VDDPA	TX decoupling cap, to be connected to VDDPA
H6	VMID	Output	Stabilizing capacitor connection output, to be connected to electrical symmetry point of antenna (typically antenna ground) by 100 nF blocking cap	Stabilizing capacitor connection output, to be connected to electrical symmetry point of antenna (typically antenna ground) by 100 nF blocking cap
RF Debug signals				

Table 5. Pin description VFBGA64*...continued*

Pin Number	Symbol	Type	Description PN5190	Description PN7642
G7	AUX_1	Output	Test bus 1	Test bus 1
F7	AUX_2	Output	Test bus 2	Test bus 2
H8	AUX_3 / VTUNE0	Output	Test bus 3 / VTUNE0 (digital-to-analog output 0)	Test bus 3
Antenna connections				
H5	RXP	Input	Receiver input "Positive"	Receiver input "Positive"
H4	RXN	Input	Receiver input "Negative"	Receiver input "Negative"
H1	TX1	Output	Antenna driver output 1	Antenna driver output 1
H3	TX2	Output	Antenna driver output 2	Antenna driver output 2
Analog/Digital inputs and outputs				
H7	VTUNE1	Output	Digital-to-analog output 1	Do not connect
E8	GPIO0	Input/ Output	General Purpose Output 0	General Purpose I/O 0 / PWM 0
D8	GPIO1	Input/ Output	General Purpose Output 1	General Purpose I/O 1 / PWM 1
E7	GPIO2	Input/ Output	General Purpose Output 2	General Purpose I/O 2 / PWM 2
D7	GPIO3	Input/ Output	General Purpose Input/Output 3 If ULPCD is used, GPIO3 cannot be used for any other purpose than aborting the ULPCD.	General Purpose I/O 3 / PWM 3 If ULPCD is used, GPIO3 cannot be used for any other purpose than aborting the ULPCD.
Security feature				
B4	PRD1	Input/ Output	Package removal detection, internally connected to PRD2	Package removal detection, internally connected to PRD2
G4	PRD2	Input/ Output	Package removal detection, internally connected to PRD1	Package removal detection, internally connected to PRD1
Pins connected on PN76 family only				
A5	PVDD_ OUT	Output	Do not connect	PVDD LDO output
A6	I2CM_ SDA	Input/ Output	Do not connect	I^2C controller SDA
A7	DWL_REQ	Input	Recommended: Do not connect - entering secure firmware download by command. If connected, this pin allows to enter the Secure firmware download mode if set high during hardware reset.	Download request (optional)
B5	GPIO5	Input/ Output	Do not connect	General Purpose I/O 5
B6	I2CM_SCL	Input	Do not connect	I^2C controller SCL
B8	SWDIO	Input/ Output	Do not connect	Single Wire Debug Interface Data

Table 5. Pin description VFBGA64*...continued*

Pin Number	Symbol	Type	Description PN5190	Description PN7642
C2	TEST	Input/ Output	Internal test pin. Do not connect	Internal test pin. Do not connect.
C4	ISO_INT_ AUX	Input/ Output	Do not connect	Auxiliary Card Interrupt
C5	GPIO4	Input/ Output	Do not connect	General Purpose I/O 5
C6	HOST_IF_ SEL1	Input	Do not connect	Host interface select 1
C7	HOST_IF_ SEL0	Input	Do not connect	Host interface select 0
C8	SWD_CLK	Input	Do not connect	Single Wire Debug Interface Clock
D1	USB_ VBUS	Input	Do not connect	Used for USB VBUS detection
D4	ISO_IO_ AUX	Input/ Output	Do not connect	Auxiliary Card I/O
E2	AD1	Input	Do not connect	Analog/Digital converter Input 1
E4	ISO_CLK_ AUX	Input	Do not connect	Auxiliary Card Clock
F5	SPIM_ MOSI	Input	Do not connect	SPI controller MOSI
F6	SPIM_ MISO	Output	Do not connect	SPI controller MISO
G5	SPIM_ SCLK	Input	Do not connect	SPI controller clock
G6	SPIM_ NSS	Input	Do not connect	SPI controller NSS

[1] Updated the terms "master/slave" to "controller/target" to align with the recommendation of the NXP - I^2C and JEDEC SPI standards organization

For good RF performance, all blocking capacitors shall be placed on the same side of the PCB, traces from pin to capacitor shall be as short as possible.

All Supply GND connections shall be connected by low-ohmic connections on the PCB.

9 Functional description

9.1 Functional overview

The PN7642 is a Cortex M33 microcontroller that integrates an NFC frontend with high transmitter output power. It implements the RF functionality like an antenna driving and receiver circuit and all the low-level functionality to realize an NFC Forum-compliant reader.

The PN7642 contains a secure cryptographic subsystem that consists of secure DMA, one accelerator for symmetric cryptography, one accelerator for asymmetric cryptography, one key obfuscation and transfer unit, one True Random Number Generator and a secure symmetric key store.

Arm Cortex M33 processor

The Arm Cortex-M33 is based on the ARMv8-M architecture that offers systems enhancements, such as low power consumption, enhanced debug features, and a high level of support block integration. The Arm Cortex-M33 CPU employs a 7-stage instruction pipe and includes an internal prefetch unit that supports speculative branching. A hardware floating-point processor is integrated into the core. On the PN7642, the Cortex-M33 is augmented with one hardware co-processors providing accelerated support for cryptography.

Nested vectored interrupt controller (NVIC) for Cortex-M33

The NVIC is an integral part of the Cortex-M33. The tight coupling to the CPU allows for low interrupt latency and efficient processing of the late arriving interrupts.

NVIC features

- Controls system exceptions and peripheral interrupts.
- 48 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Configurable levels of interrupt priority from 8 to 256. This is configured at implementation to support 8 priority levels.
- Non-maskable Interrupt (NMI).
- Software interrupt generation.

Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

System tick timer (SysTick)

The Arm Cortex-M33 core includes a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the system clock or the SYSTICK clock.

On-chip static RAM

The PN7642 supports up to 32 kB SRAM with separate bus controller access for higher throughput and individual power control for low-power operation. 20 kB RAM are available to the user.

On-chip flash

The PN7642 supports up to 256 kB of on-chip flash memory, where 180 kB is accessible by the user. 76 kB are reserved by the system.

Clock supply

The PN7642 uses an external 27.12 MHz crystal as clock source for generating the RF field and its internal digital logic. Alternatively, an internal PLL allows using an accurate external clock source of either 24 MHz, 32 MHz, and 48 MHz (configured in EEPROM register CLK_INPUT_FREQ, 0012h)). This allows saving the 27.12 MHz crystal in systems which implement one of the mentioned clock frequencies.

Integrated DC-DC

The integrated DC-DC allows a single supply voltage while delivering maximum RF output power. Dependent on the application target either a direct transmitter supply or a transmitter supply by the integrated DC-DC can be chosen. The usage of the integrated DC-DC is the preferred choice for stable RF performance, even in case of a de-charged battery. Optimized usage of a battery charge can be achieved by directly connecting the transmitters to the supply. The DC-DC is controlled by the Dynamic Power Control 2.0 to keep the power dissipation of the chip minimized in antenna loading cases which require a reduction of the RF output power.

The DC-DC is a step-up converter and is able to deliver an output voltage from approx. 2.8 V up to 6.0 V. The targeted output voltage can be configured by software.

The DC-DC clock is synchronized with the clock of the receiver - this avoids the typical performance reduction by DC-DC noise which can be seen in systems using external DC-DCs.

Transmitter LDO (VDDPALDO)

The transmitter output drivers are supplied by a transmitter LDO which reduces external noise and is used for the DPC functionality to lower the supply voltage of the transmitters. The high granularity of 100 mV for setting the VDDPALDO output voltage together with a sophisticated control loop and true current measurement ensures that a DPC regulation is not accidentally treated as received data.

Ultra Low-power card detection

The ultra low-power card detection (ULPCD) enables saving battery charge during polling for NFC counterparts like cards and mobile phones. In general, the ultra low-power card detection provides a functionality, which allows to power down the NFC controller for a certain amount of time to safe energy. After some time, the NFC controller becomes active again to poll for cards. If no card is detected, the device can go back to the power down state.

Dynamic power control 2.0

The next generation dynamic power control (DPC2.0) with true transmitter current measurement works autonomously without host interaction. Avoiding additional host controller processing load is important for time critical applications like payment. A fast control response time of less than 1 ms allows using optimized antenna matching.

Adaptive waveshape control

The adaptive waveshape control (AWC) helps to keep the wave shapes within specification limits, even in case of antenna detuning. This simplifies the time-consuming antenna-matching procedure and does not require any matching compromises to be taken.

Receiver signal level control

The receiver signal chain consists of an automatic controller RF input attenuator and a true baseband amplifier (BBA). This feature delivers an outstanding communication range with tags, labels, cards, and mobile phones.

RF Debugging

Comprehensive and innovative debug features are implemented to support the NFC reader development even for difficult and non-standard compliant cards and mobile phones. An Integrated Chip scope allows for performing a non-intrusive debugging of receiver signals without the need to connect additional wires to the chip. Capturing of chip-internal signals is done by configuring flexible trigger conditions, sampled internal data is stored in RAM memory, transferred by SPI to a host microcontroller and visualized on a PC by the NFC Cockpit development tool. A virtual COM interface (VCOM) is supported by the NFC cockpit tool, which allows to use the NFC cockpit together with any host microcontroller. Analog debug signals (AUX1, AUX2) are available as well and allow the connection of an Oscilloscope for analog and digital signal debugging.

The receiver signal processing is optimized to cope with noisy environments. This is beneficial, especially in case a TFT display or DC-DCs are part of the NFC system.

Automatic EMD error handling

An automatic EMD handling performed without host interaction relaxes the timing requirements on the Host controller. Automatic EMD error handling according to ISO/IEC14443 and EMVCo 3.0 is supported. In addition, the EMD error handling is widely configurable, which allows adaptions in case of future possible specification changes.

Firmware update

The PN7642 supports a secure update of the implemented firmware. The secure firmware download mode is using a dedicated command set. The firmware download does not require any additional hardware pin to be

handled, instead the download mode is activated by a command, followed by a hardware reset. After booting from reset, the PN7642 will be in download mode.

For the secure firmware update, the following interfaces can be used: I^2C, I^3C, SPI, and UART.

Register configuration

Internal registers of the PN7642 store volatile configuration data. The internal registers are reset to configurable initial values in case of power-on, hardware-reset, and standby.

The configuration for dedicated RF protocols and antenna-dependent configuration is defined in non-volatile memory. This configuration is typically done only once during production, and is performed by a command issued from the PN7642 user application.

EEPROM configuration

Non-volatile EEPROM memory of the PN7642 is used to store configuration data that must be preserved in case the PN7642 is not connected to any supply voltage. The configuration for dedicated RF protocols and antenna-dependent configuration is defined in this non-volatile memory and copied to volatile registers by the PN7642 user application. In addition, other configuration data which must be preserved during power supply disconnect is stored in this EEPROM memory as well. Examples for this are configurations for DPC and ULPCD configurations.

RF configuration

The PN7642 allows a fast RF protocol selection based on the command Load_RF_configuraton and pre-defined user configuration data in non-volatile memory (EEPROM).

On the one hand, the configuration of modulation-related parameters can be done (e.f. selection of ISO/IEC14443-A), on the other hand antenna-specific parameters can be configured

Cryptographic subsystem

The PN7642 includes a cryptographic subsystem that accelerates symmetric and asymmetric operations. Furthermore it contains a symmetric key store that helps to securely store customer keys. With the help of the key transfer unit, keys can be loaded directly into the crypto subsystem without passing the CPU, which significantly enhances the confidentiality of the keys.

9.2 Endianness

The endianness describes the order of bytes or bits within a binary representation of a value in the memory, which can be a register or EEPROM.

"Array size" defines the number of elements of "type size". Type size can be uint8 (8 bit), uint16 (16 bit) or uint32 (32 bit).

The location of byte-sized data (8 bit) with an array size of 2 is as follows:

Value hex: 0x1234

address x: 12

address x+1: 34

The location of word-sized data (16 bit) is as follows:

Value hex: 0x1234

address x: 34

address x+1: 12

The location of word-sized data (16 bit) in an array size of 2 is as follows:

The placement of the array is large endian, the placement of nibbles of the variable is small endian.

Value hex: 0xAABBCCDD

address x: BB

address x+1: AA

address x+2: DD

address x+3: CC

The location of double word-sized data (32 bit) is as follows:

Value hex: 0xAABBCCDD

address x: DD

address x+1: CC

address x+2: BB

address x+3: AA

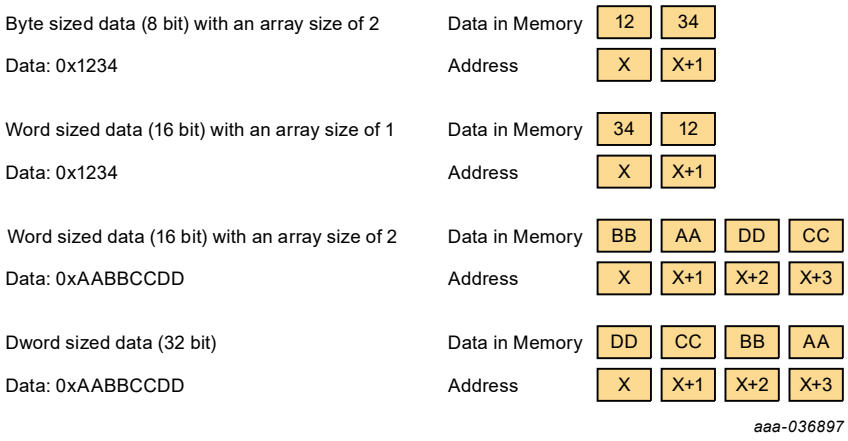


Figure 3. Endianness examples

The PN7642 is a little-endian system. This means that the byte at the lower address is read first.

9.3 CPU Sub System

9.3.1 Overview

The PN7642 device is controlled using a CPU (Arm) subsystem described in the following section. The CPU Sub-System is controlled by an Arm Cortex M33 Processor that runs the application firmware. It incorporates two DMA controllers of type PL080 which aim to transfer data between peripherals and the system RAM but also between memories only. These DMA controllers are connected to an AHB Lite multi controller matrix and an AHB-to-APB bridge that gives access to the various target peripheral IPs (e.g. HostIF)

The CPU Sub-System includes two external Implementation Defined Attribution Units (IDAUs), one for each of its two AHB controller ports, and a special firewall IP for memory segmentation and access right management. Together with Arm's Trust Zone concept, this is the core concept to enable an open platform architecture by

configuring memory apertures to protect/restrict specific memory regions and IP accesses from user application code or debug accesses.

9.3.2 Features

The PN7642 CPU subsystem provides the following set of features:

- Arm Cortex M33 Processor with Security Add-ons (Trust Zone)
  Note: The Trust Zone is not available to the user. It is used for internal purposes.
- Single Cycle Multiplier, Vector Table Offset Register (allowing relocation of Vector Table), SysTick, NVIC with 48 user interrupts, SWD DAP, and debug options
- Code Patch Module with 48 entries
- AHB-Lite multilayer (6 AHB Controllers, 11 AHB Targets)
- AHB to APB bridge (19 APB Targets)
- SRAM/ROM controllers and FLASH controller
- Standard Arm CoreSight Debug Architecture
  - Single Wire Debug Access Port (SW-DP)
  - Embedded Trace Macro cell (ETM)
  - Cross Trigger Interface (CTI)
  - 4 kB Embedded Trace Buffer (ETB)
- Internal Trace RAM configurable for normal usage if debug is not needed
- Secure and Application accessible high performance DMACs (PL080)
- One IDAU per CPU AHB controller port, and firewall IP monitoring any AHB-Lite Interconnect for CPU mode aware access control to AHB targets
- AHB split, retry and locked transfers are not supported

9.3.3 Block diagram

The block diagram is showing the high-level CPU subsystem integration and its surrounding IPs.

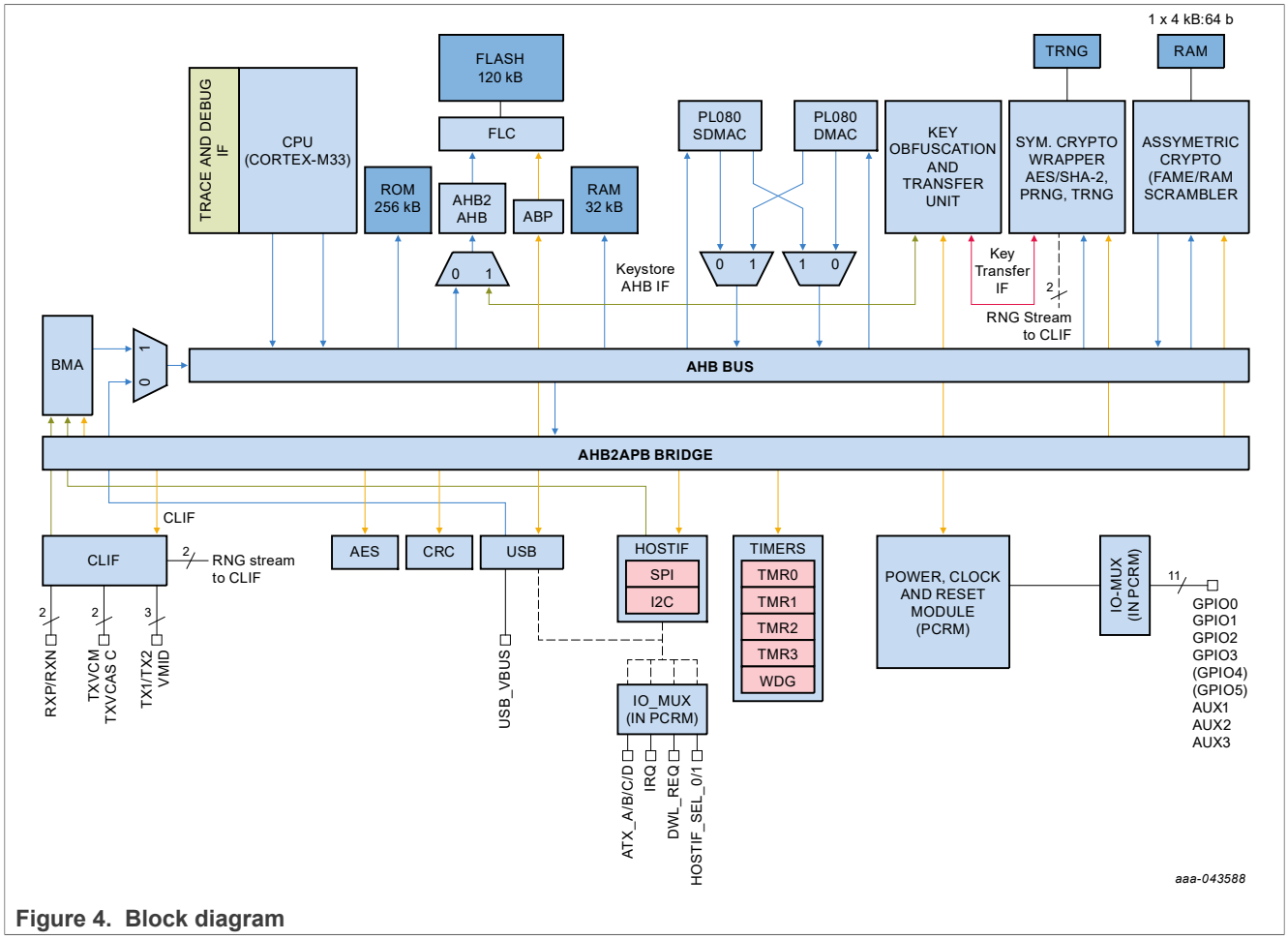


Figure 4. Block diagram

The AHB multilayer brings high-bandwidth connections between the processor and the memories, and access to the APB bridge. It also provides a direct connection from the host interface IP to the SRAM memory. Furthermore, Crypto IPs and USB are AHB controller as well.

The ETB RAM, the main RAM, ROM, and FLASH controllers are part of the CPU subsystem and provide interfaces to the bare memory modules which are typically located outside at the top level of the system.

The DMA subsystem consists of two DMA controllers of type PL080, and both are sharing the two available AHB DMA controller ports at the AHB interconnect. One DMAC is intended to be accessible in Secured CPU mode only, whereas the other is accessible in both Secured and Non-secured CPU Mode. The sharing is done to keep the number of AHB controllers small which is beneficial also for the firewall, since every AHB controller introduces a new port to be monitored and an AHB blocker in this IP.

Another AHB controller port is the Buffer Management and Arbitration Unit's (BMA) port, which can be considered a special purpose DMA port, whose one side will always be an external communication unit. Its other side will always be the system RAM where the BMA maps its receive/transmit buffers. The PN7642 contains a separate communication option for USB which implements its own AHB controller interface. BMA and USB controller normally are never active in parallel, so sharing the AHB lite controller port is acceptable. However in case of access collisions between BMA and USB, the latter takes precedence because the IP does not implement any deep buffering of its data streams.

Firewall and an individual IDAU per CPU AHB port monitor any AHB activities of any AHB controller, and decide based on the given access rights and CPU mode whether access is granted or will lead to an exception.

The AHB-to-ABP bridge translates the high performance AHB protocol into the more compact APB protocol which is the standard protocol for peripherals in an Arm CPU system. The bridge acts on one side like an AHB target. It dissolves the address space into apertures of 4 kB which are assigned to the peripherals of the PN7642 system. Any accesses to non-assigned apertures cause an exception.

Furthermore, the AHB-to-APB bridge supports power down monitoring for each of its APB targets. If an APB target is powered down or its system clock is gated, respectively, it typically indicates this by a flag that is connected to the bridge. If the CPU tries to access such an IP, the bridge converts this access into an exception (HRESP will be set to “ERROR”). This is important for clock gated IPs in particular because otherwise access will never be terminated and the system would stall.

Note: The PN7642 supports a system clock of 90 MHz but the Flash controller 45 MHz only. In order to benefit from the 90 MHz for the rest of the system, the AHB as well as the APB ports of the FLASH controller are connected to the AHB interconnect and the APB bridge via special clock scalers. They guarantee a division of the FLASH controller’s system clock by two if the high system clock option is active. If 45 MHz are selected as system clock, then the scalers are bypassed.

9.3.4 System tick timer

The system tick timer (SysTick timer) is an integral part of the Arm Cortex-M33 core. It is basically a 24 bit down counter which can be started and configured with an automatic reload value. If the timer is running and its IRQ is enabled, it generates periodic interrupts intended to be used, for example, by an operating system, in particular Real-Time operating Systems (RTOS) or other system management software. The intent is to provide a fixed time interval between interrupts so that the OS can carry out task management — for example, to allow multiple tasks to run at different time slots and to make sure that no single task can lock up the whole system. The SysTick timer is clocked internally by a dedicated system tick timer clock.

9.3.4.1 Features

- 24-bit timer
- Uses dedicated exception vector
- Dedicated system tick timer clock
- Clock source configurable (system clock or SYSTICK clock)

9.3.5 Memories maps

9.3.5.1 General

The PN7642 contains 256 kB on-chip flash programming memory, where parts are reserved for the system. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip bootloader software.

The following section gives an overview on the PN7642 memories.

9.3.5.2 Main memory map

The following table shows, how the Cortex M33 global AHB address space is dissolved into regions, and what AHB controllers and targets can be accessed via what memory window. Accesses to the gaps in between are caught by a “default target” which is connected to every AHB controller port as a terminal unit in order to avoid deadlocks by unauthorized memory access request. The default targets make sure that access is correctly handled and raises a bus fault.

Note: From the user application, only a reduced part of the AHB addresses is accessible. The remaining peripherals can be accessed via the System Services API only.

Table 6. Global AHB Memory map

Address Range	Region	Size	Application
0xE0100000 - 0xFFFFFFFF	System	Reserved	Default target error response
0xE00FF000 - 0xE00FFFFF	External PPB bus	4 kB	Reserved
0xE00FE000 - 0xE00FEFFF		4 kB	Reserved
0xE0046000 - 0xE00FDFFF		Reserved	Default target error response
0xE0046000 - 0xE0046FFF		4 kB	Reserved
0xE0045000 - 0xE0045FFF		4 kB	Reserved
0xE0044000 - 0xE0044FFF		4 kB	Reserved
0xE0043000 - 0xE0043FFF		Reserved	Default target error response
0xE0042000 - 0xE0042FFF		4 kB	Reserved
0xE0041000 - 0xE0041FFF		4 kB	Reserved
0xE0040000 - 0xE0040FFF		4 kB	Reserved
0xE003E000 - 0xE003FFFF	PPB internal	Reserved	Default target error response
0xE002E000 - 0xE002EFFF		4 kB	Reserved
0xE000F000 - 0xE001EFFF		Reserved	Default target error response
0xE000E000 - 0xE000EFFF		4 kB	Reserved
0xE0003000 - 0xE000DFFF		Reserved	Default target error response
0xE0002000 - 0xE0002FFF		4 kB	Reserved
0xE0001000 - 0xE0001FFF		4 kB	Reserved
0xE0000000 - 0xE0000FFF		4 kB	Reserved
0xA0000000 - 0xDFFFFFFF	EXT Device	Reserved	Default target error response
0x60000000 - 0x9FFFFFFF	EXT Ram	Reserved	Default target error response
0x40029000 - 0x5FFFFFFF	Peripheral	Reserved	Default target error response
0x40028000 - 0x40028FFF		4 kB	Reserved
0x40023000 - 0x40027FFF		Reserved	Default target error response
0x40022000 - 0x40022FFF		4 kB	SPI controller
0x40021000 - 0x40021FFF		4 kB	PWM control (utimer)
0x40020000 - 0x40020FFF		4 kB	DMAC Configuration
0x40010000 - 0x4001FFFF		64 kB	Reserved
0x40000000 - 0x4000FFFF		64 kB	Application accessible APB-Peripherals
0x20020000 - 0x3FFFFFFF	SRAM	Reserved	Default target error response
0x2001C000 - 0x2001FFFF		16 kB	Reserved
0x20018000 - 0x2001BFFF		16 kB	Reserved
0x20011000 - 0x20017FFF		Reserved	Default target error response
0x20010000 - 0x20010FFF		4 kB	Reserved
0x20009000 - 0x2000FFFF		Reserved	Default target error response
0x20008000 - 0x20008FFF		4 kB	NFC_RAM_ALV

Table 6. Global AHB Memory map*...continued*

Address Range	Region	Size	Application
0x20000000 - 0x20007FFF		32 kB	NFC_RAM
0x00240000 - 0x1FFFFFFF	Code	Reserved	Default target error response
0x00200000 - 0x0023FFFF		256 kB	NFC_FLASH
0x00040000 - 0x001FFFFF		Reserved	Default target error response
0x00000000 - 0x0003FFFF		256 kB	Reserved

9.3.5.3 Peripheral memory map

PN7642 incorporates a total number of 19 peripherals which area accessible by the CPU via an AHBtoAPB bridge. This bridge reacts like an AHB target toward the CPU and translates AHB accessed into APB accesses toward the addressed peripheral. The bridge is configured for peripheral aperture sizes of 0x1000 bytes (4 kB), and maps all peripherals into the global 64 kB AHB windows. The following subset of the peripherals is accessible from the user area directly.

Table 7. Peripheral memory map

APB ID	APB interface	Start Address	End Address	Size (kB)
15	Reserved	0x4000F000	0x4000FFFF	4
14	Reserved	0x4000E000	0x4000EFFF	4
13	Reserved	0x4000D000	0x4000DFFF	4
12	Reserved	0x4000C000	0x4000CFFF	4
11	LP_UART	0x4000B000	0x4000BFFF	4
10	Reserved	0x4000A000	0x4000AFFF	4
9	BMA_APB	0x40009000	0x40009FFF	4
8	Reserved	0x40008000	0x40008FFF	4
7	Reserved	0x40007000	0x40007FFF	4
6	Reserved	0x40006000	0x40006FFF	4
5	TIMERS_APB	0x40005000	0x40005FFF	4
4	Reserved	0x40004000	0x40004FFF	4
3	CT_APB	0x40003000	0x40003FFF	4
2	I2CM_APB	0x40002000	0x40002FFF	4
1	USB_APB	0x40001000	0x40001FFF	4
0	HOSTIF_APB	0x40000000	0x40000FFF	4

9.3.5.4 On-chip flash memory map

The flash memory mapping is described in the following table.

Table 8. Flash memory map

Description	Size	Start - End
NXP firmware	32 kB	0x200000 - 0x207FFF
User application	180 kB	0x208000 - 0x234FFF

Table 8. Flash memory map*...continued*

Description	Size	Start - End
NXP firmware	44 kB	0x235000 - 0x23FFFF

The memory region described as "User application" is the region that is accessible by the developer and from where the user application is being executed. The regions described as "NXP firmware" cannot be accessed from the "User application" region.

9.3.5.5 On-chip RAM memory map

The PN7642 contains a total of 32 kB of RAM memory. The memory mapping is shown in the table below.

Table 9. RAM memory map

Description	Size	Start - End
System reserved	12 kB	0x20000000 - 0x20002FFF
User	20 kB	0x20003000 - 0x20007FFF
Application ALV (Always On) RAM	2.5 kB	0x20008000 - 0x20008A3F Memory addresses 0x20008600 - 0x20008A3F is reserved for NXP FW.

9.3.5.6 On-chip ROM memory

The PN7642 includes 256 kB of on-chip ROM memory. The on-chip ROM contains the bootloader, USB mass storage primary download and parts of the NXP firmware.

9.3.5.7 On-chip flash data memory

The PN7642 includes 4 kB of on-chip flash data memory. The flash data memory is accessible via the EEPROM HAL APIs from the user application. It used to store persistent configuration data of the PN7642.

Table 10. EEPROM memory map

Description	Size	Start - End
User flash data memory	4 kB	0x0000 - 0xFFF User data region (E_PN76_EEPROM_USER_AREA) 0x0000-0x03FF (1 kB) Secure FW settings region (E_PN76_EEPROM_SECURE_LIB_CONFIG) 0x0000-0x07FF (2 kB) IC configuration region (E_PN76_EEPROM_IC_CONFIG) 0x0000-0x03FF (1 kB)

9.4 NFC Sub System

9.4.1 Initial calibration

The PN7642 requires a calibration before the RF field is switched on for the first time with unloaded condition.

"Unloaded" means: Without any additional metal in proximity of the antenna, except for the NFC reader components itself.

During development of new readers, this calibration shall be done each time the antenna design, antenna matching, or EMC filter is modified.

The calibration sequence is the following:

Write EEPROM NOV_CFG_CAL

Write REGISTER TX_NOV_CALIBRATE_AND_STORE

Write EEPROM NOV_CFG_CAL

9.4.2 Transmitter overcurrent and temperature protection

The PN7642 implements different mechanisms to protect the chip against damage.

On the one hand, an overcurrent protection exists which shuts down the Transmitter Driver in case of a out of spec current. This can be enabled in EEPROM TXLDO_CONFIG, bit 1: overcurrent enable (0: disable, 1: enable)

The actual measured temperature is available in the register TEMP_SENSOR.

This is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

9.4.3 Dynamic power control (DPC)

The DPC is used for a special antenna tuning, called "symmetric antenna tuning". For an "asymmetric antenna tuning", the DPC is not required.

However, even for "asymmetric antenna tuning" with high output power needs, it might turn out that the RF field is too strong in close proximity of the antenna to be compliant with ISO/IEC14443 requirements. In this case, the DPC can be used as well to reduce the RF output power dependent on the distance of the card from the reader antenna.

The DPC works very well with a tuning called "symmetric tuning". With symmetric tuning, a detuning of the antenna is causing a reduction of the antenna impedance. This low antenna impedance might lead to a current which is too high for the targeted application. The DPC allows to limit the transmitter current even under antenna detuning conditions.

DPC is useful:

- To achieve NFC Forum and ISO/IEC 14443 compliancy (e.g. NFC Forum Power Transfer Maximum, ISO/IEC 14443 Field Emission Maximum)
- To improve interoperability

The Dynamic Power Control (DPC 2.0) allows controlling the transmitter driver voltage in 100 mV steps dependent on the actual transmitter current.

A lookup table is used to configure the transmitter output voltage and by this control the RF output power.

Features of the Dynamic power control (DPC 2.0):

- True current measurement provides maximum information for the regulation loop
- The transmitter current can be limited and additionally reduced according to detected transmitter current condition / antenna detuning condition
- DPC works autonomously without host interaction causing no additional processing load on the host
- Fastest response time of 1 ms for regulation
- Used for adaptive waveshape control (AWC)
- Used for adaptive RX sensitivity control (ARC)

The DPC is able to operate in two modes:

1. Current limiting mode
2. Current limiting + Current reduction mode

The DPC is configured in the EEPROM, this configuration is used after startup. This avoids that the host must configure the chip after each reset or power off.

The following EEPROM registers are most relevant for the DPC configuration:

DPC_Config: Enables/Disables the DPC (enable: 0x39, disable: 0x00)

DPC_TARGET_CURRENT: Unloaded VDDPA target current in mA, the target current +/- Hysteresis is limiting the current for the DPC.

- The DPC_TARGET_CURRENT is the current which can be measured for the selected antenna impedance and transmitter supply voltage in unloaded condition. This is the current the system is designed to operate at.

DPC_Hysteresis: Absolute difference to current target current in mA that triggers a DPC update event.

- The configuration of the hysteresis ensures, that the DPC is not regulating if small changes of the transmitter current occur due to external disturbances. A typical value for the DPC_Hysteresis is e.g. 20 mA.

DPC_Lookup_Table: Configures the current reduction

The DPC_LOOKUP_TABLE allows in addition to the limitation of the current, to configure

- an additional current reduction on top of the current limitation, achieved by further lowering the transmitter supply voltage
- a relative change of modulated amplitude level
- and a relative change of falling and raising edge time constant for ASK10% and ASK100% modulations

This lookup table is initialized with 0x00 for devices delivered from the factory. (The customer development board is already initialized with useful data in EEPROM which work well with the antenna of the board).

The 0x00 entry in the DPC_LOOKUP_TABLE means that no additional function then the current limitation takes place for the DPC.

In order to achieve a limitation of the current even in the case of an antenna impedance that is lowered, the Transmitter supply voltage is reduced accordingly.

This transmitter supply voltage reduction is now used as index for the DPC_LOOKUP_TABLE.

For a specific transmitter supply voltage, it is possible to further reduce the current below the value of DPC_TARGET_CURRENT or to configure parameters for waveshaping and modulation. All these entries are relative values, granularity of the entries dependent on the transmitter supply voltage is 0.1 V, resulting in 42 table entries.

The DPC updates the content of the following register dependent on the antenna load / lookup table configuration:

DGRM_RSSI

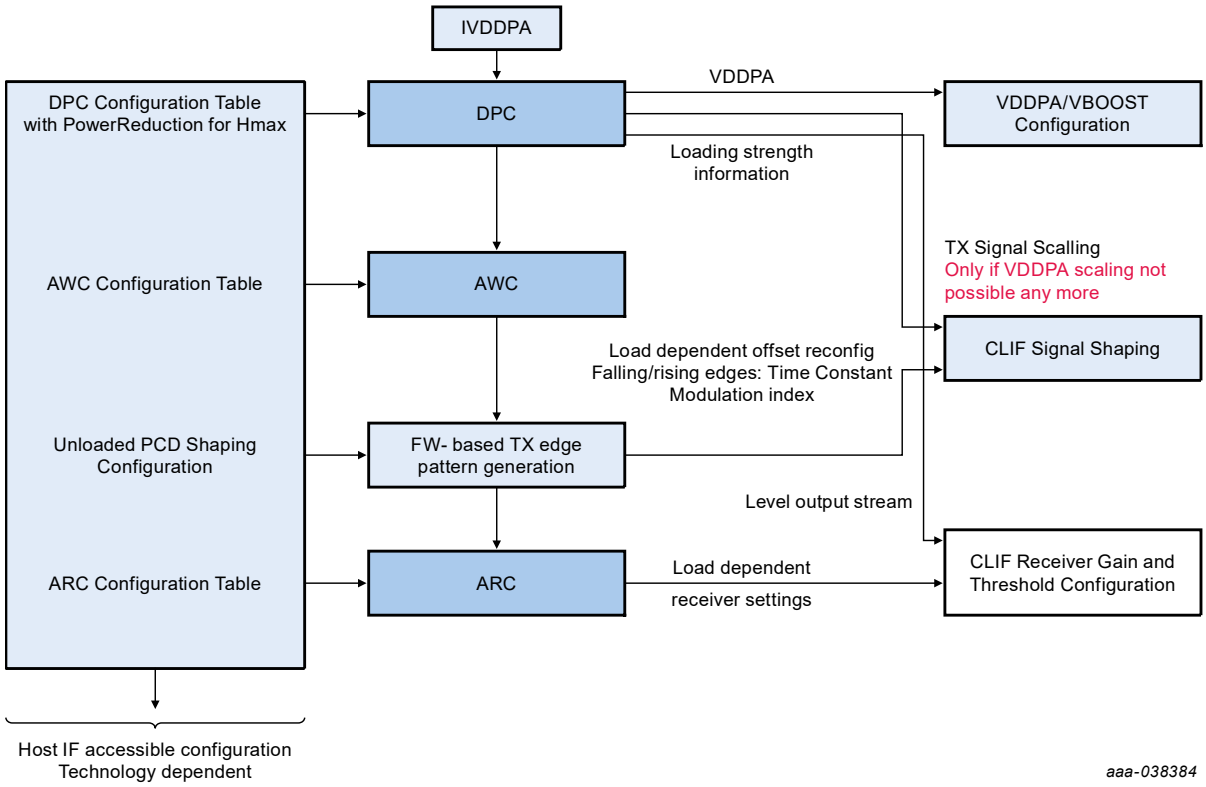


Figure 5. System overview: DPC, AWC, and ARC

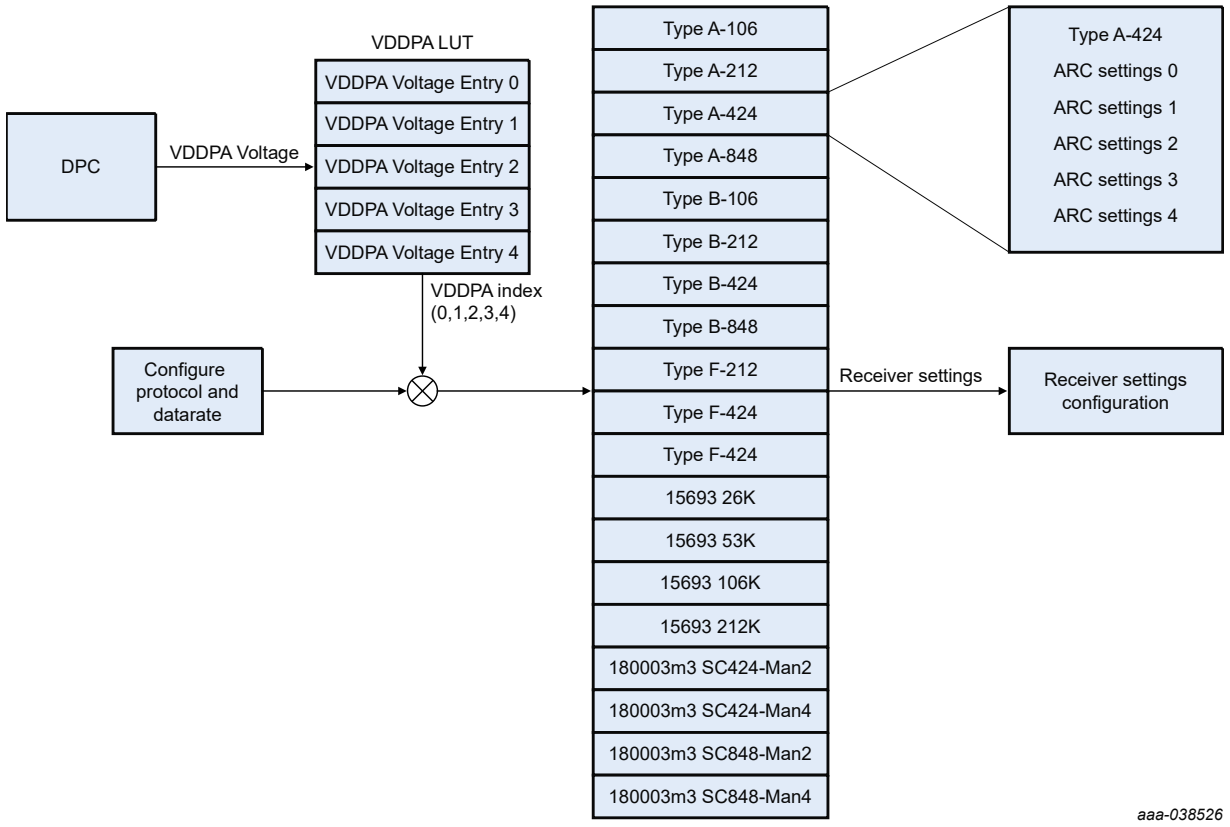


Figure 6. System overview: DPC, AWC, and ARC

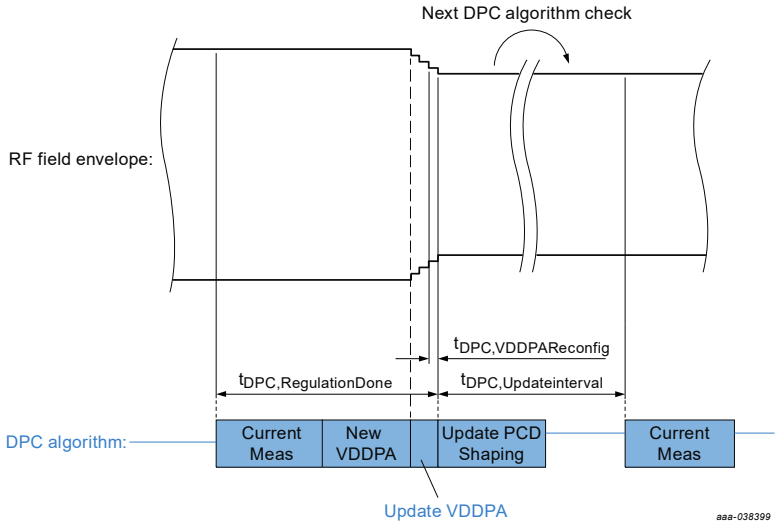


Figure 7. System overview: DPC, AWC, and ARC

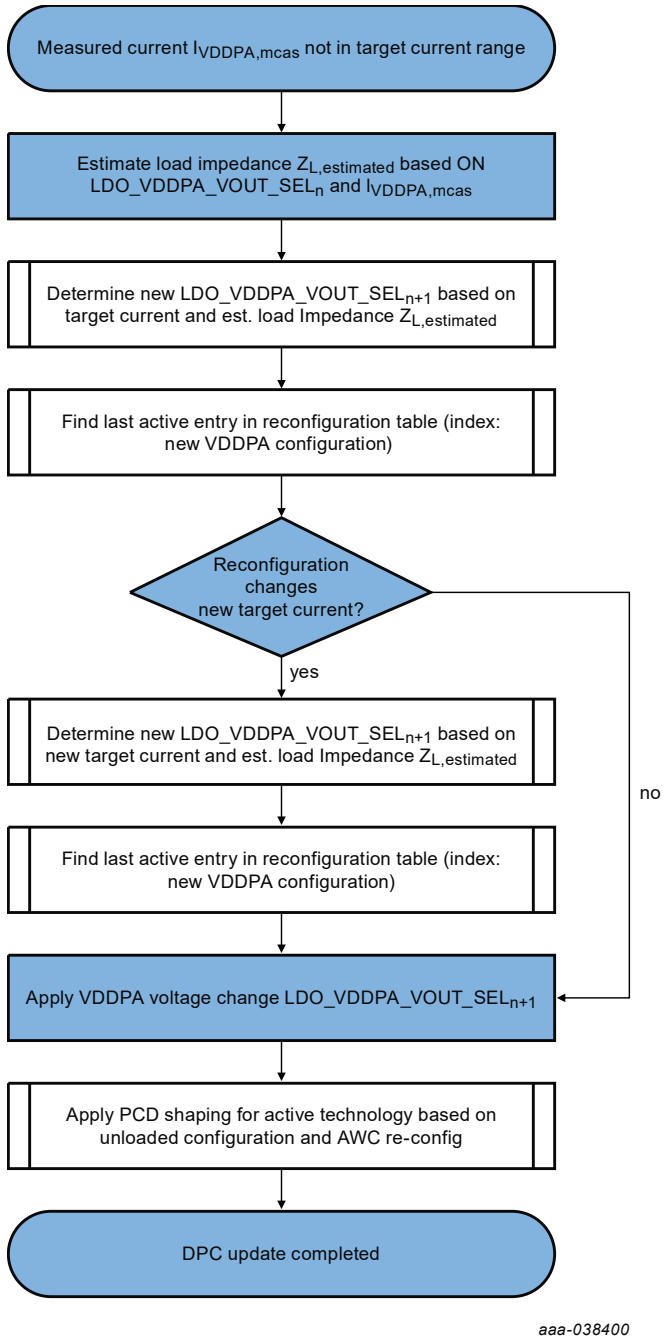


Figure 8. System overview: DPC, AWC, and ARC

9.4.3.1 DPC algorithm

The DPC algorithm is controlling the transmitter current. It is using the following states:

1. Current measurement: Performs VDDPA current measurement
2. New VDDPA: Determine new VDDPA configuration based on measured current
   VDDPA New (for target current of Itarget) = VDDPA Voltage / VDDPA current * Itarget
3. Update VDDPA: Perform output power update
4. Update PCD Shaping: Apply AWC configuration updates for active technology
5. Update RX sensitivity parameter only for short duration

Reconfiguration table includes Relative changes of target current and of waveform parameters adaption for all VDDPA voltage configurations. The VDDPA configuration is implicitly defined by the row index. The first row refers to LDO_VDDPA_VOUT_SEL=0 (represents 1V5).

EXAMPLE:

Unloaded configuration After Field ON:

VDDPA max set to 42 (5.7 V) ·Target current set to 280 mA

Technology B106: amp_mod=200

Falling edge time constant=rising edge time constant=3

Table 11. DPC_LOOKUP_TABLE element, defining the configuration for one dedicated VDDPA voltage

Function	Bit	Description
ENTRY 0	31:0	This is the entry for 1.5 V.
Target current reduction	31:23	ENTRY 0 -LSB - byte 0 Voltage step between DPC entries = 100 mV. Voltage offset start = 1.5 V bEntry_00 = 1V5 ... bEntry_42 = 5V7 Bits[7:0] = Target current reduction in mA (unsigned)
AWC amp mod change	23:16	ENTRY 0 - byte 1 Bits[7:0] = Relative change of modulated amplitude level (signed)
AWC edge time constant for ASK100	15:8	ENTRY 0 - byte 2 Bits[3:0] = ASK100, Relative change of falling edge time constant (signed) Bits[7:4] = ASK100, Relative change of rising edge time constant (signed)
AWC falling edge time constant for ASK10	7:0	ENTRY 0 -MSB - byte 4 Bits[3:0] = ASK10, Relative change of falling edge time constant (signed) Bits[7:4] = ASK10, Relative change of rising edge time constant (signed)

Loaded configuration After Field ON:

DPC regulates from unloaded VDDPA configuration 42 to 31. Consequently, new configuration to be applied based on index entry 31.

Target current stays at 280 mA.

Technology B106: amp_mod=205, falling edge time constant=2, rising edge time constant=0

9.4.3.2 DPC characteristics

Table 12. Dynamic power control characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Minimum hysteresis configured in EEPROM DPC_HYSTERESIS	Depends on application target current	ApplicationTargetCurrent * 0.0609 + 2 mA	-	-	mA
	Max target current configured in EEPROM DPC_TARGET_ CURRENT	Hysteresis as configured in DPC_ HYSTERESIS		-	350-Hysteresis	mA

9.4.4 Adaptive waveshape control (AWC)

Depending on the level of detected detuning of the antenna, wave shaping related register settings can be automatically updated.

Two different waveshaping mechanisms can be used:

1. Firmware based shaping (1,2,3)

2. Lookup table based shaping (4,5,6)

The Firmware based shaping allows to correct rise times and overshoot with linear transition shapes.

The lookup table based shaping allows maximum flexibility and enables to configure almost any possible correction.

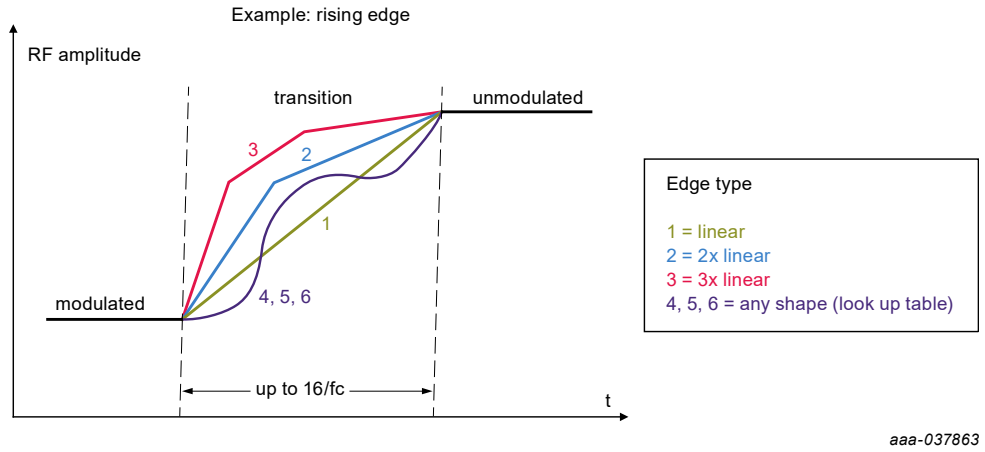


Figure 9. Waveshaping transitions (example falling edge)

The shaping related register settings are stored in a lookup table located in EEPROM, and selected dependent on the actual detected detuning condition.

Each lookup table entry allows the configuration not only of a dedicated wave shaping configuration for the corresponding detuning condition. But allows in addition to configure the wave shaping individually dependent on the actual protocol which is active.

Features of the Adaptive Waveshape Control:

- No external components required
- No need to compromise antenna matching to meet waveshape requirements
- Waveshapes automatically adapted according to detected detuning condition
- RF standards define envelope timing and residual carrier parameters required for compliance and interoperability.

The device supports the design of compliant antennas by allowing to actively shaping the style of edge transition for falling and rising edges. The shaping of modulation edges is achieved by selecting one from three edge transition styles:

1. Linear transition between two amplitude levels

2. Two linear transition´s between amplitude levels and

3. Three linear transitions between amplitude levels.

The type of the transition is selected in the EEPROM registers EDGE_TYPE_(protocol), and can be defined independent for each RF protocol and data rate - for both falling and rising edge.

The EEPROM registers EDGE_STYLE_(protocol) define the time constant "s" of falling/rising edge (depends on edge style).

The EEPROM registers EDGE_LENGTH_(protocol) define the total length of the edge pattern.

The figures below illustrate the edge type for the falling edge.

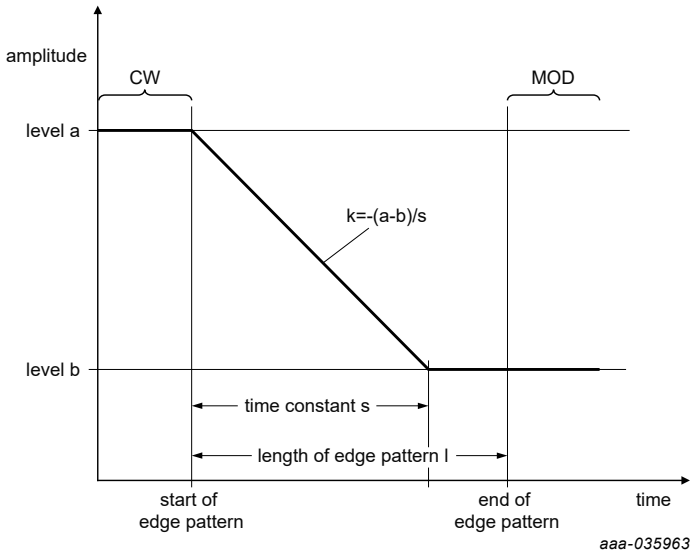


Figure 10. One linear transition (example falling edge)

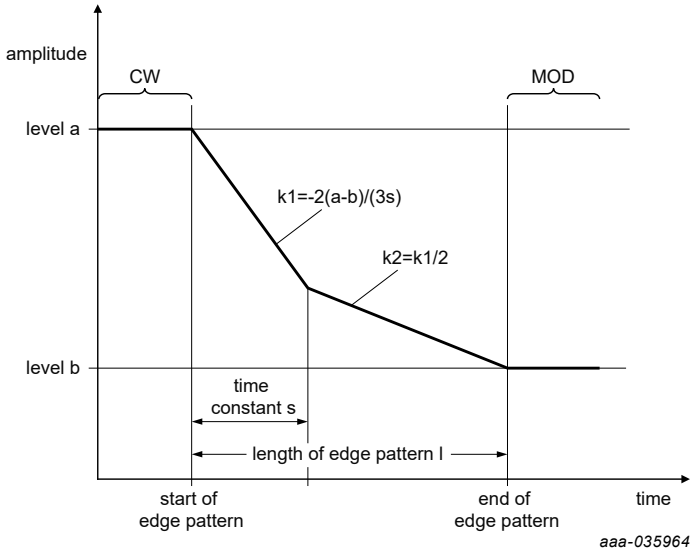


Figure 11. Two linear transitions (example falling edge)

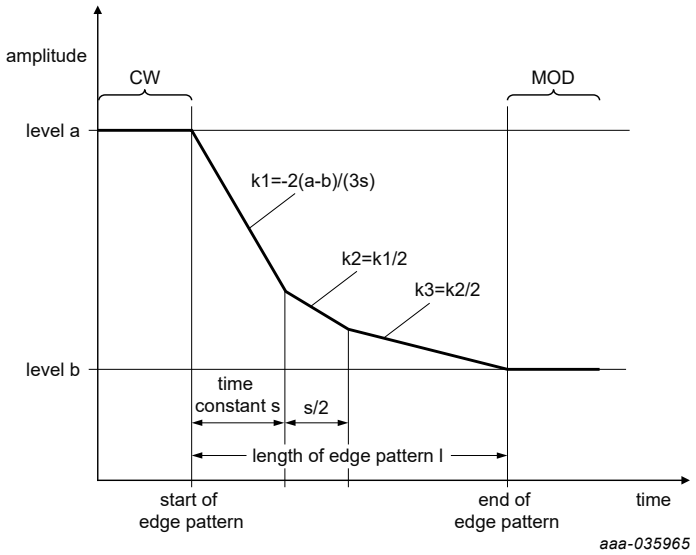


Figure 12. Three linear transitions (example falling edge)

The transition patterns are used as implicit pre-distortion to compensate effects of TX loading circuitry (e.g. resonant circuitry parameters) to the emitted RF envelope.

9.4.5 Adaptive receiver control (ARC)

Depending on the level of detected antenna detuning, receiver-related register settings can be automatically updated. The receiver-related registers which are allowed to be dynamically controlled are:

DGRM_RSSI_REG ->DGRM_SIGNAL_DETECT_TH_OVR_VAL

SIGPRO_RM_TECH_REG ->RM_MF_GAIN,

The adaptive receiver control settings override the default RM_MF_GAIN and DGRM_SIGNAL_DETECT_TH_OVR_VAL settings configured by the command LOAD_RF_CONFIGURATION.

The ARC algorithm is called when VDDPA voltage changes after DPC. There are two lookup tables used in ARC algorithm i.e VDDPA lookup and ARC lookup. In case of a VDDPA change, an EEPROM lookup (at current protocol and baud rate) is performed. The receiver-related settings i.e RM_MF_GAIN, DGRM_SIGNAL_DETECT_TH_OVR_VAL and IIR_ENABLE are read from EEPROM lookup table and configured in registers.

VDDPA lookup table:

VDDPA lookup table define maximum five voltage ranges. Number of VDDPA voltage ranges used in ARC algorithm is configured in bArcConfig[2:0]. VDDPA voltage output from DPC algorithm is input to VDDPA lookup. VDDPA lookup returns VDDPA_range_index (i.e 0,1,2,3,4).

Table 13. ARC_VDDPA EEPROM configuration bit description

Function	Bit	Description
ARC VDDPA Setting	7:0	Byte[4] = ARC_VDDPA_0: ARC_VDDPA_3 > VDDPA < ARC_VDDPA_4
	7:0	Byte[3] = ARC_VDDPA_0: ARC_VDDPA_2 > VDDPA < ARC_VDDPA_3
	7:0	Byte[2] = ARC_VDDPA_0: ARC_VDDPA_1 > VDDPA < ARC_VDDPA_2

Table 13. ARC_VDDPA EEPROM configuration bit description*...continued*

Function	Bit	Description
	7:0	Byte[1] = ARC_VDDPA_0: ARC_VDDPA_0 > VDDPA < ARC_VDDPA_1
	7:0	Byte[0] = ARC_VDDPA_0: 1.5 > VDDPA < ARC_VDDPA_0

ARC lookup table:

VDDPA index and **RF protocol/datarates** are input to ARC lookup. There are five Receiver settings entries for each protocol and data rates. ARC algorithm select one out of five entries (at current protocol and baud rate) based on VDDPA_range_index.

Following table show ARC settings for Type A-106.

Table 14. ARC_RM_A106 EEPROM configuration bit description

Function	Bit	Description
RM_RX_ ARC_4	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ ARC_3	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ ARC_2	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ ARC_1	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)

Table 14. ARC_RM_A106 EEPROM configuration bit description*...continued*

Function	Bit	Description
		Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *For ISO14443-A: In case ARC is disabled, it requires DPC_ SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default))*

Note: *For ISO14443-A: In case Bit[15] is configured to 0, it requires DPC_ SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default)) if the ARC is enabled.*

9.4.6 Energy-saving card detection

There is no trimming for the Low Frequency Timer required.

9.4.6.1 Ultra low-power card detection (ULPCD)

The ULPCD (ultra low-power card detection) offers highest current saving. In this mode, the only wake-up sources to escape from the card detection loop are either a detected antenna detuning, a signal on GPIO3 or a reset (RESET_N) of the PN7642.

The ULPCD cannot be used together with the DC-DC function. A connection as described in the chapter "TX_LDO transmitter supply" or "Direct transmitter supply" is recommended.

Only the wake-up timer is active during ULP standby state.

The ULPCD comprises 2 phases:

1. **Calibration phase**
   In this phase, an RF field is established and the field strength(RSSI) for the unloaded state of the antenna is measured to be used during the measurement phase and stored in a low-power persistent register.
2. **Measurement phase**
   In the measurement phase, the card detection activity is performed autonomously by the hardware at configurable time intervals. This configuration is passed as a parameter to the ULPCD system service API. The RSSI value is measured and compared against the reference value measured in the calibration phase. A card is detected to be in the proximity of the reader when the measured RSSI differs from the reference RSSI by more than a configurable threshold.

The host can set the PN7642 into ultra-low power card detection state (ULP standby state) via the ULPCD system service API.

XTAL_CHECK_DELAY allows to optimize the startup of the crystal for the LPCD and ULPCD modes.

The following EEPROM configuration is available:

- ULPCD_VOLTAGE_CTRL

- ULPCD_RSSI_GUARD_TIME
- ULPCD_RSSI_SAMPLE_CFG
- ULPCD_THRESH_LVL
- ULPCD_GPIO3 - Allows to abort the ULPCD based on GPIO input.

9.4.7 Automatic EMD error handling

The PN7642 supports a configurable EMD handling according to the ISO14443 or EMVCo standard. To support further extensions or changes of these standards, the EMD block is configurable.

After being configured, the PN7642 restarts both the receiver and a timeout timer automatically without host interaction in case of a detected EMD event.

Features of the Automatic EMD Error Handling:

- No real-time constraints
- Less processing load on the host processor
- Configurable, anticipating future specification changes

In addition to the EMD error handling according to ISO14443 and EMVCo, the PN7642 implements special features for FeliCa™ preamble processing.

Registers CLIF_RX_EMD_1_CONFIG and CLIF_RX_EMD_0_CONFIG hold the configurations for the EMD configurations for ISO/IEC14443, and NFC Forum.

EMVCo EMD configuration is supported in the register EMD_CONTROL.

9.4.8 Autocoll (card emulation)

The Autocoll state machine performs the time critical activation for Type-A PICC and for NFC-Forum Active and Passive Target activation (card emulation mode).

The PICC state machine supports three configurations:

- Autocoll mode0: Autocoll mode is left when no RF field is present
- Autocoll mode1: Autocoll mode is left when one technology is activated by an external reader. During RFoff, the chip enters standby mode automatically
- Autocoll mode2: Autocoll mode is left when one technology is activated by an external reader. During RFoff, the chip does not enter standby mode.

At start-up, the Autocoll state machine automatically performs a LOAD_RF_CONFIG with the General Target Mode Settings. When a technology is detected during activation, the Autocoll state machine performs an additional LOAD_RF_CONFIG with the corresponding technology.

The card configuration for the activation is stored in EEPROM. If RandomUID is enabled (EEPROM configuration), a random UID is generated after each RF-off.

For all active target modes, the own RF field is automatically switched on after the initiator has switched off its own filed.

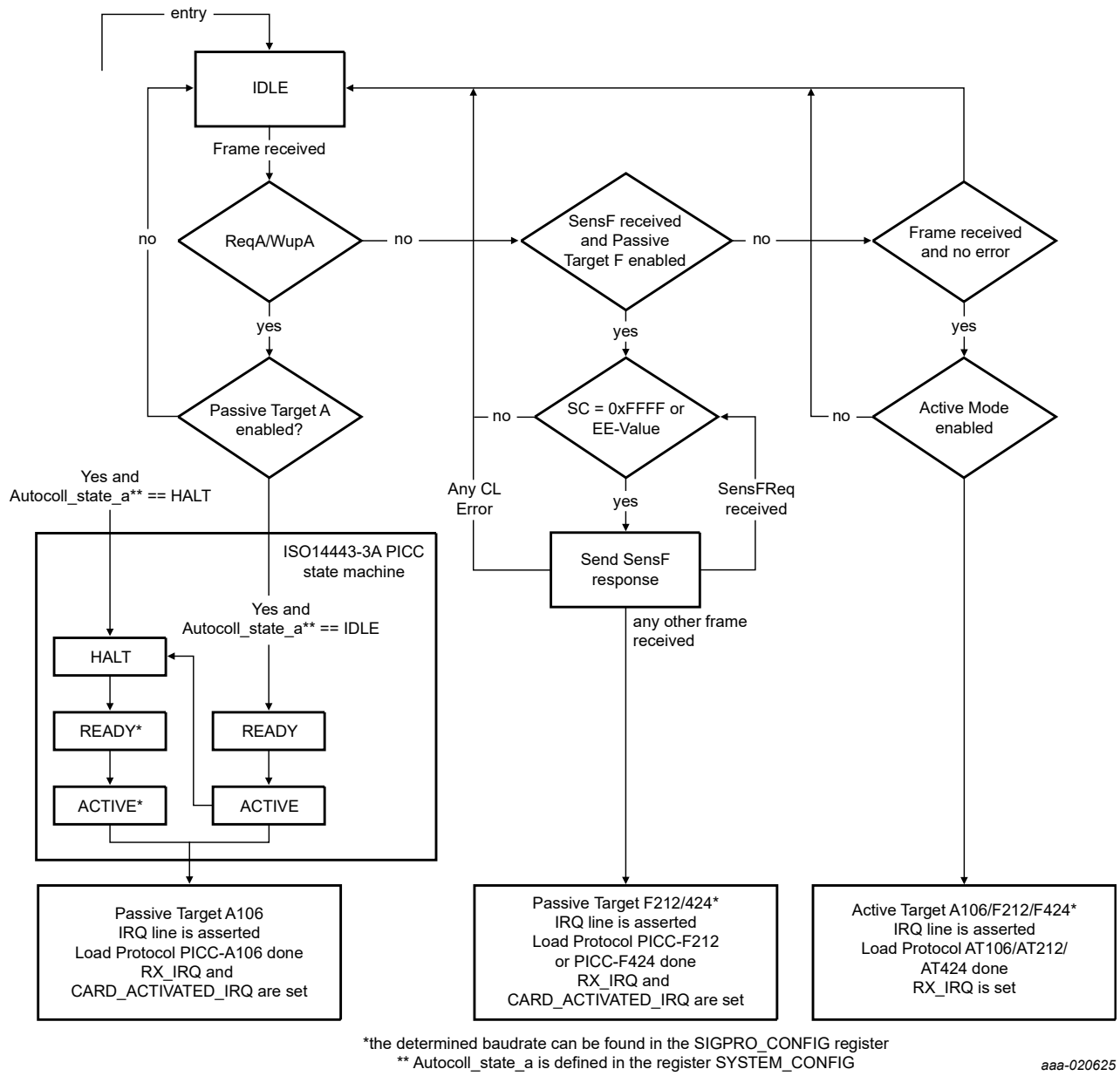


Figure 13. Autocall state machine

9.4.9 RF-level detection

The PN7642 implements an RF level detector (RFLD) and an NFC level detector (NFCLD) which allows to detect the presence of an external RF field.

RF Level Detector:

During low-power card detection (LPCD), the RF level detector (RFLD) acts as wake-up source from power-saving mode.

During ultra low-power card detection (ULPCD), a specific ultra low-power RF level detector is used as RF level detector(RFLD). This can be enabled as wake-up source.

The purpose of the RFLD function is to detect any signal at 13.56 MHz in order to wake up the PN7642 from power-saving mode.

NFC Level Detector:

The NFC Level detector (NFCLD) is used during full power mode. The NFCLD function is required by NFC Forum to support the "RF collision avoidance".

The sensitivity of the NFCLD sensor can be configured by EEPROM register to meet the NFC Forum requirements.

It can be used as well in card mode to detect an external field.

9.4.10 Antenna tuning with variable capacitors

The PN7642 allows the tuning of the connected antenna based on variable capacitors.

Variable capacitors are devices which allow to change their capacity dependent on a supplied control voltage. Typically, these capacitors are used as serial and parallel capacitors in an antenna matching network.

The PN7642 allows to measure a detuning of the connected antenna caused e.g. by surrounding metal and correct the actual detuning by applying an appropriate control voltage on 2 analog outputs.

To correct a potential detuning of the connected antenna, a phase measurement needs to be performed. The following sequence is required to read out the phase information:

Step 1: Disable DPC

Step 2: Perform Type A-106 load protocol

Step 3: Set the VDDPA Voltage as $V\_(Vddpa\_AAT)$

Step 4: Perform RF ON

Step 5: Read out RXM phase

Step 6: Perform RF OFF

Step 7: Enable DPC

For reading the RXM phase, refer to the related application note. Based on the phase information, a host is able to calculate the DAC output voltages to correct a detuning.

The antenna tuning requires the DPC to be disabled, and is typically not suitable for dynamic tuning e.g. during card communication.

Note:

Since disabling of the DPC requires a modification of the EEPROM is required, care must be taken not to exceed the maximum permitted number of Erase/Write cycles.

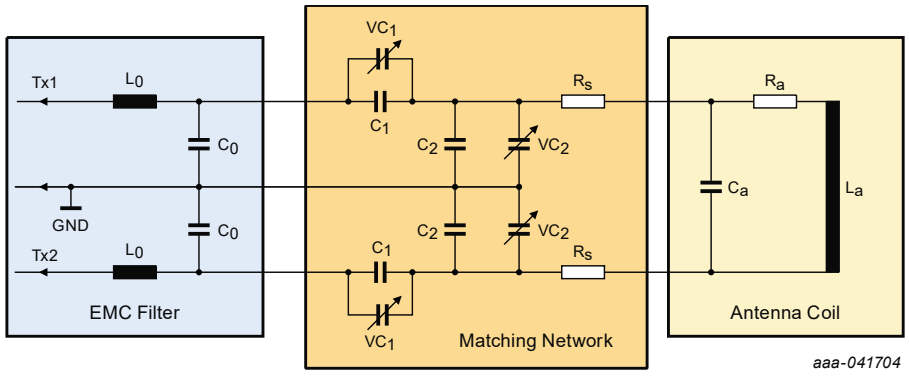


Figure 14. Antenna connection using variable capacitors

9.4.11 RF debug signals

The following signals are available for debugging purposes:

The test signals are selected by sending a command string to the PN7642. The commands CONFIGURE_TESTBUS_DIGITAL and CONFIGURE_TESTBUS_ANALOG are used to configure the dedicated signal on an output pin.

If used, **ADC-Q needs to be routed always to AUX1, ADC-I needs to be routed always to AUX2**.

The analog test signals are analog representation of an internal digital value. The internal digital signal is converted by an 8-bit wide DAC to the analog signal.

This overview indicates the signals which are available for debugging purposes (indicated by numbers):

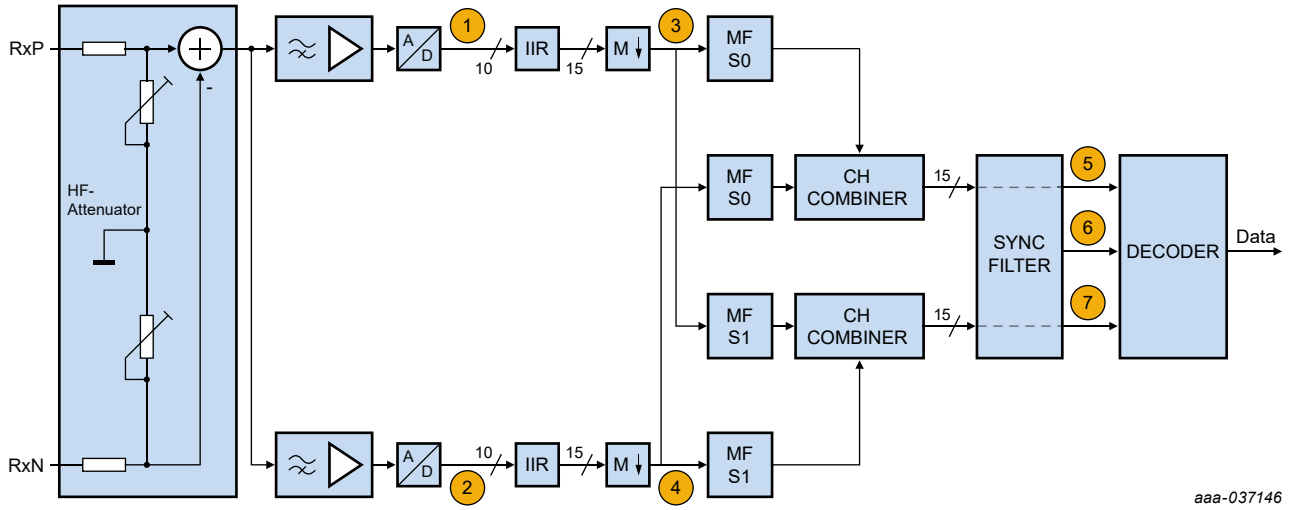


Figure 15. Receiver block diagram

Table 15. DEBUG SIGNALS

Signal	REGISTER	SIGNAL NAME	BITS	Description
ADC Data I Channel (1)	obs_clif_ tbcontrol_ patchbox0	adc_ data_i_i	9:2	Unfiltered I channel signal upper 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9)

Table 15. DEBUG SIGNALS *...continued*

Signal	REGISTER	SIGNAL NAME	BITS	Description
	obs_clif_tbcontrol_patchbox1		9; 6:0	Unfiltered I channel signal lower 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9)
ADC Data Q Channel (2)	obs_clif_tbcontrol_patchbox2	adc_data_q_i	9:2	Unfiltered Q channel signal upper 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9)
	obs_clif_tbcontrol_patchbox3		9; 6:0	Unfiltered Q channel signal lower 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9)
Preprocessor Out I Channel (3)	obs_clif_sigpro_rm0	rm_cor_adc_i_o	14:8	Pre-processed ADC data I channel upper 7bit of 15bit signed pre-processed ADC data I channel, after IIR filter and down-sampling including sign (bit14) bit 15: RFU
	obs_clif_sigpro_rm1		7:0	Pre-processed ADC data I channel lower 8bit of 15bit signed pre-processed ADC data I channel, after IIR filter and down-sampling
Preprocessor Out Q Channel (4)	obs_clif_sigpro_rm2	rm_cor_adc_q_o	14:8	Pre-processed ADC data I channel upper 7bit of 15bit signed pre-processed ADC data Q channel, after IIR filter and down-sampling including sign (bit14) bit 15: RFU
	obs_clif_sigpro_rm3		7:0	Pre-processed ADC data I channel lower 8bit of 15bit signed pre-processed ADC data Q channel, after IIR filter and down-sampling
Output MF S0 (5)	obs_clif_sigpro_rm4	mf_pt_s0_d	14:8	Delayed matched filter S0 output, after CH combiner upper 7 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore)
	obs_clif_sigpro_rm5		7:0	Delayed matched filter S0 output, after CH combiner lower 8 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner
Output MF S1 (6)	obs_clif_sigpro_rm6	mf_pt_s1_d	14:8	Delayed matched filter S1 output, after CH combiner upper 7 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore) Remark: S1 is not relevant for type A 106
	obs_clif_sigpro_rm7		7:0	Delayed matched filter S1 output, after CH combiner lower 8 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner Remark: S1 is not relevant for type A 106
Output Synchronization Filter (7)	obs_clif_sigpro_rm8	sync_filt_out	14:8	Synchronization filter output upper 7 bit of the 15 bit signed synchronization filter output including sign (bit14) bit 15: RFU (ignore)
	obs_clif_sigpro_rm9		7:0	Synchronization filter output lower 8 bit of the 15 bit signed synchronization filter output
clif_status	transceive_state		7:5	

Table 15. DEBUG SIGNALS *...continued*

Signal	REGISTER	SIGNAL NAME	BITS	Description
	rx_cl_error		4	
	tx_envelope		3	
	rx_enevelope		2	
	svalid		1	
	sdata		0	
clif_transceive	rx_start_receive		7	
	rx_over_ok		6	
	rx_over_term		5	
	rx_resume		4	
	sgp_msg_busy		3	
	fig_reset_sigpro		2	
	fig_reset_rxdec		1	
	cfg_sw_reset_ sigpro		0	

Table 16. TRIGGER SIGNALS

TRIGGER	REGISTER	SIGNAL NAME	BITS	Description
TX Active	obs_clif_txenc1	tx_active_o	1	high level indicates transmission of data Remark: Falling edge can be used to trigger on end of transmission.
RX Enable	obs_clif_sigpro_ rm15	rx_enable_o	1	high level indicates that the reception is ongoing Remark: can be used to trigger on the start /end of reception
RX collision detected	obs_clif_sigpro_ rm14	rm_scoll_o	1	high-level pulse indicates that the collision is detected during reception

9.5 Power, Clock and Reset Management

9.5.1 General

In PN7642 the Power, Clock and Reset Management (PCRM) Unit is a collection of sub systems whose key functions are:

- Controlling the PN7642 system’s hardware boot sequence
- Managing the power modes the system can operate in, inclusively power domain enabling/disabling and isolation control
- Managing wake-up event capturing and the transitions between the power modes (i.e. make sure that blocks are enabled/disabled according to their power profiles in the currently active power mode)
- Monitoring environmental conditions (supply state, battery power state, temperature, IO pad state, etc.)
- Digital clock management, clock distribution and architectural clock gating
- Digital reset management and reset distribution
- General-purpose AD converter with 10 logical channels and various data post processing options (filtering, min, max, moving average, etc.)

- IO pad control
- Interrupt controller
- 2 Antenna tuning control (Antenna Tuning DACs)
- Low-power and ultra low-power field/card detection controller

9.5.2 Interrupt controller

The power, clock and reset (PCRM) unit of PN7642 implements various interrupt sources which are collected to a single interrupt line, connected to the Cortex M33's Nested Vectored Interrupt Controller (NVIC). The PCRM interrupt controller manages these triggers, allows for masking them, resp. for configuration whether an interrupt request should be generated based on an interrupt source's rising or falling edge or whether a request shall be generated on both edges.

The following figure shows a high-level view of the interrupt controller and its connectivity to the PCRM configuration registers:

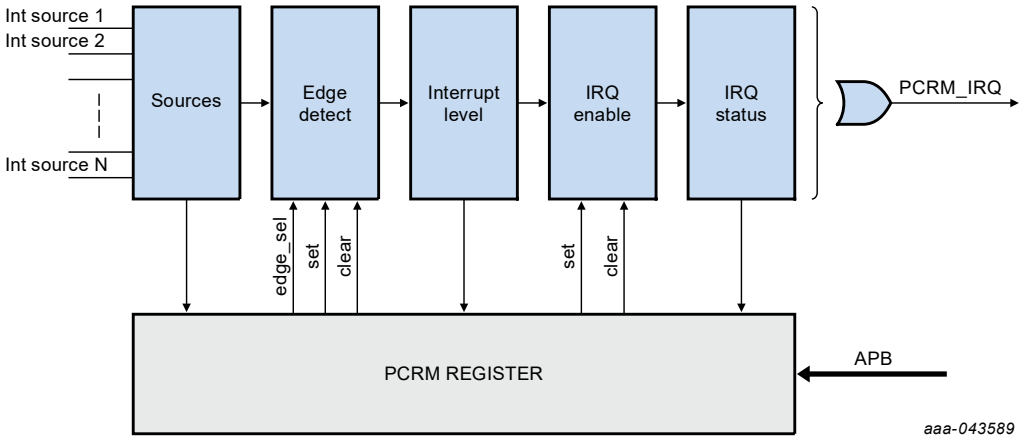


Figure 16. PCRM Interrupt controller

The following table shows a consolidated list of PCRM interrupt events, and their configuration options:

Table 17. PCRM Interrupt Sources

Source / Event	Possible Event Type
GPIO 0 Activity	Rising / Falling / Both
GPIO 2 Activity	Rising / Falling / Both
GPIO 3 Activity	Rising / Falling / Both
GPIO X Common Activity	Rising / Falling / Both
VDDIO OK	Rising / Falling
XTAL Ready	Rising
XTAL Error	Rising
GPADC Channel 0	Rising
GPADC Channel 1	Rising
GPADC Channel 2	Rising
GPADC Channel 3	Rising
GPADC Channel 4	Rising
GPADC Channel 5	Rising

Table 17. PCRM Interrupt Sources*...continued*

Source / Event	Possible Event Type
GPADC Channel 6	Rising
GPADC Channel 7	Rising
NFC Temperature warning	Rising / Falling
PMU Temperature warning	Rising
PMU ADPLL Locked	Rising / Falling
Field Clock OK	Rising / Falling / Both
VUP OK	Rising / Falling
VDDPA over current	Rising
RX Protection Alarm	Rising

9.5.3 Brownout detection

The PN7642 includes a brownout detector to monitor the voltage of VBAT. If the voltage falls below the specified threshold, the BOD generates a shutdown request to the system.

In order to avoid any ringing of the generated status output, the voltage is expected to be in good condition for a certain time interval during the checking window, otherwise it is considered to be a false signal and will be ignored.

9.5.4 VEN monitor

The VEN monitor is implemented as a small Finite State Machine (FSM), and is in charge of

- monitoring the VEN pad status
- monitoring whether the external PADIO voltage was lost
- generating a request to either HARD POWER DOWN or PMU OFF mode.

The FSM is clocked by the LFO and similar to the Brownout detector, it introduces some filtering when sampling the VEN pad. Furthermore, the VEN low pulse width is used to distinguish between a standard system reset and a request to go to either HARD POWER DOWN or PMU OFF mode.

9.5.5 VDDIO monitor

The VDDIO is supplying the NFC pads. The Analog Power Management Unit (PMU_ANA) has a monitor which outputs VDDIO_OK to the PCRM. The PCRM requires to monitor VDDIO_OK continuously in order to initiate power down to HPD or OFF mode. Or initiate a wake-up from HPD mode depending on the value of VEN internal.

The VDDIO loss detection can be also a condition to exit OFF-mode. The behavior is configurable through the PMU_ANA which is supplied even in OFF-mode.

9.6 Peripherals

9.6.1 Communication peripherals

The PN7642 embeds the following interfaces for host connection:

- USB
- SPI target

- I^2C target
- I^3C target
- UART
- SPI controller
- I^2C controller

The host interfaces share the same pins and cannot be used at the same time. The type of host interface is selected by configuring the PCRM registers.

Table 18. Pin description for host interface

Pin name	SPI	I^2C	USB
ATX_A	SPI MISO	I^2C SDA	-
ATX_B	SPI SCK	I^2C SCL	-
ATX_C	SPI NSS	I^2C Adr Bit 0	USB D+
ATX_D	SPI MOSI	I^2C Adr Bit 1	USB D-

Note: The host interface pins should not be kept floating.

The host interfaced to be used on the product must be selected by the pins HOST_IF_SEL0 and HOST_IF_SEL1 according to the following table.

Table 19. Selection of the host interface

HOST_IF_SEL1	HOST_IF_SEL0	Resulting interface
LOW	LOW	I^2C target
LOW	HIGH	SPI target
HIGH	LOW	UART
HIGH	HIGH	I^3C target

9.6.1.1 SPI target interface

The maximum SPI speed is 15 Mbit/s and fixed to CPOL = 0 and CPHA = 0. Only a half-duplex data transfer is supported. There is no chaining allowed, meaning that the whole instruction has to be sent or the whole receive buffer has to be read out. The whole transmit buffer shall be written at once as well. No NSS assertion is allowed during data transfer.

The SPI host interface is designed to support the typical interface supply voltages of 1.8 V and 3.3 V of CPUs. A dedicated supply input which defines the host interface supply voltage independent from other supplies is available (pin VDDIO).

There is no external pull-up / pull-down resistor required, the SPI pads are automatically configured by the PN7642.

Only a voltage of 1.8 V or 3.3 V is supported, but no voltage in the range of 1.95 V to 2.4 V.

Note: The Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT.

Controller in target out (MISO)

The MISO line is configured as an output in a target device. It is used to transfer data from the target to the controller, with the most significant bit sent first. The MISO signal is put into 3-state mode when NSS is high.

Controller out target in (MOSI)

The MOSI line is configured as an input in a target device. It is used to transfer data from the controller to a target, with the most significant bit sent first.

Serial clock (SCK)

The serial clock is used to synchronize data movement both in and out of the device through its MOSI and MISO lines.

Not target select (NSS)

The target select input (NSS) line is used to select a target device. It shall be set to low before any data transaction starts and must stay low during the transaction.

9.6.1.2 I^2C target interface

The I^2C interface is compliant with the I^2C Bus Specification 3.0.

Key features of the I^2C target interface are:

- 8-bit I^2C target address, where 2 LSBs can be configured.
- Supported transfer modes

Table 20. I^2C modes and maximum bit rates

Mode	Max Bitrate
Standard-mode (Sm)	100 Kbit/s
Fast-mode (Fm)	400 Kbit/s
Fast-mode Plus (Fm+)	1 Mbit/s
High-speed mode (Hs-mode)	3.4 Mbit/s

- Half duplex mode
- I^2C target mode
- Selection of the I^2C address done by two pins. I^2C_ADR1 and I^2C_ADR0.
  - It supports multiple addresses
  - The upper bits of the I^2C target address are hard-coded. The value corresponds to the NXP identifier for I^2C blocks. The value is 01010XXb

Table 21. I²C interface addressing

I^2C_ADR1	I^2C_ADR0	I^2C address (R/W = 0, write)	I^2C address (R/W = 0, read)
0	0	0x28	0x28
0	1	0x29	0x29
1	0	0x2A	0x2A
1	1	0x2B	0x2B

9.6.1.3 I^3C target interface

The I^3C target interface is compliant to the MIPI I^3C standard. It implements major improvements in terms of usage and power consumption and therefore can be used as an alternative to SPI communication for mid-level communication speeds.

Key features of the I^3C target interface are:

- 2 wire multi-drop bus capable of 12 MHz clock speeds with up to 11 devices

- Target addresses are dynamically assigned, but may have a static address at start
- In-Band interrupts, allowing targets to notify the controller without requiring a separate GPIO
- Interrupts can be started even when controller is not active on the bus, and yet no free running clock is needed
- Built-in commands in separate "space" do not collide with normal controller to target messages
- Hot-join onto bus allows devices to get online later than the initial bus bring up. Hot-join is supported to request for a new dynamic address after wake-up
- High data rate DDR option (HDR-DDR) provides about twice the data rate of SDR (about 20 Mbit/s)

9.6.1.4 UART interface

The PN7642 integrates a Low-Power Universal Asynchronous Receiver / Transmitter (LPUART) module.

The LPUART shares the pins with the I2C, I3C, SPI, and USB interfaces. The LPUART operation need to be selected by configuring the pins HOST_IF_SEL0 and HOST_IF_SEL1 accordingly.

The following features are supported:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4x to 32x
- Transmit and receive baud rate can operate asynchronous to the bus clock:
  - Baud rate can be configured independently of the bus clock frequency
  - Supports operation in Stop modes
- Hardware parity generation and checking
- Programmable 7-bit, 8-bit, 9-bit, or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wake-up methods:
  - Idle line wake-up
  - Address mark wake-up
  - Receiver data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width
- Independent FIFO structure for transmit and receive
  - Separate configurable watermark for receive and transmit requests
  - Option for receiver to assert request after a configurable number of idle characters if receive FIFO is not empty

9.6.1.5 USB device interface

PN7642 incorporates a USB 2.0 Full-Speed device, compliant with USB 3.0 Hub connectivity capability.

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, and endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer.

The status of a completed USB transfer or error condition is indicated via status registers. If enabled, an interrupt is generated.

Features:

- Fully compliant with USB 2.0 specification (full speed)
- Dedicated USB PLL available
- Supports 12 physical endpoints including one control endpoint (3 Irq-In, 3 Irq-Out, 3 Bulk-In and 3 Bulk-Out). The first generic endpoint starts at logical endpoint number 1.
- Supports 6 logical endpoints
- Single or double buffering allowed
- Resume By Host
- Wake-up from suspend mode on USB activity and remote wake-up
- Suspend and Resume for power management
- SoftConnect Supported

9.6.1.5.1 Connecting the USB interface

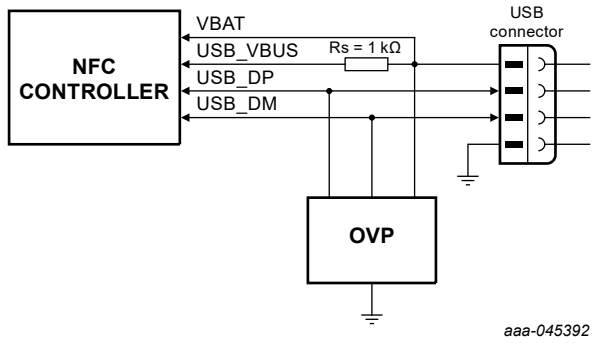


Figure 17. USB interface on a bus-powered device

The resistor R_s is used to minimize the impact of transient responses on the USB line. The resistance must be greater or equal to 1 kΩ to avoid damage to the device. When the USB interface is not used, the USB_VBUS pin shall be connected to the ground.

9.6.1.6 SPI controller interface

The device implements an SPI controller interface to connect to any external SPI devices.

The SPI controller interface implements separate receive and transmit FIFOs for data buffering and also implements separate DMA control for reception and transmission.

The SPI controller interface supports data frames of 1 to 16 bits. The transmit and receive FIFOs have a capacity of 8 entries each, whereas an entry represents 16 bits.

Up to four target select inputs/outputs are available. Clock phase/polarity and frame/transfer delays of the SPI protocol are all programmable through registers.

Features:

- Motorola SPI-compatible interface
- Data frames of 8 bits
- DMA support for both transmit and receive (full duplex)
- Option to "write without read" and "simultaneous control with data"
- Multiple target select pins

- Programmable delays (Pre delay, Post delay, Frame delay, Transfer delay)
- FIFOs have 8 entries with 16 bits each
- Data rate is firmware configurable.
- Max baud rate is ~22.5 MHz, considering clock of 45 MHz.
- Configurable Clock polarity and phase (SPO/SPH)
- Supports MSB/LSB first switch
- Supports generation of EOT, EOF

The SPI subsystem can be configured to drive up to four targets. Different protocol parameters (e.g. frame, transfer delays) are programmable. Data transmission and reception from/to the system memory is done via FIFOs in order to bridge any wait cycles in case of an access conflict to the system RAM.

Interrupt requests to the CPU occur on receiver data availability or on transmitter readiness to accept data. Also, the FIFOs can be programmed with a certain trigger level so that interrupts occur before the FIFOs run empty or reach a critical filling level.

DMA requests to the DMA controller occur as soon as space is available in TX FIFO or as soon as data becomes available in RX FIFO.

9.6.1.7 I^2C controller interface

The device implements an I^2C controller interface in order to connect any external I^2C target device.

The I^2C controller interface allows for operation in controller mode, target mode and also supports monitor mode. It is able to handle the following communication modes:

- Standard Mode (up to 100 kbit/s)
- Fast Mode (up to 400 kbits/s)
- Fast Mode (up to 1 Mbit/s)
- Fast Mode Plus (up to 3.4 Mbit/s)

Features:

- Independent controller, target and monitor functions
- Supports both
  multi controller
  multi controller with target
- Multiple I^2C target addresses supported in hardware
- One target address can be selectively qualified with an address range in order to allow versatile responses to multiple I^2C target addresses
- 10-bit addressing supported with software assistance
- Support for control and data transfer via DMA in all three modes (controller, target, monitor)
  – AMBA 3.0 compliant APB interface
- Automatic target acknowledgment or non-acknowledgement in conjunction with DMA
- The I^2C target function needs no on-chip clock to receive and compare an address and can thus wake up the host CPU from power down. The monitor function can also wake up the host.
- Supports System Management Bus (SMBus)
- Extra GPIO available to indicate data available to the I^2C controller
- Supports Device ID command
  (with firmware assistance. Payload prepared by firmware to map to this command)
- Supports Generic Call Address command
  (with firmware assistance. Payload prepared by firmware to map this command)
- Supports Soft Reset command
  (with firmware assistance. Payload prepared by firmware to map to this command)

The I2C controller interface can be configured as Controller or Target. The default application mode is controller.

9.6.2 Digital peripherals

9.6.2.1 General-purpose I/O

The PN7642 provides 6 GPIO pins.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow for setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin.

9.6.2.1.1 Features

- Bit-level set, clear, and toggle registers allow a single instruction set, clear or toggle of any number of bits in one port.
- Direction control of individual bits.
- All GPIO pins can be selected to create an edge or level-sensitive GPIO interrupt request.
- All GPIO pins can be used to wake up the device from different power-saving modes.

9.7 System power states

The PN7642 can operate in different power states. The functionality and current consumption is dependent on the actual system power state.

Power states can be changed by the level on the pin RESET_N and by connecting/disconnecting the power supply of VBAT.

In addition, state changes are triggered from the user application of the device.

Disconnecting and connecting the power supply on VBAT restarts the PN7642 always in Active State after releasing the pin RESET_N (transition low to high).

A transition of low to high on pin RESET_N restarts the PN7642 always in Active State.

The following power states are supported:

Power state	Description
Power OFF state	The PN7642 device (supply pin VBAT, RF transmitter) is not supplied by a battery/system PMU. Other domains might be supplied (for example, I/O pad interface on pin VDDIO)
PMU OFF state	The PN7642 device is disabled via a low signal on pin RESET_N. No internal clocks of the PN7642 are active. Wake-up events to change PMU OFF state: Power reset on pin VBAT, VEN rising edge, RX ULPCD detect, ULP abort signal on PIN3
ULPCD state	The ULPCD (ultra low-power card detection) offers highest current saving. In this mode, the only wake-up sources to escape from the card detection loop are either a detected antenna detuning or a reset (RESET_N) of the PN7642. Only the wake-up timer is active during ULP Standby state. The ULPCD comprises 2 phases: 1. Calibration phase: In this phase, an RF field is established and the field strength(RSSI) for the unloaded state of the antenna is measured to be used during the measurement phase and stored in a low-power persistent register. 2. Measurement phase: In the measurement phase, the card detection activity is performed autonomously by the hardware at configurable time intervals. This configuration is passed

Power state	Description
	as a parameter to the SWITCH_MODE_LPCD command. The RSSI value is measured and compared against the reference value measured in the calibration phase. A card is detected to be in the proximity of the reader when the measured RSSI differs from the reference RSSI by more than a configurable threshold. The user application can set the PN7642 into Ultra-low power card detection state (ULP Standby state) via programming of the ULPCD bit. XTAL_CHECK_DELAY allows to optimize the startup of the crystal for the LPCD and ULPCD modes. The following EEPROM configuration is available: ULPCD_VOLTAGE_CTRL ULPCD_RSSI_GUARD_TIME ULPCD_RSSI_SAMPLE_CFG ULPCD_THRESH_LVL ULPCD_GPIO3
Hard power down state	The PN7642 is disabled via the reset/enable signal on VEN or by detecting an external condition (for example, battery voltage monitor). The power dissipation is reduced to a minimum. No power dissipation or leakage is expected on the different interfaces. Low-power resources are enabled (VDDC_LP, VHV_LP, LQ_REF, LQ-BIAS). LFO clock is available. PCRM is supplied and is running in low-power state. I/Os are supplied by VDDC_HP. Wake-up events: Power reset on pin VBAT, VEN rising edge, RX ULP detect
Standby state	The user application can set the PN7642 into a low-power mode to minimize power dissipation. The state of external interfaces is maintained properly. PMU operates in low-power state. Wake-up counter clock is available. PCRM is supplied and running in low-power mode. I/Os are supplied by VDDC_LP. PMU FSM in PCRM manages the transition in power state. Wake-up sources: Activity on host IF, SWPM communication, ULPDET, LPDET, wake-up counter, power loss on VDDIO, GPIO, RxPROT, No High Temp on TX and so on.
Suspend state	Suspend state is associated to the operation of the USB interface but can also be applied for other purposes. During Suspend state, the NFC digital subsystem including NV memory is kept powered. System RAM state is maintained. ROM is put to ShutDown mode. The I/O state is maintained. USB main clock supply is gated off under control of usb_need_clk. The HFO is switched off. The LFO is active. Wake-up sources: USB, host IF, wake-up counter, ULPDET, LPDET, Temp sensor, GPIO, VUP detected, power loss on VDDIO, interrupt from ISO AUX IF, RxPROT
Active state	The PN7642 is able to process internal or external events or data. All external power supply sources and the external clock need to be available, and all internal clocks are active.

9.8 Power supply

The device allows to configure different power supply options for the transmitter power amplifier. To make use of them, a combination of external connections and chip internal configurations needs to be done. The following supply options are available:

- Internal VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX_LDO). In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX_LDO is adding an improved rejection of noise on the supply lines.
- Direct VDDPA configuration: This configuration is recommended for applications which require highest efficiency, like battery supplied devices. In this configuration, a battery can be connected directly to the transmitter supply avoiding the voltage drop of approximately 0.3 V caused by the TX_LDO. A clean supply voltage without noise is required to achieve a good RF performance.
  In this configuration the DPC, current measurement and overcurrent protection is not available.

9.8.1 System power supply overview

The PN7642 is using three different supplies each for the following functional blocks:

1. Supply for the host interface and GPIO's (VDDIO)
2. Supply for the analog and digital blocks (VBAT/VBAT_PWR)
3. Supply of the RF drivers (VDDPA), DC-DC (VBAT_PWR) and TX_LDO (VUP)

The functionality of the GPIO's, Host Interface and internal analog and digital blocks is independent from the supply of the RF Driver. This allows to configure a dedicated transmitter supply configuration at any time. Care shall be taken to switch on the RF field only after the transmitter-related power supply had been configured according to the external physical supply connections (VDDPA, VBAT_PWR, VUP).

The power supply configuration is configured in EEPROM and therefore will not get lost in case of power supply loss or reset of the chip. Typically, this configuration is only performed once during the production of a reader.

RF field shall not be turned on without setting the correct power supply configuration in the EEPROM.

Note: The Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT. This limitation is not applicable in Power off mode.

9.8.2 Connecting blocking capacitors

Some pins are connected to blocking supply capacitors. PCB traces to these capacitors need to be as short as possible, and a low-ohmic grounding of the GND-side of the capacitors is required for optimized RF performance.

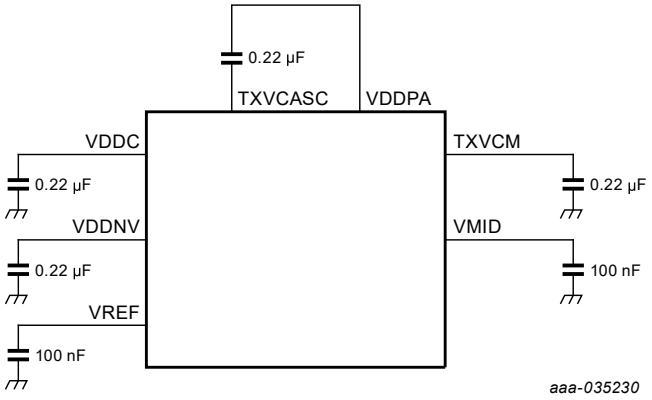


Figure 18. Blocking capacitors

9.8.3 Transmitter power supply

The PN7642 is configured by EEPROM for the different power supply options.

The following EEPROM Addresses are used to configure the power supply of the transmitter:

DCDC_PWR_CONFIG - Enables/disables and configures the DC-DC according to the external supply connections.

TX_LDO_CONFIG - Enables/disables and configures the TX_LDO.

TX_LDO_VDDPA_HIGH - initial out voltage when DPC is used.

TX_LDO_VDDPA_LOW - lowest VDDPA when DPC is used.

TX_LDO_VDDPA_MAX_RDR - maximum voltage to be set in reader mode used by DPC.

TX_LDO_VDDPA_MAX_CARD - VDDPA maximum voltage to be set in card mode used by DPC.

No specific registers are required to configure the pad supply (VDDIO) or the supply for the analog and digital blocks (VUP).

9.8.3.1 TX_LDO transmitter supply

TX_LDO supplied VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX_LDO).

In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX_LDO is adding an improved rejection of noise on the supply lines.

A decoupling cap is required on VDDPA pin.

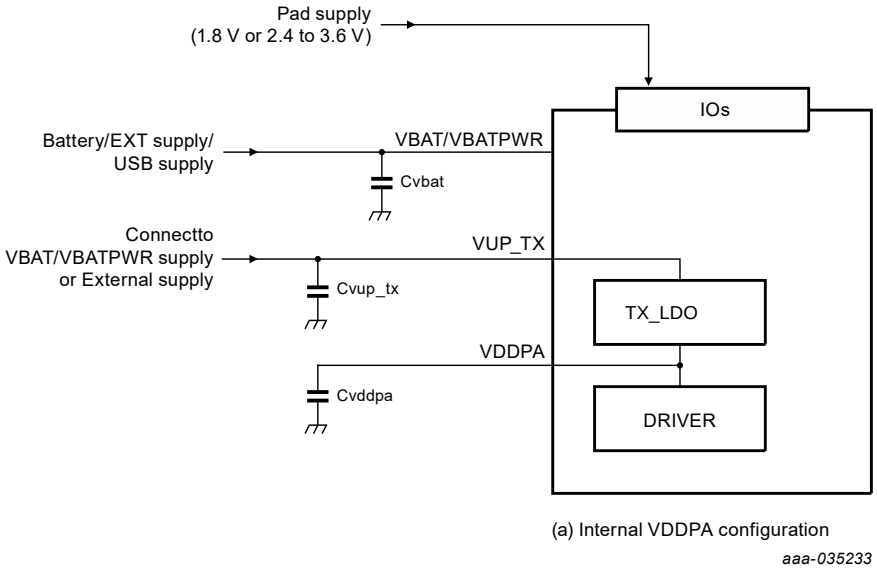


Figure 19. Transmitter supply

9.8.3.2 Direct transmitter supply

Direct VDDPA configuration:

TX_LDO must be configured OFF by SW configuration. VUP_TX and VDDPA connected to VBAT/VBATPWR.

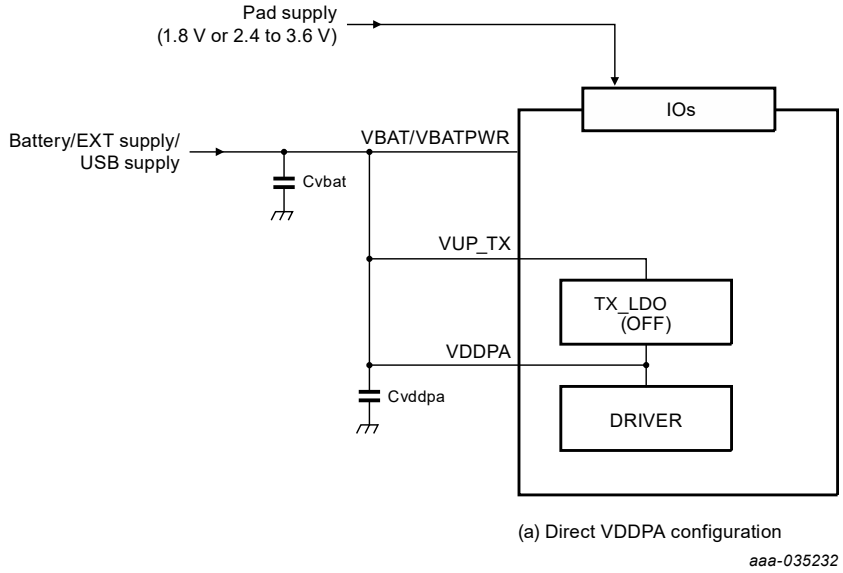


Figure 20. Direct transmitter supply

9.8.3.3 DC-DC (boost) supply

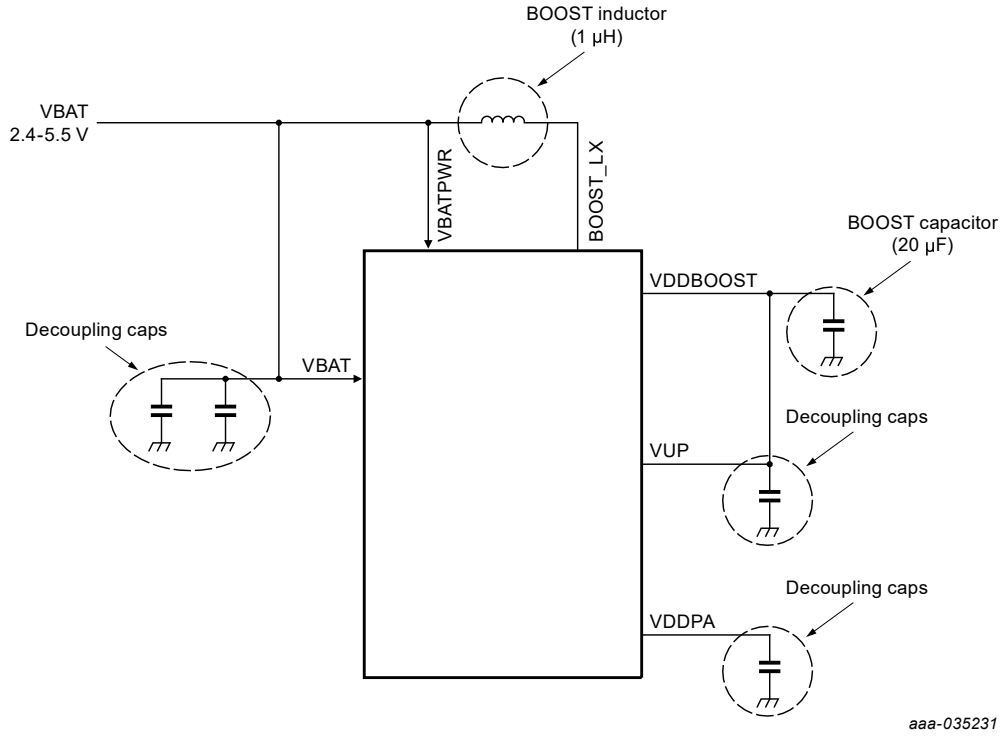


Figure 21. Transmitter supply by DC-DC

9.8.3.4 Configuration example 1: TX_LDO transmitter supply - DC-DC active

VBAT is connected to VBATPWR.

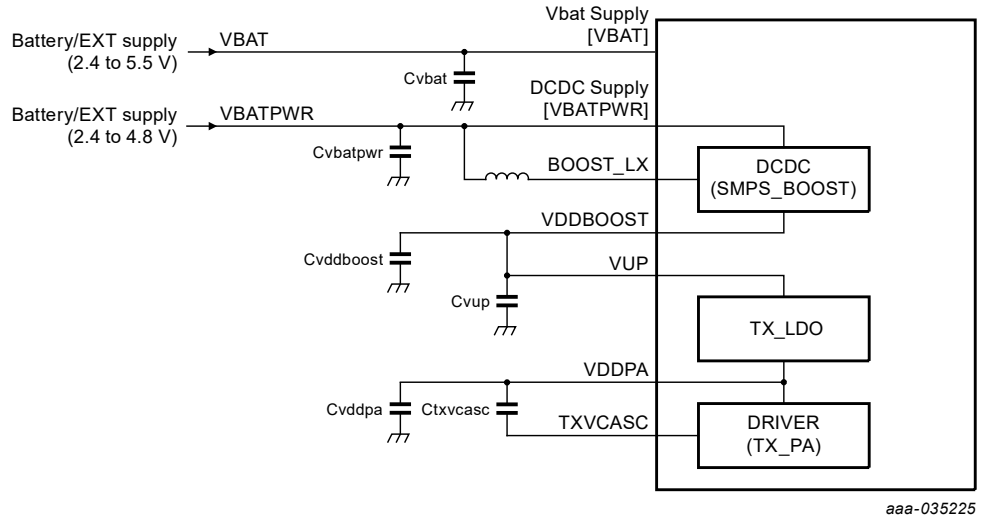


Figure 22. DC-DC active

9.8.3.5 Configuration example 2: TX_LDO transmitter supply - DC-DC bypassed

VBAT is connected to VBATPWR.

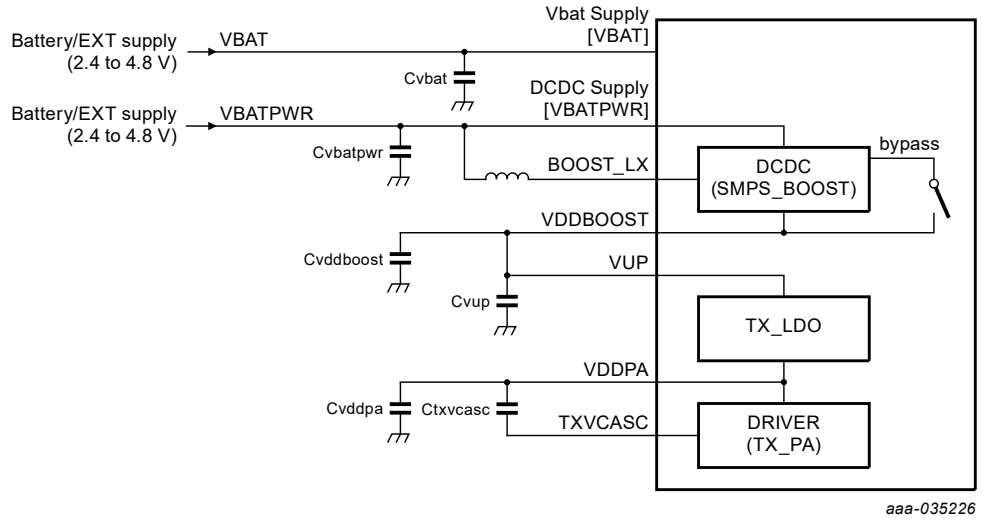


Figure 23. DC-DC bypassed (in DCDC_PWR_CONFIG)

9.8.3.6 Configuration example 3: TX_LDO transmitter supply connected to VBAT - no DC-DC

VBAT is connected to VBATPWR.

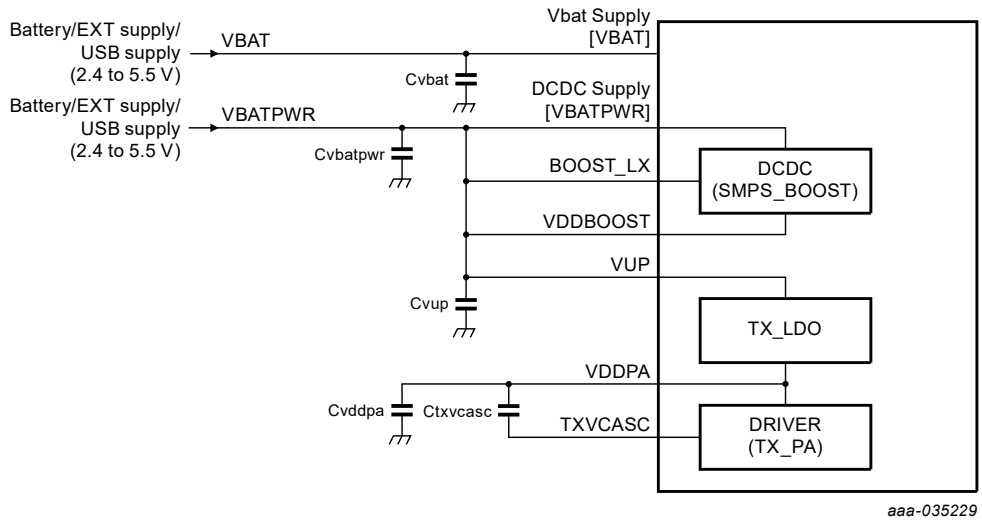


Figure 24. No DC-DC used

9.8.3.7 Configuration example 4: TX_LDO supplied independent from VBAT - no DC-DC

VBAT is connected to VBATPWR.

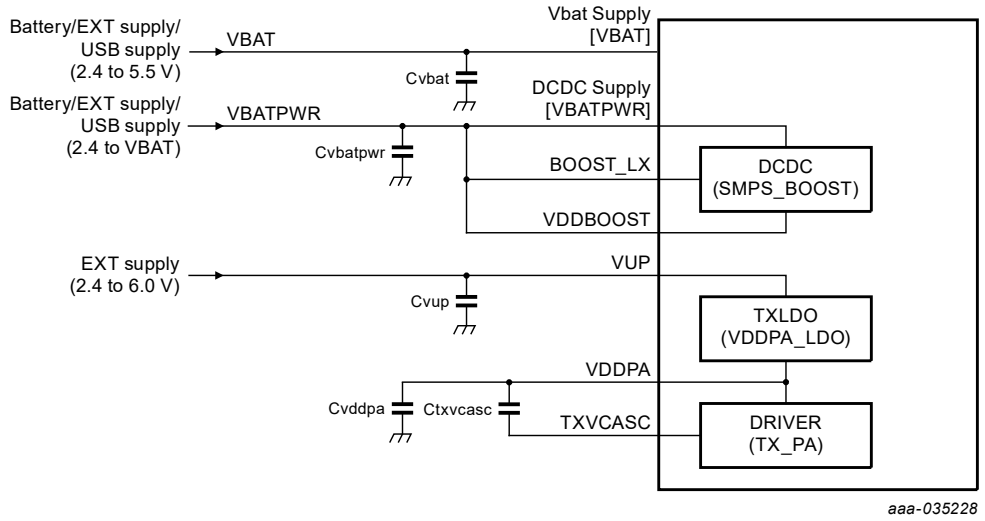


Figure 25. No DC-DC used

9.8.3.8 Configuration example 5: TX_LDO not used - no DC-DC

VBAT is connected to VBATPWR.

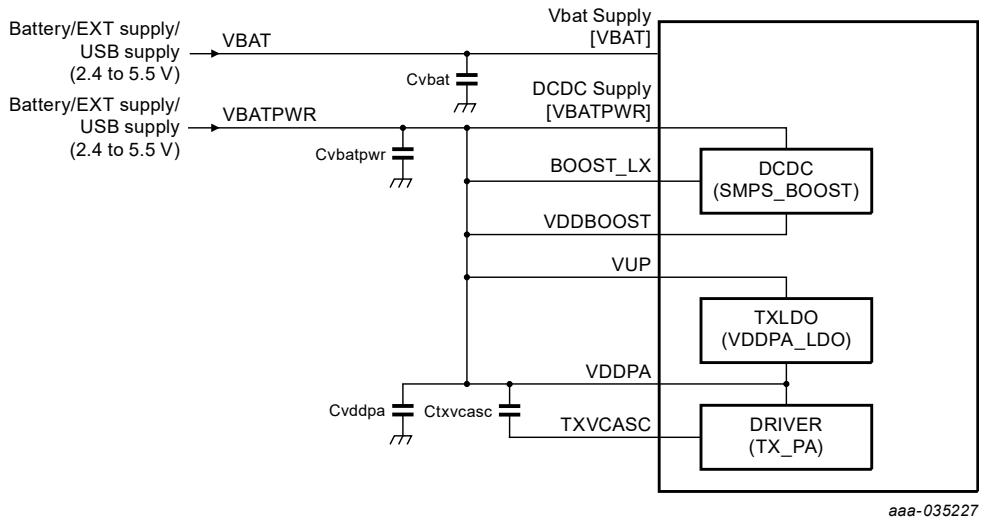


Figure 26. No DC-DC used - no TX_LDO

9.8.3.9 Supply voltage range for transmitter supply configuration examples

Table 22. Supply voltage range configuration

Supply	Config1: TX_LDO transmitter supply DC-DC active	Config2: TX_LDO transmitter supply DC-DC bypassed	Config3: TX_LDO transmitter supply connected to VBAT no DC-DC	Config4: TX_LDO supplied independent from VBAT no DC-DC	Config5: TX_LDO not used no DC-DC
EEPROM configuration for DPC ENABLED - configured in DPC_CONFIG (EEPROM)					
DCDC_PWR_CONFIG (EEPROM)	- 0xE4(Variable BOOST with Auto Bypass). - 0xE2(Fixed BOOST)	0xE4 (Variable BOOST with Auto Bypass)	0x21	0x21	NA
TXLDO_VDDPA_HIGH (EEPROM)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	NA
TXLDO_VDDPA_MAX_RDR (EEPROM)	0x2A (5.7 V)	0x1C (4.3 V)	0x25 (5.2 V)	0x2A (5.7 V)	NA
BOOST_DEFAULT_VOLTAGE (EEPROM)	0x1D (6 V).	NA	NA	NA	NA
EEPROM configuration - DPC DISABLED - configured in DPC_CONFIG (EEPROM)					
DCDC_PWR_CONFIG (EEPROM)	- 0xE4(Variable BOOST with Auto Bypass). - 0xE2(Fixed BOOST)	0xE4 (Variable BOOST with Auto Bypass)	0x21	0x21	0x00
TXLDO_VDDPA_HIGH (EEPROM)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)
TXLDO_VDDPA_MAX_RDR (EEPROM)	NA	NA	NA	NA	NA
BOOST_DEFAULT_VOLTAGE (EEPROM)	0x1D (6 V).	NA	NA	NA	NA

Table 23. Supply voltage range

Supply	Config1: TX_LDO transmitter supply DC-DC active	Config2: TX_LDO transmitter supply DC-DC bypassed	Config3: TX_LDO transmitter supply connected to VBAT no DC-DC	Config4: TX_LDO supplied independent from VBAT no DC-DC	Config5: TX_LDO not used no DC-DC
VBAT	2.8 V … 4.8 V	2.8 V … 4.8 V	2.4 V … 5.5 V	2.4 V … 5.5 V	2.4 V … 5.5 V
VBATPWR	2.8 V ... 4.8 V	2.8 V … 4.8 V	2.4 V … 5.5 V	2.4 V ... 5.5 V	2.4 V … 5.5 V
VUP	3.1 V … 6.0 V	2.8 V … < VBATPWR	2.4 V ... 5.5 V	2.4 V … 6.0 V	2.4 V … 5.5 V
VDDPA	VUP-0.3V drop of TX_LDO. max 5.7 V	VBATPWR - 0.5 V voltage drop	VUP-0.3V drop of TX_LDO	VUP-0.3V drop of TX_LDO	2.4 V … 5.5 V

9.9 Energy-saving card detection

There is no trimming for the Low Frequency Timer required.

9.9.1 Low-power card detection (LPCD)

The low-power card detection (LPCD) is an energy-saving card polling configuration for the PN7642. During LPCD, a host microcontroller can be set into power-saving mode, as no host controller interaction is required. The host microcontroller is woken up from power-saving mode by an IRQ send by the PN7642.

The LPCD mode offers highest sensitivity at the cost of slightly higher current consumption compared to the ULPCD mode.

A low frequency oscillator (there is no trimming for the low frequency oscillator required) is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short RF pulse. This RF pulse allows to detect a detuning of the antenna by presence of conductive objects in proximity of the antenna (card, cell phone, metal).

In case of a detected antenna detuning, the system wakes up from power-saving mode. It sends an interrupt signal to the connected host microcontroller to wake up the host microcontroller from power-saving mode and to indicate a change of the antenna detuning condition.

A low frequency oscillator (LFO) is implemented to drive a wake-up counter, waking-up PN7642 from Standby mode. This allows implementation of low-power card detection polling loop at application level.

The host microcontroller can then perform a card polling sequence to verify if the technology of the object causing the antenna detuning is supported by the system.

The SWITCH_MODE instruction allows entering the LPCD mode with a given standby duration value.

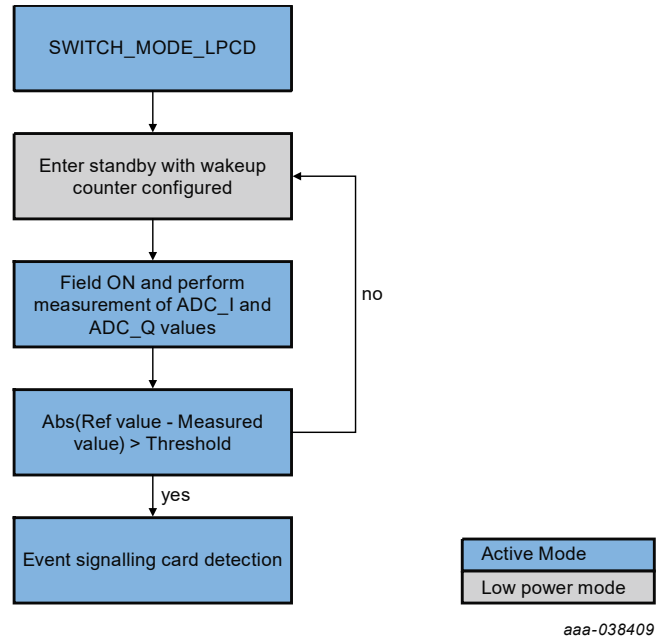


Figure 27. LPCD configuration

The LPCD mode is entered by the instruction SWITCH_MODE_LPCD, and terminated by toggling a GPIO, by a reset (VEN) of the PN7642 or a signal of the RF Level detector.

Before entering the LPCD mode, ADC_I and ADC_Q reference value needs to be determined. This is done during the so-called calibration.

LPCD calibration phase

a) An initial calibration measurement is performed to set up the RX chain parameters namely HFATT, DCO_DAC_I_CTRL and DCO_DAC_Q_CTRL values.

b) The next measurement is done using the RX chain parameters that are set up, to arrive at the ADC_I and ADC_Q values which are used as reference values. All following LPCD measurements are done relative to the LPCD calibration measurement.

The LPCD loop itself works in two phases:

First the standby phase is controlled by the wake-up counter (timing defined in the instruction), which defines the duration of the standby of the PN7642.

Second phase is the detection-phase. The RF field is switched on for a defined time (EEPROM configuration) and then the ADC_I and ADC_Q values are compared to a reference value.

- If the ADC_I and ADC_Q values exceed the reference value, a LPCD_IRQ is raised to the host. The register configurations done by the host to support a dedicated RF protocol are not restored after wake-up command. The host has to configure the NFC frontend for a dedicated protocol operation to allow a polling for a card.
- If the ADC_I and ADC_Q values do not exceed the thresholds of the reference value, no LPC_IRQ is raised and the IC is set to the first phase (Standby mode) again.

These two phases are executed in a loop until:

- Card / metal is detected (LPCD_IRQ is raised).

- Reset occurs, which resets all the system configurations. The LPCD is also terminated in this case.

- NTS on host interface
- RF Level Detected
- GPIO toggle

The behavior of the generated field is different dependent on the activation state of the DPC function:

- If the DPC feature is not active, the ISO/IEC14443 type A 106 kbit/s settings are used during the sensing time.
- If the DPC is active, the RF_ON command is executed. The RF field is switched on as soon as the timer configured by the SWITCH_MODE command elapses. The RF field is switched on for a duration as defined for an activated DPC. The timer for the LPCD_FIELD_ON_TIME starts to count as soon as the RF_ON command terminates.

Table 24. Low-Power Card Detection: relevant EEPROM configuration

Name	Description
LPCD_AVG_SAMPLES	Defines how many samples of the I and Q values are used for the averaging. Used to optimize the system to achieve highest detection sensitivity versus false alarms.
LPCD_RSSI_TARGET	Value to be used as the RSSI target in the calibration phase to arrive at the RX chain parameters. This parameter is used to arrive at an optimal target voltage level at RXP.
LPCD_RSSI_HYST	Value to be used as the RSSI hysteresis in the calibration phase to arrive at the RX chain parameters. This is used to avoid oscillations while arriving at the target voltage level at RXP.
LPCD_THRESHOLD	If the difference between the measured value of I/Q and the reference value for I/Q is greater than the threshold on either channels, then a card is detected.
LPCD_VDDPA	VDDPA voltage when DC-DC (internal or external) or external power source is used to feed TXLDO
XTAL_CHECK_DELAY	Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18,8us). For fastest start-up this time, a check is performed at a time slightly higher than the expected startup time of the crystal.

9.9.2 Semi-autonomous mode (LPCD)

LPCD semi-autonomous mode

The LPCD can be invoked by the host in the semi-autonomous mode wherein the ADC_I and ADC_Q values that are measured is returned back to the host.

In this mode, standby is not entered and the difference between the measured and reference values are not checked against the threshold. Nevertheless, the host may check the measured values against a reference and threshold to detect a card and also put the PN7642 in Standby mode between measurements, using the SWITCH_MODE_STANDBY command.

This mode is especially useful to find optimized settings for the LPCD, since it does not offer no significant current saving.

9.9.3 Ultra low-power card detection (ULPCD)

The ULPCD (ultra low-power card detection) offers highest current saving. In this mode, the only wake-up sources to escape from the card detection loop are either a detected antenna detuning, a signal on GPIO3 or a reset (RESET_N) of the PN7642.

The ULPCD cannot be used together with the DC-DC function. A connection as described in the chapter "TX_LDO transmitter supply" or "Direct transmitter supply" is recommended.

Only the wake-up timer is active during ULP standby state.

The ULPCD comprises 2 phases:

1. **Calibration phase**
   In this phase, an RF field is established and the field strength(RSSI) for the unloaded state of the antenna is measured to be used during the measurement phase and stored in a low-power persistent register.
2. **Measurement phase**
   In the measurement phase, the card detection activity is performed autonomously by the hardware at configurable time intervals. This configuration is passed as a parameter to the ULPCD system service API. The RSSI value is measured and compared against the reference value measured in the calibration phase. A card is detected to be in the proximity of the reader when the measured RSSI differs from the reference RSSI by more than a configurable threshold.

The host can set the PN7642 into ultra-low power card detection state (ULP standby state) via the ULPCD system service API.

XTAL_CHECK_DELAY allows to optimize the startup of the crystal for the LPCD and ULPCD modes.

The following EEPROM configuration is available:

- ULPCD_VOLTAGE_CTRL
- ULPCD_RSSI_GUARD_TIME
- ULPCD_RSSI_SAMPLE_CFG
- ULPCD_THRESH_LVL
- ULPCD_GPIO3 - Allows to abort the ULPCD based on GPIO input.

9.10 External interfaces

The PN7642 requires the connection of a power supply, and a clock source like crystal or external clock.

Additional connections of the package require the connection of stabilizing capacitors and ground.

The RF interface connects transmitter and receiver to the EMC filter of a connected antenna matching network. Additional connections are available for the GPIO's and 2x DAC functionality (analog outputs).

The GPIO's implement internal Pull-up/Pull-down resistors. The output of the GPIO's can be configured in the pad configuration PAD_CONFIG.

9.11 Secure firmware update

The PN7642 supports a secure update of the implemented firmware.

The secure firmware download mode is using dedicated commands, but does not require a dedicated physical handling of the host interface lines.

For version C100, the firmware download mode is activated by asserting the DWL_REQ pin.

For version C101, the secure firmware download mode is entered by setting a register in non-volatile memory followed by a trigger of the VEN pin.[2]

The firmware binary file which is used to update the PN7642 is protected with an RSA signature and AES encryption.

The key length of the RSA is 2048 bits, the public exponent supports any 32-bit integer value.

2 For applications using the USB interface, the usage if version C100 is recommended. If USB_VBUS is high on C101, then IC will always boot into USB download mode.

A pre-computed Montgomery format of signature is used, and the signature hash computation is based on SHA256 algorithm.

This prevents a download of any other software which is not released by NXP.

The customer firmware of the user area has to be encrypted using the same cryptographic scheme as described above. The keys for signing and encryption can be provisioned and set by the customer.

To download unencrypted and unsigned firmware binary, the USB or SWD interfaces can be used.

An anti-tearing function is implemented in order to detect supply voltage removal or memory fault.

During the secure firmware download, the NFC operation is not available, only the command set defined for the secure firmware download is valid.

Updating the PN7642 with the default firmware binaries programs the memories for user configuration with default values. Any previous user configuration is overwritten. The user has to take care to restore the data of these memories after a secure firmware update.

If this is not intended, special firmware versions are available which do not overwrite the configuration. If the standard firmware file is named e.g. FW XX.YY, the name of the firmware which does not overwrite existing settings is then FW XX.FY. (The "F" is indicating the non-overwrite version)

The PN7642 checks if the new major version number is equal or higher than the current one. In case the major version number of the new firmware to be installed is smaller than the already installed version number of the firmware, the secure firmware update is rejected. Downgrading major firmware versions is therefore not possible. Upgrading and therefore increasing major firmware versions is always possible.

In case of any failure or exception during the download (e.g. caused by a communication error or power off), the PN7642 remains in the secure firmware download mode until a complete and valid NXP firmware is available in the device.

In case the firmware download of the user firmware was interrupted, but the NXP firmware is still valid, the device will boot into the application after a reset, except the DWL_REQ pin is still asserted.

Features of the automatic secure firmware update:

- Works without download request pin
- No special implementation of host interface handling
- Maximum integrity: Only encrypted and signed firmware images download possible via the secure firmware update functionality
- Updating the firmware overwrites existing all previous EEPROM configurations, unless a special version of the firmware was used.

9.12 Security Sub System

9.12.1 Asymmetric crypto unit

PN7642 provides an asymmetric cryptography coprocessor in order to support public-key cryptographic algorithms like RSA, ECC in finite prime and binary fields including Montgomery multiplication and reduction, plain and modular addition and subtraction. Additionally, this coprocessor can also be used to support other cryptographic operations like SHA, SM4, SEED, shift and rotate, logical functions (AND/OR/XOR), comparison and substitution.

All asymmetric cryptographic features are made available through a so called wrapper API based on mbedTLS library.

9.12.1.1 Features

- HKDF
- HMAC
- Elliptic Curve algorithms
  - ECKA
  - ECC key generation
  - ECDSA signing and verification
  - EdDSA signature generation and verification for Edward curve
  - Curves
    - Brainpool P256r1
    - Brainpool P384r1
    - SECP256
    - SECP384
    - Ed25519 signature generation and verification
    - Additional curves on Weierstrass and Prime are supported by feeding the specific domain parameters

9.12.2 Symmetric crypto unit

PN7642 implements a symmetric cryptography coprocessor that allows for fast execution of cryptographically strong en- and decryption based on the AES standard, and also supports fast hashing based on SHA256. Furthermore, it contains units for true and pseudo random number generation and secure key handling.

The symmetric crypto unit implements a separate protected communication channel into a special section in the flash memory where master keys, download keys, etc. are stored. This section is not accessible for the CPU or via any other AHB bus controller. This so-called Secure Key Transfer Unit manages the transfers between memory and crypto core, it automatically obfuscates the key material before physically writing it into the FLASH key store, generates a de-obfuscation mask upon reading from key store, and protects the communication channel between FLASH and crypto cores with transaction-specific masks.

All symmetric cryptographic features are made available through a so-called wrapper API based on mbedTLS library.

9.12.2.1 Features

- Fast AES-128 or AES-256 en/decryption
- Support for chaining modes: CBC, CTR
- SHA256 coprocessor
- AES en/decryption via DMA
- SHA256 hashing via DMA
- Random number generator (RNG)
- Countermeasures against side channel information leakage
- Supported algorithms
  - AES-CCM
  - AES-CBC
  - AES-ECB
  - AES-CTR
  - AES-GCM (in software)
  - AES-GMAC
  - SHA-256

9.12.2.2 Random number generator

The random number generator (RNG) is a digital module composed of a pseudo random number generator (PRNG) and an APB registers bank for control and access to the pseudo random number material. To provide the complete random number generation functionality within PN7642, the RNG module is directly linked to the analog random number generator (ARNG), also called true random number generator (TRNG). The ARNG/TRNG is needed for loading a new seed into the PRNG at start-up and for increasing entropy of the system when generating random numbers while the PRNG is used to generate the final 32-bit random number.

Features

- Generates a 32-bit random number
- 32-bit APB target register interface

9.12.2.2.1 PRNG unit

The pseudo random number generator (PRNG) is used for the following purposes:

- Generating mask data for secure key transfer
- Generate mask and blinding bits for the symmetric crypto core

It is based on two cross coupled linear feedback shift registers.

9.12.2.2.2 TRNG unit

The analog true random number generator (TRNG) unit is used for:

- Generating high-quality random numbers for firmware use
- Generating a random bit stream towards the contactless interface

The TRNG is directly incorporated into the symmetric crypto unit.

9.12.3 Secure key store

The secure key store is a subsystem that secures key material stored in the flash memory and manages the access rights toward the CPU and cryptographic components.

Note: The device is provisioned with factory default transport keys. These transport keys are considered public information and it is strongly recommended to replace these keys by customer-specific secret keys. Information about how to replace the factory default transport key can be found in [2]. Refer to Table 4 to obtain the factory default keys for the specific product.

Features

- 1 APP_ROOT_KEY AES-128
- 1 APP_ROOT_KEY AES-256
- Up to 13 pcs of AES-128 bit keys OR up to 6 pcs AES-256 bit keys (APP_MASTER_KEYs)
- 11 pcs of AES-128 or AES-256 keys stored in extended key store (APP_FIXED_KEYs)
- 7 pcs of Asymmetric keys (APP_ASYMM_KEY) with any of the key curves (NIST SECP256R1 / NIST SECP384R1 / BP256R1 (Brainpool) / BP384R1 (Brainpool))

The secure key store component has its own AHB controller port that completely bypasses the CPU subsystem's firewall and AHB interconnect matrix. The 4 kB large "key store" can only be accessed via the key store unit but not by any other AHB controller because the firewall implements a special rule that does not allow any access.

The PN7642 key management system differentiates between the following key types:

1. NXP_TPT_KEY

These AES 128/256 bit keys are by default provisioned in the NXP factory in each of the IC and are published. These keys are referred as NXP Transport Keys. These keys are loaded onto the internal security IP, where in a key must be derived from these keys to perform the operations required. These keys are stored in secure key storage enclave, where the CPU will not have access.

2. APP_ROOT_KEY
   These AES 128/256 bit symmetric keys are provisioned by application in place of NXP_TPT_KEYs. These keys are the application root keys which can be provisioned as long as these are not locked out. The application can lock the APP_ROOT_KEYs from further provisioning once the application development is complete and ready to be roll-out to production. These keys are loaded onto the internal security IP, where in a key must be derived from these keys to perform the operations required. These keys are stored in secure key storage enclave, where in CPU will not access.
3. APP_MASTER_KEY
   The secure key storage enclave can store additional application keys. A mix of 128-bit and 256-bit keys can also be stored. These keys are derived from NXP_TPT_KEY/APP_ROOT_KEY. A key must be derived from these keys for further operations. These keys are stored in secure key storage enclave, where in CPU will not have access.
4. APP_FIXED_KEY
   To enhance the storage of fixed keys, PN7642 provides a way to store the AES 128/256 symmetric keys in a secure flash. Only the encrypted key data and wrapping key derivation message is stored in secure flash. These keys are stored in secure key storage extension enclave, where in keys are stored in encrypted format. These encrypted keys are loaded onto secure key IP, where in key can be used directly with the key properties for the operations. The CPU will not have access to the loaded keys in secure key IP.
5. APP_ASYMM_KEY
   Secure key store also supports storing of asymmetric keys with different key length and different key curve types. The asymmetric private keys are encrypted with a key derived from NXP_TPT_KEY/ APP_ROOT_KEY.

9.12.4 General-purpose CRC unit

A cyclic redundancy check (CRC) is a type of hash function used to produce a checksum for a block of data. The checksum is used to detect errors after transmission or storage. A CRC is computed and appended before transmission or storage and verified afterwards by recipient to confirm that no changes occurred on transit.

The general purposes CRC coprocessor is used to speed up these kinds of operations, since they are quite time consuming or require large lookup tables if emulated in software. The coprocessor is accessible by the CPU via the AHBtoAPB bridge. Control and data transfer is done via the corresponding APB registers.

9.12.4.1 Features

- Supports 16-bit CRC compliant to CRC-16-CCITT
- Supports 32-bit CRC compliant to IEEE 802.3
- Supports PRBS9 and PRBS15 modes (pseudo random bit stream mode)
- Configurable seed value
- Optional MSB or LSB first data processing
- BYTE, WORD or DWORD data input

9.12.4.2 Functional description

This block implements a configurable 16/32bit parallel CRC and serial PRBS9/15 coprocessor. The 16-bit CRC is compliant to X.25 (CRC-CCITT, ISO/IEC13239) standard with a polynomial generator of:

$$g(x) = x^{16} + x^{12} + x^5 + 1$$

The 32-bit CRC is compliant to the Ethernet / AAL5 (IEEE 802.3) standard with a polynome generator of:

$$g(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

Note: No final XORing or inversion is performed.

CRC calculation is done in parallel, meaning that the CRC computation for a complete 8/16/32 bit data input is performed within one clock cycle from the moment an input data is written.

For the PRBS9 (and PRBS15), the sequence is generated in a nine-stage (fifteen stage for PRBS15) shift register shared with the CRC16 shift register.

The PRBS9 generator polynome used in this block is:

$$g(x) = x^9 + x^5 + 1$$

The PRBS15 generator polynome used in this block is:

$$g(x) = x^{15} + x^{14} + 1$$

Note: No automatic clearing is performed on the shift registers implementing the aforementioned generator polynomials, if the CRC mode is changed. It is at the responsibility of the user to correctly initialize them after a mode change.

9.13 Firmware Partitioning

9.13.1 General

The PN7642 differentiates between two execution environments. The secure area and the Application area. Software that is executed in the secure area is running in the Arm Trust Zone environment. Most parts of the NXP firmware are running in this secure area.

In contrast, the user application is running entirely in the Application area. Every time a peripheral from the secure firmware needs to be accessed (e.g accessing the contactless interface or the security subsystem), a context switch from the Application area to the secure area needs to happen. In order to provide a controlled interface from the secure area to the Application area, the System Service API Layer is implemented into the NXP firmware. This API layer is the only possibility to exchange data between Application and secure execution environments.

9.13.2 System service API

The following figure illustrates the firmware architecture design and the separation between secure and application area of the PN7642.

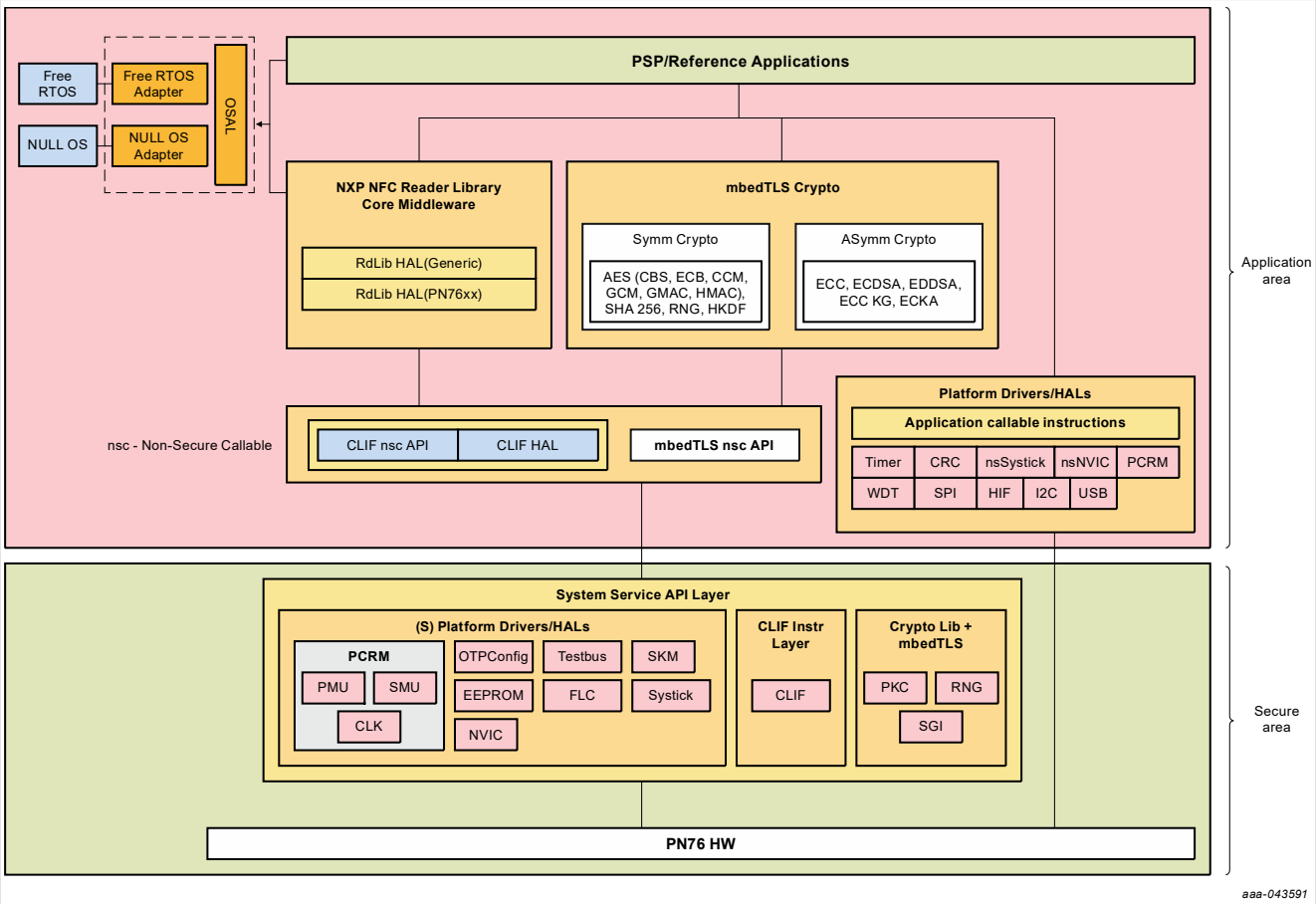


Figure 28. Firmware Architecture Design

The system service API is implemented as part of the NXP firmware within the secure area of the flash memory that is executed in secure execution environment. These APIs are callable from the application area.

The APIs can be broadly divided into following categories:

- In application programming API
- Life-Cycle management API
- Boot/download configuration API
- CLIF HAL/instruction API
- PCRM HAL API
- Symmetric crypto wrapper API
- Asymmetric crypto wrapper API
- Secure Key Mode API
- Utility APIs

Note: A customer can call these APIs by a valid code executing from flash memory or RAM memory. Hence during initial boot, the configuration set by some of these APIs are default set and used by the boot and primary download function in ROM.

9.13.2.1 In application programming API

This API is used by a customer during upgrade of the customer developed firmware (also called secondary firmware). Since customer's secondary downloader executes in Flash memory, it cannot write(programmed) at the same time. Hence the programming of flash page is performed from ROM memory with the help of this API.

This API returns error if Code Write Protection is enabled in Secrow.

9.13.2.2 Lifecycle management API

There are 4 lifecycle parameters that can be used by customers at various stages of product development. They are:

1. USB-based download / Mass Storage disable: Customer can use this API to set this parameter to 1 and during subsequent boots, the ROM will not execute primary download function even if DWL_REQ pin is HIGH and USB VBUS is sensed.
2. Secrow Lock: The Secrow contains some lifecycle parameters such as SWD Access and Code Write Protection. Using this API, any further writes to Secrow is prevented permanently.
3. SWD Access Level: SWD Access can have 2 configurations:
   a. Customer enabled access used by customers to debug their flash code
   b. No Access enabling customers to deploy their product

   When the IC is delivered from production, the default SWD access will be "Customer enabled access". Customers can irreversibly change this to No Access before deploying in the field. When SECROW LOCK is set, SWD is changed to No Access.
4. Code Write Protection (CWP): Using this API, a customer can prevent any intentional/unintentional over writing of Flash memory at the hardware level. If CWP is enabled, USB primary download does not expose the flash memory as mass storage device.

9.13.2.3 Boot/download configuration API

Three configurations are required during boot and primary download.

1. USB Configuration: This API is used to set the USB descriptors used during primary download function. Eg: PID, VID, Manufacturer String, Product String, Self/Bus Powered and MaxPower. By default, the PID and VID are NXP assigned {0x1FC9, 0x0117}.
2. Primary Download Configuration: This API is used to set the Code Read Protection Levels and Data Read Protection Levels during USB Primary download function. Refer to Table 25.
3. PVDD Config: The customer can configure whether the boot should wait for external PVDD or turn on the internal PVDD LDO to generate the requisite PVDD. It also provides options to configure, how long the boot code should wait for PVDD to ramp up if external PVDD LDO is used (depending on the characteristic of external PVDD LDO). There are 2 timeouts (in steps of 100us and max of 200 ms).

Table 25. CRP Levels

CRP Level	CRP / DRP explanation
No CRP	The user flash can be read or written
CRP1	The user flash cannot be read, flash memory regions are updated depending on the new firmware/data image
CRP2	The user flash cannot be read, flash memory regions are entirely erased before copying new firmware/data
CRP3	The user flash cannot be read/written

9.13.2.4 Contactless interface HAL / instruction API

The contactless interface HAL / instruction API can be divided into the following categories:

1. Register manipulation API
2. User flash data manipulation API
3. Protocol configuration API
4. Transceiver abstraction API
5. RF ISR callback API

9.14 System settings and configuration

The configuration and behavior of the device is controlled at a central place.

CLIF registers which can be used to control the RF exchange.

PCRM registers which can be used to set up the various functionalities required by the applications such as GPIO configuration, IP configurations etc.

EEPROM settings are a collection of all available configuration parameters that are needed for different operation modes. EEPROM settings serve as the source for the register settings.

The following chapters list down the CLIF and PCRM registers that are available to the user, as well as all available EEPROM configuration options.

9.14.1 CLIF Register description

The default setting of a bit within a register is indicated by the "*" or "Reset value". Value indicates the allowed range for the bits of a symbol.

Note, that some registers change its content by the firmware between an RF Exchange followed by an RF Reset command.

The detailed description of the registers is available in the User API documentation.

9.14.1.1 List of CLIF registers

List of CLIF registers and its addresses

Table 26. List of CLIF registers

Register Name	Register address (Hex)	Register address (Decimal)
SYSTEM_CONFIG (0x00)	0x00	0
EMD_CONTROL (0x03)	0x03	3
FELICA_EMD_CONTROL (0x04)	0x04	4
CLIF_RX_STATUS (0x05)	0x05	5
CLIF_RX_STATUS_ERROR (0x06)	0x06	6
CLIF_STATUS (0x07)	0x07	7
CLIF_TRANSCEIVE_CONTROL (0x08)	0x08	8
CLIF_TX_SYMBOL01_MOD (0x09)	0x09	9
CLIF_TX_SYMBOL1_DEF (0x0A)	0x0A	10
CLIF_TX_SYMBOL0_DEF (0x0B)	0x0B	11

Table 26. List of CLIF registers*...continued*

Register Name	Register address (Hex)	Register address (Decimal)
CLIF_TX_SYMBOL23_MOD (0x0C)	0x0C	12
CLIF_TX_SYMBOL23_DEF (0x0D)	0x0D	13
CLIF_TX_SYMBOL_CONFIG (0x0E)	0x0E	14
CLIF_TX_FRAME_CONFIG (0x0F)	0x0F	15
CLIF_TX_DATA_MOD (0x10)	0x10	16
CLIF_TX_WAIT (0x11)	0x11	17
CLIF_CRC_TX_CONFIG (0x12)	0x12	18
CLIF_TX_UNDERSHOOT_CONFIG (0x13)	0x13	19
CLIF_TX_OVERSHOOT_CONFIG (0x14)	0x14	20
CLIF_SS_TX_CFG (0x15)	0x15	21
CLIF_SS_TX1_RMCFG (0x16)	0x16	22
CLIF_SS_TX2_RMCFG (0x17)	0x17	23
CLIF_SS_TX_SCALE_CFG (0x18)	0x18	24
CLIF_SS_TX_TRANS_CFG (0x19)	0x19	25
CLIF_ANACTRL_TX1_GSN (0x1A)	0x1A	26
CLIF_ANACTRL_TX2_GSN (0x1B)	0x1B	27
CLIF_ANACTRL_TX_GSP (0x1C)	0x1C	28
CLIF_SIGPRO_CONFIG (0x1D)	0x1D	29
CLIF_SIGPRO_RM_WAIT (0x1E)	0x1E	30
CLIF_SIGPRO_RM_CONFIG (0x1F)	0x1F	31
CLIF_SIGPRO_RM_PATTERN (0x20)	0x20	32
CLIF_SIGPRO_RM_ENABLES (0x21)	0x21	33
CLIF_SIGPRO_RM_TECH (0x22)	0x22	34
CLIF_SIGPRO_NOISE_CONFIG1 (0x23)	0x23	35
CLIF_SIGPRO_NOISE_CONFIG2 (0x24)	0x24	36
CLIF_RX_PROTOCOL_CONFIG (0x25)	0x25	37
CLIF_RX_FRAME_LENGTH (0x26)	0x26	38
CLIF_RX_ERROR_CONFIG (0x27)	0x27	39
CLIF_RXCTRL_STATUS (0x28)	0x28	40
CLIF_SIGPRO_IIR_CONFIG1 (0x29)	0x29	41
CLIF_SIGPRO_IIR_CONFIG0 (0x2A)	0x2A	42
CLIF_DGRM_DAC_FILTER (0x2B)	0x2B	43
CLIF_DGRM_CONFIG (0x2C)	0x2C	44
CLIF_DGRM_BBA (0x2D)	0x2D	45
CLIF_DGRM_DCO (0x2E)	0x2E	46
CLIF_DGRM_HF_ATT (0x2F)	0x2F	47

Table 26. List of CLIF registers*...continued*

Register Name	Register address (Hex)	Register address (Decimal)
CLIF_DGRM_RSSI (0x30)	0x30	48
CLIF_CRC_RX_CONFIG (0x31)	0x31	49
CLIF_RX_WAIT (0x32)	0x32	50
CLIF_DCOC_CONFIG (0x33)	0x33	51
CLIF_RXM_NFCLD_LVL (0x34)	0x34	52
CLIF_RXM_CTRL (0x35)	0x35	53
CLIF_ANA_AGC_DCO_CTRL (0x36)	0x36	54
CLIF_SIGPRO_CM_CONFIG (0x37)	0x37	55
CLIF_GCM_CONFIG2 (0x38)	0x38	56
CLIF_GCM_CONFIG1 (0x39)	0x39	57
CLIF_GCM_CONFIG0 (0x3A)	0x3A	58
CLIF_SS_TX1_CMCFG (0x3B)	0x3B	59
CLIF_SS_TX2_CMCFG (0x3C)	0x3C	60
CLIF_TIMER0_CONFIG (0x3D)	0x3D	61
CLIF_TIMER0_RELOAD (0x3E)	0x3E	62
CLIF_TIMER1_CONFIG (0x3F)	0x3F	63
CLIF_TIMER1_RELOAD (0x40)	0x40	64
CLIF_ANA_STATUS (0x41)	0x41	65
CLIF_ANA_RX_CTRL (0x43)	0x43	67
CLIF_ANACTRL_TX_CONFIG (0x44)	0x44	68
CLIF_ANACTRL_TX_NOV (0x45)	0x45	69
CLIF_RX_EOF_PATTERN (0x46)	0x46	70
CLIF_RX_EMD_1_CONFIG (0x47)	0x47	71
CLIF_RX_EMD_0_CONFIG (0x48)	0x48	72
CLIF_SIGPRO_CM_FILT128B (0x49)	0x49	73
CLIF_SIGPRO_CM_FILT128A (0x4A)	0x4A	74
CLIF_SIGPRO_CM_FILT64 (0x4B)	0x4B	75
CLIF_SIGPRO_CM_FILT16_32 (0x4C)	0x4C	76
CLIF_SIGPRO_CM_CONFIG2 (0x4D)	0x4D	77
CLIF_SIGPRO_CM_CONFIG3 (0x4E)	0x4E	78
CLIF_SIGPRO_PRE_CONFIG (0x4F)	0x4F	79
LPCD_CALIBRATE_CTRL (0x50)	0x50	80
IQ_CHANNEL_VALS (0x51)	0x51	81
CALIBRATE_STATUS (0x53)	0x53	83
TXLDO_VDDPA_CONFIG (0x54)	0x54	84
TXLDO_VOUT_CURR (0x56)	0x56	84

Table 26. List of CLIF registers*...continued*

Register Name	Register address (Hex)	Register address (Decimal)
CLIF_RXM_FREQ (0x59)	0x59	89
CLIF_RXM_RSSI (0x5A)	0x5A	90
INTERPOLATED_RSSI_REG (0x5C)	0x5C	92
TX_NOV_CALIBRATE_AND_STORE_VAL_REG (0x5D)	0x5D	93
CLIF_TIMER0_OUTPUT (0x5F)	0x5F	95
CLIF_TIMER1_OUTPUT (0x60)	0x60	96
CLIF_TIMER2_CONFIG (0x61)	0x61	97
CLIF_TIMER2_RELOAD (0x62)	0x62	98
CLIF_TIMER2_OUTPUT (0x63)	0x63	99
CLIF_BM_TX_BUFFER (0x66)	0x66	102
CLIF_BM_RX_WATERLEVEL (0x67)	0x67	103
CLIF_BM_RX_BUFFER (0x68)	0x68	104
CLIF_RF_CONTROL (0x69)	0x69	105
CLIF_TX_DATA_CONFIG (0x6A)	0x6A	106
CLIF_CONTROL (0x6B)	0x6B	107
CLIF_INT_SET_ENABLE (0x6C)	0x6C	108
CLIF_INT_CLR_ENABLE (0x6D)	0x6D	109
CLIF_INT_STATUS (0x6E)	0x6E	110
CLIF_INT_ENABLE (0x6F)	0x6F	111
CLIF_INT_CLR_STATUS (0x70)	0x70	112
BMA_INT_ENABLE (0x71)	0x71	113
BMA_INT_CLR_ENABLE (0x72)	0x72	114
BMA_INT_SET_ENABLE (0x73)	0x73	115
BMA_INT_STATUS (0x74)	0x74	116
BMA_INT_CLR_STATUS (0x75)	0x75	117
CLIF_SS_TX1_RTRANS0 (0x80)	0x80	128
CLIF_SS_TX1_RTRANS1 (0x81)	0x81	129
CLIF_SS_TX1_RTRANS2 (0x82)	0x82	130
CLIF_SS_TX1_RTRANS3 (0x83)	0x83	131
CLIF_SS_TX2_RTRANS0 (0x84)	0x84	132
CLIF_SS_TX2_RTRANS1 (0x85)	0x85	133
CLIF_SS_TX2_RTRANS2 (0x86)	0x86	134
CLIF_SS_TX2_RTRANS3 (0x87)	0x87	135
CLIF_SS_TX1_FTRANS0 (0x88)	0x88	136
CLIF_SS_TX1_FTRANS1 (0x89)	0x89	137
CLIF_SS_TX1_FTRANS2 (0x8A)	0x8A	138

Table 26. List of CLIF registers*...continued*

Register Name	Register address (Hex)	Register address (Decimal)
CLIF_SS_TX1_FTRANS3 (0x8B)	0x8B	139
CLIF_SS_TX2_FTRANS0 (0x8C)	0x8C	140
CLIF_SS_TX2_FTRANS1 (0x8D)	0x8D	141
CLIF_SS_TX2_FTRANS2 (0x8E)	0x8E	142
CLIF_SS_TX2_FTRANS3 (0x8F)	0x8F	143

9.14.1.2 SYSTEM_CONFIG (0x00)

This register provides the system configuration on Autocoll, MFC Crypto bit generation, ISO15693 baud-rate, TXNOV calibration.

Table 27. SYSTEM_CONFIG (0x00) register bit description

Bit	Symbol	Access	Value	Description
[31:9]	RFU	rw		Reserved
[8:8]	TX_NOV_CALIBRATE	rw		One time calibration when the host writes a 1 into this register, a one time calibration will be performed. **Note:**The calibration is resulting a short RF-on. All the power configurations shall the configured before setting this bit.
[7:7]	RFU	rw		Reserved
[6:5]	15693_CHANGE_DATARATE	rw		15693_changedatarate. By default, the basic data rate of 26kB/sec will be loaded, switching to a different higher data rate requires this config register to be updated. All relevant related registers will be updated automatically.
			0	RFU
			1	Change Data Rate to 53kB/sec
			2	Change Data Rate to 106kB/sec
			3	Change Data Rate to 212kB/sec
[4:2]	RFU	rw		Reserved
[1:1]	MFC_CRYPTO_ON	rw		MIFARE crypto bit generation for MIFARE Classic en/de-cryption
			0	MIFARE - crypto bit is not generated for MIFARE Classic en-/de-cryption
			1	MIFARE - crypto bit is generated for MIFARE Classic en-/de-cryption
[0:0]	AUTOCOLL_STATE_A	rw		Autocoll state for Type A
			0	TypeA Card mode: Autocoll entry with IDLE state of the card
			1	TypeA Card mode: Autocoll entry with HALT state of the card

9.14.1.3 EMD_CONTROL (0x03)

This register provides the settings for EMD_CONTROL.

Table 28. EMD_CONTROL (0x03) register bit description

Bit	Symbol	Access	Value	Description
[31:12]	RFU	rw		Reserved
[11:10]	EMD_RM_EMD_SENSITIVITY	rw		RM EMD SENSITIVITY value that will be applied to SIGPRO_RM_CONFIG, At layer 4, when EMD is enabled, the value of EMD_RM_SENSITIVITY can be lowered to ensure robust EMD suppression, if during the layer 3 activation, the value of EMD_RM_SENSITIVITY in the protocol area is set to a high value to ensure collision detection and resolution when multiple typeA cards are presented at close distance to the antenna.
[9:8]	EMD_TRANSMISSION_TIMER_USED	rw		Timer used for RF communication.
[7:7]	EMD_MISSING_CRC_IS_PROTOCOL_ERROR_TYPE_B	rw		Missing CRC treated as protocol error in case of Type B based communication
[6:6]	EMD_MISSING_CRC_IS_PROTOCOL_ERROR_TYPE_A	rw		Missing CRC treated as protocol error in case of Type A based communication
[5:2]	EMD_NOISE_BYTES_THRESHOLD	rw		Defines the threshold under which transmission errors are treated as noise. Note: CRC bytes are NOT included/counted!
[1:1]	EMD_TRANSMISSION_ERROR_ABOVE_NOISE_THRESHOLD_IS_NO_EMD	rw		Transmission errors with received byte length more than or equal EMD_NOISE_BYTES_THRESHOLD is never treated as EMD
[0:0]	EMD_ENABLE	rw		EMD handling enabled

9.14.1.4 FELICA_EMD_CONTROL (0x04)

This register provides the settings for FELICA_EMD_CONTROL.

Table 29. FELICA_EMD_CONTROL (0x04) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	FELICA_EMD_RC_BYTE_VALUE	rw		RC byte value that needs to be received to not treat the frame as EMD
[23:16]	FELICA_EMD_LENGTH_BYTE_MAX	rw		Maximum Legth byte value that needs to be received to not treat the frame as EMD
[15:8]	FELICA_EMD_LENGTH_BYTE_MIN	rw		Minimum Legth byte value that needs to be received to not treat the frame as EMD
[7:5]	RESERVED	rw		Reserved
[6:6]	FELICA_EMD_LOG_ENABLE	rw		Log Enable bit to send RX Status during EMD
			0	Log Enable bit to send RX Status during EMD
			1	Log Enable bit to send RX Status during EMD
[5:5]	FELICA_EMD_RC_CHECK_ON_CRC_CORRECT_ENABLE	rw		RC byte check enabled for FeliCa EMD handling on complete RF Frame when there is no Integrity Error observed

Table 29. FELICA_EMD_CONTROL (0x04) register bit description*...continued*

Bit	Symbol	Access	Value	Description
			0	RC byte check enabled for FeliCa EMD handling on complete RF Frame when there is no Integrity Error observed
			1	RC byte check enabled for FeliCa EMD handling on complete RF Frame when there is no Integrity Error observed
[4:4]	FELICA_EMD_INTEGRITY_ERR_CHECK_ENABLE	rw		FeliCa EMD handling enabled when integrity error is set
[3:3]	FELICA_EMD_PROTOCOL_ERR_CHECK_ENABLE	rw		FeliCa EMD handling enabled when protocol error is set
[2:2]	FELICA_EMD_RC_CHECK_ENABLE	rw		FeliCa RC byte check enabled for FeliCa EMD handling
[1:1]	FELICA_EMD_LEN_CHECK_ENABLE	rw		FeliCa Length byte check enabled for FeliCa EMD handling
[0:0]	FELICA_EMD_ENABLE	rw		FeliCa EMD handling enabled

9.14.1.5 CLIF_RX_STATUS (0x05)

This register provides the CLIF RX status.

Table 30. CLIF_RX_STATUS (0x05) register bit description

Bit	Symbol	Access	Value	Description
[31:27]	RESERVED	r-	0x0	Reserved
[26:20]	RX_COLL_POS	r-	0x0	Status indicating the bit position of the first collision detected in the data bit. The value is valid only when RX_COLLISION_DETECTED==1. The value of the RX_BIT_ALIGN is also taken intoaccount (RX_COLL_POS = physical bit position in the flow + RX_BIT_ALIGN value).Indicates the collision position in the first 8 bytes only. Can be used during the Type A/ICODE/EPC anticollision procedure.0x00 - 1st bit 0x01 - 2nd bit...0x7F - 128th bit.The status register is not updated by the collision detected on stop or parity bit.
[19:17]	RX_NUM_LAST_BITS	r-	0x0	Indicating the number of valid bits in the last byte received.This is generally used during ISO/IEC14443 type A anti-collision
			0	0: all bits are valid
			1	1: 1 bit is valid
			2	2: 2 bits are valid
			3	3: 3 bits are valid
			4	4: 4 bits are valid
			5	5: 5 bits are valid
			6	6: 6 bits are valid
			7	7: 7 bits are valid

Table 30. CLIF_RX_STATUS (0x05) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[16:13]	RX_NUM_FRAMES_RECEIVED	r-	0x0	Indicates the number of frames received. The value is updated after every normal frame reception in RX_MULTIPLE mode.The value is valid only if the bit RX_MULTIPLE_ENABLE==1.
[12:0]	RX_NUM_BYTES_RECEIVED	r-	0x0	Number of bytes received on the RF interface. This field is not relevant when RX_MULTIPLE_ENABLE=='1'.

9.14.1.6 CLIF_RX_STATUS_ERROR (0x06)

This register provides the CLIF_RX_ERROR status.

Table 31. CLIF_RX_STATUS_ERROR (0x06) register bit description

Bit	Symbol	Access	Value	Description
[31:30]	RESERVED	r-	0x0	Reserved
[29:29]	EMD_DETECTED_IN_RXDEC	r-	0x0	The high level indicates that the EMD was detected (in the SigPro or in the RxDecoder or in both) during the reception.
[28:28]	EMD_DETECTED_IN_SIGPRO	r-	0x0	The high level indicates that the EMD was detected on the Physical layer (in the SigPro) during the reception.
[27:27]	EXT_RFOFF_DETECTED	r-	0x0	The high level indicates that the received frame length violated the configured minimum limit.
[26:26]	RX_FRAME_MAXLEN_VIOL	r-	0x0	The high level indicates that the received frame length is less or equal to the expected CRC field length
[25:25]	RX_FRAME_MINLEN_VIOL	r-	0x0	The high level indicates that the last received character in the frame has less than 8 bits.
[24:24]	RX_FRAME_LE_CRC	r-	0x0	The high level indicates that the last received character in the frame has 8 data bits but the expected parity bit is absent.
[23:23]	RX_NOT_FULL_BYTE	r-	0x0	The high level indicates that the last received character in the frame has 8 data bits but the expected stop bit is absent.
[22:22]	RX_MISSING_PARBIT_DETECTED	r-	0x0	The high level indicates that the collision was detected on the parity bit position.
[21:21]	RX_MISSING_STOPBIT_DETECTED	r-	0x0	The high level indicates that the collision was detected on the stop bit position.
[18:18]	RX_COLLISION_DETECTED	r-	0x0	The high level indicates that the collision was detected during the frame reception.
[17:17]	RX_STOP_ON_RXOVER	r-	0x0	The high level indicates that the frame reception was stopped by SGP_MSG_RXOVER_* message reception.
[16:16]	RX_STOP_ON_RFOFF	r-	0x0	The high level indicates that the frame reception was interrupted by external RF-field vanishing event.
[15:15]	RX_STOP_ON_ERR	r-	0x0	The high level indicates that the frame reception was stopped by detected communication error event.

Table 31. CLIF_RX_STATUS_ERROR (0x06) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[14:14]	RX_STOP_ON_LEN	r-	0x0	The high level indicates that the frame reception was normally stopped by byte counter expiration event. Relates to the protocols where the LEN field is used in the frame format (Felica RM/CM, FWEC RM/CM).
[13:13]	RX_STOP_ON_INVPAR	r-	0x0	The high level indicates that the frame reception was normally stopped by the inverted parity detection event. Relates to the TypeA RM 212-848 kbps modes. 12 RX_STOP_ON_PATTERN R 0h The high level indicates that the frame reception was normally stopped by EOF pattern detection event. Relates to the TypeB RM/CM, B prime RM/CM modes.
[12:12]	RX_STOP_ON_PATTERN	r-	0x0	The high level indicates that the frame reception was normally stopped by EOF pattern detection event. Relates to the TypeB RM/CM, B prime RM/CM modes.
[11:11]	RX_STOP_ON_ANTICOLL	r-	0x0	The high level indicates that the frame reception was normally stopped by collision detected on data bit position. Relates to the bit-oriented frame reception in TypeA RM 106 kbps mode during the anticollision procedure.
[10:10]	RX_CRC_ERROR	r-	0x0	The high level indicates that the CRC error is detected in the received frame.
[9:9]	RX_LEN_ERROR	r-	0x0	The high level is set if the received frame is shorter than the length stated in the received frame LEN field OR if the LEN parameter in the received frame violates the configured [RX_FRAME_MINLEN:RX_ FRAME_MAX LEN] limits. Can assert only in the mode swhere the LEN field is used in the frame format (Felica RM/CM, FWEC RM/CM).
[8:8]	RX_SIGPRO_ERROR	r-	0x0	The high level indicates that the communication error/ errors were detected during the frame reception on physical layer(in the SigPro).
[7:7]	RX_PARITY_ERROR	r-	0x0	The high level indicates that the parity error was detected during the frame reception.
[6:6]	RX_STOPBIT_ERROR	r-	0x0	The high level indicates that the stop bit error (0 level instead of 1 on the stop bit position) was detected during the frame reception.
[5:5]	RX_WRITE_ERROR	r-	0x0	The high level indicates that the error acknowledge status was received on theCLIF-system interface during the received frame transmission to the System RAM.
[4:4]	RX_BUFFER_OVFL_ERROR	r-	0x0	The high level indicates that the data payload length in the received frame exceeds the 28 bytes limit. Relates to the PollReq procedure in the Felica RM mode only.
[3:3]	RX_LATENCY_ERROR	r-	0x0	The high level indicates that the write request flow was corrupted due to traffic congestion on the system interface during the received frame transmission to the System RAM.

Table 31. CLIF_RX_STATUS_ERROR (0x06) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[2:2]	RX_DATA_INTEGRITY_ERROR	r-	0x0	The high level indicates that the data integrity corruption (parity/CRC/etc error)was detected in the received frame.
[1:1]	RX_PROTOCOL_ERROR	r-	0x0	The high level indicates that the protocol requirements violation (stop bit error,missing parity bit, not full byte received, etc) was detected in the received frame.
[0:0]	RX_CL_ERROR	r-	0x0	The high level indicates that some protocol/data integrity erorr/errors were detected during the frame reception

9.14.1.7 CLIF_STATUS (0x07)

Table 32. CLIF_STATUS (0x07) register bit description

Bit	Symbol	Access	Value	Description
[31:30]	RESERVED	r-	0x0	Reserved
[29:29]	CRC_OK	r-	0x1	This bit indicates the status of the actual CRC calculation. If 1 the CRC is correct. meaning the CRC register has the value 0 or the residue value if inverted CRC is used. Note: This flag should only by evaluated at the end of a communication
[28:28]	RX_SC_DETECTED	r-	0x0	Status signal indicating that a sub-carrier is detected.
[27:27]	RX_SOF_DETECTED	r-	0x0	Status signal indicating that a SOF has been detected.
[26:26]	TX_RF_STATUS	r-	0x0	If set to 1 this bit indicates that the drivers are turned on. meaning an RF-Field is created by the device itself.
[25:25]	RF_DET_STATUS	r-	0x0	If set to 1 this bit indicates that an external RF-Field is detected by the rf level detectors (after digital filtering)
[24:24]	ADC_Q_CLIPPING	r-	0x0	Indicates that the Q-Channel ADC has clipped (value 0 or 63), This bit is reset with Rx-reset (enabling of receiver).
[23:23]	ADC_I_CLIPPING	r-	0x0	Indicates that the I-Channel ADC has clipped (value 0 or 63), This bit is reset with Rx-reset (enabling of receiver).
[22:22]	DPLL_SATURATED_LIMIT	r-	0x0	Status signal indicating that the DPLL has reached its locking limits (integrator is at 0 or maximum)
[21:21]	DPLL_SATURATED_LOCK_RANGE	r-	0x0	Status signal indicating that the DPLL has reached its locking limits. (Saturation range configured via DPLL_SATURATION_VAL)
[20:20]	DPLL_FREQ_LOCK_SUPER_FINE	r-	0x0	Status signal indicating that the DPLL has reached frequency-lock with ~1.4Hz accuracy
[19:19]	DPLL_FREQ_LOCK_FINE	r-	0x0	Status signal indicating that the DPLL has reached frequency-lock with ~5Hz accuracy
[18:18]	DPLL_FREQ_LOCK_COARSE	r-	0x0	Status signal indicating that the DPLL has reached frequency-lock with ~50Hz accuracy

Table 32. CLIF_STATUS (0x07) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[17:17]	DPLL_PHASE_LOCK	r-	0x0	Status signal indicating that the DPLL has reached phase-lock (typically happens before DPLL_ FREQUENCY_LOCK_COARSE is set).
[16:16]	DPLL_ENABLE	r-	0x0	This bit indicates that the DPLL Controler has enabled the DPLL (RF on RF frequency ok PLL locked)
[15:15]	RESERVED	r-	0x0	Reserved
[14:14]	BMA_TRANSFER_ONGOING	r-	0x0	Status signal from Buffer Manager to indicate that a transfer is actually ongoing.
[13:13]	TX_READ_ERROR	r-	0x0	This error flag is set to 1 if for an ongoing transmission data is not copied from RAM in time (BMA encountered read error) and therefor the transmission is aborted. **Note:**This case should not happen in normal operation
[12:12]	TX_LATENCY_ERROR	r-	0x0	This error flag is set to 1. if for an ongoing transmission data is not available in time (BMA latency to big) and therefor the transmission is aborted. **Note:** This case should not happen in normal operation
[11:11]	TX_NO_DATA_ERROR	r-	0x0	This error flag is set to 1. in case a transmission is started but no data is available (register NumBytesTo Send == 0).
[10:8]	RF_ACTIVE_ERROR_CAUSE	r-	0x00	This status flag indicates the cause of an NFC-Active error. **Note:** This bits are only valid when the RF_ACTIVE_ ERROR_IRQ is raised and will be cleared as soon as the bit TX_RF_ENABLE is set to 1.
			0x00	reset value
			0x01	External field was detected on within TIDT timing
			0x02	External field was detected on within TADT timing
			0x03	No external field was detected within TADT timings
			0x04	Peer did switch off RFField without but no Rx event was raised (no data received)
			0x05-0x07	Reserved.
[7:6]	RESERVED	r-	0x0	Reserved
[5:5]	RX_ENABLE	r-	0x0	This bit indicates if the RxDecoder is enalbed. If 1 the RxDecoder was enabled by the Transceive Unit and is now ready for data reception
[4:4]	TX_ACTIVE	r-	0x0	This bit indicates activity of the TxEncoder. If 1 a transmission is ongoing otherwise the TxEncoder is in idle state.

Table 32. CLIF_STATUS (0x07) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[3:3]	RX_ACTIVE	r-	0x0	This bit indicates activity of the RxDecoder. If 1 a data reception is ongoing. otherwise the RxDecoder is in idle state.
[2:0]	TRANSCEIVE_STATE	r-	0x0	This registers hold the command bits
			0	0: IDLE state
			1	1: WaitTransmit state
			2	2: Transmitting state
			3	3: WaitReceive state
			4	4: WaitForData state
			5	5: Receiving state
			6	6: LoopBack state
			7	7: reserved

9.14.1.8 CLIF_TRANSCEIVE_CONTROL (0x08)

This register provides the CLIF_TRANSCEIVE_CONTROL.

Table 33. CLIF_TRANSCEIVE_CONTROL (0x08) register bit description

Bit	Symbol	Access	Value	Description
[31:30]	RESERVED	r-	0x0	Reserved
[29:24]	STATE_TRIGGER_SELECT	rw	0x0	Register to select the state to trigger the STATE_CHANGE_IRQ flag. Each bit of the bit field enables one state - several states are possible. **Note:**If all bits are 0 no IRQ is triggered.
			xxxxx1	IDLE state enabled to trigger IRQ
			xxxx1x	WaitTransmit state enabled to trigger IRQ
			xxx1xx	Transmitting state enabled to trigger IRQ
			xx1xxx	WaitReceive state enabled to trigger IRQ
			x1xxxx	WaitForData state enabled to trigger IRQ
			1xxxxx	Receiving state enabled to trigger IRQ
[23:18]	RESERVED	r-	0x0	Reserved
[17:17]	TX_WAIT_RFON_ENABLE	rw	0x0	If set to 1 the TxWait guard time will be started when the own RF-Field is switched on. **Note:** In default configuration the TxWait guard time is started at the end of reception. This feature is intended to be used for NFC-Active communication
[16:16]	RX_WAIT_RFON_ENABLE	rw	0x0	If set to 1 the RxWait guard time will be started when the own RF-Field is switched off and an external RF-Field was detected. **Note:** In default configuration the RxWait guard time is started at the end of transmission. This feature is intended to be used for NFC-Active communication

Table 33. CLIF_TRANSCEIVE_CONTROL (0x08) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[15:8]	TX_BITPHASE	rw	0x0	Defines the number of 13.56 MHz cycles used for adjustment of TX_WAIT to meet the FDT. This is applicable for CardMode only.
[7:7]	RESERVED	r-	0x0	Reserved
[6:6]	TX_MILLER_SYNC_ENABLE	rw	0x0	If set to 1 guard time is synchronized to miller envelope for transmission. Used for AGC.
[5:5]	TX_SKIP_SEND_ENABLE	rw	0x0	If set to 1 not transmission is started after tx_wait is expired and START_SEND was set **Note:** The bit is cleared by HW when the Wait Receive state is entered.
[4:4]	TX_PICC2_TIMESLOT_ENABLE	rw	0x0	If set to 1 two PICC responses are transmitted in different timeslots. **Note:** Only valid when command Transceive is active.
[3:3]	TX_FRAMESTEP_ENABLE	rw	0x0	If set to 1. at every start of transmission. each byte of data is sent in a seperate frame. SOF and EOF is appended to the data byte according to the framing settings. After one byte is transmitted. the TxEncoder waits for a new start trigger to continue with the next byte.
[2:2]	RX_MULTIPLE_ENABLE	rw	0x0	If this bit is set to 1. the receiver is re-activated after the end of a reception. A statusbyte is written to the RAM containing all relevant status information of the frame. **Note:** Data in RAM is word aligned therefore empty bytes of a data Word in RAM are padded with 0x00 bytes. SW has to calculate the correct address for the following frame.
[1:1]	MILLER_SYNC_ENABLE	rw	0x0	If set to one miller pulse synchronisation is enabled. **Note:** TX_BITPHASE is used to adjust the prescaler of the guard timer. Note: This bit is set by HW when TypeA protocol is detected in automatic mode detection.
[0:0]	INITIATOR	rw	0x0	Set to 1. theCLIF is configured for initiator mode. Depending on this setting the behavior of the transceive command is different

9.14.1.9 CLIF_TX_SYMBOL01_MOD (0x09)

This register provides the CLIF_TX_SYMBOL01_MOD.

Table 34. CLIF_TX_SYMBOL01_MOD (0x09) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	RESERVED	r-	0x0	Reserved
[23:16]	TX_S01_MODWIDTH	rw	0x0	Specifies the length of a pulse for sending data of symbol 0/1. The length is given by the number of carrier clocks + 1.
[15:9]	RESERVED	r-	0x0	Reserved

Table 34. CLIF_TX_SYMBOL01_MOD (0x09) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[8:8]	TX_S01_MILLER_ENABLE	rw	0x0	If set to 1. pulse modulation is applied according to modified miller coding.
[7:7]	TX_S01_INV_ENV	rw	0x0	If set to 1. the output envelope is inverted.
[6:4]	TX_S01_ENV_TYPE	rw	0x0	Specifies the type of envelope used for transmission of data packets. The selected envelope type is applied to the pseudo bit stream. 000b Direct output 001b Manchester code 010b Manchster code with subcarrier 011b BPSK 100b RZ (pulse of half bit length at beginning of second half of bit) 101b RZ (pulse of half bit length at beginning of bit) 110b Manchester tupple 111b RFU
			000b	000b -> Direct output
			001b	001b -> Manchester code
			010b	010b -> Manchester code with subcarrier
			011b	011b -> BPSK
			100b	100b -> RZ (pulse of half bit length at beginning of second half of bit)
			101b	101b -> RZ(pulse of half bit length at beginning of bit)
			110b	110b -> Manchester tupple
			111b	111b -> RFU.
[3:3]	TX_S01_SC_FREQ	rw	0x0	Specifies the frequency of the subcarrier.
			0	0: 424 kHz
			1	1: 848 kHz
[2:0]	TX_S01_BIT_FREQ	rw	0x0	Specifies the frequency of the bit-stream. 000b -> 1.695 MHz. 001b -> Reserved. 010b -> 26 kHz. 011b -> 53 kHz. 100b -> 106 kHz. 101b -> 212 kHz. 110b -> 424 kHz. 111b -> 848 kHz.
			000b	000b -> 1.695 MHz
			001b	001b -> Reserved
			010b	010b -> 26 kHz
			011b	011b -> 53 kHz
			100b	100b -> 106 kHz
			101b	101b -> 212 kHz.
			110b	110b -> 424 kHz.
			111b	111b -> 848 kHz.

9.14.1.10 CLIF_TX_SYMBOL1_DEF (0x0A)

This register provides the settings for CLIF_TX_SYMBOL1_DEF

Table 35. CLIF_TX_SYMBOL1_DEF (0x0A) register bit description

Bit	Symbol	Access	Value	Description
[31:0]	TX_SYMBOL1_DEF	rw	0x0	Pattern definition for Symbol1

9.14.1.11 CLIF_TX_SYMBOL0_DEF (0x0B)

This register provides the settings for CLIF_TX_SYMBOL0_DEF

Table 36. CLIF_TX_SYMBOL0_DEF (0x0B) register bit description

Bit	Symbol	Access	Value	Description
[31:0]	TX_SYMBOL0_DEF	rw	0x0	Pattern definition for Symbol0

9.14.1.12 CLIF_TX_SYMBOL23_MOD (0x0C)

This register provides the settings for CLIF_TX_SYMBOL23_MOD

Table 37. CLIF_TX_SYMBOL23_MOD (0x0C) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	RESERVED	r-	0x0	Reserved
[23:16]	TX_S23_MODWIDTH	rw	0x0	Specifies the length of a pulse for sending data of symbol 2/3. The length is given by the number of carrier clocks + 1.
[15:9]	RESERVED	r-	0x0	Reserved
[8:8]	TX_S23_MILLER_ENABLE	rw	0x0	If set to 1 pulse modulation is applied according to modified miller coding.
[7:7]	TX_S23_INV_ENV	rw	0x0	If set to 1 the output envelope is inverted.
[6:4]	TX_S23_ENV_TYPE	rw	0x0	Specifies the type of envelope used for transmission of data packets. The selected envelope type is applied to the pseudo bit stream.
			000b	000b -> Direct output
			001b	001b -> Manchester code
			010b	010b -> Manchester code with subcarrier
			011b	011b -> BPSK
			100b	100b -> RZ (pulse of half bit length at beginning of second half of bit)
			101b	101b -> RZ(pulse of half bit length at beginning of bit)
			110b	110b -> Manchester tupple
			111b	111b -> RFU.
[3:3]	TX_S23_SC_FREQ	rw	0x0	Specifies the frequency of the subcarrier.
			0	0: 424 kHz
			1	1: 848 kHz
[2:0]	TX_S23_BIT_FREQ	rw	0x0	Specifies the frequency of the bit-stream.
			000b	000b -> 1.695 MHz
			001b	001b -> Reserved

Table 37. CLIF_TX_SYMBOL23_MOD (0x0C) register bit description*...continued*

Bit	Symbol	Access	Value	Description
			010b	010b -> 26 kHz
			011b	011b -> 53 kHz
			100b	100b -> 106 kHz
			101b	101b -> 212 kHz.
			110b	110b -> 424 kHz.
			111b	111b -> 848 kHz.

9.14.1.13 CLIF_TX_SYMBOL23_DEF (0x0D)

This register provides the settings for CLIF_TX_SYMBOL23_DEF

Table 38. CLIF_TX_SYMBOL23_DEF (0x0D) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	RESERVED	r-	0x0	Reserved
[23:16]	TX_SYMBOL3_DEF	rw	0x0	Pattern definition for Symbol3
[15:8]	RESERVED	r-	0x0	Reserved
[7:0]	TX_SYMBOL2_DEF	rw	0x0	Pattern definition for Symbol2

9.14.1.14 CLIF_TX_SYMBOL_CONFIG (0x0E)

This register provides the settings for CLIF_TX_SYMBOL_CONFIG

Table 39. CLIF_TX_SYMBOL_CONFIG (0x0E) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x0	Reserved
[30:27]	TX_SYMBOL1_BURST_LEN	rw	0x0	Specifies the number of bits issued for symbol 1 burst. The 3 bits encode a range from 8 to 256 bit length
			0000b	0000b -> 8 bit
			0001b	0001b -> 12 bit
			0010b	0010b -> 16 bit
			0011b	0011b -> 24 bit
			0100b	0100b -> 32 bit
			0101b	0101b -> 40 bit
			0110b	0110b -> 48 bit
			0111b	0111b -> 64 bit
			1000b	1000b -> 80 bit
			1001b	1001b -> 96 bit
			1010b	1010b -> 112 bit
			1011b	1011b -> 128 bit
			1100b	1100b -> 160 bit

Table 39. CLIF_TX_SYMBOL_CONFIG (0x0E) register bit description*...continued*

Bit	Symbol	Access	Value	Description
			1101b	1101b -> 192 bit
			1110b	1110b -> 224 bit
			1111b	1111b -> 256 bit
[26:26]	TX_SYMBOL1_BURST_TYPE	rw	0x0	Specifies the type of the burst of Symbol1 (logical zero / logical one)
[25:25]	TX_SYMBOL1_BURST_ONLY	rw	0x0	If set to 1. Symbol1 consists only of a burst and no symbol pattern
[24:24]	TX_SYMBOL1_BURST_ ENABLE	rw	0x0	If set to 1. the burst of Symbol0 of the length defined in bit field SYMBOL1_BURST_LEN is enabled
[23:23]	RESERVED	r-	0x0	Reserved
[22:19]	TX_SYMBOL0_BURST_LEN	rw	0x0	Specifies the number of bits issued for symbol 0 burst. The 3 bits encode a range from 8 to 256 bit length
			0000b	0000b -> 8 bit
			0001b	0001b -> 12 bit
			0010b	0010b -> 16 bit
			0011b	0011b -> 24 bit
			0100b	0100b -> 32 bit
			0101b	0101b -> 40 bit
			0110b	0110b -> 48 bit
			0111b	0111b -> 64 bit
			1000b	1000b -> 80 bit
			1001b	1001b -> 96 bit
			1010b	1010b -> 112 bit
			1011b	1011b -> 128 bit
			1100b	1100b -> 160 bit
			1101b	1101b -> 192 bit
			1110b	1110b -> 224 bit
			1111b	1111b -> 256 bit
[18:18]	TX_SYMBOL0_BURST_TYPE	rw	0x0	Specifies the type of the burst of Symbol0 (logical zero / logical one)
[17:17]	TX_SYMBOL0_BURST_ONLY	rw	0x0	If set to 1. Symbol0 consists only of a burst and no symbol pattern
[16:16]	TX_SYMBOL0_BURST_ ENABLE	rw	0x0	If set to 1. the burst of Symbol0 of the length defined in bit field SYMBOL0_BURST_LEN is enabled
[15:13]	TX_SYMBOL3_LEN	rw	0x0	Specifies the number of valid bits of the symbol definition of Symbol3. The range is from 1 bit (value 0000) to 8 bit (value 111)

Table 39. CLIF_TX_SYMBOL_CONFIG (0x0E) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[12:10]	TX_SYMBOL2_LEN	rw	0x0	Specifies the number of valid bits of the symbol definition of Symbol2. The range is from 1 bit (value 0000) to 8bit (value 111)
[9:5]	TX_SYMBOL1_LEN	rw	0x0	Specifies the number of valid bits of the symbol definition of Symbol1. The range is from 1 bit (value 0000) to 31 bits (value 11110)
[4:0]	TX_SYMBOL0_LEN	rw	0x0	Specifies the number of valid bits of the symbol definition of Symbol0. The range is from 1 bit (value 0000) to 31 bits (value 11110)

9.14.1.15 CLIF_TX_FRAME_CONFIG (0x0F)

This register provides the settings for CLIF_TX_FRAME_CONFIG

Table 40. CLIF_TX_FRAME_CONFIG (0x0F) register bit description

Bit	Symbol	Access	Value	Description
[31:19]	RESERVED	r-	0x0	Reserved
[18:16]	TX_DATA_CODE_TYPE	rw	0x0	Specifies the type of encoding of data to be used
			000b	000b -> No special code
			001b	001b -> 1 out of 4 code [I-Code SLI]
			010b	010b -> 1 out of 256 code [I-Code SLI]
			011b	011b -> Pulse interval encoding (PIE) [I-Code EPC-V2]
			100b	100b -> 2bit tupple code (intended only for test purpose)
			101b	101b -> Reserved
			110b	110b -> Reserved
			111b	111b -> Reserved
[15:13]	TX_STOPBIT_TYPE	rw	0x0	Enables the stop bit (logic 1) and extra guard time (logic 1). The value 0 disables transmission of stop-bits.
			001b	001b -> stop-bit. no EGT
			010b	010b -> stop-bit + 1 EGT
			011b	011b -> stop-bit + 2 EGT
			100b	100b -> stop-bit + 3 EGT
			101b	101b -> stop-bit + 4 EGT
			110b	110b -> stop-bit + 5 EGT
			111b	111b -> stop-bit + 6 EGT
[12:12]	TX_STARTBIT_ENABLE	rw	0x0	If set to 1. a start-bit (logic 0) will be send
[11:11]	TX_MSB_FIRST	rw	0x0	If set to 1. data bytes are interpreted MSB first for data transmission

Table 40. CLIF_TX_FRAME_CONFIG (0x0F) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[10:10]	TX_PARITY_LAST_INV_ ENABLE	rw	0x0	If set to 1. the parity bit of last sent data byte is inverted
[9:9]	TX_PARITY_TYPE	rw	0x1	Defines the type of the parity bit 0 Even Parity is calculated 1 Odd parity is calculated
[8:8]	TX_PARITY_ENABLE	rw	0x0	If set to 1. a parity bit is calculated and appended to each byte transmitted. If the Transmission Of Data Is Enabled and TX_NUM_BYTES_2_SEND is zero. then a NO_DATA_ERROR occurs.
[7:5]	RESERVED	r-	0x0	Reserved
[4:4]	TX_DATA_ENABLE	rw	0x0	If set to 1. transmission of data is enabled otherwise only symbols are transmitted.
[3:2]	TX_STOP_SYMBOL	rw	0x0	Defines which pattern symbol is sent as frame stop
			00b	00b -> No symbol pattern is sent
			01b	01b -> Symbol1 is sent
			10b	10b -> Symbol2 is sent
			11b	11b -> Symbol3 is sent
[1:0]	TX_START_SYMBOL	rw	0x0	Defines which symbol pattern is sent as frame start
			00b	00b -> No symbol pattern is sent
			01b	01b -> Symbol0 is sent
			10b	10b -> Symbol1 is sent
			11b	11b -> Symbol2 is sent

9.14.1.16 CLIF_TX_DATA_MOD (0x10)

This register provides the settings for CLIF_TX_DATA_MOD

Table 41. CLIF_TX_DATA_MOD (0x10) register bit description

Bit	Symbol	Access	Value	Description
[31:25]	RESERVED	r-	0x0	Reserved
[24:24]	TX_ICODE_DATA_MODWIDTH_ ENABLE	rw	0x0	Enables modulation width of icode data. Width of modulation is defined by the TX_DATA_MODWIDTH field. When 1, we should have TX_DATA_ENV_ TYPE=0 and TX_DATA_INV_ENV=0
[23:16]	TX_DATA_MODWIDTH	rw	0x0	Specifies the length of a pulse for sending data with miller pulse modulation enabled. The length is given by the number of carrier clocks + 1.
[15:9]	RESERVED	r-	0x0	Reserved
[8:8]	TX_DATA_MILLER_ENABLE	rw	0x0	If set to 1 pulse modulation is applied according to modified miller coding
[7:7]	TX_DATA_INV_ENV	rw	0x0	If set to 1 the output envelope is inverted
[6:4]	TX_DATA_ENV_TYPE	rw	0x0	Specifies the type of envelope used for transmission of data packets. The selected envelope type is applied to the pseudo bit stream.

Table 41. CLIF_TX_DATA_MOD (0x10) register bit description*...continued*

Bit	Symbol	Access	Value	Description
			000b	000b -> Direct output
			001b	001b -> Manchester code
			010b	010b -> Manchester code with subcarrier
			011b	011b -> BPSK
			100b	100b -> RZ (pulse of half bit length at beginning of second half of bit)
			101b	101b -> RZ(pulse of half bit length at beginning of bit)
			110b	110b -> Manchester tupple
			111b	111b -> RFU.
[3:3]	TX_DATA_SC_FREQ	rw	0x0	Specifies the frequency of the subcarrier.
			0	0: 424 kHz
			1	1: 848 kHz
[2:0]	TX_DATA_BIT_FREQ	rw	0x0	Specifies the frequency of the bit-stream.
			000b	000b -> 1.695 MHz
			001b	001b -> Reserved
			010b	010b -> 26 kHz
			011b	011b -> 53 kHz
			100b	100b -> 106 kHz
			101b	101b -> 212 kHz.
			110b	110b -> 424 kHz.
			111b	111b -> 848 kHz.

9.14.1.17 CLIF_TX_WAIT (0x11)

This register provides the settings for CLIF_TX_WAIT

Table 42. CLIF_TX_WAIT (0x11) register bit description

Bit	Symbol	Access	Value	Description
[31:28]	RESERVED	r-	0x0	Reserved
[27:8]	TX_WAIT_VALUE	rw	0x0	Defines the tx_wait timer reload value. Note: If set to 00000h the tx_wait guard time is disabled Note: This bit is set by HW a protocol is detected in automatic mode detection
[7:0]	TX_WAIT_PRESCALER	rw	0x0	Defines the prescaler reload value for the tx_wait timer. Note: This bit is set by HW a protocol is detected in automatic mode detection

9.14.1.18 CLIF_CRC_TX_CONFIG (0x12)

This register provides the settings for CLIF_CRC_TX_CONFIG

Table 43. CLIF_CRC_TX_CONFIG (0x12) register bit description

Bit	Symbol	Access	Value	Description
[31:16]	TX_CRC_PRESET_VALUE	rw	0x0	Arbitrary preset value for the Tx-Encoder CRC calculation.
[15:7]	RESERVED	r-	0x0	Reserved
[6:6]	TX_CRC_BYTE2_ENABLE	rw	0x0	If set. the CRC is calculated from the 2nd byte onwards (intended for HID). Note that this option is used in the Tx-Encoder.
[5:3]	TX_CRC_PRESET_SEL	rw	0x000	Preset value of the CRC register for the Tx-Encoder. For a CRC calculation using 5bits. only the LSByte is used.
			000b	000b -> 0000h reset value
			001b	001b -> 6363h
			010b	010b -> A671h
			011b	011b -> FFFFh
			100b	100b -> 0012h
			101b	101b -> E012h
			110b	110b -> RFU
			111b	111b -> Use arbitrary preset value TX_CRC_ PRESET_VALUE
[2:2]	TX_CRC_TYPE	rw	0x0	Controls the type of CRC calulation for the Tx-Encoder 0* 16bit CRC calculation. reset value 1 5bit CRC calculation
[1:1]	TX_CRC_INV	rw	0x0	Controls the sending of an inverted CRC value by the Tx-Encoder 0* Not inverted CRC checksum. reset value 1 Inverted CRC checksum
[0:0]	TX_CRC_ENABLE	rw	0x0	If set to one. the Tx-Encoder will compute and transmit a CRC.

9.14.1.19 CLIF_TX_UNDERSHOOT_CONFIG (0x13)

This register provides the settings for CLIF_TX_UNDERSHOOT_CONFIG

Table 44. CLIF_TX_UNDERSHOOT_CONFIG (0x13) register bit description

Bit	Symbol	Access	Value	Description
[31:16]	TX_UNDERSHOOT_PATTERN	rw	0x0	Undershoot pattern which is transmitted after each falling egde.
[15:8]	RESERVED	r-	0x0	Reserved
[7:6]	TX_EXTENDED_ TRANSMISSION	rw	0x0	Extends the transmission with envelope of continuously 1 for SL-ALM transmission in BPSK mode. Refer to (PN552-ECO-RF-02-DIG4)
[5:5]	TX_UNDERSHOOT_PROT_ LAST_SC_ENABLE	rw	0x0	This mode activates the undershoot prevention circuit only for the last sub-carrier cycle for card-mode transmission - Note: The bit TX_UNDERSHOOT_ PROT_ENABLE must not be set in this mode.

Table 44. CLIF_TX_UNDERSHOOT_CONFIG (0x13) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[4:1]	TX_UNDERSHOOT_PATTERN_LEN	rw	0x0	Defines length of the undershoot prevention pattern (value +1). The pattern is applied starting from the LSB of the defined pattern. all other bits are ignored.
[0:0]	TX_UNDERSHOOT_PROT_ENABLE	rw	0x0	If set to 1. the undershoot protection is enabled

9.14.1.20 CLIF_TX_OVERSHOOT_CONFIG (0x14)

This register provides the settings for CLIF_TX_OVERSHOOT_CONFIG

Table 45. CLIF_TX_OVERSHOOT_CONFIG (0x14) register bit description

Bit	Symbol	Access	Value	Description
[31:16]	TX_OVERSHOOT_PATTERN	rw	0x0	Overshoot pattern which is transmitted after each rising egde.
[15:5]	RESERVED	r-	0x0	Reserved
[4:1]	TX_OVERSHOOT_PATTERN_LEN	rw	0x0	Defines length of the overshoot prevention pattern (value +1). The pattern is applied starting from the LSB of the defined pattern. all other bits are ignored.
[0:0]	TX_OVERSHOOT_PROT_ENABLE	rw	0x0	If set to 1. the overshoot protection is enabled.

9.14.1.21 CLIF_SS_TX_CFG (0x15)

This register provides the settings for CLIF_SS_TX_CFG

Table 46. CLIF_SS_TX_CFG (0x15) register bit description

Bit	Symbol	Access	Value	Description
[31:14]	RESERVED	r-	0x00	Reserved
[13:13]	TX2_USE_TX1_CONF	rw	0x0	When 1, the tx1 configuration is used also for tx2: allCLIF_SS_TX2_* registers are discarded and configurations from correspondingCLIF_SS_TX1 register is used.
[12:6]	TX_FRCZERO_THR	rw	0x0A	angle below which output is set to 0. Values lower than 10 (0xa) are forbidden; they would lead to too short transmitters activations.
[5:3]	TX2_CLK_MODE_DEFAULT	rw	0x00	TX2 clk mode without field (RM and CM)
[2:0]	TX1_CLK_MODE_DEFAULT	rw	0x00	TX1 clk mode without field (RM and CM) 000,001,010,011...,111

9.14.1.22 CLIF_SS_TX1_RMCFG (0x16)

This register provides the settings for CLIF_SS_TX1_RMCFG

Table 47. CLIF_SS_TX1_RMCFG (0x16) register bit description

Bit	Symbol	Access	Value	Description
[31:25]	RESERVED	r-	0x00	Reserved
[24:22]	TX1_CLK_MODE_TRANS_RM	rw	0x00	TX1 clock mode in RM during transition

Table 47. CLIF_SS_TX1_RMCFG (0x16) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[21:19]	TX1_CLK_MODE_MOD_RM	rw	0x00	TX1 clock mode of modulated wave in RM
[18:16]	TX1_CLK_MODE_CW_RM	rw	0x00	TX1 clock mode of unmodulated wave in RM
[15:8]	TX1_AMP_MOD_RM	rw	0x00	TX1 amplitude of modulated wave in RM (0x00 = 0%modulaton, 0xFF: 100% modulation)
[7:0]	TX1_AMP_CW_RM	rw	0xFF	TX1 amplitude of unmodulated wave in RM (0x00 =0% signal, 0xFF: 100% signal)

9.14.1.23 CLIF_SS_TX2_RMCFG (0x17)

This register provides the settings for CLIF_SS_TX2_RMCFG

Table 48. CLIF_SS_TX2_RMCFG (0x17) register bit description

Bit	Symbol	Access	Value	Description
[31:25]	RESERVED	r-	0x00	Reserved
[24:22]	TX2_CLK_MODE_TRANS_RM	rw	0x00	TX2 clock mode in RM during transition
[21:19]	TX2_CLK_MODE_MOD_RM	rw	0x00	TX2 clock mode of modulated wave in RM
[18:16]	TX2_CLK_MODE_CW_RM	rw	0x00	TX2 clock mode of unmodulated wave in RM
[15:8]	TX2_AMP_MOD_RM	rw	0x00	TX2 amplitude of modulated wave in RM (0x00 = 0%modulaton, 0xFF: 100% modulation)
[7:0]	TX2_AMP_CW_RM	rw	0xFF	TX2 amplitude of unmodulated wave in RM (0x00 =0% signal, 0xFF: 100% signal)

9.14.1.24 CLIF_SS_TX_SCALE_CFG (0x18)

This register provides the settings for CLIF_SS_TX_SCALE_CFG

Table 49. CLIF_SS_TX_SCALE_CFG (0x18) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_SCALE_UPD_TIME	rw	0x00	time between scaling factor inc/decrement to reach TX2_SS_TARGET_SCALE in 8/13.56MHz multiples (0: immediate update with target value)
[23:16]	TX1_SS_SCALE_UPD_TIME	rw	0x00	time between scaling factor inc/decrement to reach TX1_SS_TARGET_SCALE in 8/13.56MHz multiples (0: immediate update with target value)
[15:8]	TX2_SS_TARGET_SCALE	rw	0xFF	TX2 scaling factor
[7:0]	TX1_SS_TARGET_SCALE	rw	0xFF	TX1 scaling factor

9.14.1.25 CLIF_SS_TX_TRANS_CFG (0x19)

This register provides the settings for CLIF_SS_TX_TRANS_CFG

Table 50. CLIF_SS_TX_TRANS_CFG (0x19) register bit description

Bit	Symbol	Access	Value	Description
[31:12]	RESERVED	r-	0	Reserved

Table 50. CLIF_SS_TX_TRANS_CFG (0x19) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[11:11]	TX2_SS_TRANS_RATE	rw	0	TX2 shaping edge rate. 1/fc should be selected for CM.
			0	0: 1/fc
			1	1: 2/fc
[10:10]	TX1_SS_TRANS_RATE	rw	0	TX2 shaping edge rate. 1/fc should be selected for CM
			0	0: 1/fc
			1	1: 2/fc
[9:5]	TX2_SS_TRANS_LENGTH	rw	0	TX2 shaping edge length: from 0 (disable) to 16. for CM, only 0 or 4 values are valid
[4:0]	TX1_SS_TRANS_LENGTH	rw	0	TX1 shaping edge length: from 0 (disable) to 16. for CM, only 0 or 4 values are valid

9.14.1.26 CLIF_ANACTRL_TX1_GSN (0x1A)

This register provides the settings for CLIF_ANACTRL_TX1_GSN

Table 51. CLIF_ANACTRL_TX1_GSN (0x1A) register bit description

Bit	Symbol	Access	Value	Description
[31:25]	RESERVED	r-	0x0	Reserved
[24:20]	GSN_DEFAULT_TX1	rw	0x0	low side transistor default conductance for tx1
[19:15]	GSN_MOD_CM_TX1	rw	0x0	low side transistor conductance in card mode, mod, for tx1
[14:10]	GSN_CW_CM_TX1	rw	0x0	low side transistor conductance in card mode, cw, for tx1
[9:5]	GSN_MOD_RM_TX1	rw	0x0	low side transistor conductance in reader mode, mod, for tx1
[4:0]	GSN_CW_RM_TX1	rw	0x0	low side transistor conductance in reader mode, cw, for tx1

9.14.1.27 CLIF_ANACTRL_TX2_GSN (0x1B)

This register provides the settings for CLIF_ANACTRL_TX2_GSN

Table 52. CLIF_ANACTRL_TX2_GSN (0x1B) register bit description

Bit	Symbol	Access	Value	Description
[31:25]	RESERVED	r-	0x0	Reserved
[24:20]	GSN_DEFAULT_TX2	rw	0x0	low side transistor default conductance for tx2
[19:15]	GSN_MOD_CM_TX2	rw	0x0	low side transistor conductance in card mode, mod, for tx2
[14:10]	GSN_CW_CM_TX2	rw	0x0	low side transistor conductance in card mode, cw, for tx2
[9:5]	GSN_MOD_RM_TX2	rw	0x0	low side transistor conductance in reader mode, mod, for tx2

Table 52. CLIF_ANACTRL_TX2_GSN (0x1B) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[4:0]	GSN_CW_RM_TX2	rw	0x0	low side transistor conductance in reader mode, cw, for tx2

9.14.1.28 CLIF_ANACTRL_TX_GSP (0x1C)

This register provides the settings for CLIF_ANACTRL_TX_GSP

Table 53. CLIF_ANACTRL_TX_GSP (0x1C) register bit description

Bit	Symbol	Access	Value	Description
[31:30]	RESERVED	r-	0x0	Reserved
[29:25]	GSP_DEFAULT_TX2	rw	0x0	high side transistor default conductance for tx2
[24:20]	GSP_DEFAULT_TX1	rw	0x0	high side transistor default conductance for tx1
[19:15]	GSP_CM_TX2	rw	0x0	high side transistor conductance in card mode for tx2
[14:10]	GSP_CM_TX1	rw	0x0	high side transistor conductance in card mode for tx1
[9:5]	GSP_RM_TX2	rw	0x0	high side transistor conductance in reader mode for tx2
[4:0]	GSP_RM_TX1	rw	0x0	high side transistor conductance in reader mode for tx1

9.14.1.29 CLIF_SIGPRO_CONFIG (0x1D)

This register provides the settings for CLIF_SIGPRO_CONFIG

Table 54. CLIF_SIGPRO_CONFIG (0x1D) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	DGRM_SOFT_RESET	rw	0	When high (1) resets the DGRM block.
[30:30]	DGRM_RESET_ON_FALSE_ALARM	rw	0	When high (1) resets the DGRM state on false alarm.
[29:28]	DGRM_MINMAX_AVG_SEL	rw	0	Defines the number of samples to average ADC I/Q min/max value: averages over 2^(DRGM_MINMAX_AVG_SEL+1) samples.
[27:26]	SIGPRO_SPARE_CTRL	rw	0	Spare Control Bits reserved for ECO and Last Minutes fixes.
[25:24]	DGRM_SPARE_CTRL	rw	0	Spare Control Bits reserved for ECO and Last Minutes fixes.
[23:23]	CM_DISABLE_BVSFELICA_PROT	rw	0	Chicken bit to disable the protection preventing typeB detection while Felica decoder is running in GTM
[22:21]	CM_GTM_TYPEA_LGTH	rw	0	Number of typeA bits required to validate typeA
[20:19]	RM_DCO_FILT_SEL	rw	0	RM_DCO_FILT_SEL
[18:8]	RESERVED	r-	0	Reserved
[7:7]	RXCTRL_ENABLE	rw	0	Enables the RXCTRL module
[6:4]	SIGPRO_BAUDRATE	rw	0	Baud-Rates: 0x00 ..
			0x00	0x00 .. 6.6kBd

Table 54. CLIF_SIGPRO_CONFIG (0x1D) register bit description*...continued*

Bit	Symbol	Access	Value	Description
			0x01	0x01 .. 26kBd
			0x02	0x02 .. 53kBd
			0x03	0x03 .. 106kBd
			0x04	0x04 .. 212kBd
			0x05	0x05 .. 424kBd
			0x06	0x06 .. 848kBd
			0x07	0x07 .. RFU
[3:1]	SIGPRO_FRAMING	rw	0	Transfer Types::: Card mode
			000	000 ->TypeA
			001	001 ->NFC
			010	010 ->Felica
			011	011 ->TypeB
			1xx	1xx ->RFU
[3:1]	SIGPRO_FRAMING	rw	0	Transfer Types: Reader mode
			000	000 ->TypeA
			001	001 ->NFC
			010	010 ->Felica
			011	011 ->TypeB
			100	100 ->ICode
			101	101 ->EPC-V2 4Manchester
			110	110 ->EPC-V2 2Manchester
			111	111 ->RFU
[0:0]	SIGPRO_MODE_SEL	rw	0	Selects between Card or Reader mode.
			0	0 -> Card mode
			1	1 ->Reader mode

9.14.1.30 CLIF_SIGPRO_RM_WAIT (0x1E)

This register provides the settings for CLIF_SIGPRO_RM_WAIT

Table 55. CLIF_SIGPRO_RM_WAIT (0x1E) register bit description

Bit	Symbol	Access	Value	Description
[31:25]	RM_NOISE_COLL_TH	rw	0x0	Noise threshold used to declare collision.
[24:20]	RM_MF_SC_TH	rw	0x00	Threshold to compare MF output inorder to detect sub-carriers in A106
[19:16]	RM_SC_CNT_RECEIVE_TH	rw	0x00	Number of sub-carriers to be received before transitioning to RECEIVE state in Type A106.
[15:8]	RM_BBA_DECR_WAIT	rw	0x00	Number of (13.56MHz/2) cycles to supperss A106 re-sync mechanism after reduction in BBA gain

Table 55. CLIF_SIGPRO_RM_WAIT (0x1E) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[7:0]	RM_HF_ATT_UPDATE_WAIT	rw	0x00	Number of (13.56MHz/2) cycles to supperss A106 SoF detection after change in HF-attenuator

9.14.1.31 CLIF_SIGPRO_RM_CONFIG (0x1F)

This register provides the settings for CLIF_SIGPRO_RM_CONFIG

Table 56. CLIF_SIGPRO_RM_CONFIG (0x1F) register bit description

Bit	Symbol	Access	Value	Description
[31:30]	RESERVED	r-	0x0	RESERVED
[29:25]	RM_PREAMBLE_SC_TRIGGER	rw	0x0	Number of sub-carrier cycles required for response detection in BPSK modulated schemes
[24:24]	RM_OOK_COL_IS_NOISE	r-	0x0	When set, treats collision as noise
[23:23]	RM_EOFMF_COND_ENABLE	rw	0x0	Enables the IS_eofmf condition to detect EOF. Used in Type A HDR decoder and Felica
[22:22]	RM_SILENT_COND_ENABLE	rw	0x0	Enables the IS_silent condition to detect EOF in Type A HDR and Felica
[21:21]	RM_BIT2BIT_VALUE_COND_ ENABLE	rw	0x0	Enables the bit-2-bit similarity figure condition to detect silence. Used for data rates higher than 106kBd.
[20:20]	RM_BIT2BIT_RATIO_COND_ ENABLE	rw	0x0	Enables the bit-2-bit similarity figure ratio condition to detect silence. Used for data rates higher than 106kBd.
[19:19]	RM_DOWNMIX_MODE	rw	0x0	Defines the down sampling mode
[18:15]	RM_EOF_2_FALSE_ALARM	rw	0x0	Defines the number of bits to differentiate false alarm from EOF. Used only in Type A 106kBd and I-Code.
[14:14]	RM_OOK_ERROR_MODE	rw	0x0	When set, data_invalid will not occur for OOK modulations
[13:12]	RM_CH_COMB_MODE_SEL	rw	0x0	Selects channel combiner mode.
[11:11]	RM_EMD_RESTART_MODE	rw	0x0	Selects emd restart mode (default 0 for direct restart)
[10:8]	RM_SILENCE_FACTOR	rw	0x0	Defines the threshold for comparing consecutive bit-to-bit similarity figures. Used in detection of silence for data rates 106kBd and lower.
[7:5]	RM_CORR_DISTANCE	rw	0x0	Defines the threshold for comparing the distance between the two correlator outputs. Used for data rates higher than 106kBd
[4:2]	RM_CORR_FACTOR	rw	0x0	Defines the threshold for comparing the matched filter. Used for data rates higher than 106kBd
[1:0]	RM_EMD_SENSITIVITY	rw	0x0	Defines the threshold for EMD.

9.14.1.32 CLIF_SIGPRO_RM_PATTERN (0x20)

This register provides the settings for CLIF_SIGPRO_RM_PATTERN

Table 57. CLIF_SIGPRO_RM_PATTERN (0x20) register bit description

Bit	Symbol	Access	Value	Description
[31:16]	RM_SYNC_PATTERN	rw	0x0	Sync pattern for Felica. LSB transmitted last
[15:15]	RM_SYNC_PATTERN_EXT4	rw	0x0	extend Felica sync pattern with 16 leading 0s
[14:14]	RM_SYNC_PATTERN_EXT2	rw	0x0	extend Felica sync pattern with 8 leading 0s
[13:13]	RM_RECEIVE_TILL_END	rw	0x0	do not stop the reception before RxDecoder sends a stop command
[12:12]	RESERVED	r-	0x0	Reserved
[11:0]	RM_SOF_PATTERN	rw	0x0	SOF pattern for Type B. LSB transmitted last or Start Byte pattern for NFC passive.

9.14.1.33 CLIF_SIGPRO_RM_ENABLES (0x21)

This register provides the settings for CLIF_SIGPRO_RM_ENABLES

Table 58. CLIF_SIGPRO_RM_ENABLES (0x21) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RM_STOP_ON_EGT_ERROR	rw	0x0	When enabled (A0 mode), Type B FSM stops on EGT error. When disabled, FSM continues reception after asserting EGT error.
[30:30]	RM_STOP_AFTER_2_ ATTEMPTS	rw	0x0	When enabled (A0 mode), A106 FSM stops after the 2nd EMD restart if the 1st EMD restart was followed by 4 or more valid bits. When disabled, A106 FSM continues to restart on EMD and false alarms.
[29:26]	RM_EOF_2_VALID_DELAY	rw	0x0	Defines the #of ETU cycles after EOF detection when valid is released. Used only in Type A 106kBd I-Code and EPC.
[25:25]	RM_SOF_COLL_DET_ENABLE	rw	0x0	Enables collision detection at SOF to declare false alarm
[24:24]	RM_UPDT_SYNCREF_ON_ CLIPPING	rw	0x0	Update sync_ref_level when ADC data is clipped
[23:23]	RM_RESET_ONLY_ON_FALSE_ ALARM	rw	0x0	Enables reset only on false alarm and not for correct frame or re-sync
[22:22]	RM_DELAY_ONLY_WAITRES	rw	0x0	In TypeB mode, when set, transition from WAITRE SDELAY to WAITSYNC is only based on delay counter. Else, the transition will be based on the MF outputs as well.
[21:21]	RM_EMD_TH_BASED_ON_ SIGNAL	rw	0x0	When high, EMD threshold = max(signal_level)/2. Else, EMD threshold is based on max_noise
[20:20]	RM_COMM_TH_TRACK_ ENABLE	rw	0x0	Enables tracking of comm threshold for A106 based on signal level
[19:19]	RM_SUP_COLL_DET_ON_ GAIN_CHG	rw	0x0	When high, suppress collision detection when BBA gain is reduced
[18:17]	RM_OOK_COL_HIGH_SLOPE	rw	0x0	EMD upper slope for the collision region
			0	0 -> Threshold of 1
			1	1 ->Threshold of 1.125
			0	0 -> Threshold of 1.25

Table 58. CLIF_SIGPRO_RM_ENABLES (0x21) register bit description*...continued*

Bit	Symbol	Access	Value	Description
			1	1 ->Threshold of 1.5
[16:15]	RM_OOK_COL_LOW_SLOPE	rw	0x0	EMD lower slope for the collision region
			0	0 -> Threshold of 1
			1	1 ->Threshold of 0.875
			0	0 ->Threshold of 0.75
			1	1 ->Threshold of 0.5
[14:8]	RM_NOISE_INVALID_TH	rw	0x0	Noise threshold used to declare invalid data.
[7:7]	RM_LMA_READ_ENABLE	rw	0x0	When set, HW updates RM_LOAD_MOD_ AMPLITUDE.
[6:6]	RM_LMA_TRACKING_ENABLE	rw	0x0	Enables load modulation amplitude tracking through the frame.
[5:5]	RM_EMD_RESET_ENABLE	rw	0x0	Enables EMD reset handling Type A 106kBd, EPC and I-Code
[4:4]	RM_SILENT_RESET_ENABLE	rw	0x0	Enables receiver reset due to silence detection
[3:3]	RM_COLLISION_DET_ENABLE	rw	0x0	Enables receiver reset due to collision detection
[2:2]	RM_FALSE_ALARM_SOF_ RESET_ENABLE	rw	0x0	Enables receiver reset due to false alarm
[1:1]	RM_RESYNC_RESET_ENABLE	rw	0x0	Enables receiver reset due to re-sync
[0:0]	RM_WDT_RESET_ENABLE	rw	0x0	Enables receiver reset when watch dog timer expires

9.14.1.34 CLIF_SIGPRO_RM_TECH (0x22)

This register provides the settings for CLIF_SIGPRO_RM_TECH

Table 59. CLIF_SIGPRO_RM_TECH (0x22) register bit description

Bit	Symbol	Access	Value	Description
[31:30]	RM_NCO_PERIOD_SEL	rw	0x0	Defines the reset value for the NCO counter
[29:27]	RM_WAIT_RES_PERIOD_SEL	rw	0x0	Defines the reset value for the Delay counter
[26:26]	RM_EGT_WINDOW_TH_SEL	rw	0x0	Defines the EGT window threshold for Type B
[25:25]	RM_DC_REMOVAL_ENABLE	rw	0x0	Reserved
[24:23]	RM_DOWNSAMPLE_RATE_SEL	rw	0x0	Defines the down sample rate for the reader demod.
[22:20]	RM_SOF_NUM_CYCLES_SEL	rw	0x0	Defines the number of samples in I-Code SOF.
[19:17]	RM_MF_SEL	rw	0x0	Defines the selection for the Matched-Filters
[16:15]	RM_MF_GAIN	rw	0x0	Defines the gain of the Matched-Filters
[14:13]	RM_MRC_WEIGHT_SEL	rw	0x0	Defines the channel combiner weight on the lower channel
[12:12]	RM_AVG_FILT_GAIN	rw	0x0	Defines the averaging filter gain
[11:10]	RM_AVG_FILT_SEL	rw	0x0	Defines the averaging filter selection
[9:8]	RM_SYNC_FILT_IN_SEL	rw	0x0	Defines the input selection for the sync filter.
[7:6]	RM_SYNC_FILT_SEL	rw	0x0	Defines the synchronization filter selection

Table 59. CLIF_SIGPRO_RM_TECH (0x22) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[5:3]	RM_WATCH_DOG_PERIOD_SEL	rw	0x0	Defines the reset value for the watch-dog counter
[2:2]	RM_EST_RESTART_ENABLE	rw	0x0	Reserved
[1:0]	RM_OOK_STAT_LEN	rw	0x3	Defines the number of samples used to check for invalid at the beginning of a reception in A106 and Icode. Value 0x0 = 2 samples, value 0x1 = 4 samples, value 0x2 = 8 samples, value 0x3 = 16 samples

9.14.1.35 CLIF_SIGPRO_NOISE_CONFIG1 (0x23)

This register provides the settings for CLIF_SIGPRO_NOISE_CONFIG1

Table 60. CLIF_SIGPRO_NOISE_CONFIG1 (0x23) register bit description

Bit	Symbol	Access	Value	Description
[31:28]	RESERVED	r-	0	Reserved
[27:25]	SIGPRO_NPD_MRC_SCALE_VALUE	rw	0	starts noise power estimation sent by FW
[24:24]	SIGPRO_NPD_START	rw	0	starts noise power estimation sent by FW
[23:23]	SIGPRO_NPD_FAST_MODE	rw	0	enables/disable fast mode
[22:22]	SIGPRO_NPD_INPUT_SEL	rw	0	selects noise power detector input
[21:16]	SIGPRO_NPD_ROUGH_WIN_SIZE	rw	0	defines noise power detector rough window length
[15:10]	SIGPRO_NPD_FINE_WIN_SIZE	rw	0	defines noise power detector fine window length
[9:7]	SIGPRO_NPD_PEAK_FACTOR	rw	0	defines noise power factor to apply on the peak noise
[6:5]	SIGPRO_NPD_PEAK_ABS_TH	rw	0	defines absolute threshold used to detect peaks
[4:3]	SIGPRO_NPD_PEAK_REL_TH	rw	0	defines relative threshold used to detect peaks
[2:1]	SIGPRO_NPD_AVG_LGTH	rw	0	defines the averaging window length used to calculate noise
[0:0]	SIGPRO_NPD_ENABLE	rw	0	enables noise power detector

9.14.1.36 CLIF_SIGPRO_NOISE_CONFIG2 (0x24)

This register provides the settings for CLIF_SIGPRO_NOISE_CONFIG2

Table 61. CLIF_SIGPRO_NOISE_CONFIG2 (0x24) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	RESERVED	r-	0	Reserved
[23:23]	SIGPRO_NPD_Q_OVR_ENABLE	rw	0	enables the overwritting of Q channel noise power value by FW
[22:22]	SIGPRO_NPD_I_OVR_ENABLE	rw	0	enables the overwritting of I channel noise power value by FW
[21:20]	SIGPRO_NPD_UPDT_COND	rw	0	update condition for the noise status register
[19:10]	SIGPRO_NPD_Q_OVR_VALUE	rw	0	Noise value for Q channel that the FW can force

Table 61. CLIF_SIGPRO_NOISE_CONFIG2 (0x24) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[9:0]	SIGPRO_NPD_I_OVR_VALUE	rw	0	Noise value for I channel that the FW can force

9.14.1.37 CLIF_RX_PROTOCOL_CONFIG (0x25)

This register provides the settings for CLIF_RX_PROTOCOL_CONFIG

Table 62. CLIF_RX_PROTOCOL_CONFIG (0x25) register bit description

Bit	Symbol	Access	Value	Description
[31:23]	RESERVED	rw	0	Reserved
[22:22]	RX_LEN_SIZE	rw	0	If the LEN field is a part of the frame format - the parameter defines the LEN field size in the frame.0: the LEN field consists of 1 byte (E.g. Felica frames). 1: the LEN field consists of 2 bytes (E.g. FWEC frames).
[21:19]	RX_EOFDET_MASK	rw	0	Bit scale which defines the permitted position of the EOF pattern in the frame. If the corresponding bit of the scale is set to 1, the EOF pattern in the corresponding position is considered. Otherwise its ignored.bit[0] - Next to stop bit position.bit[1] - Next to parity bit position.bit[2] - Next to any data bit position.
[18:15]	RX_EOF_LENGTH	rw	0	The length of the EOF pattern set in theCLIF_RX_EOF_PATTERN_REG register in 2-bits symbols units.0 - 1 symbols...15 - 16 symbols.If set to n, only N=n+1 least significant 2-bit symbols are taken from theCLIF_RX_EOF_PATTERN_REG vector for the EOF pattern detection.
[14:13]	EOC_COND_SCALE	rw	2	End of Communication (EOC) condition bit scale. If the corresponding bit of the scale is set to 1 - the condition is activated.bit[0] - EOC is detected EOF defined by the EOF_COND_SCALE register value.bit[1] - EOC is External RF-Off event. Any combination of set bits is allowed. The SGP_MSG_RXOVER_* message is hardcoded EOC condition and cant be disabled.
[12:8]	EOF_COND_SCALE	rw	10	End of Frame (EOF) condition bit scale. If the corresponding bit of the scale is set to 1 - the condition is activated.bit[0] - EOF is Data symbol pattern.bit[1] - EOF is Inverted parity.bit[2] - EOF is defined by LEN frame parameter.bit[3] - EOF is TypeA Anticollision pattern. bit[4] - EOF is communication error event. Any combination of set bits is allowed. The SGP_MSG_RXOVER_* message is hardcoded EOF condition and cant be disabled.
[7:7]	RX_MSB_FIRST	rw	0	If set to 1, the first received bit is MSB in the frame character. Otherwise its LSB.
[6:6]	VALUES_AFTER_COLLISION	rw	0	If set to 0, every received bit after a collision is replaced by a zero (needed for TypeA Anticollision procedure).if set to 1 - the bits keep their values. The collision bit is always replaced by 1 for both settings.

Table 62. CLIF_RX_PROTOCOL_CONFIG (0x25) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[5:3]	RX_BIT_ALIGN	rw	0	Defines the position of the 1st received data bit in the formed data byte.000b - 0 position...111b - 7th position
[2:2]	RX_PARITY_TYPE	rw	1	0 - data + parity bits contain even number of 1. 1 - data + parity bits contain odd number of 1. Valid if cfg_rx_parity_enable_i ==1.
[1:1]	RX_PARITY_ENABLE	rw	0	If set to 1, the bit following last data bit in the frame character is considered as parity bit.
[0:0]	RX_STOPBIT_ENABLE	rw	0	if set to 1, a stopbit is a part of the input frame character.

9.14.1.38 CLIF_RX_FRAME_LENGTH (0x26)

This register provides the settings for CLIF_RX_FRAME_LENGTH

Table 63. CLIF_RX_FRAME_LENGTH (0x26) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0	Reserved
[30:16]	RX_FRAME_MAXLEN	rw	7FFF	Maximal number of received [DATA + CRC] bits in theframe. The violation of the maximum length limit can be also configured as an Error/EMD condition. If the max length violation is configured as error - the frame reception is stopped in case of maximum length limit exceeding. Otherwise the reception is continued.0x0000 - 1 bit...0x7FFF - 32K bits
[15:15]	RESERVED	r-	0	Reserved
[14:0]	RX_FRAME_MINLEN	rw	3	Minimal number of received [DATA + CRC] bits in the frame. The violation of the minimum length limit can be also configured as an Error/EMD condition.The parameter also defines the number of received[DATA + CRC] bits before which any of the EOF pattern or INVPAR stop condition events are ignored.0x0000 - 1 bit...0x7FFF - 32K bits

9.14.1.39 CLIF_RX_ERROR_CONFIG (0x27)

This register provides the settings for CLIF_RX_ERROR_CONFIG

Table 64. CLIF_RX_ERROR_CONFIG (0x27) register bit description

Bit	Symbol	Access	Value	Description
[31:14]	RESERVED	r-	0	Reserved
[13:13]	RX_NO_STOP_COND_IS_ ERROR	rw	1	If asserted and:1) The frame reception is over and was not interrupted by any detected protocol/data integrity error or external rf-off event AND 2) No any stop conditions, configured via EOF_COND_SCALE register, were detected. The scenario is considered as communication error. If the frame reception was interrupted by Rxdecoder or if any of the configured

Table 64. CLIF_RX_ERROR_CONFIG (0x27) register bit description*...continued*

Bit	Symbol	Access	Value	Description
				stop conditions is detected - the no stop conditions error is not asserted.
[12:12]	RX_CRC_ERROR_IS_ERROR	rw	1	If asserted, the detection of the CRC error is considered as communication error. Otherwise its ignored and just reported to the FW.
[11:11]	RX_NOT_FULL_BYTE_IS_ERROR	rw	0	If asserted, the reception of last byte with size 8 data bits is considered as communication error.
[10:10]	RX_MISSING_PARITY_IS_ERROR	rw	0	If asserted and the parity bit is a part of the frame character, the reception of the last character with 8 data bits but without parity bit is considered as communication error.
[9:9]	RX_MISSING_STOPBIT_IS_ERROR	rw	0	If asserted and the stop bit is a part of the frame character, the reception of the last character with 8 data bits but without stop bit is considered as communication error.
[8:8]	RX_LEN_ERROR_IS_ERROR	rw	1	If asserted and the LEN field is a part of the frame, the wrong received value in the field is considered as communication error.
[7:7]	RX_MINLEN_FRAME_VIOL_IS_ERROR	rw	0	If asserted and the received frame length violates the min frame length configured via the RX_RX_FRAME_MINLEN register - the event is considered as communication error.
[6:6]	RX_MAXLEN_FRAME_VIOL_IS_ERROR	rw	1	If asserted and the received frame length violates the max frame length configured via the RX_RX_FRAME_MAXLEN register - the event is considered as communication error. The Rxdecoder is always stopped on max length violation.
[5:5]	RX_SIGPRO_ERR_IS_ERROR	rw	1	If asserted and either SGP_MSG_RXOVER_ERROR or SGP_MSG_ERROR message is received - the event is considered as communication error.
[4:4]	RX_PARBIT_ERR_IS_ERROR	rw	1	If asserted, the detected parity error is considered as communication error.
[3:3]	RX_STOPBIT_ERR_IS_ERROR	rw	1	If asserted, the detected stop bit error (0 level instead of 1) is considered as communication error.
[2:2]	RX_COLL_PARBIT_IS_ERROR	rw	0	If asserted, the collision detected on parity bit position is considered as communication error.
[1:1]	RX_COLL_STOPBIT_IS_ERROR	rw	0	If asserted, the collision detected on stop bit position is considered as communication error.
[0:0]	RX_COLL_DATA_IS_ERROR	rw	0	If asserted, the collision detected on any data bit position is considered as communication error.

9.14.1.40 CLIF_RXCTRL_STATUS (0x28)

This register provides the settings for CLIF_RXCTRL_STATUS

Table 65. CLIF_RXCTRL_STATUS (0x28) register bit description

Bit	Symbol	Access	Value	Description
[31:29]	RESERVED	r-	0x0	Reserved

Table 65. CLIF_RXCTRL_STATUS (0x28) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[28:19]	RXCTRL_DCO_DAC_Q_CTRL	r-	0x0	DCO dac value for Q channel
[18:9]	RXCTRL_DCO_DAC_I_CTRL	r-	0x0	DCO dac value for I channel
[8:3]	RXCTRL_HF_ATT_VAL	r-	0x0	HF attenuator value
[2:0]	RXCTRL_BBA_CTRL	r-	0x0	BBA value

9.14.1.41 CLIF_SIGPRO_IIR_CONFIG1 (0x29)

This register provides the settings for CLIF_SIGPRO_IIR_CONFIG1

Table 66. CLIF_SIGPRO_IIR_CONFIG1 (0x29) register bit description

Bit	Symbol	Access	Value	Description
[31:28]	RESERVED	r-	0x0	Reserved
[27:27]	IIR_SIGN_B3	rw	0x0	IIR B3 sign
[26:21]	IIR_COEF_B3	rw	0x0	IIR B3 coef (unsigned, MSB unused) Value is coded value/32
[20:20]	IIR_SIGN_B2	rw	0x0	IIR B2 sign
[19:14]	IIR_COEF_B2	rw	0x0	IIR B2 coef (unsigned, MSB unused) Value is coded value/32
[13:13]	IIR_SIGN_B1	rw	0x0	IIR B1 sign
[12:7]	IIR_COEF_B1	rw	0x0	IIR B1 coef (unsigned, MSB unused) Value is coded value/32
[6:6]	IIR_SIGN_B0	rw	0x0	IIR B0 sign
[5:0]	IIR_COEF_B0	rw	0x0	IIR B0 coef (unsigned, MSB unused) Value is coded value/32

9.14.1.42 CLIF_SIGPRO_IIR_CONFIG0 (0x2A)

This register provides the settings for CLIF_SIGPRO_IIR_CONFIG0

Table 67. CLIF_SIGPRO_IIR_CONFIG0 (0x2A) register bit description

Bit	Symbol	Access	Value	Description
[31:20]	RESERVED	r-	0x0	Reserved
[19:19]	IIR_SIGN_A2	rw	0x0	IIR A1 sign
[18:12]	IIR_COEF_A2	rw	0x0	IIR A1 coef (unsigned, MSB unused) Value is coded value/64
[11:11]	IIR_SIGN_A1	rw	0x0	IIR A0 sign
[10:4]	IIR_COEF_A1	rw	0x0	IIR A0 coef (unsigned, MSB unused) Value is coded value/64
[3:1]	IIR_GAIN	rw	0x0	IIR filter gain
[0:0]	IIR_ENABLE	rw	0x0	Enable the IIR filter

9.14.1.43 CLIF_DGRM_DAC_FILTER (0x2B)

This register provides the settings for CLIF_DGRM_DAC_FILTER

Table 68. CLIF_DGRM_DAC_FILTER (0x2B) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	RESERVED	r-	0x0	Reserved
[23:22]	DGRM_CLIP_AMP_TH	rw	0x0	defines the clipping level
[21:15]	DGRM_CLIP_DET_TH	r-	0x0	defines the number of clipping signal required to generate clip_det_o
[14:14]	DGRM_CLIP_WIN_SIZE	rw	0x0	defines the monitoring window length
[13:13]	DGRM_DOUBLE_MEAN_LGTH_WINDOW	rw	0x0	Doubles the window length used to calculate the mean value. This must never be set for Icode 6kBd.
[12:12]	DGRM_DC_STEP_CANCEL_OFF	rw	0x0	disable the dc step cancelation mechanism. To be set if IIR filter is used
[11:11]	DGRM_DC_STEP_CANCEL_RATE	rw	0x0	DGRM_DC_STEP_CANCEL_RATE
			0	0: DC cancel step is reduced by 1 each clock cycle
			1	1: DC cancel step is reduced by 2 each clock cycle
[10:10]	DGRM_DC_STEP_CANCEL_MODE	rw	0x0	DGRM_DC_STEP_CANCEL_MODE
			0	0: DC cancel step is initialized to step in ADC data
			1	1: DC cancel step is initialized to half of step in ADC data
[9:8]	DGRM_HF_ATT_SLOW_ADJ_SEL	rw	0x0	Defines HF-ATT index increment during slow mode
[7:7]	DGRM_HT_ATT_QUICK_ADJ_ENABLE	rw	0x0	Enables setting of HF-attenuator to its max. value when RSSI is above a maximum threshold
[6:4]	DGRM_DCO_TRACK_MAX_ITER	rw	0x0	Defines the maximum number of iterations in the SET_DCO_DAC state in TRACK MODE
[3:3]	DGRM_DCO_TRACK_MAX_ITER_SEL	rw	0x0	When high, DGRM_DCO_TRACK_MAX_ITER gives the maximum number of iterations in the SET_DCO_DAC state in TRACK mode. When low, DGRM_DCO_MAX_ITER_SEL is used
[2:2]	DGRM_FINE_DAC_FILTER_K2	rw	0x0	Defines K2 of the frequency response of the filter for the Fine DAC control.
[1:0]	DGRM_FINE_DAC_FILTER_K1	rw	0x0	Defines K1 of the frequency response of the filter for the Fine DAC control.
			0	0 -> K1=2
			1	1 -> K1=4
			2	2 -> K1=8
			3	3 -> Reserved

9.14.1.44 CLIF_DGRM_CONFIG (0x2C)

This register provides the settings for CLIF_DGRM_CONFIG

Table 69. CLIF_DGRM_CONFIG (0x2C) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	DGRM_STATISTICS_READ_ENABLE	rw	0x0	When set, HW updates DGRM_MEAN_I, DGRM_SWING_I, DGRM_MEAN_Q and DGRM_SWING_Q.
[30:30]	DGRM_MEASURE_ENABLE	rw	0x0	Enables measurement of statistics (swing, mean) of both channels
[29:29]	DGRM_GAIN_SHIFT_OVR	rw	0x0	Enables the override of digital gain shift. Override value is set based on DGRM_GAIN_SHIFT_OVR_VAL
[28:26]	DGRM_GAIN_SHIFT_OVR_VAL	rw	0x0	Defines the override value for digital gain shift when DGRM_GAIN_SHIFT_OVR is set
[25:25]	DGRM_DCO_STEP_OVR	rw	0x0	Enables override of DC step cancellation signal. Override value is set based on DGRM_DCO_STEP_OVR_VAL
[24:24]	DGRM_TRACK_AFTER_FRAME_ENABLE	rw	0x0	Sets the HF-attenuator after frame
[23:23]	DGRM_TRACK_DURING_FRAME_ENABLE	rw	0x0	Enables the BBA gain and DCO tracking during frame
[22:22]	DGRM_TRACK_BEFORE_FRAME_ENABLE	rw	0x0	Enables the HF-attenuator and DCO tracking before frame
[21:18]	DGRM_SNR_LIM_DB	rw	0x0	Scales noise power estimate
[17:15]	DGRM_SNR_LIM_INF	rw	0x0	Used to set signal threshold when noise power estimate is zero
[14:13]	DGRM_DCO_TRACK_TH_SEL	rw	0x0	Defines the DCO threshold for tracking during card response
[12:10]	DGRM_DCO_STEP_DELAY	rw	0x0	Defines the delay for the DC step cancellation
[9:0]	DGRM_DCO_STEP_OVR_VAL	rw	0x0	Defines the override value for the digital DC step when DGRM_DCO_STEP_OVR is set

9.14.1.45 CLIF_DGRM_BBA (0x2D)

This register provides the settings for CLIF_DGRM_BBA

Table 70. CLIF_DGRM_BBA (0x2D) register bit description

Bit	Symbol	Access	Value	Description
[31:30]	DGRM_FALSE_ALARM_WAIT	rw	0x0	False alarm wait in multiples of 256 cycles
[29:29]	DGRM_BBA_FAST_MODE_ENABLE	rw	0x0	Enables the BBA fast mode
[28:26]	DGRM_GAIN_SHIFT_DELAY	rw	0x0	Defines the delay for digital gain compensation to match the latency from BBA gain
[25:24]	DGRM_BBA_TH_SEL	rw	0x0	Defines the threshold for the max absolute ADC value
[23:22]	DGRM_MAX_SWING_TH_SEL	rw	0x0	Defines the maximum swing threshold for decreasing BBA gain
[21:20]	DGRM_MIN_SWING_TH_SEL	rw	0x0	Defines the minimum swing threshold for increasing BBA gain

Table 70. CLIF_DGRM_BBA (0x2D) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[19:18]	DGRM_WATER_LEVEL_TH_SEL	rw	0x0	Defines the water level threshold
[17:17]	RESERVED	rw	0x0	RESERVED
[16:14]	DGRM_BBA_MIN_VAL	rw	0x0	Defines the minimum value of BBA gain.
[13:11]	DGRM_BBA_MAX_VAL	rw	0x0	Defines the maximum value of BBA gain.
[10:8]	DGRM_BBA_INIT_VAL	rw	0x0	Defines initial value of BBA gain. If BBA fast and slow modes are disabled, this value defines the forced value.
[7:7]	DGRM_GUESS_BBA_GAIN_ENABLE	rw	0x0	Enables the initial guess of BBA gain based on noise power estimate
[5:5]	DGRM_NOISE_POWER_EST_ENABLE	rw	0x0	Enables the noise power estimator in free running mode
[4:2]	DGRM_NOISE_POWER_SHIFT_VAL	rw	0x0	Defines the number of bits to shift right in order to scale the noise power. This is in addition to the scaling due to accumulation
[1:0]	RESERVED	r-	0x0	Reserved

9.14.1.46 CLIF_DGRM_DCO (0x2E)

This register provides the settings for CLIF_DGRM_DCO

Table 71. CLIF_DGRM_DCO (0x2E) register bit description

Bit	Symbol	Access	Value	Description
[31:30]	DGRM_DCO_TRACK_AVG_LEN_SEL	rw	0x0	Defines the number of ADC samples to average during TRACK mode
[29:28]	DGRM_DCO_INIT_AVG_LEN_SEL	rw	0x0	Defines the number of ADC samples to average during INIT mode
[27:26]	DGRM_DCO_WAIT_PERIOD_SEL	rw	0x0	Defines the wait period after DCO DAC update and before estimating DCO
[25:24]	DGRM_DCO_TH_SEL	rw	0x0	Defines the DCO DAC threshold
[23:22]	DGRM_DCO_MAX_ITER_SEL	rw	0x0	Defines the maximum number of iterations in DCO DAC fast mode
[21:21]	DGRM_DCO_DAC_SLOW_MODE_ENABLE	rw	0x0	Enables DCO DAC slow mode before card response.
[20:20]	DGRM_DCO_DAC_FAST_MODE_ENABLE	rw	0x0	Enables DCO DAC fast mode
[19:10]	DGRM_DCO_DAC_Q_INIT_VAL	rw	0x0	Defines the initial value of the composite DAC for the Q channel. This is also the forced value if DCO DAC fast and slow modes are disabled. The 5 MSBs control the coarse DAC and the 5 MSBs control the fine DAC.
[9:0]	DGRM_DCO_DAC_I_INIT_VAL	rw	0x0	Defines the initial value of the composite DAC for the I channel. This is also the forced value if DCO DAC fast and slow modes are disabled. The 5 MSBs control the coarse DAC and the 5 MSBs control the fine DAC.

9.14.1.47 CLIF_DGRM_HF_ATT (0x2F)

This register provides the settings for CLIF_DGRM_HF_ATT

Table 72. CLIF_DGRM_HF_ATT (0x2F) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	DGRM_MINMAX_AVG_COUNT_FORCE	rw	0x0	Forces number of min or max samples to be averaged to 16.
[30:30]	DGRM_HF_ATT_FREEZE_ENABLE	rw	0x0	Enable HF attenuator freeze based on tx_active, miller bit-grid and signal_detection.
[29:23]	DGRM_MILLER_BG_HIGH_FREEZE_TH	rw	0x0	Defines the upper threshold of Miller bit-grid value to freeze HF-attenuator.
[22:16]	DGRM_MILLER_BG_LOW_FREEZE_TH	rw	0x0	Defines the lower threshold of Miller bit-grid value to freeze HF-attenuator.
[15:14]	DGRM_HF_ATT_MAX_ITER_SEL	rw	0x0	Defines the maximum number of iterations in HF-attenuator fast mode
[13:8]	DGRM_HF_ATT_MAX_VAL	rw	0x0	Maximum value of HF-attenuator.
[7:2]	DGRM_HF_ATT_INIT_VAL	rw	0x0	Initial value of HF-attenuator. This value will also be used as the forced value when fast mode is disabled.
[1:1]	DGRM_HF_ATT_SLOW_MODE_ENABLE	rw	0x0	Enables HF-attenuator slow regulation mode
[0:0]	DGRM_HF_ATT_FAST_MODE_ENABLE	rw	0x0	Enables HF-attenuator fast settling mode

9.14.1.48 CLIF_DGRM_RSSI (0x30)

This register provides the settings for CLIF_DGRM_RSSI

Table 73. CLIF_DGRM_RSSI (0x30) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	DGRM_DEMOD_EN_FORCE	rw	0x0	When set, forces demod_enable high
[30:30]	DGRM_NUM_GAIN_UPDT_FORCE	rw	0x0	When set, forces dgrm_num_gain_updt to be zero
[29:29]	DGRM_SIGNAL_DETECT_TH_OVR	rw	0x0	Enables the override of signal detect threshold. Override value is set based on DGRM_SIGNAL_DETECT_TH_OVR_VAL.
[28:27]	DGRM_RSSI_TRACK_AVG_LEN_SEL	rw	0x0	Defines the number of RSSI samples to average during track mode
[26:25]	DGRM_RSSI_INIT_AVG_LEN_SEL	rw	0x0	Defines the number of RSSI samples to average during INIT mode
[24:23]	DGRM_RSSI_WAIT_PERIOD	rw	0x0	Defines the number of RSSI samples to discard before averaging
[22:17]	DGRM_RSSI_HYST	rw	0x0	Hysteresis value for RSSI target
[16:7]	DGRM_RSSI_TARGET	rw	0x0	RSSI target value
[6:0]	DGRM_SIGNAL_DETECT_TH_OVR_VAL	rw	0x0	Defines the override value for signal detect threshold. when DGRM_SIGNAL_DETECT_TH_OVR is set. These bits are modified dynamically by the ARC algorithm based on the DPC voltage.Only if the ARC

Table 73. CLIF_DGRM_RSSI (0x30) register bit description*...continued*

Bit	Symbol	Access	Value	Description
				is disabled, the value written during LOAD_RF_CONFIGURATION(0x0D) is retained throughout the RF Field session

9.14.1.49 CLIF_CRC_RX_CONFIG (0x31)

This register provides the settings for CLIF_CRC_RX_CONFIG

Table 74. CLIF_CRC_RX_CONFIG (0x31) register bit description

Bit	Symbol	Access	Value	Description
[31:16]	RX_CRC_PRESET_VALUE	rw	0x0	Arbitrary preset value for the Rx-Decoder CRC calculation.
[15:8]	RESERVED	r-	0x0	Reserved
[7:7]	RX_FORCE_CRC_WRITE	rw	0x0	If set. the Rx-Decoder will send to the RAM the CRC bits as well.
[6:6]	RX_CRC_ALLOW_BITS	rw	0x0	If activated the frame with length less than or equal CRC_length will be always sent to the System RAM as is, without CRC bits removal.
[5:3]	RX_CRC_PRESET_SEL	rw	0x000	Preset value of the CRC register for the Rx-Decoder. For a CRC calculation using 5bits only the LSByte is used.
			000b	000b -> 0000h reset value Note that this configuration is set by the Mode detector for FeliCa.
			001b	001b -> 6363h Note that this configuration is set by the Mode detector for ISO14443 type A.
			010b	010b -> A671h
			011b	011b -> FFFFh Note that this configuration is set by the Mode detector for ISO14443 type B
			100b	100b -> 0012h
			101b	101b -> E012h
			110b	110b -> RFU
			111b	111b -> Use arbitrary preset value RX_CRC_PRESET_VALUE
[2:2]	RX_CRC_TYPE	rw	0x0	Controls the type of CRC calculation for the Rx-Decoder 0* 16bit CRC calc
[1:1]	RX_CRC_INV	rw	0x0	Controls the comparison of the CRC checksum for the Rx-Decoder 0* Not inverted CRC value: 0000h reset value Note that this nit is cleared by the Mode detector for ISO14443 type A and FeliCa. 1 Inverted CRC value: F0B8h Note that this bit is set by the Mode detector for ISO14443 type B.
[0:0]	RX_CRC_ENABLE	rw	0x0	If set. the Rx-Decoder will check the CRC for correctness.Note that this bit is set by the Mode Detector when ISO14443 type B. or FeliCa (212 kBd or 424 kBd) is detected.

9.14.1.50 CLIF_RX_WAIT (0x32)

This register provides the settings for CLIF_RX_WAIT

Table 75. CLIF_RX_WAIT (0x32) register bit description

Bit	Symbol	Access	Value	Description
[31:28]	RESERVED	r-	0x0	Reserved
[27:8]	RX_WAIT_VALUE	rw	0x0	Defines the rx_wait timer reload value. Note: If set to 00000h the rx_wait guard time is disabled
[7:0]	RX_WAIT_PRESCALER	rw	0x0	Defines the prescaler reload value for the rx_wait timer.

9.14.1.51 CLIF_DCOC_CONFIG (0x33)

This register provides the settings for CLIF_DCOC_CONFIG

Table 76. CLIF_DCOC_CONFIG (0x33) register bit description

Bit	Symbol	Access	Value	Description
[31:22]	RESERVED	r-	0x0	RESERVED
[21:21]	DCOC_CAL_DONE_FORCE	rw	0x0	forces the signal dcoc_cal_done to 1
[20:20]	DCOC_AVERAGE_EN	rw	0x0	enables the averaging of the adc_data in the dcoc module
[19:14]	DCOC_ADD_OFFSET_Q	rw	0x0	additional offset added on Q channel (signed)
[13:8]	DCOC_ADD_OFFSET_I	rw	0x0	additional offset added on I channel (signed)
[7:4]	DCOC_TIME_DELAY	rw	0xF	Number of clock cycles given to the analog to settle after a dco calibration process
[3:3]	DCOC_START_CAL_RX_WAIT	rw	0x0	signal to start the calibration when the transceiver enters WAIT_RECEIVE state.
[1:1]	DCOC_START_CAL_NOW	rw	0x0	signal to start the calibration, can be cleared by HW.
[0:0]	DCOC_FSM_BYP	rw	0x0	Bypass the DCO FSM

9.14.1.52 CLIF_RXM_NFCLD_LVL (0x34)

This register provides the settings for CLIF_RXM_NFCLD_LVL

Table 77. CLIF_RXM_NFCLD_LVL (0x34) register bit description

Bit	Symbol	Access	Value	Description
[31:30]	RESERVED	r-	0x00	reserved
[29:16]	RXM_NFCLD_OFF_TH	rw	0x0033	RSSI OFF threshold
[15:14]	RESERVED	r-	0x00	reserved
[13:0]	RXM_NFCLD_ON_TH	rw	0x0066	RSSI ON threshold

9.14.1.53 CLIF_RXM_CTRL (0x35)

This register provides the settings for CLIF_RXM_CTRL

Table 78. CLIF_RXM_CTRL (0x35) register bit description

Bit	Symbol	Access	Value	Description
[31:26]	RESERVED	r-	0x00	reserved
[25:25]	RXM_AVRG_REQ	rw	0x0	1: run averaging of I and Q. Is reset by HW when averaging is complete. Resulting data are stored in RXM_AVRG register.
[24:24]	RXM_FORCE_NFCLDDET	rw	0x0	Forces nfcld_det_o to RXM_FORCE_NFCLDDET_VALUE.
[23:23]	RXM_FORCE_NFCLDDET_VALUE	rw	0x0	Value to force nfcld_det_o to when RXM_FORCE_NFCLDDET=1.
[22:22]	RXM_HFATT_ENABLE	rw	0x1	When 0, HF attenuation not considered for field detection When 1, consider field ON when HF attenuation is not 0
[21:17]	RXM_MAX_PHASE_DIFF	rw	0x02	maximum difference between 2 consecutive phase (bit) mesured at 1.7MHz rate. In 13.56MHz/512 multiples.when exeeded, frequency is concidered as not valid.
[16:14]	RXM_GAIN_MASK_TIME	rw	0x2	RSSI masking time after BBA gain or HFAtt changes (in 8/13,56MHz multiples)
[13:11]	RXM_RFOFF_MASK_TIME	rw	0x1	RSSI masking time after RF switched off (in 256/13,56MHz multiples)
[10:8]	RXM_RXOFF_MASK_TIME	rw	0x1	RSSI masking time after RX (in 256/13,56MHz multiples)
[7:5]	RXM_TXOFF_MASK_TIME	rw	0x1	RSSI masking time after TX (in 256/13,56MHz multiples)
[4:4]	RXM_TX_MASK_ENABLE	rw	0x1	enable frequency masking during transmission
[3:3]	RXM_RX_MASK_ENABLE	rw	0x1	enable frequency masking during reception
[2:2]	RXM_FRQ_CHECK_PCRM_ENABLE	rw	0x1	enable frequency check from pcrm
[1:1]	RXM_FRQ_CHECK_CORDIC_ENABLE	rw	0x1	enable precise frequency check from cordic phase (+/- 1.7MHz multiples)
[0:0]	RXM_ENABLE	rw	0x0	enable the all RxMeasure module.

9.14.1.54 CLIF_ANA_AGC_DCO_CTRL (0x36)

This register provides the settings for CLIF_ANA_AGC_DCO_CTRL

Table 79. CLIF_ANA_AGC_DCO_CTRL (0x36) register bit description

Bit	Symbol	Access	Value	Description
[31:26]	RESERVED	r-	0x00	reserved
[25:25]	RX_DC_CAL_EN	rw	0x00	Enable signal for RX DC calibration
[24:24]	RX_DCO_C_EN	rw	0x00	Enable signal for the DCO coarse DAC
[23:14]	RX_DCO_DAC_Q	rw	0x00	DCO DAC input control
[13:4]	RX_DCO_DAC_I	rw	0x00	DCO DAC input control
[3:3]	RX_DCO_F_EN	rw	0x00	enable signal for the DCO fine DAC

Table 79. CLIF_ANA_AGC_DCO_CTRL (0x36) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[2:0]	RESERVED	r-	0x00	reserved

9.14.1.55 CLIF_SIGPRO_CM_CONFIG (0x37)

This register provides the settings for CLIF_SIGPRO_CM_CONFIG

Table 80. CLIF_SIGPRO_CM_CONFIG (0x37) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	CM_LONG_BPRIME_ENABLE	rw	0x0	0 (default) bprime sof window has max value. 1: no max values
[30:30]	CM_SINGLE_THLD_ENABLE	rw	0x0	0 (default) to use 2 thresholds in the filters. 1 to only use 1 threshold
[29:29]	CM_INT_FILT_RESET_ENABLE	rw	0x0	0 (default) disables internal filter reset after error detection. 1 to enable it.
[28:28]	CM_EGT_CHECK	rw	0x1	enable check and error generation for EGT in TypeB
[27:27]	CM_GTM_ON	rw	0x1	enable general target mode detection
[26:26]	CM_ENABLE_GTM_A	rw	0x1	Enables TypeA detection in General Target Mode
[25:25]	CM_ENABLE_GTM_B	rw	0x1	Enables TypeB detection in General Target Mode
[24:24]	CM_ENABLE_GTM_F2	rw	0x1	Enables Felica212 detection in General Target Mode
[23:23]	CM_ENABLE_GTM_F4	rw	0x1	Enables Felica424 detection in General Target Mode
[22:22]	CM_TYPEF2_EXT_SYNC	rw	0x1	CM_TYPEF2_EXT_SYNC
[21:21]	CM_TYPEF4_EXT_SYNC	rw	0x0	change sync pattern from b24d to 0000b24d
[20:19]	CM_TYPEF2_WIN_LGTH	rw	0x0	Controls the length of the bitgrid window in the f212 decoder
[18:17]	CM_TYPEF4_WIN_LGTH	rw	0x0	Controls the length of the bitgrid window in the f424 decoder
[16:15]	CM_TYPEA_GCHANGE_DLY	rw	0x0	Programs the delay to authorize gain change during reception in the typeA decoder
[14:13]	CM_TYPEB_GCHANGE_DLY	rw	0x0	Programs the delay to authorize gain change during reception in the typeB decoder
[12:11]	CM_TYPEF2_GCHANGE_DLY	rw	0x0	Programs the delay to authorize gain change during reception in the f212 decoder
[10:9]	CM_TYPEF4_GCHANGE_DLY	rw	0x0	Programs the delay to authorize gain change during reception in the f2424 decoder
[8:5]	CM_FDT_THLD	rw	0x0	frame delay time fix threshold value
[4:1]	CM_FDT_AUTO_INIT_THLD	rw	0x0	frame delay time initial threshold value for automatic mode
[0:0]	CM_FDT_AUTO_ENABLE	rw	0x1	enable automatic threshold mode for frame delay time

9.14.1.56 CLIF_GCM_CONFIG2 (0x38)

This register provides the settings for CLIF_GCM_CONFIG2

Table 81. CLIF_GCM_CONFIG2 (0x38) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	RESERVED	r-	0x0	Reserved
[23:21]	GCM_TX_RELEASE_DLY	rw	0x0	Extends the tx_active signal received at the end of a transmission with DECIMAL(GCM_TX_RELEASE_DLY)*16 RF cycles.
[20:18]	GCM_TX_ENV_DLY	rw	0x0	GCM_TX_ENV_DLY
[17:15]	GCM_BBA_TX_VAL	rw	0x4	BBA value during transmit. Only values in the range [0:4] are allowed. Values in the range [5:7] are RFU.
[14:12]	GCM_BBA_INIT_EXT_VAL	rw	0x4	BBA start-up value on external field. Only values in the range [0:4] are allowed. Values in the range [5:7] are RFU.
[11:9]	GCM_BBA_INIT_INT_VAL	rw	0x4	BBA start-up value on internal field. Only values in the range [0:4] are allowed. Values in the range [5:7] are RFU.
[8:6]	GCM_BBA_MIN_VAL	rw	0x0	BBA minimal value. Only values in the range [0:4] are allowed. Values in the range [5:7] are RFU.
[5:3]	GCM_BBA_MAX_VAL	rw	0x4	BBA maximal value. Only values in the range [0:4] are allowed. Values in the range [5:7] are RFU.
[2:0]	Reserved	rw	0x0	0

9.14.1.57 CLIF_GCM_CONFIG1 (0x39)

This register provides the settings for CLIF_GCM_CONFIG1

Table 82. CLIF_GCM_CONFIG1 (0x39) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x0	Reserved
[30:30]	GCM_RF_OFF_ENABLE	rw	0x0	allows regulation in IDLE state
[29:24]	GCM_HF_ATT_TX_VAL	rw	0x0	HF_ATT value on Transmission
[23:18]	GCM_HF_ATT_INIT_EXT_VAL	rw	0x0	HF_ATT startup value
[17:12]	GCM_HF_ATT_INIT_INT_VAL	rw	0x0	HF_ATT startup value
[5:0]	GCM_HF_ATT_MAX_VAL	rw	0x0	HF_ATT maximal value

9.14.1.58 CLIF_GCM_CONFIG0 (0x3A)

This register provides the settings for CLIF_GCM_CONFIG0

Table 83. CLIF_GCM_CONFIG0 (0x3A) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	GCM_FREEZE_TX_WAIT_27_DLY	rw	0x0	Adds a clk27 delay before taking tx_env = 0 into account.
[30:24]	GCM_FREEZE_TX_WAIT	rw	0x0	Number of clk13 cycles before taking tx_env = 0 into account during transmission
[23:21]	GCM_MAG_HIGH_THLD	rw	0x6	High threshold value. Threshold value is (MAG_HIGH_THLD+1)*64

Table 83. CLIF_GCM_CONFIG0 (0x3A) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[20:18]	GCM_MAG_LOW_THLD	rw	0x4	Low threshold value. Threshold value is (MAG_LOW_THLD+1)*32
[17:15]	GCM_MAG_OFF_THLD	rw	0x0	Off threshold value. Threshold value is MAG_OFF_THLD*4. A value of 0 disables the off level detection.
[14:14]	GCM_MAG_OFF_FAST	rw	0x0	enables immediate reset of the gains upon field off detection
[13:12]	GCM_AVG_LENGTH	rw	0x3	length of the average window. length is 2^(AVG_LENGTH+2)
[11:11]	GCM_FAST_MODE_ENABLE	rw	0x1	enable/disable fast mode
[10:10]	GCM_FAST_MODE_RFON_INT	rw	0x0	enable/disable forced fast mode at startup on RFON internal event
[9:9]	GCM_FAST_MODE_RFON_EXT	rw	0x0	enable/disable forced fast mode at startup on RFON external event
[8:8]	GCM_RX_CHANGE_ENABLE	rw	0x1	enable gain change during reception
[7:6]	GCM_FREEZE_TX_MODE	rw	0x0	controls the switching value used during transmission envelop pattern
[5:5]	GCM_FREEZE_TX_SWITCH_VAL	rw	0x1	freeze gain during transmission
[4:4]	GCM_MAX_TXRFOFF_ENABLE	rw	0x1	force max gain upon rfoff_event_i reception
[3:3]	GCM_RESET_TXRFOFF_ENABLE	rw	0x1	reset gain upon rfoff_event_i reception
[2:2]	GCM_HF_ATT_FORCE	rw	0x0	Enable / disable forcing HF_ATT value with GCM_HF_ATT_INIT_EXT_VAL
[1:1]	GCM_BBA_FORCE	rw	0x0	Enable / disable forcing BBA value with BBA_VAL
[0:0]	GCM_ENABLE	rw	0x1	module enable signal

9.14.1.59 CLIF_SS_TX1_CMCFG (0x3B)

This register provides the settings for CLIF_SS_TX1_CMCFG

Table 84. CLIF_SS_TX1_CMCFG (0x3B) register bit description

Bit	Symbol	Access	Value	Description
[31:22]	RESERVED	r-	0x00	Reserved
[21:19]	TX1_CLK_MODE_MOD_CM	rw	0x00	TX1 clock mode of modulated wave in CM
[18:16]	TX1_CLK_MODE_CW_CM	rw	0x00	TX1 clock mode of unmodulated wave in CM
[15:8]	TX1_AMP_MOD_CM	rw	0x00	TX1 amplitude of modulated wave in CM
[7:0]	TX1_AMP_CW_CM	rw	0xFF	TX1 amplitude of unmodulated wave in CM

9.14.1.60 CLIF_SS_TX2_CMCFG (0x3C)

This register provides the settings for CLIF_SS_TX2_CMCFG

Table 85. CLIF_SS_TX2_CMCFG (0x3C) register bit description

Bit	Symbol	Access	Value	Description
[31:22]	RESERVED	r-	0x00	Reserved
[21:19]	TX2_CLK_MODE_MOD_CM	rw	0x00	TX2 clock mode of modulated wave in CM
[18:16]	TX2_CLK_MODE_CW_CM	rw	0x00	TX2 clock mode of unmodulated wave in CM
[15:8]	TX2_AMP_MOD_CM	rw	0x00	TX2 amplitude of modulated wave in CM
[7:0]	TX2_AMP_CW_CM	rw	0xFF	TX2 amplitude of unmodulated wave in CM

9.14.1.61 CLIF_TIMER0_CONFIG (0x3D)

This register provides the settings for CLIF_TIMER0_CONFIG.

Table 86. CLIF_TIMER0_CONFIG (0x3D) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x0	Reserved
[30:30]	T0_STOP_ON_RX_STARTED	rw	0x0	T0_STOP_EVENT: If set. the timer T0 is stopped when a data reception begins (1st bit is received).
[29:29]	T0_STOP_ON_TX_STARTED	rw	0x0	T0_STOP_EVENT: If set. the timer T0 is stopped when a data transmission begins.
[28:28]	T0_STOP_ON_RF_ON_EXT	rw	0x0	T0_STOP_EVENT: If set. the timer T0 is stopped when the external RF field is detected.
[27:27]	T0_STOP_ON_RF_OFF_EXT	rw	0x0	T0_STOP_EVENT: If set. the timer T0 is stopped when the external RF field vanishes.
[26:26]	T0_STOP_ON_RF_ON_INT	rw	0x0	T0_STOP_EVENT: If set. the timer T0 is stopped when the internal RF field is turned on.
[25:25]	T0_STOP_ON_RF_OFF_INT	rw	0x0	T0_STOP_EVENT: If set. the timer T0 is stopped when the internal RF field is turned off.
[24:24]	T0_STOP_ON_RX_ENDED	rw	0x0	T0_STOP_EVENT: If set the timer T0 is stopped when an activity on RX is detected.
[23:18]	RESERVED	r-	0x0	Reserved
[17:17]	T0_START_ON_RX_STARTED	rw	0x0	T0_START_EVENT: If set. the timer T0 is started when a data reception begins (1st bit is received).
[16:16]	T0_START_ON_RX_ENDED	rw	0x0	T0_START_EVENT: If set. the timer T0 is started when a data reception ends.
[15:15]	T0_START_ON_TX_STARTED	rw	0x0	T0_START_EVENT: If set. the timer T0 is started when a data transmission begins.
[14:14]	T0_START_ON_TX_ENDED	rw	0x0	T0_START_EVENT: If set. the timer T0 is started when a data transmission ends.
[13:13]	T0_START_ON_RF_ON_EXT	rw	0x0	T0_START_EVENT: If set. the timer T0 is startedwhen the external RF field is detected.
[12:12]	T0_START_ON_RF_OFF_EXT	rw	0x0	T0_START_EVENT: If set. the timer T0 is started when the external RF field is not detected any more.
[11:11]	T0_START_ON_RF_ON_INT	rw	0x0	T0_START_EVENT: If set. the timer T0 is started when an internal RF field is turned on.

Table 86. CLIF_TIMER0_CONFIG (0x3D) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[10:10]	T0_START_ON_RF_OFF_INT	rw	0x0	T0_START_EVENT: If set. the timer T0 is started when an internal RF field is turned off.
[8:8]	T0_START_NOW	rw	0x0	T0_START_EVENT: If set. the timer T0 is started immediatly.
[7:7]	RESERVED	r-	0x0	Reserved
[6:6]	T0_ONE_SHOT_MODE	rw	0x00	When set to 1 the counter value does not reload again until the counter value has reached zero
[5:3]	T0_PRESCALE_SEL	rw	0x00	Controls input frequency/period of the timer T0 when the prescaler is activated in T0_MODE_SEL.
			000b	000b -> 6.78 MHz counter
			001b	001b -> 3.39 MHz counter
			010b	010b -> 1.70 MHz counter
			011b	011b -> 848 kHz counter
			100b	100b -> 424 kHz counter
			101b	101b -> 212 kHz counter
			110b	110b -> 106 kHz counter
			111b	111b -> 53 kHz counter
[2:2]	T0_MODE_SEL	rw	0x00*	Configuration of the timer T0 clock.
			0b	Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56MHz).
			1b	Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T0_ PRESCALE_SEL).
[1:1]	T0_RELOAD_ENABLE	rw	0x00*	If set to 0.the timer T0 will stop on expiration.
			0b	After expiration the timer T0 will stop counting. i.e.. remain zero. reset value.
			1b	After expiration the timer T0 will reload its preset value and continue counting down.
[0:0]	T0_ENABLE	rw	0x0	Enables the timer T0

9.14.1.62 CLIF_TIMER0_RELOAD (0x3E)

This register provides the settings for CLIF_TIMER0_RELOAD

Table 87. CLIF_TIMER0_RELOAD (0x3E) register bit description

Bit	Symbol	Access	Value	Description
[31:20]	RESERVED	r-	0x0	Reserved
[19:0]	T0_RELOAD_VALUE	rw	0x0000	Reload value of the timer T0.

9.14.1.63 CLIF_TIMER1_CONFIG (0x3F)

This register provides the settings for CLIF_TIMER1_CONFIG

Table 88. CLIF_TIMER1_CONFIG (0x3F) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x0	Reserved
[30:30]	T1_STOP_ON_RX_STARTED	rw	0x0	T1_STOP_EVENT: If set. the timer T1 is stopped when a data reception begins (1st bit is received).
[29:29]	T1_STOP_ON_TX_STARTED	rw	0x0	T1_STOP_EVENT: If set. the timer T1 is stopped when a data transmission begins.
[28:28]	T1_STOP_ON_RF_ON_EXT	rw	0x0	T1_STOP_EVENT: If set. the timer T1 is stopped when the external RF field is detected.
[27:27]	T1_STOP_ON_RF_OFF_EXT	rw	0x0	T1_STOP_EVENT: If set. the timer T1 is stopped when the external RF field vanishes.
[26:26]	T1_STOP_ON_RF_ON_INT	rw	0x0	T1_STOP_EVENT: If set. the timer T1 is stopped when the internal RF field is turned on.
[25:25]	T1_STOP_ON_RF_OFF_INT	rw	0x0	T1_STOP_EVENT: If set. the timer T1 is stopped when the internal RF field is turned off.
[24:24]	T1_STOP_ON_RX_ENDED	rw	0x0	T1_STOP_EVENT: If set the timer T1 is stopped when an activity on RX is detected.
[23:18]	RESERVED	r-	0x0	Reserved
[17:17]	T1_START_ON_RX_STARTED	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when a data reception begins (1st bit is received).
[16:16]	T1_START_ON_RX_ENDED	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when a data reception ends.
[15:15]	T1_START_ON_TX_STARTED	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when a data transmission begins.
[14:14]	T1_START_ON_TX_ENDED	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when a data transmission ends.
[13:13]	T1_START_ON_RF_ON_EXT	rw	0x0	T1_START_EVENT: If set. the timer T1 is startedwhen the external RF field is detected.
[12:12]	T1_START_ON_RF_OFF_EXT	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when the external RF field is not detected any more.
[11:11]	T1_START_ON_RF_ON_INT	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when an internal RF field is turned on.
[10:10]	T1_START_ON_RF_OFF_INT	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when an internal RF field is turned off.
[8:8]	T1_START_NOW	rw	0x0	T1_START_EVENT: If set. the timer T1 is started immediatly.
[7:7]	RESERVED	r-	0x0	Reserved
[6:6]	T1_ONE_SHOT_MODE	rw	0x00	When set to 1 the counter value does not reload again until the counter value has reached zero
[5:3]	T1_PRESCALE_SEL	rw	0x00	Controls input frequency/period of the timer T0 when the prescaler is activated in T1_MODE_SEL.
			000b	000b -> 6.78 MHz counter
			001b	001b -> 3.39 MHz counter
			010b	010b -> 1.70 MHz counter
			011b	011b -> 848 kHz counter

Table 88. CLIF_TIMER1_CONFIG (0x3F) register bit description*...continued*

Bit	Symbol	Access	Value	Description
			100b	100b -> 424 kHz counter
			101b	101b -> 212 kHz counter
			110b	110b -> 106 kHz counter
			111b	111b -> 53 kHz counter
[2:2]	T1_MODE_SEL	rw	0x00*	Configuration of the timer T1 clock.
			0b	Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56MHz).
			1b	Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T1_ PRESCALE_SEL).
[1:1]	T1_RELOAD_ENABLE	rw	0x00*	If set to 0.the timer T1 will stop on expiration.
			0b	After expiration the timer T1 will stop counting. i.e.. remain zero. reset value.
			1b	After expiration the timer T1 will reload its preset value and continue counting down.
[0:0]	T1_ENABLE	rw	0x0	Enables the timer T1

9.14.1.64 CLIF_TIMER1_RELOAD (0x40)

This register provides the settings for CLIF_TIMER1_RELOAD

Table 89. CLIF_TIMER1_RELOAD (0x40) register bit description

Bit	Symbol	Access	Value	Description
[31:20]	RESERVED	r-	0x0	Reserved
[19:0]	T1_RELOAD_VALUE	rw	0x0000	Reload value of the timer T1.

9.14.1.65 CLIF_ANA_STATUS (0x41)

This register provides the settings for CLIF_ANA_STATUS

Table 90. CLIF_ANA_STATUS (0x41) register bit description

Bit	Symbol	Access	Value	Description
[31:21]	RESERVED	r-	0x00	reserved
[20:11]	ADC_DATA_I	r-	0x00	RX adc I output for validation purposes
[10:1]	ADC_DATA_Q	r-	0x00	RX adc Q output for validation purposes
[0:0]	PLL_LOCK_STATUS	r-	0x00	PLL lock status indicator

9.14.1.66 CLIF_ANA_RX_CTRL (0x43)

This register provides the settings for CLIF_ANA_RX_CTRL

Table 91. CLIF_ANA_RX_CTRL (0x43) register bit description

Bit	Symbol	Access	Value	Description
[31:27]	RESERVED	r-	0x00	reserved

Table 91. CLIF_ANA_RX_CTRL (0x43) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[26:26]	RX_CLK_BUF_HP_EN	rw	0x00	RX_CLK_BUF_HP_EN
[25:25]	RX_CLK_BUF_MON_EN	rw	0x00	enable signal for the monitoring buffer
[24:24]	RX_CLK_BUF_LATCH_EN	rw	0x00	enable signal for the DPLL latch
[23:23]	RX_CLK_BUF_BUFFER_EN	rw	0x00	enable signal for the ADPLL buffer
[22:22]	RX_MIXER_SS_MODE_EN	rw	0x00	13M56 sampling rate, to be used for test purpose only, makes the mixer sensitive to DC
[21:19]	RX_ATB_MON_SEL	rw	0x00	configuration bits for ATB signal monitoring, validation/test purpose
[18:16]	RX_CLKGEN_PH_CTRL	rw	0x00	used to add delay to the I/Q RX mixer CLK - step is 1 / 108M
[15:15]	RX_CLKGEN_EN	rw	0x00	Signal enable for RX_CLKGEN synchro
[14:14]	RX_BIAS_EN	rw	0x00	enable signal for RX bias circuit
[13:13]	RX_RSSI_EN	rw	0x00	enable signal for RSSI
[12:12]	RFU	rw	0x00	Reserved
[11:11]	RX_RSSI_HIGAIN	rw	0x00	RX_RSSI_HIGAIN
[10:7]	RX_RSSI_DC_TRIM	rw	0x00	used for adjusting RSSI DC Offset
[6:6]	RX_MIXER_SE_MODE_EN	rw	0x00	enable signal for selecting single ended mode
[5:4]	RX_BBA_FTRIM_SEL	rw	0x00	used to adjust RX BBA filter cut off frequency
[3:3]	RX_BBA_MON_EN	rw	0x00	enable signal for diff to single monitoring buffers
[2:2]	RX_ADC_EN	rw	0x00	enable signal for RX ADCs
[1:1]	RX_MIXER_EN	rw	0x00	enable signal for RX mixers
[0:0]	RX_BBA_EN	rw	0x00	enable signal for the baseband amplifiers

9.14.1.67 CLIF_ANACTRL_TX_CONFIG (0x44)

This register provides the settings for CLIF_ANACTRL_TX_CONFIG

Table 92. CLIF_ANACTRL_TX_CONFIG (0x44) register bit description

Bit	Symbol	Access	Value	Description
[31:22]	RESERVED	r-	0x0	Reserved
[21:18]	TX_PH_SHIFT_MOD10	rw	0x0	Applies a tx_ph_shift_mod10x0.9 degree on ck13m56_tx wrt ck13m56. Value is unsigned, ranging from 0 to 9. Final tx phase shift is the following: (tx_ph_shift_div10x10+tx_ph_shift_mod10)x0.9 degree
[17:13]	TX_PH_SHIFT_DIV10	rw	0x0	Applies a tx_ph_shift_div10x10x0.9 degree on ck13m56_tx wrt ck13m56. Value is signed 2s complement, ranging from -16 to 15, corresponding to -144 degree to 135 degree, with steps of 9 degree
[12:11]	TX_INVP_CW_CM	rw	0x0	Shift driver waves of 180 degrees in CM Continuous Wave.
			0	0 -> TX1
			1	1 -> TX2

Table 92. CLIF_ANACTRL_TX_CONFIG (0x44) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[10:9]	TX_INVP_MOD_CM	rw	0x0	Shift driver waves of 180 degrees in CM Modulated Wave.
			0	0 -> TX1
			1	1 -> TX2
[8:7]	TX_INVL_CM	rw	0x0	inverse polarity of driver waves in CM.
			0	0 -> TX1
			1	1 -> TX2
[6:6]	TX_PWM_MODE_CM	rw	0x0	PWM scheme for CM
			0	0 -> TX1/2 3-levels (If at least either clk_mode_tx1 or clk_mode_tx2 is set on a clocked mode)
			1	1 -> TX1/2 2-levels with differentiated pulses
[5:4]	TX_INVP_RM	rw	0x0	shift driver waves of 180 in RM.
			0	0 -> TX1
			1	1 -> TX2
[3:2]	TX_INVL	rw	0x0	inverse polarity of driver waves in RM.
			0	0 -> TX1
			1	1 -> TX2
[1:1]	TX_PWM_MODE_RM	rw	0x0	PWM scheme for RM
			0	0 -> TX1/2 3-levels (If at least either clk_mode_tx1 or clk_mode_tx2 is set on a clocked mode)
			1	1 -> TX1/2 2-levels with differentiated pulses
[0:0]	TX_EN	rw	0x0	Enables transmitter

9.14.1.68 CLIF_ANACTRL_TX_NOV (0x45)

This register provides the settings for CLIF_ANACTRL_TX_NOV

Table 93. CLIF_ANACTRL_TX_NOV (0x45) register bit description

Bit	Symbol	Access	Value	Description
[31:27]	RESERVED	r-	0x0	Returns non-overlap regulation counter selected by SEL_OF FSET_CNT
[26:22]	TX_NOV_OFFSET_IN	rw	0x0	Offset value to be loaded based on SEL_OFFSET_CNT
[21:19]	TX_SEL_OFFSET_CNT	rw	0x0	Non-overlap regulation counter selection
[18:18]	TX_OFFSET_LOAD	rw	0x0	If set to 1, overrides the non-overlap regulation counter selected by SEL_OFFSET_CNT with NOV_OFFSET_IN
[17:15]	TX_SET_NOV_TIME_FW	rw	0x0	Non-overlap window target setting for the PMOS/NMOS/free-wheel in the 3-levels mode (400ps*(set_nov_time+1))
[14:12]	TX_SET_NOV_TIME_FP	rw	0x0	Non-overlap window target setting for the PMOS/NMOS in 2-levels modes (400ps*(set_nov_time+1))

Table 93. CLIF_ANACTRL_TX_NOV (0x45) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[4:1]	TX_AUTO_NOV	rw	0x0	Automatic triggering of non overlap regulation loop at RF. 0 : disable, /=0 : enable regulation during 128/13.56MHz*AUTO_NOV after Rfon
[0:0]	TX_FREEZE_NOV	rw	0x1	Freezes the automatic non-overlap regulation mechanism

9.14.1.69 CLIF_RX_EOF_PATTERN (0x46)

This register provides the settings for CLIF_RX_EOF_PATTERN

Table 94. CLIF_RX_EOF_PATTERN (0x46) register bit description

Bit	Symbol	Access	Value	Description
[31:0]	RX_EOF_PATTERN	rw	0	

9.14.1.70 CLIF_RX_EMD_1_CONFIG (0x47)

This register provides the settings for CLIF_RX_EMD_1_CONFIG

Table 95. CLIF_RX_EMD_1_CONFIG (0x47) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x0	Reserved
[16:16]	RX_EMD_IRQ_MASK	rw	0x1	If asserted, the detected EMD is not reported via EMD IRQ. Otherwise every detected EMD causes the EMD IRQ assertion.
[15:8]	RX_EMD_LEVEL_THRESH_1	rw	0x0	Defines the EMD detection threshold when the number of received bits >RX_EMD_LENGTH_THRESH_0 If currently calculated EMD level more than RX_EMD_LEVEL_THRESH_1 - the frame is classified as EMD, otherwise its normal Frame.
[7:0]	RX_EMD_LEVEL_THRESH_0	rw	0x0	Defines the EMD detection threshold when the number of received bits less than or equal to RX_EMD_LENGTH_THRESH_0 If currently calculated EMD level more than RX_EMD_LEVEL_THRESH_0 - the frame is classified as EMD, otherwise its normal Frame.

9.14.1.71 CLIF_RX_EMD_0_CONFIG (0x48)

This register provides the settings for CLIF_RX_EMD_0_CONFIG

Table 96. CLIF_RX_EMD_0_CONFIG (0x48) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	RX_EMD_LENGTH_THRESH_0	rw	0x1F	Threshold in number of received data bits which defines which group of EMD config parameters must be used for the EMD detection.If the number of received bits >RX_EMD_LENGTH_THRESH_0 the *_IS_EMD_1 group of parameters must be used for the EMD classification, otherwise the*_IS_EMD_0 group.

Table 96. CLIF_RX_EMD_0_CONFIG (0x48) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[23:23]	RESERVED	r-	0x0	Reserved
[22:22]	RX_MAXLEN_FRAME_IS_EMD	rw	0x0	If asserted and the received frame length violates the max frame length configured via the RX_FRAME_MAXLEN register - the event is considered as EMD symptom.
[21:21]	RX_MINLEN_FRAME_IS_EMD	rw	0x1	If asserted and the received frame length violates the min frame length configured via the RX_FRAME_MINLEN register - the event is considered as EMD symptom.
[20:20]	RX_LEN_ERR_IS_EMD	rw	0x0	If asserted and the LEN field is a part of the frame, the wrong received value in the field is considered as EMD symptom.
[19:19]	RX_SIGPRO_TERM_IS_EMD_1	rw	0x0	If asserted, the number of received bits>RX_EMD_LENGTH_THRESH_0 and the SGP_MSG_RXOVER_TERM message is received - the event is considered as EMD symptom.
[18:18]	RX_SIGPRO_ERR_IS_EMD_1	rw	0x0	If asserted, the number of received bits >RX_EMD_LENGTH_THRESH_0 and either SGP_MSG_RXOVER_ERROR or SGP_MSG_ERROR message is received - the event is considered as EMD symptom.
[17:17]	RX_NOSTOP_DET_IS_EMD_1	rw	0x0	If asserted, the number of received bits >RX_EMD_LENGTH_THRESH_0 and the frame reception is over being not interrupted by any detected error or external rf-off event but no any stop conditions, configured via EOF_COND_SCALE register, were detected -the scenario is considered as EMD symptom.
[16:16]	RX_CRC_ERR_IS_EMD_1	rw	0x0	If asserted and the number of received bits>RX_EMD_LENGTH_THRESH_0 - the detection of the CRC error is considered as EMD symptom.
[15:15]	RX_NOT_FULL_BYTE_IS_EMD_1	rw	0x0	If asserted and the number of received bits is greater than RX_EMD_LENGTH_THRESH_0 - the reception of last byte with size less than 8 data bits is considered as EMD symptom.
[14:14]	RX_MISSING_STOPBIT_IS_EMD_1	rw	0x0	If asserted, the number of received bits >RX_EMD_LENGTH_THRESH_0 and the stop bit is a part of the frame character, the reception of the last character with 8 data bits but without stop bit is considered as EMD symptom.
[13:13]	RX_MISSING_PARITY_IS_EMD_1	rw	0x0	If asserted, the number of received bits >RX_EMD_LENGTH_THRESH_0 and the parity bit is a part of the frame character, the reception of the last character with 8 data bits but without parity bit is considered as EMD symptom.
[12:12]	RX_PARBIT_ERR_IS_EMD_1	rw	0x0	If asserted and the number of received bits >RX_EMD_LENGTH_THRESH_0 - the detected parity error is considered as EMD symptom.
[11:11]	RX_STOPBIT_ERR_IS_EMD_1	rw	0x0	If asserted and the number of received bits >RX_EMD_LENGTH_THRESH_0 - the detected stop bit

Table 96. CLIF_RX_EMD_0_CONFIG (0x48) register bit description*...continued*

Bit	Symbol	Access	Value	Description
				error (0 level instead of 1 on the stop bit position) is considered as EMD symptom.
[10:10]	RX_COLL_IS_EMD_1	rw	0x0	If asserted and the number of received bits >RX_EMD_LENGTH_THRESH_0 - the collision is considered as EMD symptom.
[9:9]	RX_SIGPRO_TERM_IS_EMD_0	rw	0x0	If asserted, the number of received bits less than or equal to RX_EMD_LENGTH_THRESH_0 And the SGP_MSG_RXOVER_TERM message is received - the event is considered as EMD symptom.
[8:8]	RX_SIGPRO_ERR_IS_EMD_0	rw	0x0	If asserted, the number of received bits less than or equal RX_EMD_LENGTH_THRESH_0 and either SGP_MSG_RXOVER_ERROR or SGP_MSG_ERROR message is received - the event is considered as EMD symptom.
[7:7]	RX_NOSTOP_DET_IS_EMD_0	rw	0x0	If asserted, the number of received bits less than or equal to RX_EMD_LENGTH_THRESH_0 and the frame reception is over being not interrupted by any detected error or external rf-off event but no any stop conditions, configured via EOF_COND_SCALE register, were detected -the scenario is considered as EMD symptom.
[6:6]	RX_CRC_ERR_IS_EMD_0	rw	0x0	If asserted and the number of received bits less than or equal to RX_EMD_LENGTH_THRESH_0 - the detection of the CRC error is considered as EMD symptom.
[5:5]	RX_NOT_FULL_BYTE_IS_EMD_0	rw	0x0	If asserted and the number of received bits less than or equal to RX_EMD_LENGTH_THRESH_0 - the reception of last byte with size is less than 8 data bits is considered as EMD symptom.
[4:4]	RX_MISSING_STOPBIT_IS_EMD_0	rw	0x0	If asserted, the number of received bits less than or equal to RX_EMD_LENGTH_THRESH_0 and the stop bit is a part of the frame character, the reception of the last character with 8 data bits but without stop bit is considered as EMD symptom.
[3:3]	RX_MISSING_PARITY_IS_EMD_0	rw	0x0	If asserted, the number of received bits less than or equal to RX_EMD_LENGTH_THRESH_0 and the parity bit is a part of the frame character, the reception of the last character with 8 data bits but without parity bit is considered as EMD symptom.
[2:2]	RX_PARBIT_ERR_IS_EMD_0	rw	0x0	If asserted and the number of received bits less than or equal to RX_EMD_LENGTH_THRESH_0 - the detected parity error is considered as EMD symptom.
[1:1]	RX_STOPBIT_ERR_IS_EMD_0	rw	0x0	If asserted and the number of received bits less than or equal to RX_EMD_LENGTH_THRESH_0 - the detected stop bit error (0 level instead of 1 on the stop bit position) is considered as EMD symptom.
[0:0]	RX_COLL_IS_EMD_0	rw	0x0	If asserted and the number of received bits less than or equal to RX_EMD_LENGTH_THRESH_0 - the collision is considered as EMD symptom.

9.14.1.72 CLIF_SIGPRO_CM_FILT128B (0x49)

This register provides the settings for CLIF_SIGPRO_CM_FILT128B

Table 97. CLIF_SIGPRO_CM_FILT128B (0x49) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x0	RESERVED
[30:29]	CM_THLD_INIT_GAIN_128B	rw	0x0	CM_THLD_INIT_GAIN_128B
[28:25]	CM_FILT_DLY_128B	rw	0x0	number of clock cycles used for consecutive edges decision logic
[24:24]	CM_FILT_DLY_128B_ENABLE	rw	0x0	enables consecutive edges decision logic
[23:21]	CM_FILT_COEF_128B_0_8	rw	0x1	Filter coefficient for the 128 tap length TypeB filter
[20:18]	CM_FILT_COEF_128B_1_7	rw	0x0	Filter coefficient for the 128 tap length TypeB filter
[17:15]	CM_FILT_COEF_128B_2_6	rw	0x0	Filter coefficient for the 128 tap length TypeB filter
[14:12]	CM_FILT_COEF_128B_3_5	rw	0x0	Filter coefficient for the 128 tap length TypeB filter
[11:10]	CM_FILT_COEF_128B_4	rw	0x0	Filter coefficient for the 128 tap length TypeB filter
[9:7]	CM_THLD_DYN_FACTOR_128B	rw	0x0	initial value of the typeB 128-filter threshold value
[6:0]	CM_THLD_INIT_128B	rw	0x0	initial value of the typeB 128-filter threshold value

9.14.1.73 CLIF_SIGPRO_CM_FILT128A (0x4A)

This register provides the settings for CLIF_SIGPRO_CM_FILT128A

Table 98. CLIF_SIGPRO_CM_FILT128A (0x4A) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x0	RESERVED
[30:29]	CM_THLD_INIT_GAIN_128A	rw	0x0	CM_THLD_INIT_GAIN_128A
[28:25]	CM_FILT_DLY_128A	rw	0x0	number of clock cycles used for consecutive edges decision logic
[24:24]	CM_FILT_DLY_128A_ENABLE	rw	0x0	enables consecutive edges decision logic
[23:21]	CM_FILT_COEF_128A_0_8	rw	0x1	Filter coefficient for the 128 tap length TypeA filter
[20:18]	CM_FILT_COEF_128A_1_7	rw	0x0	Filter coefficient for the 128 tap length TypeA filter
[17:15]	CM_FILT_COEF_128A_2_6	rw	0x0	Filter coefficient for the 128 tap length TypeA filter
[14:12]	CM_FILT_COEF_128A_3_5	rw	0x0	Filter coefficient for the 128 tap length TypeA filter
[11:10]	CM_FILT_COEF_128A_4	rw	0x0	Filter coefficient for the 128 tap length TypeA filter
[9:7]	CM_THLD_DYN_FACTOR_128A	rw	0x0	initial value of the typeA 128-filter threshold value
[6:0]	CM_THLD_INIT_128A	rw	0x0	initial value of the typeA 128-filter threshold value

9.14.1.74 CLIF_SIGPRO_CM_FILT64 (0x4B)

This register provides the settings for CLIF_SIGPRO_CM_FILT64

Table 99. CLIF_SIGPRO_CM_FILT64 (0x4B) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x0	RESERVED
[30:29]	CM_THLD_INIT_GAIN_64	rw	0x0	CM_THLD_INIT_GAIN_64
[28:25]	CM_FILT_DLY_64	rw	0x0	number of clock cycles used for consecutive edges decision logic
[24:24]	CM_FILT_DLY_64_ENABLE	rw	0x0	enables consecutive edges decision logic
[23:21]	CM_FILT_COEF_64_0_8	rw	0x1	Filter coefficient for the 64 tap length filter
[20:18]	CM_FILT_COEF_64_1_7	rw	0x0	Filter coefficient for the 64 tap length filter
[17:15]	CM_FILT_COEF_64_2_6	rw	0x0	Filter coefficient for the 64 tap length filter
[14:12]	CM_FILT_COEF_64_3_5	rw	0x0	Filter coefficient for the 64 tap length filter
[11:10]	CM_FILT_COEF_64_4	rw	0x0	Filter coefficient for the 64 tap length filter
[9:7]	CM_THLD_DYN_FACTOR_64	rw	0x0	initial value of the 64-filter threshold value
[6:0]	CM_THLD_INIT_64	rw	0x0	initial value of the 64-filter threshold value

9.14.1.75 CLIF_SIGPRO_CM_FILT16_32 (0x4C)

This register provides the settings for CLIF_SIGPRO_CM_FILT16_32

Table 100. CLIF_SIGPRO_CM_FILT16_32 (0x4C) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x0	RESERVED
[30:29]	CM_THLD_INIT_GAIN_16_32	rw	0x0	CM_THLD_INIT_GAIN_16_32
[28:25]	CM_FILT_DLY_16_32	rw	0x0	number of clock cycles used for consecutive edges decision logic
[24:24]	CM_FILT_DLY_16_32_ENABLE	rw	0x0	enables consecutive edges decision logic
[23:21]	CM_FILT_COEF_16_32_0_8	rw	0x1	Filter coefficient for the 16/32 tap length filter
[20:18]	CM_FILT_COEF_16_32_1_7	rw	0x0	Filter coefficient for the 16/32 tap length filter
[17:15]	CM_FILT_COEF_16_32_2_6	rw	0x0	Filter coefficient for the 16/32 tap length filter
[14:12]	CM_FILT_COEF_16_32_3_5	rw	0x0	Filter coefficient for the 16/32 tap length filter
[11:10]	CM_FILT_COEF_16_32_4	rw	0x0	Filter coefficient for the 16/32 tap length filter
[9:7]	CM_THLD_DYN_FACTOR_16_32	rw	0x0	initial value of the 16/32-filter threshold value
[6:0]	CM_THLD_INIT_16_32	rw	0x0	initial value of the 16/32-filter threshold value

9.14.1.76 CLIF_SIGPRO_CM_CONFIG2 (0x4D)

This register provides the settings for CLIF_SIGPRO_CM_CONFIG2

Table 101. CLIF_SIGPRO_CM_CONFIG2 (0x4D) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	RESERVED	r-	0	Reserved

Table 101. CLIF_SIGPRO_CM_CONFIG2 (0x4D) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[23:20]	CM_TYPEF2_BITG_ADPT_HLF_LGTH	rw	0	filter threshold factor half window length
[19:16]	CM_TYPEF2_BITG_ADPT_SLOPE	rw	0	filter threshold factor update rate
[15:10]	CM_TYPEF2_BITG_ADPT_MIN	rw	0	filter threshold factor min value
[9:4]	CM_TYPEF2_BITG_ADPT_MAX	rw	0	filter threshold factor max value
[3:0]	CM_TYPEF2_BITG_DLY	rw	0	number of clock cycle required to align the bitgrid to the filter

9.14.1.77 CLIF_SIGPRO_CM_CONFIG3 (0x4E)

This register provides the settings for CLIF_SIGPRO_CM_CONFIG3

Table 102. CLIF_SIGPRO_CM_CONFIG3 (0x4E) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	RESERVED	r-	0	Reserved
[23:20]	CM_TYPEF4_BITG_ADPT_HLF_LGTH	rw	0	filter threshold factor half window length
[19:16]	CM_TYPEF4_BITG_ADPT_SLOPE	rw	0	filter threshold factor update rate
[15:10]	CM_TYPEF4_BITG_ADPT_MIN	rw	0	filter threshold factor min value
[9:4]	CM_TYPEF4_BITG_ADPT_MAX	rw	0	filter threshold factor max value
[3:0]	CM_TYPEF4_BITG_DLY	rw	0	number of clock cycle required to align the bitgrid to the filter

9.14.1.78 CLIF_SIGPRO_PRE_CONFIG (0x4F)

This register provides the settings for CLIF_SIGPRO_PRE_CONFIG

Table 103. CLIF_SIGPRO_PRE_CONFIG (0x4F) register bit description

Bit	Symbol	Access	Value	Description
[31:10]	RESERVED	r-	0x0000	Reserved
[9:9]	PRE_ENABLE_STEP_RANGE	rw	0x1	Defines the input selection for the sync filter.
[8:8]	PRE_PHASE_FREEZE	rw	0x0	Freezes the current value of the phase rotator
[7:7]	PRE_COMB_SETTING	rw	0x0	Selects the gain combiner mode
[6:3]	PRE_WINDOW_STOP	rw	0xF	gain cancelation window end count
[2:0]	PRE_WINDOW_START	rw	0x4	gain cancelation window start count

9.14.1.79 LPCD_CALIBRATE_CTRL (0x50)

This register provides the settings for LPCD_CALIBRATE_CTRL

This register is used for LPCD semi autonomous mode. Writing to this register triggers the LPCD calibration with the RSSI_HYSTERESIS and RSSI_TARGET values as given in bits 23:16 and 15:0. After calibration is completed, calibration status is available in LPCD_CALIBRATE_STATUS. If the calibration is successful, the I/Q channel values can be read from register IQ_CHANNEL_VALS (51h).

Note: *This register is accessible from PN7642 FW v02.02 and above.*

Table 104. LPCD_CALIBRATE_CTRL (0x50) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x0	Reserved
[30:30]	FREEZE_VALUE	rw		Write RSSI_TARGET and RSSI_HYSTERESIS into LPCD_CALIBRATE_CTRL register.
			0x00	This calibrates the Semi-autonomous LPCD. The calibration status can be checked in bit 31 of CALIBRATE_STATUS register (0x53).
			0x01	This writes the RSSI_TARGET and RSSI_HYSTERESIS into the EEPROM configuration LPCD_RSSI_TARGET (0x03E0) and LPCD_RSSI_HYST (0x03E2).
[29:24]	RESERVED	r-		Reserved
[23:16]	RSSI_HYSTERESIS	rw		Value to be set in CLIF_DGRM_RSSI->DGRM_RSSI_HYST used for calibration
[15:0]	RSSI_TARGET	rw		Value to be set in CLIF_DGRM_RSSI->DGRM_RSSI_TARGET used for calibration

9.14.1.80 IQ_CHANNEL_VALS (0x51)

This register provides the reading from IQ_CHANNEL_VALS register.

Note: *This register is accessible from PN7642 FW v02.02 and above.*

Table 105. IQ_CHANNEL_VALS (0x51) register bit description

Bit	Symbol	Access	Value	Description
[31:16]	Q_CHANNEL_VAL	r-		Q Channel value
[15:0]	I_CHANNEL_VAL	r-		I Channel value

9.14.1.81 CALIBRATE_STATUS (0x53)

This register provides the reading from CALIBRATE_STATUS register

Note: *This register is accessible from PN7642 FW v02.02 and above.*

Table 106. CALIBRATE_STATUS (0x53) register bit description

Bit	Symbol	Access	Value	Description
[31]	LPCD_CALIBRATION_STATUS	r-		LPCD calibration status
			0x00	Calibration Not Done
			0x01	Calibration Done
[30:1]	RESERVED	r-		Reserved
[0]	TXNOV_CALIBRATION_STATUS	r-		TXNOV calibration status
			0x00	Calibration Not Done
			0x01	Calibration Done

9.14.1.82 TXLDO_VDDPA_CONFIG (0x54)

This register provides the settings for TXLDO_VDDPA_CONFIG

If DPC is disabled, the VDDPA supply voltage can be set with this register. These register settings are overruled by the DPC.

This register does allow to read the actual VDDPA supply voltage independent from having the DPC enabled/disabled, this allows to read-out the actual transmitter supply voltage.

Table 107. TXLDO_VDDPA_CONFIG (0x54) register bit description

Bit	Symbol	Access	Value	Description
[31:8]	RESERVED	rw		Reserved
[7:0]	VDDPA_CONFIG	rw		VDDPALDO output voltage VDDPA_1V50

9.14.1.83 TXLDO_VOUT_CURR (0x56)

This register provides the settings for TXLDO_VOUT_CURR

Table 108. TXLDO_VOUT_CURR (0x56) register bit description

Bit	Symbol	Access	Value	Description
[23:8]	TXLDO_CURRENT	r-		Indicates the TXLDO Current, measured value is indicated in mA (1 bit = 1 mA)
[7:0]	VDDPA_VOUT	r-		VDDPALDO output voltage VDDPA_1V50

9.14.1.84 CLIF_RXM_FREQ (0x59)

This register provides the settings for CLIF_RXM_FREQ

Table 109. CLIF_RXM_FREQ (0x59) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RXM_FREQ_VALID	r-	0x00	CLIF_RXM_FREQ_REG fields are valid
[30:25]	RESERVED	r-	0x00	Reserved
[24:16]	RXM_FREQ	r-	0x00	frequence difference between the last two consecutive measures at 1.7 MHz (multiple of 13.56 MHz/4096). Signed. 2-Complement coded.
[15:9]	RESERVED	r-	0x00	Reserved
[8:0]	RXM_PHASE	r-	0x00	phase value

9.14.1.85 CLIF_RXM_RSSI (0x5A)

This register provides the settings for CLIF_RXM_RSSI

Table 110. CLIF_RXM_RSSI (0x5A) register bit description

Bit	Symbol	Access	Value	Description
[31:23]	RESERVED	r-	0x00	Reserved
[22:22]	RXM_RSSI_FROZEN	r-	0x00	The RSSI value is not currently updated
[21:21]	RXM_FRQ_OK	r-	0x00	The carrier frequency detected is OK.
[20:20]	RXM_RSSI_VALID	r-	0x00	CLIF_RXM_RSSI_REG fields are valid
[19:14]	RXM_HFATT	r-	0x00	HFAtt latched with RSSI
[13:0]	RXM_RSSI	r-	0x00	RSSI value

9.14.1.86 INTERPOLATED_RSSI_REG (0x5C)

This register provides the settings for INTERPOLATED_RSSI_REG

Table 111. INTERPOLATED_RSSI_REG (0x5C) register bit description

Bit	Symbol	Access	Value	Description
[31:0]	INTERPOLATED_RSSI	r-		Callculated Interpolated RSSI

9.14.1.87 TX_NOV_CALIBRATE_AND_STORE_VAL_REG (0x5D)

This register provides the settings for TX_NOV_CALIBRATE_AND_STORE_VAL_REG

Table 112. TX_NOV_CALIBRATE_AND_STORE_VAL_REG (0x5D) register bit description

Bit	Symbol	Access	Value	Description
[31:2]	RFU	rw		Reserved
[1:0]	TX_NOV_CALIBRATE_STORE	rw		Perform TX_NOV Calibration and store in User Area

9.14.1.88 CLIF_TIMER0_OUTPUT (0x5F)

This register provides the settings for CLIF_TIMER0_OUTPUT

Table 113. CLIF_TIMER0_OUTPUT (0x5F) register bit description

Bit	Symbol	Access	Value	Description
[31:25]	RESERVED	r-	0x0	Reserved
[24:24]	T0_RUNNING	r-	0x0	Indicates that timer T0 is running (busy)
[19:0]	T0_VALUE	r-	0x00000	Value of 20bit counter in timer T0

9.14.1.89 CLIF_TIMER1_OUTPUT (0x60)

This register provides the settings for CLIF_TIMER1_OUTPUT

Table 114. CLIF_TIMER1_OUTPUT (0x60) register bit description

Bit	Symbol	Access	Value	Description
[31:25]	RESERVED	r-	0x0	Reserved
[24:24]	T1_RUNNING	r-	0x0	Indicates that timer T1 is running (busy)
[19:0]	T1_VALUE	r-	0x00000	Value of 20bit counter in timer T1

9.14.1.90 CLIF_TIMER2_CONFIG (0x61)

This register provides the settings for CLIF_TIMER2_CONFIG

Table 115. CLIF_TIMER2_CONFIG (0x61) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x0	Reserved
[30:30]	T2_STOP_ON_RX_STARTED	rw	0x0	T2_STOP_EVENT: If set. the timer T2 is stopped when a data reception begins (1st bit is received).
[29:29]	T2_STOP_ON_TX_STARTED	rw	0x0	T2_STOP_EVENT: If set. the timer T2 is stopped when a data transmission begins.
[28:28]	T2_STOP_ON_RF_ON_EXT	rw	0x0	T2_STOP_EVENT: If set. the timer T2 is stopped when the external RF field is detected.
[27:27]	T2_STOP_ON_RF_OFF_EXT	rw	0x0	T2_STOP_EVENT: If set. the timer T2 is stopped when the external RF field vanishes.
[26:26]	T2_STOP_ON_RF_ON_INT	rw	0x0	T2_STOP_EVENT: If set. the timer T2 is stopped when the internal RF field is turned on.
[25:25]	T2_STOP_ON_RF_OFF_INT	rw	0x0	T2_STOP_EVENT: If set. the timer T2 is stopped when the internal RF field is turned off.
[24:24]	T2_STOP_ON_RX_ENDED	rw	0x0	T2_STOP_EVENT: If set the timer T2 is stopped when an activity on RX is detected.
[23:18]	RESERVED	r-	0x0	Reserved
[17:17]	T2_START_ON_RX_STARTED	rw	0x0	T2_START_EVENT: If set. the timer T2 is started when a data reception begins (1st bit is received).
[16:16]	T2_START_ON_RX_ENDED	rw	0x0	T2_START_EVENT: If set. the timer T2 is started when a data reception ends.

Table 115. CLIF_TIMER2_CONFIG (0x61) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[15:15]	T2_START_ON_TX_STARTED	rw	0x0	T2_START_EVENT: If set. the timer T2 is started when a data transmission begins.
[14:14]	T2_START_ON_TX_ENDED	rw	0x0	T2_START_EVENT: If set. the timer T2 is started when a data transmission ends.
[13:13]	T2_START_ON_RF_ON_EXT	rw	0x0	T2_START_EVENT: If set. the timer T2 is started when the external RF field is detected.
[12:12]	T2_START_ON_RF_OFF_EXT	rw	0x0	T2_START_EVENT: If set. the timer T2 is started when the external RF field is not detected any more.
[11:11]	T2_START_ON_RF_ON_INT	rw	0x0	T2_START_EVENT: If set. the timer T2 is started when an internal RF field is turned on.
[10:10]	T2_START_ON_RF_OFF_INT	rw	0x0	T2_START_EVENT: If set. the timer T2 is started when an internal RF field is turned off.
[8:8]	T2_START_NOW	rw	0x0	T2_START_EVENT: If set. the timer T2 is started immediatly.
[7:7]	RESERVED	r-	0x0	Reserved
[6:6]	T2_ONE_SHOT_MODE	rw	0x00	When set to 1 the counter value does not reload again until the counter value has reached zero
[5:3]	T2_PRESCALE_SEL	rw	0x00	Controls input frequency/period of the timer T2 when the prescaler is activated in T2_MODE_SEL.
			000b	000b -> 6.78 MHz counter
			001b	001b -> 3.39 MHz counter
			010b	010b -> 1.70 MHz counter
			011b	011b -> 848 kHz counter
			100b	100b -> 424 kHz counter
			101b	101b -> 212 kHz counter
			110b	110b -> 106 kHz counter
			111b	111b -> 53 kHz counter
[2:2]	T2_MODE_SEL	rw	0x00*	Configuration of the timer T2 clock.
			0b	Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56MHz).
			1b	Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T2_ PRESCALE_SEL).
[1:1]	T2_RELOAD_ENABLE	rw	0x00*	If set to 0.the timer T2 will stop on expiration.
			0b	After expiration the timer T2 will stop counting. i.e.. remain zero. reset value.
			1b	After expiration the timer T2 will reload its preset value and continue counting down.
[0:0]	T2_ENABLE	rw	0x0	Enables the timer T2

9.14.1.91 CLIF_TIMER2_RELOAD (0x62)

This register provides the settings for CLIF_TIMER2_RELOAD

Table 116. CLIF_TIMER2_RELOAD (0x62) register bit description

Bit	Symbol	Access	Value	Description
[31:20]	RESERVED	r-	0x0	Reserved
[19:0]	T2_RELOAD_VALUE	rw	0x0000	Reload value of the timer T2.

9.14.1.92 CLIF_TIMER2_OUTPUT (0x63)

This register provides the settings for CLIF_TIMER2_OUTPUT

Table 117. CLIF_TIMER2_OUTPUT (0x63) register bit description

Bit	Symbol	Access	Value	Description
[31:25]	RESERVED	r-	0x0	Reserved
[24:24]	T2_RUNNING	r-	0x0	Indicates that timer T2 is running (busy)
[19:0]	T2_VALUE	r-	0x00000	Value of 20bit counter in timer T2

9.14.1.93 CLIF_BM_TX_BUFFER (0x66)

This register provides the settings for CLIF_BM_TX_BUFFER

Table 118. CLIF_BM_TX_BUFFER (0x66) register bit description

Bit	Symbol	Access	Value	Description
[31:28]	RESERVED	r-	0x0	Reserved
[27:26]	TX_HEADER_BYTE_OFFSET	rw	0x0	Defines the number of bytes to be skipped of the 1st data word transmitted
[25:16]	TX_BUFFER_LENGTH	rw	0x0	Defines the number of bytes to be skipped of the 1st data word transmitted
[15:14]	RESERVED	r-	0x0	Reserved
[13:0]	TX_BUFFER_START_ADDRESS	rw	0x0	Defines the relative buffer (word) address of the Tx buffer. Note: Changing the buffer address while the transmitter is active will trigger a BMA error.

9.14.1.94 CLIF_BM_RX_WATERLEVEL (0x67)

This register provides the settings for CLIF_BM_RX_WATERLEVEL

Table 119. CLIF_BM_RX_WATERLEVEL (0x67) register bit description

Bit	Symbol	Access	Value	Description
[31:11]	RESERVED	r-	0x0	Reserved
[10:0]	RX_WATERLEVEL	rw	0x0	Defines a warning level to indicate that RX_ WATERLEVEL number of words were already received in the actual frame. When this level is reached the corresponding IRQ is set. Note: 0 disables the waterlevel

9.14.1.95 CLIF_BM_RX_BUFFER (0x68)

This register provides the settings for CLIF_BM_RX_BUFFER

Table 120. CLIF_BM_RX_BUFFER (0x68) register bit description

Bit	Symbol	Access	Value	Description
[31:26]	RESERVED	r-	0x0	Reserved
[25:16]	RX_BUFFER_LENGTH	rw	0x0	Defines the length of the Rx buffer (in data words)
[15:14]	RESERVED	r-	0x0	Reserved
[13:0]	RX_BUFFER_START_ ADDRESS	rw	0x0	Defines the relative buffer (word) address of the Rx buffer. Note: Changing the buffer address while the receiver is enabled will trigger a BMA error.

9.14.1.96 CLIF_RF_CONTROL (0x69)

This register provides the settings for CLIF_RF_CONTROL

Table 121. CLIF_RF_CONTROL (0x69) register bit description

Bit	Symbol	Access	Value	Description
[31:5]	RESERVED	r-	0x0	Reserved
[4:4]	TX_RF_ENABLE	rw	0x0	Set to 1. turning on the driver in reader or active mode is requested. Note: According to the setting of InitialRFOn. AutoRFOn and CAOn the driver is turned after a defined time and depended on the presence of an external RF field. Note: In case of an RFActive Error this bit is cleared by HW
[3:3]	TX_COLL_AV_ENABLE	rw	0x0	Set to 1.enables automatic collision avoidance. See ISO18092 for more details.
[2:2]	TX_INITIAL_RFON	rw	0x0	Set to 1. the drivers are automatically turned on when no external field is present. In the case an external field is detected. the turning on the drivers is delay until the external field vanishes. Note: The driver on procedure must be triggered by setting TX_RF_ ENABLE. Note: This bit is reset to 0 as soon as the drivers turned on.
[1:1]	TX_AUTO_RFON	rw	0x0	Set to 1. the drivers are automatically turned on after a before present external field vanished. Note: The driver on procedure must be triggered by setting TX_ RF_ENABLE.
[0:0]	TX_AUTO_RFOFF	rw	0x0	Set to 1. the drivers are automatically turned off after data is transmitted.

9.14.1.97 CLIF_TX_DATA_CONFIG (0x6A)

This register provides the settings for CLIF_TX_DATA_CONFIG

Table 122. CLIF_TX_DATA_CONFIG (0x6A) register bit description

Bit	Symbol	Access	Value	Description
[31:19]	TX_PICC2_NUM_BYTES_2_ SEND	rw	0x0	Defines the number of bytes to be transmit in case a second PICC response is enabled. The maximum number of bytes is 260 (0x104). If the Transmission

Table 122. CLIF_TX_DATA_CONFIG (0x6A) register bit description*...continued*

Bit	Symbol	Access	Value	Description
				Of Data Is Enabled (TX_DATA_ENABLE) and TX_PICC2_NUM_BYTES_2_SEND is zero then a NO_DATA_ERROR occurs.
[18:16]	TX_LAST_BITS	rw	0x0	Defines how many bits of the last data byte to be sent. If set to 000b all bits of the last data byte are sent. Note: Bits are skipped at the end of the byte
[15:13]	TX_FIRST_BITS	rw	0x0	Defines how many bits of the first data byte to be sent. If set to 000b all bits of the last data byte are sent. Note: Bits are skipped at the beginning of the byte
[12:0]	TX_NUM_BYTES_2_SEND	rw	0x0	Defines the number of bytes to be transmit. The maximum number of bytes is 260 (0x104). If the Transmission Of Data Is Enabled (TX_DATA_ENABLE) and TX_NUM_BYTES_2_SEND is zero. then a NO_DATA_ERROR occurs.

9.14.1.98 CLIF_CONTROL (0x6B)

This register provides the settings for CLIF_CONTROL

Table 123. CLIF_CONTROL (0x6B) register bit description

Bit	Symbol	Access	Value	Description
[31:4]	RESERVED	r-	0x0	Reserved
[3:3]	START_SEND	rw	0x00	Set to logic 1. the data transmission is started. Note: This bit is only valid in combination with the Transceive command Note: If TxWait is set to a value other than zero the TxWait period configured must be expired as well that the transmission starts Note: As soon as the transmission started this bit is cleared by HW.
[2:0]	COMMAND	rw	0x00*	This registers hold the command bits
			0x00*	IDLE/StopCom Command. stops all ongoing communication and set the CLIF to IDLE mode. reset value
			0x01	Transmit command. starts a transmission immediately
			0x02	IReceive command. enables the receiver. After end of reception the bits are clear and IDLE
			0x03	ITransceive command. initiates a transceive cycle. **Note:** Depending on the value of the Initiator bit a transmission is started or the receiver is enabled **Note:** The transceive command does not finish automatically. It stays in the transceive cycle until stopped via the IDLE/StopCom command
			0x04	KeepCommand command. This command does not change the content of the command register and might be used in case other bits in the register are to be changed
			0x05	5 LoopBack command. This command is for test purposes only. It starts a transmission and at the same enables the receiver.
			0x06-0x07	Reserved: Do not use this settings

9.14.1.99 CLIF_INT_SET_ENABLE (0x6C)

This register provides the settings for CLIF_INT_SET_ENABLE

Table 124. CLIF_INT_SET_ENABLE (0x6C) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	CTS_IRQ_SET_ENABLE	w-		CTS_IRQ_SET_ENABLE
[30:29]	RESERVED	r-		RESERVED
[28:28]	TX_DATA_REQ_IRQ_SET_ENABLE	w-		TX_DATA_REQ_IRQ_SET_ENABLE

Table 124. CLIF_INT_SET_ENABLE (0x6C) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[27:27]	RX_DATA_AV_IRQ_SET_ENABLE	w-		RX_DATA_AV_IRQ_SET_ENABLE
[26:26]	RX_BUFFER_OVERFLOW_IRQ_SET_ENABLE	w-		RX_BUFFER_OVERFLOW_IRQ_SET_ENABLE
[25:25]	TX_WATERLEVEL_IRQ_SET_ENABLE	w-		TX_WATERLEVEL_IRQ_SET_ENABLE
[24:24]	RX_WATERLEVEL_IRQ_SET_ENABLE	w-		RX_WATERLEVEL_IRQ_SET_ENABLE
[23:23]	RESERVED	r-		RESERVED
[22:22]	RX_SC_DET_IRQ_SET_ENABLE	w-		RX_SC_DET_IRQ_SET_ENABLE
[21:21]	RX_SOF_DET_IRQ_SET_ENABLE	w-		RX_SOF_DET_IRQ_SET_ENABLE
[20:20]	RX_EMD_IRQ_SET_ENABLE	w-		RX_EMD_IRQ_SET_ENABLE
[19:19]	TIMER4_IRQ_SET_ENABLE	w-		TIMER4_IRQ_SET_ENABLE
[18:18]	TIMER3_IRQ_SET_ENABLE	w-		TIMER3_IRQ_SET_ENABLE
[17:17]	TIMER2_IRQ_SET_ENABLE	w-		TIMER2_IRQ_SET_ENABLE
[16:16]	TIMER1_IRQ_SET_ENABLE	w-		TIMER1_IRQ_SET_ENABLE
[15:15]	TIMER0_IRQ_SET_ENABLE	w-		TIMER0_IRQ_SET_ENABLE
[14:13]	RESERVED	r-		RESERVED
[12:12]	RF_ACTIVE_ERROR_IRQ_SET_ENABLE	w-		RF_ACTIVE_ERROR_IRQ_SET_ENABLE
[11:11]	TX_RFON_IRQ_SET_ENABLE	w-		TX_RFON_IRQ_SET_ENABLE
[10:10]	TX_RFOFF_IRQ_SET_ENABLE	w-		TX_RFOFF_IRQ_SET_ENABLE
[9:9]	RFON_DET_IRQ_SET_ENABLE	w-		RFON_DET_IRQ_SET_ENABLE
[8:8]	RFOFF_DET_IRQ_SET_ENABLE	w-		RFOFF_DET_IRQ_SET_ENABLE
[7:6]	RESERVED	r-		RESERVED
[5:5]	STATE_CHANGE_IRQ_SET_ENABLE	w-		STATE_CHANGE_IRQ_SET_ENABLE
[4:4]	CARD_ACTIVATED_IRQ_SET_ENABLE	w-		CARD_ACTIVATED_IRQ_SET_ENABLE
[3:3]	MODE_DETECTED_IRQ_SET_ENABLE	w-		MODE_DETECTED_IRQ_SET_ENABLE
[2:2]	IDLE_IRQ_SET_ENABLE	w-		IDLE_IRQ_SET_ENABLE
[1:1]	TX_IRQ_SET_ENABLE	w-		TX_IRQ_SET_ENABLE
[0:0]	RX_IRQ_SET_ENABLE	w-		RX_IRQ_SET_ENABLE

9.14.1.100 CLIF_INT_CLR_ENABLE (0x6D)

This register provides the settings for CLIF_INT_CLR_ENABLE

Table 125. CLIF_INT_CLR_ENABLE (0x6D) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	CTS_IRQ_CLR_ENABLE	w-		CTS_IRQ_CLR_ENABLE
[30:29]	RESERVED	r-		RESERVED
[28:28]	TX_DATA_REQ_IRQ_CLR_ENABLE	w-		TX_DATA_REQ_IRQ_CLR_ENABLE
[27:27]	RX_DATA_AV_IRQ_CLR_ENABLE	w-		RX_DATA_AV_IRQ_CLR_ENABLE
[26:26]	RX_BUFFER_OVERFLOW_IRQ_CLR_ENABLE	w-		RX_BUFFER_OVERFLOW_IRQ_CLR_ENABLE
[25:25]	TX_WATERLEVEL_IRQ_CLR_ENABLE	w-		TX_WATERLEVEL_IRQ_CLR_ENABLE
[24:24]	RX_WATERLEVEL_IRQ_CLR_ENABLE	w-		RX_WATERLEVEL_IRQ_CLR_ENABLE
[23:23]	RESERVED	r-		RESERVED
[22:22]	RX_SC_DET_IRQ_CLR_ENABLE	w-		RX_SC_DET_IRQ_CLR_ENABLE
[21:21]	RX_SOF_DET_IRQ_CLR_ENABLE	w-		RX_SOF_DET_IRQ_CLR_ENABLE
[20:20]	RX_EMD_IRQ_CLR_ENABLE	w-		RX_EMD_IRQ_CLR_ENABLE
[19:19]	TIMER4_IRQ_CLR_ENABLE	w-		TIMER4_IRQ_CLR_ENABLE
[18:18]	TIMER3_IRQ_CLR_ENABLE	w-		TIMER3_IRQ_CLR_ENABLE
[17:17]	TIMER2_IRQ_CLR_ENABLE	w-		TIMER2_IRQ_CLR_ENABLE
[16:16]	TIMER1_IRQ_CLR_ENABLE	w-		TIMER1_IRQ_CLR_ENABLE
[15:15]	TIMER0_IRQ_CLR_ENABLE	w-		TIMER0_IRQ_CLR_ENABLE
[14:13]	RESERVED	r-		RESERVED
[12:12]	RF_ACTIVE_ERROR_IRQ_CLR_ENABLE	w-		RF_ACTIVE_ERROR_IRQ_CLR_ENABLE
[11:11]	TX_RFON_IRQ_CLR_ENABLE	w-		TX_RFON_IRQ_CLR_ENABLE
[10:10]	TX_RFOFF_IRQ_CLR_ENABLE	w-		TX_RFOFF_IRQ_CLR_ENABLE
[9:9]	RFON_DET_IRQ_CLR_ENABLE	w-		RFON_DET_IRQ_CLR_ENABLE
[8:8]	RFOFF_DET_IRQ_CLR_ENABLE	w-		RFOFF_DET_IRQ_CLR_ENABLE
[7:6]	RESERVED	r-		RESERVED
[5:5]	STATE_CHANGE_IRQ_CLR_ENABLE	w-		STATE_CHANGE_IRQ_CLR_ENABLE
[4:4]	CARD_ACTIVATED_IRQ_CLR_ENABLE	w-		CARD_ACTIVATED_IRQ_CLR_ENABLE
[3:3]	MODE_DETECTED_IRQ_CLR_ENABLE	w-		MODE_DETECTED_IRQ_CLR_ENABLE
[2:2]	IDLE_IRQ_CLR_ENABLE	w-		IDLE_IRQ_CLR_ENABLE
[1:1]	TX_IRQ_CLR_ENABLE	w-		TX_IRQ_CLR_ENABLE

Table 125. CLIF_INT_CLR_ENABLE (0x6D) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[0:0]	RX_IRQ_CLR_ENABLE	w-		RX_IRQ_CLR_ENABLE

9.14.1.101 CLIF_INT_STATUS (0x6E)

This register provides the settings for CLIF_INT_STATUS

Table 126. CLIF_INT_STATUS (0x6E) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	CTS_IRQ	r-		Set to 1 by HW when the CLIF Test-Station wants to communicate the FW the end of an acquisition or a faulty condition.
[30:29]	RESERVED	r-		Reserved
[28:28]	TX_DATA_REQ_IRQ	r-		Set to 1 by HW when the BufferManager requests data for transmission from RAM. Note: Only valid if the bit DIRECT_DATA_ACCESS_ENABLE is set to 1
[27:27]	RX_DATA_AV_IRQ	r-		Set to 1 by HW when the BufferManager holds received data from reception to be written to RAM. Note: Only valid if the bit DIRECT_DATA_ACCESS_ ENABLE is set to 1
[26:26]	RX_BUFFER_OVERFLOW_IRQ	r-		Set to 1 by HW when the number of bytes received exceds the size of the RX buffer. Note: Reception is stoped in that case. Note: If RX_MULTIPLE is set to 1 this an this IRQ is raised when the sum of all frames exceed the RX buffer size
[25:25]	TX_WATERLEVEL_IRQ	r-		Set to 1 by HW when the number of bytes transmitted is equal to the TX_WATERLEVEL
[24:24]	RX_WATERLEVEL_IRQ	r-		Set to 1 by HW when the number of bytes received is equal to the RX_WATERLEVEL
[23:23]	RESERVED	r-		Reserved
[22:22]	RX_SC_DET_IRQ	r-		Set to 1 by HW when in reader mode a subcarrier is detected
[21:21]	RX_SOF_DET_IRQ	r-		Set to 1 by HW when in reader mode an SOF is detected
[20:20]	RX_EMD_IRQ	r-		Set to 1 by HW when an EMD event is detected
[19:19]	TIMER4_IRQ	r-		Set to 1 by HW when the Timer4 is expired.
[18:18]	TIMER3_IRQ	r-		Set to 1 by HW when the Timer3 is expired.
[17:17]	TIMER2_IRQ	r-		Set to 1 by HW when the Timer2 is expired.
[16:16]	TIMER1_IRQ	r-		Set to 1 by HW when the Timer1 is expired.
[15:15]	TIMER0_IRQ	r-		Set to 1 by HW when the Timer0 is expired.
[14:13]	RESERVED	r-		Reserved
[12:12]	RF_ACTIVE_ERROR_IRQ	r-		Set to 1 by HW when an RF error case occurred
[11:11]	TX_RFON_IRQ	r-		Set to 1 by HW when the internally generated RF-field was switched on.

Table 126. CLIF_INT_STATUS (0x6E) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[10:10]	TX_RFOFF_IRQ	r-		Set to 1 by HW when the internally generated RF-field was switched off.
[9:9]	RFON_DET_IRQ	r-		Set to 1 by HW when an external RF-field is detected.
[8:8]	RFOFF_DET_IRQ	r-		Set to 1 by HW when an until then preset external RF-field is switched off.
[7:6]	RESERVED	r-		Reserved
[5:5]	STATE_CHANGE_IRQ	r-		Set to 1 by HW when a transceive state is entered selected in the register field STATE_TRIGGER_ SELECT
[4:4]	CARD_ACTIVATED_IRQ	r-		Set to 1 by HW when TypeA card mode activation FSM reached the ACTIVATED or ACTIVATE_S state
[3:3]	MODE_DETECTED_IRQ	r-		Set to 1 by HW when the card mode has been detected by the ModeDetector Note: While the TypeA activation FSM is active no IRQ is issued any more
[2:2]	IDLE_IRQ	r-		Set to 1 by HW when the IDLE state is entered
[1:1]	TX_IRQ	r-		Set to 1 by HW when an ongoing transmission is finished.
[0:0]	RX_IRQ	r-		Set to 1 by HW when an ongoing reception is finished

9.14.1.102 CLIF_INT_ENABLE (0x6F)

This register provides the settings for CLIF_INT_ENABLE

Table 127. CLIF_INT_ENABLE (0x6F) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	CTS_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[30:29]	RESERVED	r-	0x0	Reserved
[28:28]	TX_DATA_REQ_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[27:27]	RX_DATA_AV_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[26:26]	RX_BUFFER_OVERFLOW_ IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[25:25]	TX_WATERLEVEL_IRQ_ ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[24:24]	RX_WATERLEVEL_IRQ_ ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[23:23]	RESERVED	r-	0x0	Reserved
[22:22]	RX_SC_DET_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[21:21]	RX_SOF_DET_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.

Table 127. CLIF_INT_ENABLE (0x6F) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[20:20]	RX_EMD_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[19:19]	TIMER4_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[18:18]	TIMER3_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[17:17]	TIMER2_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[16:16]	TIMER1_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[15:15]	TIMER0_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[14:13]	RESERVED	r-	0x0	Reserved
[12:12]	RF_ACTIVE_ERROR_IRQ_ ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[11:11]	TX_RFON_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[10:10]	TX_RFOFF_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[9:9]	RFON_DET_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[8:8]	RFOFF_DET_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[7:6]	RESERVED	r-	0x0	Reserved
[5:5]	STATE_CHANGE_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[4:4]	CARD_ACTIVATED_IRQ_ ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[3:3]	MODE_DETECTED_IRQ_ ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[2:2]	IDLE_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[1:1]	TX_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.
[0:0]	RX_IRQ_ENABLE	r-	0x0	When this bit is set to 1 the corresponding status bit is enabled to propagate to the CORE IRQ controller.

9.14.1.103 CLIF_INT_CLR_STATUS (0x70)

This register provides the settings for CLIF_INT_CLR_STATUS

Table 128. CLIF_INT_CLR_STATUS (0x70) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	CTS_IRQ_CLR_STATUS	w-		CTS_IRQ_CLR_STATUS

Table 128. CLIF_INT_CLR_STATUS (0x70) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[30:29]	RESERVED	r-		RESERVED
[28:28]	TX_DATA_REQ_IRQ_CLR_STATUS	w-		TX_DATA_REQ_IRQ_CLR_STATUS
[27:27]	RX_DATA_AV_IRQ_CLR_STATUS	w-		RX_DATA_AV_IRQ_CLR_STATUS
[26:26]	RX_BUFFER_OVERFLOW_IRQ_CLR_STATUS	w-		RX_BUFFER_OVERFLOW_IRQ_CLR_STATUS
[25:25]	TX_WATERLEVEL_IRQ_CLR_STATUS	w-		TX_WATERLEVEL_IRQ_CLR_STATUS
[24:24]	RX_WATERLEVEL_IRQ_CLR_STATUS	w-		RX_WATERLEVEL_IRQ_CLR_STATUS
[23:23]	RESERVED	r-		RESERVED
[22:22]	RX_SC_DET_IRQ_CLR_STATUS	w-		RX_SC_DET_IRQ_CLR_STATUS
[21:21]	RX_SOF_DET_IRQ_CLR_STATUS	w-		RX_SOF_DET_IRQ_CLR_STATUS
[20:20]	RX_EMD_IRQ_CLR_STATUS	w-		RX_EMD_IRQ_CLR_STATUS
[19:19]	TIMER4_IRQ_CLR_STATUS	w-		TIMER4_IRQ_CLR_STATUS
[18:18]	TIMER3_IRQ_CLR_STATUS	w-		TIMER3_IRQ_CLR_STATUS
[17:17]	TIMER2_IRQ_CLR_STATUS	w-		TIMER2_IRQ_CLR_STATUS
[16:16]	TIMER1_IRQ_CLR_STATUS	w-		TIMER1_IRQ_CLR_STATUS
[15:15]	TIMER0_IRQ_CLR_STATUS	w-		TIMER0_IRQ_CLR_STATUS
[14:13]	RESERVED	r-		RESERVED
[12:12]	RF_ACTIVE_ERROR_IRQ_CLR_STATUS	w-		RF_ACTIVE_ERROR_IRQ_CLR_STATUS
[11:11]	TX_RFON_IRQ_CLR_STATUS	w-		TX_RFON_IRQ_CLR_STATUS
[10:10]	TX_RFOFF_IRQ_CLR_STATUS	w-		TX_RFOFF_IRQ_CLR_STATUS
[9:9]	RFON_DET_IRQ_CLR_STATUS	w-		RFON_DET_IRQ_CLR_STATUS
[8:8]	RFOFF_DET_IRQ_CLR_STATUS	w-		RFOFF_DET_IRQ_CLR_STATUS
[7:6]	RESERVED	r-		RESERVED
[5:5]	STATE_CHANGE_IRQ_CLR_STATUS	w-		STATE_CHANGE_IRQ_CLR_STATUS
[4:4]	CARD_ACTIVATED_IRQ_CLR_STATUS	w-		CARD_ACTIVATED_IRQ_CLR_STATUS
[3:3]	MODE_DETECTED_IRQ_CLR_STATUS	w-		MODE_DETECTED_IRQ_CLR_STATUS
[2:2]	IDLE_IRQ_CLR_STATUS	w-		IDLE_IRQ_CLR_STATUS
[1:1]	TX_IRQ_CLR_STATUS	w-		TX_IRQ_CLR_STATUS
[0:0]	RX_IRQ_CLR_STATUS	w-		RX_IRQ_CLR_STATUS

9.14.1.104 BMA_INT_ENABLE (0x71)

This register provides the settings for BMA_INT_ENABLE

Table 129. BMA_INT_ENABLE (0x71) register bit description

Bit	Symbol	Access	Value	Description
[31:7]	RESERVED	r-	0x00	reserved
[6:6]	BMA_AHB_ERROR_ENABLE	r-	0x00	enable of functional interrupt AHB slave error
[5:5]	BMA_ADDR_RANGE_ERROR_ENABLE	r-	0x00	enable of functional interrupt Absolute address incompatible with SRAM mapping
[4:4]	RESERVED	r-	0x00	reserved
[3:3]	RESERVED	r-	0x00	reserved
[2:2]	RESERVED	r-	0x00	reserved
[1:1]	CLIF_SYS_ERROR_ENABLE	r-	0x00	enable of functional interrupt System error in Contactless interface
[0:0]	HOSTIF_SYS_ERROR_ENABLE	r-	0x00	enable of functional interrupt System error in Host interface

9.14.1.105 BMA_INT_CLR_ENABLE (0x72)

This register provides the settings for BMA_INT_CLR_ENABLE

Table 130. BMA_INT_CLR_ENABLE (0x72) register bit description

Bit	Symbol	Access	Value	Description
[31:7]	RESERVED	w-	0x00	reserved
[6:6]	BMA_AHB_ERROR_CLR_ENABLE	w-	0x00	clr of functional interrupt AHB slave error
[5:5]	BMA_ADDR_RANGE_ERROR_CLR_ENABLE	w-	0x00	clr of functional interrupt Absolute address incompatible with SRAM mapping
[4:4]	RESERVED	r-	0x00	reserved
[3:3]	RESERVED	r-	0x00	reserved
[2:2]	RESERVED	r-	0x00	reserved
[1:1]	CLIF_SYS_ERROR_CLR_ENABLE	w-	0x00	clr of functional interrupt System error in Contactless interface
[0:0]	HOSTIF_SYS_ERROR_CLR_ENABLE	w-	0x00	clr of functional interrupt System error in Host interface

9.14.1.106 BMA_INT_SET_ENABLE (0x73)

This register provides the settings for BMA_INT_SET_ENABLE

Table 131. BMA_INT_SET_ENABLE (0x73) register bit description

Bit	Symbol	Access	Value	Description
[31:7]	RESERVED	w-	0x00	reserved
[6:6]	BMA_AHB_ERROR_SET_ENABLE	w-	0x00	set of functional interrupt AHB slave error

Table 131. BMA_INT_SET_ENABLE (0x73) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[5:5]	BMA_ADDR_RANGE_ERROR_SET_ENABLE	w-	0x00	set of functional interrupt Absolute address incompatible with SRAM mapping
[4:4]	RESERVED	r-	0x00	reserved
[3:3]	RESERVED	r-	0x00	reserved
[2:2]	RESERVED	r-	0x00	reserved
[1:1]	CLIF_SYS_ERROR_SET_ENABLE	w-	0x00	set of functional interrupt System error in Contactless interface
[0:0]	HOSTIF_SYS_ERROR_SET_ENABLE	w-	0x00	set of functional interrupt System error in Host interface

9.14.1.107 BMA_INT_STATUS (0x74)

This register provides the settings for BMA_INT_STATUS

Table 132. BMA_INT_STATUS (0x74) register bit description

Bit	Symbol	Access	Value	Description
[31:7]	RESERVED	r-	0x00	reserved
[6:6]	BMA_AHB_ERROR_STATUS	r-	0x00	status of functional interrupt AHB slave error
[5:5]	BMA_ADDR_RANGE_ERROR_STATUS	r-	0x00	status of functional interrupt Absolute address incompatible with SRAM mapping
[4:4]	RESERVED	r-	0x00	reserved
[3:3]	RESERVED	r-	0x00	reserved
[2:2]	RESERVED	r-	0x00	reserved
[1:1]	CLIF_SYS_ERROR_STATUS	r-	0x00	status of functional interrupt System error in Contactless interface
[0:0]	HOSTIF_SYS_ERROR_STATUS	r-	0x00	status of functional interrupt System error in Host interface

9.14.1.108 BMA_INT_CLR_STATUS (0x75)

This register provides the settings for BMA_INT_CLR_STATUS

Table 133. BMA_INT_CLR_STATUS (0x75) register bit description

Bit	Symbol	Access	Value	Description
[31:7]	RESERVED	w-	0x00	reserved
[6:6]	BMA_AHB_ERROR_CLR_STATUS	w-	0x00	clr of functional interrupt AHB slave error
[5:5]	BMA_ADDR_RANGE_ERROR_CLR_STATUS	w-	0x00	clr of functional interrupt Absolute address incompatible with SRAM mapping
[4:4]	RESERVED	r-	0x00	reserved
[3:3]	RESERVED	r-	0x00	reserved
[2:2]	RESERVED	r-	0x00	reserved

Table 133. BMA_INT_CLR_STATUS (0x75) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[1:1]	CLIF_SYS_ERROR_CLR_STATUS	w-	0x00	clr of functional interrupt System error in Contactless interface
[0:0]	HOSTIF_SYS_ERROR_CLR_STATUS	w-	0x00	clr of functional interrupt System error in Host interface

9.14.1.109 CLIF_SS_TX1_RTRANS0 (0x80)

This register provides the settings for CLIF_SS_TX1_RTRANS0

Table 134. CLIF_SS_TX1_RTRANS0 (0x80) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_RTRANS3	rw	0x00	TX1 rising transition value 3
[23:16]	TX1_SS_RTRANS2	rw	0x00	TX1 rising transition value 2
[15:8]	TX1_SS_RTRANS1	rw	0x00	TX1 rising transition value 1
[7:0]	TX1_SS_RTRANS0	rw	0x00	TX1 rising transition value 0

9.14.1.110 CLIF_SS_TX1_RTRANS1 (0x81)

This register provides the settings for CLIF_SS_TX1_RTRANS1

Table 135. CLIF_SS_TX1_RTRANS1 (0x81) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_RTRANS7	rw	0x00	TX1 rising transition value 7
[23:16]	TX1_SS_RTRANS6	rw	0x00	TX1 rising transition value 6
[15:8]	TX1_SS_RTRANS5	rw	0x00	TX1 rising transition value 5
[7:0]	TX1_SS_RTRANS4	rw	0x00	TX1 rising transition value 4

9.14.1.111 CLIF_SS_TX1_RTRANS2 (0x82)

This register provides the settings for CLIF_SS_TX1_RTRANS2

Table 136. CLIF_SS_TX1_RTRANS2 (0x82) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_RTRANS11	rw	0x00	TX1 rising transition value 11
[23:16]	TX1_SS_RTRANS10	rw	0x00	TX1 rising transition value 10
[15:8]	TX1_SS_RTRANS9	rw	0x00	TX1 rising transition value 9
[7:0]	TX1_SS_RTRANS8	rw	0x00	TX1 rising transition value 8

9.14.1.112 CLIF_SS_TX1_RTRANS3 (0x83)

This register provides the settings for CLIF_SS_TX1_RTRANS3

Table 137. CLIF_SS_TX1_RTRANS3 (0x83) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_RTRANS15	rw	0x00	TX1 rising transition value 15
[23:16]	TX1_SS_RTRANS14	rw	0x00	TX1 rising transition value 14
[15:8]	TX1_SS_RTRANS13	rw	0x00	TX1 rising transition value 13
[7:0]	TX1_SS_RTRANS12	rw	0x00	TX1 rising transition value 12

9.14.1.113 CLIF_SS_TX2_RTRANS0 (0x84)

This register provides the settings for CLIF_SS_TX2_RTRANS0

Table 138. CLIF_SS_TX2_RTRANS0 (0x84) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_RTRANS3	rw	0x00	TX2 rising transition value 3
[23:16]	TX2_SS_RTRANS2	rw	0x00	TX2 rising transition value 2
[15:8]	TX2_SS_RTRANS1	rw	0x00	TX2 rising transition value 1
[7:0]	TX2_SS_RTRANS0	rw	0x00	TX2 rising transition value 0

9.14.1.114 CLIF_SS_TX2_RTRANS1 (0x85)

This register provides the settings for CLIF_SS_TX2_RTRANS1

Table 139. CLIF_SS_TX2_RTRANS1 (0x85) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_RTRANS7	rw	0x00	TX2 rising transition value 7
[23:16]	TX2_SS_RTRANS6	rw	0x00	TX2 rising transition value 6
[15:8]	TX2_SS_RTRANS5	rw	0x00	TX2 rising transition value 5
[7:0]	TX2_SS_RTRANS4	rw	0x00	TX2 rising transition value 4

9.14.1.115 CLIF_SS_TX2_RTRANS2 (0x86)

This register provides the settings for CLIF_SS_TX2_RTRANS2

Table 140. CLIF_SS_TX2_RTRANS2 (0x86) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_RTRANS11	rw	0x00	TX2 rising transition value 11
[23:16]	TX2_SS_RTRANS10	rw	0x00	TX2 rising transition value 10
[15:8]	TX2_SS_RTRANS9	rw	0x00	TX2 rising transition value 9
[7:0]	TX2_SS_RTRANS8	rw	0x00	TX2 rising transition value 8

9.14.1.116 CLIF_SS_TX2_RTRANS3 (0x87)

This register provides the settings for CLIF_SS_TX2_RTRANS3

Table 141. CLIF_SS_TX2_RTRANS3 (0x87) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_RTRANS15	rw	0x00	TX2 rising transition value 15
[23:16]	TX2_SS_RTRANS14	rw	0x00	TX2 rising transition value 14
[15:8]	TX2_SS_RTRANS13	rw	0x00	TX2 rising transition value 13
[7:0]	TX2_SS_RTRANS12	rw	0x00	TX2 rising transition value 12

9.14.1.117 CLIF_SS_TX1_FTRANS0 (0x88)

This register provides the settings for CLIF_SS_TX1_FTRANS0

Table 142. CLIF_SS_TX1_FTRANS0 (0x88) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_FTRANS3	rw	0x00	TX1 falling transition value 3
[23:16]	TX1_SS_FTRANS2	rw	0x00	TX1 falling transition value 2
[15:8]	TX1_SS_FTRANS1	rw	0x00	TX1 falling transition value 1
[7:0]	TX1_SS_FTRANS0	rw	0x00	TX1 falling transition value 0

9.14.1.118 CLIF_SS_TX1_FTRANS1 (0x89)

This register provides the settings for CLIF_SS_TX1_FTRANS1

Table 143. CLIF_SS_TX1_FTRANS1 (0x89) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_FTRANS7	rw	0x00	TX1 falling transition value 7
[23:16]	TX1_SS_FTRANS6	rw	0x00	TX1 falling transition value 6
[15:8]	TX1_SS_FTRANS5	rw	0x00	TX1 falling transition value 5
[7:0]	TX1_SS_FTRANS4	rw	0x00	TX1 falling transition value 4

9.14.1.119 CLIF_SS_TX1_FTRANS2 (0x8A)

This register provides the settings for CLIF_SS_TX1_FTRANS2

Table 144. CLIF_SS_TX1_FTRANS2 (0x8A) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_FTRANS11	rw	0x00	TX1 falling transition value 11
[23:16]	TX1_SS_FTRANS10	rw	0x00	TX1 falling transition value 10
[15:8]	TX1_SS_FTRANS9	rw	0x00	TX1 falling transition value 9
[7:0]	TX1_SS_FTRANS8	rw	0x00	TX1 falling transition value 8

9.14.1.120 CLIF_SS_TX1_FTRANS3 (0x8B)

This register provides the settings for CLIF_SS_TX1_FTRANS3

Table 145. CLIF_SS_TX1_FTRANS3 (0x8B) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_FTRANS15	rw	0x00	TX1 falling transition value 15
[23:16]	TX1_SS_FTRANS14	rw	0x00	TX1 falling transition value 14
[15:8]	TX1_SS_FTRANS13	rw	0x00	TX1 falling transition value 13
[7:0]	TX1_SS_FTRANS12	rw	0x00	TX1 falling transition value 12

9.14.1.121 CLIF_SS_TX2_FTRANS0 (0x8C)

This register provides the settings for CLIF_SS_TX2_FTRANS0

Table 146. CLIF_SS_TX2_FTRANS0 (0x8C) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_FTRANS3	rw	0x00	TX2 falling transition value 3
[23:16]	TX2_SS_FTRANS2	rw	0x00	TX2 falling transition value 2
[15:8]	TX2_SS_FTRANS1	rw	0x00	TX2 falling transition value 1
[7:0]	TX2_SS_FTRANS0	rw	0x00	TX2 falling transition value 0

9.14.1.122 CLIF_SS_TX2_FTRANS1 (0x8D)

This register provides the settings for CLIF_SS_TX2_FTRANS1

Table 147. CLIF_SS_TX2_FTRANS1 (0x8D) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_FTRANS7	rw	0x00	TX2 falling transition value 7
[23:16]	TX2_SS_FTRANS6	rw	0x00	TX2 falling transition value 6
[15:8]	TX2_SS_FTRANS5	rw	0x00	TX2 falling transition value 5
[7:0]	TX2_SS_FTRANS4	rw	0x00	TX2 falling transition value 4

9.14.1.123 CLIF_SS_TX2_FTRANS2 (0x8E)

This register provides the settings for CLIF_SS_TX2_FTRANS2

Table 148. CLIF_SS_TX2_FTRANS2 (0x8E) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_FTRANS11	rw	0x00	TX2 falling transition value 11
[23:16]	TX2_SS_FTRANS10	rw	0x00	TX2 falling transition value 10
[15:8]	TX2_SS_FTRANS9	rw	0x00	TX2 falling transition value 9
[7:0]	TX2_SS_FTRANS8	rw	0x00	TX2 falling transition value 8

9.14.1.124 CLIF_SS_TX2_FTRANS3 (0x8F)

This register provides the settings for CLIF_SS_TX2_FTRANS3

Table 149. CLIF_SS_TX2_FTRANS3 (0x8F) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_FTRANS15	rw	0x00	TX2 falling transition value 15
[23:16]	TX2_SS_FTRANS14	rw	0x00	TX2 falling transition value 14
[15:8]	TX2_SS_FTRANS13	rw	0x00	TX2 falling transition value 13
[7:0]	TX2_SS_FTRANS12	rw	0x00	TX2 falling transition value 12

9.14.2 PCRM Register description

The application can make use of the PCRM registers to configure the various IOs, pad settings, boot status of the IC.

The default setting of a bit within a register is indicated by the "*" or "Reset Value". Value indicates the allowed range for the bits of a symbol.

9.14.2.1 List of PCRM registers

List of registers and its addresses

Table 150. List of PCRM registers

Register Name	Register address (Hex)	Register address (Decimal)	Default Value
REG_PCRM_PMU_ANA_CTRL (0xA0)	0xA0	160	0x00000040
REF_PCRM_INT_SET_STATUS (0xA1)	0xA1	161	0x00000000
PCRM_INT_CLR_STATUS (0xA2)	0xA2	162	0x00000000
PCRM_INT_ENABLE (0xA3)	0xA3	163	0x00000000
PCRM_INT_STATUS (0xA4)	0xA4	164	0x00000000
PCRM_INT_SET_ENABLE (0xA5)	0xA5	165	0x00000000
PCRM_INT_CLR_ENABLE (0xA6)	0xA6	166	0x00000000
PCRM_PAD_GPIO5 (0xA7)	0xA7	167	0x00000004
PCRM_PAD_GPIO4 (0xA8)	0xA8	168	0x00000004
PCRM_ULPCD_STS (0xA9)	0xA9	169	0x00000000
PCRM_PMU_ANA_STS2 (0xAA)	0xAA	170	0x00000002
PCRM_PMU_ANA_MISC_CTRL (0xAB)	0xAB	171	0x00000000
PCRM_PMU_ANA_VBAT_MON2 (0xAC)	0xAC	172	0x00000000
PCRM_DIG_VBUS_DEBOUNCE_CTRL (0xAD)	0xAD	173	0x00000474
PCRM_INT_EDGE_SEL (0xAE)	0xAE	174	0x00000000
PCRM_VDDIO_LOSS_DET_DISABLE (0xAF)	0xAF	175	0x00000000
PCRM_VDDIO_LOSS_DET_ENABLE (0xB0)	0xB0	176	0x00000000
PCRM_PAD_DWL_REQ (0xB1)	0xB1	177	0x00000011
PCRM_PAD_IRQ (0xB2)	0xB2	178	0x00000012
PCRM_PAD_ATX_D (0xB3)	0xB3	179	0x00000021
PCRM_PAD_ATX_C (0xB4)	0xB4	180	0x00000021

Table 150. List of PCRM registers*...continued*

Register Name	Register address (Hex)	Register address (Decimal)	Default Value
PCRM_PAD_ATX_A (0xB5)	0xB5	181	0x00000051
PCRM_PAD_ATX_B (0xB6)	0xB6	182	0x00000051
PCRM_PAD_GPIO3 (0xB7)	0xB7	183	0x00000002
PCRM_PAD_GPIO2 (0xB8)	0xB8	184	0x00000002
PCRM_PAD_GPIO1 (0xB9)	0xB9	185	0x00000003
PCRM_PAD_GPIO0 (0xBA)	0xBA	186	0x0000000F
PCRM_PADOUT (0xBB)	0xBB	187	0x000000F0
PCRM_PADIN (0xBC)	0xBC	188	0x00000400
PCRM_GPREG7 (0xBD)	0xBD	189	0x00000000
PCRM_GPREG6 (0xBE)	0xBE	190	0x00000000
PCRM_GPREG5 (0xBF)	0xBF	191	0x00000000
PCRM_GPREG4 (0xC0)	0xC0	192	0x00000000
PCRM_GPREG3 (0xC1)	0xC1	193	0x00000706
PCRM_CLIF_ANA_TX_STANDBY (0xC2)	0xC2	194	0x009FFFFF
PCRM_SYS_LP_CLK_EN (0xC3)	0xC3	195	0x00000000
PCRM_SYS_BOOT3_STS (0xC4)	0xC4	196	0x00000071
PCRM_SYS_BOOT2_STS (0xC5)	0xC5	197	0x03FFFCDE
PCRM_SYS_BOOT1_STS (0xC6)	0xC6	198	0x00000000
PCRM_SYS_STBY1_CTRL (0xC7)	0xC7	199	0x00020000
PCRM_SYS_ULPCD_CTRL (0xC8)	0xC8	200	0x00000000
PCRM_SYS_STBY_CTRL (0xC9)	0xC9	201	0x00000000
PCRM_SYS_STBY_CFG (0xCA)	0xCA	202	0x00000000
PCRM_CLIF_ANA_AGC_RXPROT_CTRL (0xCB)	0xCB	203	0x00000000
PCRM_LPDET_FSM_CTRL2 (0xCC)	0xCC	204	0x00000000
PCRM_LPDET_FSM_CTRL1 (0xCD)	0xCD	205	0x00000000
PCRM_CLIF_ANA_XTAL (0xCE)	0xCE	206	0x00000040
PCRM_PMU_ANA_VEN_MON (0xCF)	0xCF	207	0x00000FFF
PCRM_PMU_ANA_VBAT_MON (0xD0)	0xD0	208	0x00000000
PCRM_PMU_ANA_TEMP_SNS_CTRL (0xD1)	0xD1	209	0x00000000
PCRM_PMU_ANA_VMON_CTRL (0xD2)	0xD2	210	0x00000000
PCRM_CFG_OFFPLUS (0xD3)	0xD3	211	0x00000000
PCRM_PAD_AUX_3 (0xD4)	0xD4	212	0x00000012
PCRM_PAD_AUX_2 (0xD5)	0xD5	213	0x00000012
PCRM_PAD_AUX_1 (0xD6)	0xD6	214	0x00000012
PCRM_SYS_SUSPEND_CTRL (0xD7)	0xD7	215	0x00000000
PCRM_PAD_SPIM_MISO (0xD8)	0xD8	216	0x00000004

Table 150. List of PCRM registers*...continued*

Register Name	Register address (Hex)	Register address (Decimal)	Default Value
PCRM_PAD_SPIM_MOSI (0xD9)	0xD9	217	0x00000004
PCRM_PAD_SPIM_SCLK (0xDA)	0xDA	218	0x00000004
PCRM_PAD_SPIM_SSN (0xDB)	0xDB	219	0x00000004
PCRM_PAD_I2CM_SCL (0xDC)	0xDC	220	0x00000004
PCRM_PAD_I2CM_SDA (0xDD)	0xDD	221	0x00000004
PCRM_PAD_CTAUX_IO (0xDE)	0xDE	222	0x00000005
PCRM_PAD_CTAUX_CLK (0xDF)	0xDF	223	0x00000005
PCRM_PAD_CTAUX_INT (0xE0)	0xE0	224	0x00000005
PCRM_CLIF_ULPDET_DISABLE (0xE1)	0xE1	225	0x00000000
PCRM_CLIF_ULPDET_ENABLE (0xE2)	0xE2	226	0x00000000
PCRM_ANA_USBPLL_MODE (0xE3)	0xE3	227	0x00000000
PCRM_ANA_USBPLL_DIV (0xE4)	0xE4	228	0x0500B10A
PCRM_ULPCD_CTRL3 (0xE5)	0xE5	229	0x00000000
PCRM_ULPCD_CTRL2 (0xE6)	0xE6	230	0x00000050
PCRM_ULPCD_CTRL1 (0xE7)	0xE7	231	0x007F0000
PCRM_ULPCD_CTRL0 (0xE8)	0xE8	232	0x14590000
PCRM_HP_ULPCD_STS (0xE9)	0xE9	233	0x00000000
PCRM_PMU_ANA_SMPS_CTRL (0xEA)	0xEA	234	0x00100000
PCRM_ULPCD_CTRL4 (0xEB)	0xEB	235	0x00000000
PCRM_ANA_USBPLL_STS (0xEC)	0xEC	236	0x00000000
PCRM_ANA_USBPLL_CTRL (0xED)	0xED	237	0x00000000
PCRM_ANA_USBPLL_BW (0xEE)	0xEE	238	0x00005BF0
PCRM_CLIF_DAC (0xEF)	0xEF	239	0x06000600
PCRM_HP_SYS_CLK_EN (0xF0)	0xF0	240	0x08000000
PCRM_SYS_CLK_MUX_SEL (0xF1)	0xF1	241	0x0000000E

9.14.2.2 REG_PCRM_PMU_ANA_CTRL (0xA0)

This register provides to enable the external input to GPADC AD1 pin.

Note:

Please use the GPADC driver APIs for enable/disable of external input on GPADC AD1 pin.

Table 151. REG_PCRM_PMU_ANA_CTRL (0xA0) register bit description

Bit	Symbol	Access	Value	Description
[31:18]	RESERVED	r-	0x00	reserved
[17:17]	AD1_MUX_SEL	rw	0x00	to Enable external input to GPADC
[16:0]	RESERVED	rw	0x00	reserved

9.14.2.3 REF_PCRM_INT_SET_STATUS (0xA1)

This register sets the interrupt status.

Note:

Setting of the interrupt status (triggering interrupt) shall be used during development of application software.

Table 152. REF_PCRM_INT_SET_STATUS (0xA1) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x00	reserved
[30:30]	SUSPEND_IRQ_SET_STATUS	-w	0x00	suspend interrupt
[29:29]	SUSPEND_PREV_IRQ_SET_STATUS	-w	0x00	suspend Prevention interrupt
[28:28]	PVDDLDO_OVERCURRENT_IRQ_SET_STATUS	-w	0x00	PVDDLDO Overcurrent interrupt
[27:27]	RESERVED	r-	0x00	reserved
[26:26]	OVERCURRENT_IRQ_SET_STATUS	-w	0x00	Over Current interrupt
[25:25]	VUP_OK_IRQ_SET_STATUS	-w	0x00	VUP_OK edge interrupt
[24:24]	RESERVED	-w	0x00	reserved
[23:23]	USB_VBUS_PRESENT_IRQ_SET_STATUS	-w	0x00	USB VBUS Present
[22:22]	RESERVED	r-	0x00	reserved
[21:21]	LPDET_IRQ_SET_STATUS	-w	0x00	LPDET interrupt
[20:20]	STBY_PREV_IRQ_SET_STATUS	-w	0x00	standby Prevention interrupt
[17:17]	OVER_TEMP_NFC_IRQ_ENABLE	-w	0x00	CLIF TWARN Up or Down interrupt
[16:16]	ADC_DATA_7_IRQ_SET_STATUS	-w	0x00	GPADC channel 7 interrupt
[15:15]	ADC_DATA_6_IRQ_SET_STATUS	-w	0x00	GPADC channel 6 interrupt
[14:14]	ADC_DATA_5_IRQ_SET_STATUS	-w	0x00	GPADC channel 5 interrupt
[13:13]	ADC_DATA_4_IRQ_SET_STATUS	-w	0x00	GPADC channel 4 interrupt
[12:12]	ADC_DATA_3_IRQ_SET_STATUS	-w	0x00	GPADC channel 3 interrupt
[11:11]	ADC_DATA_2_IRQ_SET_STATUS	-w	0x00	GPADC channel 2 interrupt
[10:10]	ADC_DATA_1_IRQ_SET_STATUS	-w	0x00	GPADC channel 1 interrupt
[9:9]	ADC_DATA_0_IRQ_SET_STATUS	-w	0x00	GPADC channel 0 interrupt
[8:8]	GPIO_COMMON_IRQ_SET_STATUS	-w	0x00	Common GPIO IRQ (OR condition of GPIO0,1,2,3)

Table 152. REF_PCRM_INT_SET_STATUS (0xA1) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[7:7]	RESERVED	r-	0x00	reserved
[6:5]	RESERVED	-w	0x00	reserved
[4:4]	VDDIO_OK_IRQ_SET_STATUS	-w	0x00	VDDIO OK interrupt
[3:3]	GPIO3_ZIF_IRQ_SET_STATUS	-w	0x00	GPIO3 IRQ
[2:2]	GPIO2_ZIF_IRQ_SET_STATUS	-w	0x00	GPIO2 IRQ
[1:1]	GPIO1_ZIF_IRQ_SET_STATUS	-w	0x00	GPIO1 IRQ
[0:0]	GPIO0_ZIF_IRQ_SET_STATUS	-w	0x00	GPIO0 IRQ

9.14.2.4 PCRM_INT_CLR_STATUS (0xA2)

This register clears the interrupt status

Table 153. PCRM_INT_CLR_STATUS (0xA2) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x00	reserved
[30:30]	SUSPEND_IRQ_CLEAR_STATUS	-w	0x00	suspend interrupt
[29:29]	SUSPEND_PREV_IRQ_CLEAR_STATUS	-w	0x00	suspend Prevention interrupt
[28:28]	PVDDLDO_OVERCURRENT_IRQ_CLEAR_STATUS	-w	0x00	PVDDLDO Overcurrent interrupt
[27:27]	RESERVED	r-	0x00	reserved
[25:25]	VUP_OK_IRQ_CLEAR_STATUS	-w	0x00	VUP_OK edge interrupt
[24:24]	RESERVED	-w	0x00	reserved
[23:23]	USB_VBUS_PRESENT_IRQ_CLEAR_STATUS	-w	0x00	USB VBUS Present
[22:22]	RESERVED	r-	0x00	reserved
[21:21]	LPDET_IRQ_CLEAR_STATUS	-w	0x00	LPDET interrupt
[20:20]	STBY_PREV_IRQ_CLEAR_STATUS	-w	0x00	stby prevention interrupt
[19:19]	VBAT_MON2_LOW_IRQ_CLEAR_STATUS	-w	0x00	VBAT Monitor2 Low
[18:18]	OVER_TEMP_PMU_IRQ_CLEAR_STATUS	-w	0x00	PMU TWARN Up or Down interrupt
[17:17]	OVER_TEMP_NFC_IRQ_ENABLE	-w	0x00	CLIF TWARN Up or Down interrupt
[16:16]	ADC_DATA_7_IRQ_CLEAR_STATUS	-w	0x00	GPADC channel 7 interrupt
[15:15]	ADC_DATA_6_IRQ_CLEAR_STATUS	-w	0x00	GPADC channel 6 interrupt
[14:14]	ADC_DATA_5_IRQ_CLEAR_STATUS	-w	0x00	GPADC channel 5 interrupt

Table 153. PCRM_INT_CLR_STATUS (0xA2) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[13:13]	ADC_DATA_4_IRQ_CLEAR_STATUS	-w	0x00	GPADC channel 4 interrupt
[12:12]	ADC_DATA_3_IRQ_CLEAR_STATUS	-w	0x00	GPADC channel 3 interrupt
[11:11]	ADC_DATA_2_IRQ_CLEAR_STATUS	-w	0x00	GPADC channel 2 interrupt
[10:10]	ADC_DATA_1_IRQ_CLEAR_STATUS	-w	0x00	GPADC channel 1 interrupt
[9:9]	ADC_DATA_0_IRQ_CLEAR_STATUS	-w	0x00	GPADC channel 0 interrupt
[7:7]	RESERVED	r-	0x00	reserved
[6:5]	RESERVED	-w	0x00	reserved
[4:4]	VDDIO_OK_IRQ_CLEAR_STATUS	-w	0x00	VDDIO OK interrupt
[3:3]	GPIO3_ZIF_IRQ_CLEAR_STATUS	-w	0x00	GPIO3 IRQ
[2:2]	GPIO2_ZIF_IRQ_CLEAR_STATUS	-w	0x00	GPIO2 IRQ
[1:1]	GPIO1_ZIF_IRQ_CLEAR_STATUS	-w	0x00	GPIO1 IRQ
[0:0]	GPIO0_ZIF_IRQ_CLEAR_STATUS	-w	0x00	GPIO0 IRQ

9.14.2.5 PCRM_INT_ENABLE (0xA3)

This register enables the interrupts for the functionality required.

Table 154. PCRM_INT_ENABLE (0xA3) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x00	reserved
[30:30]	SUSPEND_IRQ_ENABLE	r-	0x00	suspend interrupt
[29:29]	SUSPEND_PREV_IRQ_ENABLE	r-	0x00	suspend Prevention interrupt
[28:28]	PVDDLDO_OVERCURRENT_IRQ_ENABLE	r-	0x00	PVDDLDO Overcurrent interrupt
[27:27]	RESERVED	r-	0x00	reserved
[26:26]	OVERCURRENT_IRQ_ENABLE	r-	0x00	OVERCURRENT interrupt
[25:25]	VUP_OK_IRQ_ENABLE	r-	0x00	VUP_OK edge interrupt
[24:24]	RESERVED	r-	0x00	reserved
[23:23]	USB_VBUS_PRESENT_IRQ_IRQ_ENABLE	r-	0x00	USB VBUS Present
[22:22]	RESERVED	r-	0x00	reserved
[21:21]	LPDET_IRQ_ENABLE	r-	0x00	LPDET interrupt

Table 154. PCRM_INT_ENABLE (0xA3) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[20:20]	STBY_PREV_IRQ_ENABLE	r-	0x00	USB suspend Prev interrupt
[19:19]	VBAT_MON2_LOW_IRQ_ENABLE	r-	0x00	VBAT Monitor2 Low
[18:18]	OVER_TEMP_PMU_IRQ_ENABLE	r-	0x00	PMU TWARN Up or Down interrupt
[17:17]	OVER_TEMP_NFC_IRQ_ENABLE	r-	0x00	CLIF TWARN Up or Down interrupt
[16:16]	ADC_DATA_7_IRQ_ENABLE	r-	0x00	GPADC channel 7 interrupt
[15:15]	ADC_DATA_6_IRQ_ENABLE	r-	0x00	GPADC channel 6 interrupt
[14:14]	ADC_DATA_5_IRQ_ENABLE	r-	0x00	GPADC channel 5 interrupt
[13:13]	ADC_DATA_4_IRQ_ENABLE	r-	0x00	GPADC channel 4 interrupt
[12:12]	ADC_DATA_3_IRQ_ENABLE	r-	0x00	GPADC channel 3 interrupt
[11:11]	ADC_DATA_2_IRQ_ENABLE	r-	0x00	GPADC channel 2 interrupt
[10:10]	ADC_DATA_1_IRQ_ENABLE	r-	0x00	GPADC channel 1 interrupt
[9:9]	ADC_DATA_0_IRQ_ENABLE	r-	0x00	GPADC channel 0 interrupt
[8:8]	GPIO_COMMON_IRQ_ENABLE	r-	0x00	Common GPIO IRQ (OR condition of GPIO0,1,2,3)
[7:7]	RESERVED	r-	0x00	reserved
[6:5]	RESERVED	r-	0x00	reserved
[4:4]	VDDIO_OK_IRQ_ENABLE	r-	0x00	VDDIO OK interrupt
[3:3]	GPIO3_ZIF_IRQ_ENABLE	r-	0x00	GPIO3 IRQ
[2:2]	GPIO2_ZIF_IRQ_ENABLE	r-	0x00	GPIO2 IRQ
[1:1]	GPIO1_ZIF_IRQ_ENABLE	r-	0x00	GPIO1 IRQ
[0:0]	GPIO0_ZIF_IRQ_ENABLE	r-	0x00	GPIO0 IRQ

9.14.2.6 PCRM_INT_STATUS (0xA4)

This register provides interrupt status of the various interrups.

Table 155. PCRM_INT_STATUS (0xA4) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x00	reserved
[30:30]	SUSPEND_IRQ_STATUS	r-	0x00	suspend interrupt
[29:29]	SUSPEND_PREV_IRQ_STATUS	r-	0x00	suspend Prevention interrupt
[28:28]	PVDDLDO_OVERCURRENT_IRQ_STATUS	r-	0x00	PVDDLDO Overcurrent interrupt
[27:27]	RESERVED	r-	0x00	reserved
[26:26]	OVERCURRENT_IRQ_STATUS	r-	0x00	OVERCURRENT interrupt
[25:25]	VUP_OK_IRQ_STATUS	r-	0x00	VUP_OK edge interrupt
[24:24]	RESERVED	r-	0x00	reserved

Table 155. PCRM_INT_STATUS (0xA4) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[23:23]	USB_VBUS_PRESENT_IRQ_STATUS	r-	0x00	USB VBUS Present
[22:22]	RESERVED	r-	0x00	reserved
[21:21]	LPDET_IRQ_STATUS	r-	0x00	LPDET interrupt
[20:20]	STBY_PREV_IRQ_STATUS	r-	0x00	Stby prevention interrupt
[19:19]	VBAT_MON2_LOW_IRQ_STATUS	r-	0x00	VBAT Monitor2 Low
[18:18]	OVER_TEMP_PMU_IRQ_STATUS	r-	0x00	PMU TWARN Up or Down interrupt
[17:17]	OVER_TEMP_NFC_IRQ_STATUS	r-	0x00	CLIF TWARN Up or Down interrupt
[16:16]	ADC_DATA_7_IRQ_STATUS	r-	0x00	GPADC channel 7 interrupt
[15:15]	ADC_DATA_6_IRQ_STATUS	r-	0x00	GPADC channel 6 interrupt
[14:14]	ADC_DATA_5_IRQ_STATUS	r-	0x00	GPADC channel 5 interrupt
[13:13]	ADC_DATA_4_IRQ_STATUS	r-	0x00	GPADC channel 4 interrupt
[12:12]	ADC_DATA_3_IRQ_STATUS	r-	0x00	GPADC channel 3 interrupt
[11:11]	ADC_DATA_2_IRQ_STATUS	r-	0x00	GPADC channel 2 interrupt
[10:10]	ADC_DATA_1_IRQ_STATUS	r-	0x00	GPADC channel 1 interrupt
[9:9]	ADC_DATA_0_IRQ_STATUS	r-	0x00	GPADC channel 0 interrupt
[8:8]	GPIO_COMMON_IRQ_STATUS	r-	0x00	Common GPIO IRQ (OR condition of GPIO0,1,2,3)
[7:7]	RESERVED	r-	0x00	reserved
[6:5]	RESERVED	r-	0x00	reserved
[4:4]	VDDIO_OK_IRQ_STATUS	r-	0x00	VDDIO OK interrupt
[3:3]	GPIO3_ZIF_IRQ_STATUS	r-	0x00	GPIO3 IRQ
[2:2]	GPIO2_ZIF_IRQ_STATUS	r-	0x00	GPIO2 IRQ
[1:1]	GPIO1_ZIF_IRQ_STATUS	r-	0x00	GPIO1 IRQ
[0:0]	GPIO0_ZIF_IRQ_STATUS	r-	0x00	GPIO0 IRQ

9.14.2.7 PCRM_INT_SET_ENABLE (0xA5)

This register enables the interrupt for the feature.

Table 156. PCRM_INT_SET_ENABLE (0xA5) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x00	reserved
[30:30]	SUSPEND_IRQ_SET_ENABLE	-w	0x00	suspend interrupt
[29:29]	SUSPEND_PREV_IRQ_SET_ENABLE	-w	0x00	suspend Prevention interrupt
[28:28]	PVDDLDO_OVERCURRENT_IRQ_SET_ENABLE	-w	0x00	PVDDLDO Overcurrent interrupt

Table 156. PCRM_INT_SET_ENABLE (0xA5) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[27:27]	RESERVED	r-	0x00	reserved
[26:26]	OVERCURRENT_IRQ_SET_ENABLE	-w	0x00	OVERCURRENT interrupt
[25:25]	VUP_OK_IRQ_SET_ENABLE	-w	0x00	VUP_OK edge interrupt
[24:24]	RESERVED	-w	0x00	reserved
[23:23]	USB_VBUS_PRESENT_IRQ_SET_ENABLE	-w	0x00	USB VBUS Present
[22:22]	RESERVED	r-	0x00	reserved
[21:21]	LPDET_IRQ_SET_ENABLE	-w	0x00	LPDET interrupt
[20:20]	STBY_PREV_IRQ_SET_ENABLE	-w	0x00	stby prevention interrupt
[16:16]	ADC_DATA_7_IRQ_SET_ENABLE	-w	0x00	GPADC channel 7 interrupt
[15:15]	ADC_DATA_6_IRQ_SET_ENABLE	-w	0x00	GPADC channel 6 interrupt
[14:14]	ADC_DATA_5_IRQ_SET_ENABLE	-w	0x00	GPADC channel 5 interrupt
[13:13]	ADC_DATA_4_IRQ_SET_ENABLE	-w	0x00	GPADC channel 4 interrupt
[12:12]	ADC_DATA_3_IRQ_SET_ENABLE	-w	0x00	GPADC channel 3 interrupt
[11:11]	ADC_DATA_2_IRQ_SET_ENABLE	-w	0x00	GPADC channel 2 interrupt
[10:10]	ADC_DATA_1_IRQ_SET_ENABLE	-w	0x00	GPADC channel 1 interrupt
[9:9]	ADC_DATA_0_IRQ_SET_ENABLE	-w	0x00	GPADC channel 0 interrupt
[8:8]	GPIO_COMMON_IRQ_SET_ENABLE	-w	0x00	Common GPIO IRQ (OR condition of GPIO0,1,2,3)
[7:7]	RESERVED	r-	0x00	reserved
[6:5]	RESERVED	-w	0x00	reserved
[4:4]	VDDIO_OK_IRQ_SET_ENABLE	-w	0x00	VDDIO OK interrupt
[3:3]	GPIO3_ZIF_IRQ_SET_ENABLE	-w	0x00	GPIO3 IRQ
[2:2]	GPIO2_ZIF_IRQ_SET_ENABLE	-w	0x00	GPIO2 IRQ
[1:1]	GPIO1_ZIF_IRQ_SET_ENABLE	-w	0x00	GPIO1 IRQ
[0:0]	GPIO0_ZIF_IRQ_SET_ENABLE	-w	0x00	GPIO0 IRQ

9.14.2.8 PCRM_INT_CLR_ENABLE (0xA6)

This register disables the interrupt for the feature.

Table 157. PCRM_INT_CLR_ENABLE (0xA6) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x00	reserved
[30:30]	SUSPEND_IRQ_CLEAR_ ENABLE	-w	0x00	suspend interrupt
[29:29]	SUSPEND_PREV_IRQ_CLEAR_ ENABLE	-w	0x00	suspend Prevention interrupt
[28:28]	PVDDLDO_OVERCURRENT_ IRQ_CLEAR_ENABLE	-w	0x00	PVDDLDO Overcurrent interrupt
[27:27]	RESERVED	r-	0x00	reserved
[25:25]	VUP_OK_IRQ_CLEAR_ENABLE	-w	0x00	VUP_OK edge interrupt
[24:24]	RESERVED	-w	0x00	reserved
[23:23]	USB_VBUS_PRESENT_IRQ_ CLEAR_ENABLE	-w	0x00	USB VBUS Present
[22:22]	RESERVED	r-	0x00	reserved
[21:21]	LPDET_IRQ_CLEAR_ENABLE	-w	0x00	LPDET interrupt
[20:20]	STBY_PREV_IRQ_CLEAR_ ENABLE	-w	0x00	stby prev interrupt
[19:19]	VBAT_MON2_LOW_IRQ_ CLEAR_ENABLE	-w	0x00	VBAT Monitor2 Low
[18:18]	OVER_TEMP_PMU_IRQ_ CLEAR_ENABLE	-w	0x00	PMU TWARN Up or Down interrupt
[17:17]	OVER_TEMP_NFC_IRQ_ CLEAR_ENABLE	-w	0x00	CLIF TWARN Up or Down interrupt
[16:16]	ADC_DATA_7_IRQ_CLEAR_ ENABLE	-w	0x00	GPADC channel 7 interrupt
[15:15]	ADC_DATA_6_IRQ_CLEAR_ ENABLE	-w	0x00	GPADC channel 6 interrupt
[14:14]	ADC_DATA_5_IRQ_CLEAR_ ENABLE	-w	0x00	GPADC channel 5 interrupt
[13:13]	ADC_DATA_4_IRQ_CLEAR_ ENABLE	-w	0x00	GPADC channel 4 interrupt
[12:12]	ADC_DATA_3_IRQ_CLEAR_ ENABLE	-w	0x00	GPADC channel 3 interrupt
[11:11]	ADC_DATA_2_IRQ_CLEAR_ ENABLE	-w	0x00	GPADC channel 2 interrupt
[10:10]	ADC_DATA_1_IRQ_CLEAR_ ENABLE	-w	0x00	GPADC channel 1 interrupt
[9:9]	ADC_DATA_0_IRQ_CLEAR_ ENABLE	-w	0x00	GPADC channel 0 interrupt
[7:7]	RESERVED	r-	0x00	reserved
[6:5]	RESERVED	-w	0x00	reserved
[4:4]	VDDIO_OK_IRQ_CLEAR_ ENABLE	-w	0x00	VDDIO OK interrupt

Table 157. PCRM_INT_CLR_ENABLE (0xA6) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[3:3]	GPIO3_ZIF_IRQ_CLEAR_ENABLE	-w	0x00	GPIO3 IRQ
[2:2]	GPIO2_ZIF_IRQ_CLEAR_ENABLE	-w	0x00	GPIO2 IRQ
[1:1]	GPIO1_ZIF_IRQ_CLEAR_ENABLE	-w	0x00	GPIO1 IRQ
[0:0]	GPIO0_ZIF_IRQ_CLEAR_ENABLE	-w	0x00	GPIO0 IRQ

9.14.2.9 PCRM_PAD_GPIO5 (0xA7)

This register provides settings for GPIO5 pin.

Table 158. PCRM_PAD_GPIO5 (0xA7) register bit description

Bit	Symbol	Access	Value	Description
[31:6]	RESERVED	r-	0x00	reserved
[5:4]	GPIO5_SLEW_RATE	rw	0x00	Select Driver Strength for GPIO5
[3:2]	GPIO5_PUPD	rw	0x01	Enable PullUp/Down for GPIO5 (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	GPIO5_EN_OUT	rw	0x00	Enables Output driver for GPIO5
[0:0]	GPIO5_EN_IN	rw	0x00	Enables Input Driver for GPIO5

9.14.2.10 PCRM_PAD_GPIO4 (0xA8)

This register provides settings for GPIO4 pin.

Table 159. PCRM_PAD_GPIO4 (0xA8) register bit description

Bit	Symbol	Access	Value	Description
[31:6]	RESERVED	r-	0x00	reserved
[5:4]	GPIO4_SLEW_RATE	rw	0x00	Select Driver Strength for GPIO4
[3:2]	GPIO4_PUPD	rw	0x01	Enable PullUp/Down for GPIO4 (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	GPIO4_EN_OUT	rw	0x00	Enables Output driver for GPIO4

Table 159. PCRM_PAD_GPIO4 (0xA8) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[0:0]	GPIO4_EN_IN	rw	0x00	Enables Input Driver for GPIO4

9.14.2.11 PCRM_ULPCD_STS (0xA9)

This register provides the reference RSSI after calibration in ULPCD calibration phase.

Table 160. PCRM_ULPCD_STS (0xA9) register bit description

Bit	Symbol	Access	Value	Description
[31:11]	RESERVED	r-	0x00	reserved
[10:0]	RSSI	r-	0x00	RSSI value from ULPCD GPADC

9.14.2.12 PCRM_PMU_ANA_STS2 (0xAA)

This register provides status of VBAT, VDDIOHI and USB VBUS pin/voltage status.

Table 161. PCRM_PMU_ANA_STS2 (0xAA) register bit description

Bit	Symbol	Access	Value	Description
[31:3]	RESERVED	r-	0x00	reserved
[2:2]	USB_VBUS_PRESENT	r-	0x00	USB VBUS Present
[1:1]	VDDIOHI_OK	r-	0x00	VDDIOHI Voltage OK (VDDIO>2.1V)
[0:0]	VBAT_MON2_OK	r-	0x00	VBAT Voltage 3V8 OK (VBAT > 3.8V)

9.14.2.13 PCRM_PMU_ANA_MISC_CTRL (0xAB)

This register provides to control the USB VBUS related settings.

Table 162. PCRM_PMU_ANA_MISC_CTRL (0xAB) register bit description

Bit	Symbol	Access	Value	Description
[31:2]	RESERVED	r-	0x00	reserved
[1:1]	USB_VBUS_MON_EN	rw	0x00	Enables USB VBUS Monitor
[0:0]	USB_VBUS_PULLDOWN_EN	rw	0x00	Enables the internal pulldown resistance to pulldown the USB_VBUS

9.14.2.14 PCRM_PMU_ANA_VBAT_MON2 (0xAC)

This register provides to enable the VBAT monitor 2 that triggers when VBAT > 3.8v.

Table 163. PCRM_PMU_ANA_VBAT_MON2 (0xAC) register bit description

Bit	Symbol	Access	Value	Description
[31:1]	RESERVED	r-	0x00	reserved
[0]	VBAT_MON2_EN	rw	0b	Disable Voltage Monitor on VBAT
			1b	Enable Voltage Monitor on VBAT (Triggers when VBAT>3.8V)

9.14.2.15 PCRM_DIG_VBUS_DEBOUNCE_CTRL (0xAD)

This register provides the debounce control on the USB VBUS.

Table 164. PCRM_DIG_VBUS_DEBOUNCE_CTRL (0xAD) register bit description

Bit	Symbol	Access	Value	Description
[31:13]	RESERVED	r-	0x00	reserved
[12:12]	DEBOUNCE_BYPASS_EN	rw	0x00	USB VBUS debounce bypass
[11:11]	RESERVED	r-	0x00	reserved
[10:0]	VBUS_DEBOUNCE_TIME	rw	0x474	USB VBUS debounce time

9.14.2.16 PCRM_INT_EDGE_SEL (0xAE)

This register provides the interrupt edge selection for GPIOs.

Table 165. PCRM_INT_EDGE_SEL (0xAE) register bit description

Bit	Symbol	Access	Value	Description
[31:10]	RESERVED	r-	0x00	reserved
[9:8]	EDGE_SEL_COM	rw	0x00	GPIO_COMMON interrupt edge detect selection 00b: disable; 01b: r edge; 10b: f edge; 11b: dual edge;
[7:6]	EDGE_SEL_3	rw	0x00	GPIO3 interrupt edge detect selection 00b: disable; 01b: r edge; 10b: f edge; 11b: dual edge;
[5:4]	EDGE_SEL_2	rw	0x00	GPIO2 interrupt edge detect selection 00b: disable; 01b: r edge; 10b: f edge; 11b: dual edge;
[3:2]	EDGE_SEL_1	rw	0x00	GPIO1 interrupt edge detect selection 00b: disable; 01b: r edge; 10b: f edge; 11b: dual edge;
[1:0]	EDGE_SEL_0	rw	0x00	GPIO0 interrupt edge detect selection 00b: disable; 01b: r edge; 10b: f edge; 11b: dual edge;

9.14.2.17 PCRM_VDDIO_LOSS_DET_DISABLE (0xAF)

This register provides settings to disable VDDIO_LOSS detection.

Table 166. PCRM_VDDIO_LOSS_DET_DISABLE (0xAF) register bit description

Bit	Symbol	Access	Value	Description
[31:1]	RESERVED	r-	0x00	reserved
[0:0]	VDDIO_LOSS_DET_DISABLE	rw	0x00	Write '1' and sequentially write '0' after minimum of 1 LFO cycle will disable VDDIO LOSS detection function in PMU_ANA

9.14.2.18 PCRM_VDDIO_LOSS_DET_ENABLE (0xB0)

This register provides settings to enable VDDIO_LOSS detection.

Table 167. PCRM_VDDIO_LOSS_DET_ENABLE (0xB0) register bit description

Bit	Symbol	Access	Value	Description
[31:1]	RESERVED	r-	0x00	reserved

Table 167. PCRM_VDDIO_LOSS_DET_ENABLE (0xB0) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[0:0]	VDDIO_LOSS_DET_ENABLE	rw	0x00	Write '1' and sequentially write '0' after minimum of 1 LFO cycle will enable VDDIO LOSS detection function in PMU_ANA

9.14.2.19 PCRM_PAD_DWL_REQ (0xB1)

This register provides settings for DWL_REQ pin.

Table 168. PCRM_PAD_DWL_REQ (0xB1) register bit description

Bit	Symbol	Access	Value	Description
[31:6]	RESERVED	r-	0x00	reserved
[5:4]	DWL_REQ_SLEW_RATE	rw	0x00	Selects Driver Strength for DWL_REQ
[3:2]	DWL_REQ_PUPD	rw	0x00	Enables PullUp/Down for DWL_REQ (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	DWL_REQ_EN_OUT	rw	0x00	Enables Output driver for DWL_REQ
[0:0]	DWL_REQ_EN_IN	rw	0x00	Enables Input Driver for DWL_REQ

9.14.2.20 PCRM_PAD_IRQ (0xB2)

This register provides settings for IRQ pin.

Table 169. PCRM_PAD_IRQ (0xB2) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x00	reserved
[16:16]	IRQ_ENABLE	rw	0x00	If set them IRQ unit output is driving the GPIO
[15:6]	RESERVED	r-	0x00	reserved
[5:4]	IRQ_SLEW_RATE	rw	0x00	Selects Driver Strength for IRQ
[3:2]	IRQ_PUPD	rw	0x00	Enables PullUp/Down for IRQ (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	IRQ_EN_OUT	rw	0x00	Enables Output driver for IRQ
[0:0]	IRQ_EN_IN	rw	0x00	Enables Input Driver for IRQ

9.14.2.21 PCRM_PAD_ATX_D (0xB3)

This register provides settings for ATX_D pin.

Table 170. PCRM_PAD_ATX_D (0xB3) register bit description

Bit	Symbol	Access	Value	Description
[31:6]	RESERVED	r-	0x00	reserved
[5:4]	ATX_D_SLEW_RATE	rw	0x00	Selects Driver Strength for ATX_D
[3:2]	ATX_D_PUPD	rw	0x03	Enables PullUp/Down for ATX_D (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	ATX_D_EN_OUT	rw	0x00	Enables Output driver for ATX_D
[0:0]	ATX_D_EN_IN	rw	0x01	Enables Input Driver for ATX_D

9.14.2.22 PCRM_PAD_ATX_C (0xB4)

This register provides settings for ATX_C pin.

Table 171. PCRM_PAD_ATX_C (0xB4) register bit description

Bit	Symbol	Access	Value	Description
[31:7]	RESERVED	r-	0x00	reserved
[6:6]	ATX_C_EN_RTS_CONTROL	rw	0x00	Selector for output value in case UART as Host Interface is selected (PCRM_SYS_CTRL_REG.HIF_SELECT == 3 (uart)) 0 - HW control (same as for PN552); 1 - FW control (output value == PCRM_PADOUT_REG.PADOUT_ATX_C)
[5:4]	ATX_C_SLEW_RATE	rw	0x00	Selects Driver Strength for ATX_C
[3:2]	ATX_C_PUPD	rw	0x03	Enables PullUp/Down for ATX_C (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	ATX_C_EN_OUT	rw	0x00	Enables Output driver for ATX_C
[0:0]	ATX_C_EN_IN	rw	0x01	Enables Input Driver for ATX_C

9.14.2.23 PCRM_PAD_ATX_A (0xB5)

This register provides settings for ATX_A pin.

Table 172. PCRM_PAD_ATX_A (0xB5) register bit description

Bit	Symbol	Access	Value	Description
[31:9]	RESERVED	r-	0x00	reserved
[8:8]	ATX_A_I3C_ZI_ZIF_SEL	rw	0x00	Select ZI or ZIF pad pin when I3C is active (0: ZI, 1: ZIF)
[7:7]	ATX_A_ECS	rw	0x00	Enables Pull-up current source for ATX_A (I2C_SDA)
[6:6]	ATX_A_EGP	rw	0x00	Enables GPIO mode (0: I2C mode; 1: GPIO mode)for ATX_A (I2C_SDA)
[5:5]	ATX_A_FSEL	rw	0x00	Selects Input Filter value for I2C mode (0: 50ns; 1: 10ns) for ATX_A (I2C_SDA)
[4:4]	ATX_A_SLEW_RATE	rw	0x00	Selects Driver Strength / Speed mode (0: Low speed GPIO / SF and FP I2C mode; 1: Medium speed GPIO / HS I2C mode) on ATX_A (I2C_SDA)
[3:2]	ATX_A_PUPD	rw	0x01	Enables PullUp/Down for ATX_A (I2C_SDA) (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	ATX_A_EN_OUT	rw	0x00	Enables Output driver for ATX_A (I2C_SDA)
[0:0]	ATX_A_EN_IN	rw	0x01	Enables Input Driver for ATX_A (I2C_SDA)

9.14.2.24 PCRM_PAD_ATX_B (0xB6)

This register provides settings for ATX_B pin.

Table 173. PCRM_PAD_ATX_B (0xB6) register bit description

Bit	Symbol	Access	Value	Description
[31:9]	RESERVED	r-	0x00	reserved
[8:8]	ATX_B_I3C_ZI_ZIF_SEL	rw	0x00	Select ZI or ZIF pad pin when I3C is active (0: ZI, 1: ZIF)
[7:7]	ATX_B_ECS	rw	0x00	Enables Pull-up current source for ATX_B (I2C_SCL)
[6:6]	ATX_B_EGP	rw	0x00	Enables GPIO mode (0: I2C mode; 1: GPIO mode) for ATX_B (I2C_SCL)
[5:5]	ATX_B_FSEL	rw	0x00	Selects Input Filter value for I2C mode (0: 50ns; 1: 10ns) for ATX_B (I2C_SCL)
[4:4]	ATX_B_SLEW_RATE	rw	0x00	Selects Driver Strength / Speed mode (0: Low speed GPIO / SF and FP I2C mode; 1: Medium speed GPIO / HS I2C mode) on ATX_B (I2C_SCL)
[3:2]	ATX_B_PUPD	rw	0x01	Enables PullUp/Down for ATX_B (I2C_SCL) (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull

Table 173. PCRM_PAD_ATX_B (0xB6) register bit description*...continued*

Bit	Symbol	Access	Value	Description
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	ATX_B_EN_OUT	rw	0x00	Enables Output driver for ATX_B (I2C_SCL)
[0:0]	ATX_B_EN_IN	rw	0x01	Enables Input Driver for ATX_B (I2C_SCL)

9.14.2.25 PCRM_PAD_GPIO3 (0xB7)

This register provides settings for GPIO3 pin.

Table 174. PCRM_PAD_GPIO3 (0xB7) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x00	reserved
[16:16]	GPIO3_PWM_ENABLE	rw	0x00	If set them PWM unit output 3 is driving the GPIO3
[15:6]	RESERVED	r-	0x00	reserved
[5:4]	GPIO3_SLEW_RATE	rw	0x11	Select Driver Strength for GPIO3
[3:2]	GPIO3_PUPD	rw	0x00	Enable PullUp/Down for GPIO3 (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	GPIO3_EN_OUT	rw	0x00	Enables Output driver for GPIO3
[0:0]	GPIO3_EN_IN	rw	0x01	Enables Input Driver for GPIO3

9.14.2.26 PCRM_PAD_GPIO2 (0xB8)

This register provides settings for GPIO2 pin.

Table 175. PCRM_PAD_GPIO2 (0xB8) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x00	reserved
[16:16]	GPIO2_PWM_ENABLE	rw	0x00	If set them PWM unit output 2 is driving the GPIO2
[15:6]	RESERVED	r-	0x00	reserved
[5:4]	GPIO2_SLEW_RATE	rw	0x11	Select Driver Strength for GPIO2
[3:2]	GPIO2_PUPD	rw	0x00	Enable PullUp/Down for GPIO2 (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper

Table 175. PCRM_PAD_GPIO2 (0xB8) register bit description*...continued*

Bit	Symbol	Access	Value	Description
			11b	Weak Pull-Up
[1:1]	GPIO2_EN_OUT	rw	0x00	Enables Output driver for GPIO2
[0:0]	GPIO2_EN_IN	rw	0x01	Enables Input Driver for GPIO2

9.14.2.27 PCRM_PAD_GPIO1 (0xB9)

This register provides settings for GPIO1 pin.

Table 176. PCRM_PAD_GPIO1 (0xB9) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x00	reserved
[16:16]	GPIO1_PWM_ENABLE	rw	0x00	If set them PWM unit output 1 is driving the GPIO1
[15:6]	RESERVED	r-	0x00	reserved
[5:4]	GPIO1_SLEW_RATE	rw	0x11	Selects Driver Strength for GPIO1
[3:2]	GPIO1_PUPD	rw	0x00	Enables PullUp/Down for GPIO1 (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	GPIO1_EN_OUT	rw	0x00	Enables Output driver for GPIO1
[0:0]	GPIO1_EN_IN	rw	0x01	Enables Input Driver for GPIO1

9.14.2.28 PCRM_PAD_GPIO0 (0xBA)

This register provides settings for GPIO0 pin.

Table 177. PCRM_PAD_GPIO0 (0xBA) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x00	reserved
[16:16]	GPIO0_PWM_ENABLE	rw	0x00	If set them PWM unit output 0 is driving the GPIO0
[15:6]	RESERVED	r-	0x00	reserved
[5:4]	GPIO0_SLEW_RATE	rw	0x11	Selects Driver Strength for GPIO0
[3:2]	GPIO0_PUPD	rw	0x00	Enables PullUp/Down for GPIO0 (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up

Table 177. PCRM_PAD_GPIO0 (0xBA) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[1:1]	GPIO0_EN_OUT	rw	0x00	Enables Output driver for GPIO0
[0:0]	GPIO0_EN_IN	rw	0x01	Enables Input Driver for GPIO0

9.14.2.29 PCRM_PADOUT (0xBB)

This register sets the pin status of different GPIOs when it is configured as output.

Table 178. PCRM_PADOUT (0xBB) register bit description

Bit	Symbol	Access	Value	Description
[31:27]	RESERVED	r-	0x00	reserved
[26:26]	PADOUT_INT_AUX	rw	0x00	Output Value for CT_AUX_INT
[25:25]	PADOUT_CLK_AUX	rw	0x00	Output Value for CT_AUX_CLK
[24:24]	PADOUT_IO_AUX	rw	0x00	Output Value for CT_AUX_IO
[23:23]	RESERVED	r-	0x00	reserved
[22:22]	PADOUT_AUX_2	rw	0x00	Output Value for AUX_2
[21:21]	PADOUT_AUX_1	rw	0x00	Output Value for AUX_1
[20:20]	PADOUT_GPIO5	rw	0x00	Output Value for GPIO5
[19:19]	PADOUT_GPIO4	rw	0x00	Output Value for GPIO4
[18:18]	PADOUT_I2CM_SCL	rw	0x00	Output Value for I2CM_SCL
[17:17]	PADOUT_I2CM_SDA	rw	0x00	Output Value for I2CM_SDA
[16:16]	PADOUT_SPIM_SSN	rw	0x00	Output Value for SPIM_SSN
[15:15]	PADOUT_SPIM_SCLK	rw	0x00	Output Value for SPIM_SCLK
[14:14]	PADOUT_SPIM_MOSI	rw	0x00	Output Value for SPIM_MOSI
[13:13]	PADOUT_SPIM_MISO	rw	0x00	Output Value for SPIM_MISO
[12:12]	PADOUT_AUX_3	rw	0x00	Output Value for AUX_3
[11:10]	RESERVED	r-	0x00	reserved
[9:9]	PADOUT_DWL_REQ	rw	0x00	Output Value for DWL_REQ
[8:8]	PADOUT_IRQ	rw	0x00	Output Value for IRQ
[7:7]	PADOUT_ATX_D	rw	0x01	Output Value for HSU_TX (also i2c_adr1 or spi_mosi)
[6:6]	PADOUT_ATX_A	rw	0x01	Output Value for HSU_RX (also i2c_sda or spi_miso)
[5:5]	PADOUT_ATX_C	rw	0x01	Output Value for HSU_RTS (also i2c_adr0 or spi_nss)
[4:4]	PADOUT_ATX_B	rw	0x01	Output Value for HSU_CTS (also i2c_scl or spi_sck)
[3:3]	PADOUT_GPIO3	rw	0x00	Output Value for GPIO3
[2:2]	PADOUT_GPIO2	rw	0x00	Output Value for GPIO2
[1:1]	PADOUT_GPIO1	rw	0x00	Output Value for GPIO1
[0:0]	PADOUT_GPIO0	rw	0x00	Output Value for GPIO0

9.14.2.30 PCRM_PADIN (0xBC)

This register provides the value of pin status of different GPIOs when it is configured as input.

Table 179. PCRM_PADIN (0xBC) register bit description

Bit	Symbol	Access	Value	Description
[31:27]	RESERVED	r-	0x00	reserved
[26:26]	PADIN_INT_AUX	r-	0x00	Input Value for CT_AUX_INT
[25:25]	PADIN_CLK_AUX	r-	0x00	Input Value for CT_AUX_CLK
[24:24]	PADIN_IO_AUX	r-	0x00	Input Value for CT_AUX_IO
[23:23]	PADIN_TEST	r-	0x00	Input Value for TEST
[22:22]	PADIN_AUX_2	r-	0x00	Input Value for AUX_2
[21:21]	PADIN_AUX_1	r-	0x00	Input Value for AUX_1
[20:20]	PADIN_GPIO5	r-	0x00	Input Value for GPIO5
[19:19]	PADIN_GPIO4	r-	0x00	Input Value for GPIO4
[18:18]	PADIN_I2CM_SCL	r-	0x00	Input Value for I2CM_SCL
[17:17]	PADIN_I2CM_SDA	r-	0x00	Input Value for I2CM_SDA
[16:16]	PADIN_SPIM_SSN	r-	0x00	Input Value for SPIM_SSN
[15:15]	PADIN_SPIM_SCLK	r-	0x00	Input Value for SPIM_SCLK
[14:14]	PADIN_SPIM_MOSI	r-	0x00	Input Value for SPIM_MOSI
[13:13]	PADIN_SPIM_MISO	r-	0x00	Input Value for SPIM_MISO
[12:12]	PADIN_AUX_3	r-	0x00	Input Value for AUX_3
[11:11]	PADIN_HOSTIF_SEL1	r-	0x00	Input Value for HOSTIF_SEL1
[10:10]	PADIN_HOSTIF_SEL0	r-	0x00	Input Value for HOSTIF_SEL0
[9:9]	PADIN_DWL_REQ	r-	0x00	Input Value for DWL_REQ
[8:8]	PADIN_IRQ	r-	0x00	Input Value for IRQ
[7:7]	PADIN_ATX_D	r-	0x00	Input Value for HSU_TX (also i2c_adr1 or spi_mosi)
[6:6]	PADIN_ATX_A	r-	0x00	Input Value for HSU_RX (also i2c_sda or spi_miso)
[5:5]	PADIN_ATX_C	r-	0x00	Input Value for HSU_RTS (also i2c_adr0 or spi_nss)
[4:4]	PADIN_ATX_B	r-	0x00	Input Value for HSU_CTS (also i2c_scl or spi_sck)
[3:3]	PADIN_GPIO3	r-	0x00	Input Value for GPIO3
[2:2]	PADIN_GPIO2	r-	0x00	Input Value for GPIO2
[1:1]	PADIN_GPIO1	r-	0x00	Input Value for GPIO1
[0:0]	PADIN_GPIO0	r-	0x00	Input Value for GPIO0

9.14.2.31 PCRM_GPREG7 (0xBD)

This register provides a value that can be used by the application. The value is retained even when the IC is soft-reset.

Table 180. PCRM_GPREG7 (0xBD) register bit description

Bit	Symbol	Access	Value	Description
[31:0]	PCRM_GPREG7	rw	0x00	General Purpose Register 7 for SW

9.14.2.32 PCRM_GPREG6 (0xBE)

This register provides a value that can be used by the application. The value is retained even when the IC is soft-reset.

Table 181. PCRM_GPREG6 (0xBE) register bit description

Bit	Symbol	Access	Value	Description
[31:0]	PCRM_GPREG6	rw	0x00	General Purpose Register 6 for SW

9.14.2.33 PCRM_GPREG5 (0xBF)

This register provides a value that can be used by the application. The value is retained even when the IC is soft-reset.

Table 182. PCRM_GPREG5 (0xBF) register bit description

Bit	Symbol	Access	Value	Description
[31:0]	PCRM_GPREG5	rw	0x00	General Purpose Register 5 for SW

9.14.2.34 PCRM_GPREG4 (0xC0)

This register provides a value that can be used by the application. The value is retained even when the IC is soft-reset.

Table 183. PCRM_GPREG4 (0xC0) register bit description

Bit	Symbol	Access	Value	Description
[31:0]	PCRM_GPREG4	rw	0x00	General Purpose Register 4 for SW

9.14.2.35 PCRM_GPREG3 (0xC1)

This register provides a value that can be used by the application. The value is retained even when the IC is soft-reset.

Table 184. PCRM_GPREG3 (0xC1) register bit description

Bit	Symbol	Access	Value	Description
[31:0]	PCRM_GPREG3	rw	0x00	General Purpose Register 3 for SW

9.14.2.36 PCRM_CLIF_ANA_TX_STANDBY (0xC2)

This register provides analog settings for TX before entering standby.

Table 185. PCRM_CLIF_ANA_TX_STANDBY (0xC2) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x00	reserved
[30:30]	TX_RESTART	rw	0x00	Clears TX_SHUTDOWN flag

Table 185. PCRM_CLIF_ANA_TX_STANDBY (0xC2) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[29:29]	TX_SHUTDOWN	rw	0x00	Shutdown of Power Amplifier due to overcurrent detection
[28:28]	TX_PROT_DISABLE	rw	0x00	disable signal for the TX protection circuitry
[27:27]	TX_EN	rw	0x00	Main enable signal for the TX section
[26:26]	TX_GS_SRC_SEL	rw	0x00	Source of GSN value (0: PCRM; 1: CLIF digital)
[25:23]	TX_CLK_MODE_TX2	rw	0x01	selects how the TX_SET_GS are controlled; HIGHZ is 000
[22:20]	TX_CLK_MODE_TX1	rw	0x01	selects how the TX_SET_GS are controlled; HIGHZ is 000
[19:15]	TX_SET_GS_P_TX2	rw	0x1F	GSP Value to be applied suring NFC_STBY power state to TX2 driver; sits here because these are VHV controls
[14:10]	TX_SET_GS_P_TX1	rw	0x1F	GSP Value to be applied suring NFC_STBY power state to TX1 driver; sits here because these are VHV controls
[9:5]	TX_SET_GS_N_TX2	rw	0x1F	GSN Value to be applied suring NFC_STBY power state to TX2 driver
[4:0]	TX_SET_GS_N_TX1	rw	0x1F	GSN Value to be applied suring NFC_STBY power state to TX1 driver

9.14.2.37 PCRM_SYS_LP_CLK_EN (0xC3)

This register enable the clocks required by the peripherals in case of standby mode.

Table 186. PCRM_SYS_LP_CLK_EN (0xC3) register bit description

Bit	Symbol	Access	Value	Description
[31:2]	RESERVED	r-	0x00	reserved
[1:1]	RECOVERY_CLK_ENABLE	rw	0x00	Enables clock source for recovery logic; will be also manage by FSM
[0:0]	LFO_WUC_CLK_ENABLE	rw	0x00	Enables clock source for WUC

9.14.2.38 PCRM_SYS_BOOT3_STS (0xC4)

This register provides the reason for boot (reset reason) of IC.

Table 187. PCRM_SYS_BOOT3_STS (0xC4) register bit description

Bit	Symbol	Access	Value	Description
[31:7]	RESERVED	r-	0x00	reserved
[6:6]	RST_STS_NFC	r-	0x00	Reset source reason NFC SW Reset
[5:5]	RST_STS_FSM	r-	0x00	Reset source reason PMU FSM
[4:4]	RST_STS_CMD	r-	0x00	Reset source reason VEN CMD
[3:3]	RST_STS_WDG	r-	0x00	Reset source reason Watchdog
[2:2]	RESERVED	r-	0x00	reserved
[1:1]	RST_STS_HOST	r-	0x00	Reset source reason host command

Table 187. PCRM_SYS_BOOT3_STS (0xC4) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[0:0]	RST_STS_CPU	r-	0x00	Reset source reason cpu command

9.14.2.39 PCRM_SYS_BOOT2_STS (0xC5)

This register provides Standby/Suspend prevention reason when tried to enter into standby/suspend.

Table 188. PCRM_SYS_BOOT2_STS (0xC5) register bit description

Bit	Symbol	Access	Value	Description
[31:26]	RESERVED	r-	0x00	reserved
[25:25]	PREV_USB	r-	0x00	SUSPEND Prevention Reason, \n \note USB prevention is not applicable for standby mode
[24:24]	PREV_TEMP	r-	0x00	Standby/Suspend Prevention Reason due to temperature.
[23:23]	PREV_CTAUX	r-	0x00	Standby/Suspend Prevention Reason
[22:22]	PREV_HOSTCOMM	r-	0x00	Standby/Suspend Prevention Reason
[21:21]	PREV_SPI	r-	0x00	Standby/Suspend Prevention Reason due to activity on SPI bus.
[20:20]	PREV_I2C	r-	0x00	Standby/Suspend Prevention Reason due to activity on I2C bus, and matches with slave address.
[19:19]	PREV_I3C	r-	0x00	Standby/Suspend Prevention Reason due to activity on I3C bus, and matches with slave address.
[18:18]	PREV_HSU	r-	0x00	Standby/Suspend Prevention Reason due to activity on UART bus.
[17:17]	PREV_GPIO3	r-	0x00	Standby/Suspend Prevention Reason due to GPIO3.
[16:16]	PREV_GPIO2	r-	0x00	Standby/Suspend Prevention Reason due to GPIO2.
[15:15]	PREV_GPIO1	r-	0x00	Standby/Suspend Prevention Reason due to GPIO1.
[14:14]	PREV_GPIO0	r-	0x00	Standby/Suspend Prevention Reason due to GPIO0.
[13:13]	PREV_WUC	r-	0x00	Standby/Suspend Prevention Reason due to wake-up counter.
[12:12]	PREV_LPDET	r-	0x00	Standby/Suspend Prevention Reason LPDET.
[11:11]	PREV_RX_ULPDET	r-	0x00	Standby/Suspend Prevention Reason
[10:10]	PREV_INT_NO_VDDIO	r-	0x00	Standby/Suspend Prevention Reason
[9:9]	RESERVED	r-	0x00	reserved
[8:8]	RESERVED	r-	0x00	reserved
[7:7]	PREV_PVDDLDO_ OVERCURRENT	r-	0x00	Standby/Suspend Prevention Reason due to PVDDLDO overcurrent situation.
[6:6]	PREV_INTERFACE	r-	0x00	Standby/Suspend Prevention Reason
[5:5]	RESERVED	r-	0x00	reserved
[4:4]	PREV_VDDIO_LOSS	r-	0x00	Standby/Suspend Prevention Reason due to loss of VDDIO.
[3:3]	PREV_VDDIO_START	r-	0x00	Standby/Suspend Prevention Reason, indicates VDDIO is already available and standby is prevented

Table 188. PCRM_SYS_BOOT2_STS (0xC5) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[2:2]	PREV_NOENABLE	r-	0x00	Standby/Suspend Prevention Reason
[1:1]	RESERVED	r-	0x00	reserved
[0:0]	RESERVED	r-	0x00	reserved

9.14.2.40 PCRM_SYS_BOOT1_STS (0xC6)

This register provides the reason for boot (reset reason) of IC.

Table 189. PCRM_SYS_BOOT1_STS (0xC6) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	BOOT_ULPCD_XTAL_TIMEOUT	r-	0x00	ULPCD exit due to XTAL timeout
[30:30]	BOOT_ULPCD_CLKDET_ ERROR	r-	0x00	ULPCD CLK_DET error
[29:29]	BOOT_ULPCD_CARD_DETECT	r-	0x00	ULPCD card detect
[28:28]	BOOT_ULPCD_CALIBRATION_ DONE	r-	0x00	ULPCD calibration complete
[27:27]	BOOT_ULPCD_GPIO_ABORT	r-	0x00	ULPCD GPIO Abort
[26:26]	BOOT_ULP_STANDBY	r-	0x00	ULPCD Standby
[25:25]	BOOT_ULPCD_LDO_VDDPA_ OVERCURRENT	r-	0x00	ULPCD LDO VDDPA Overcurrent
[24:24]	BOOT_USB	r-	0x00	Bootup Reason
[23:23]	BOOT_CTAUX	r-	0x00	Bootup Reason
[22:22]	BOOT_ULPCD_RX_ULPDET	r-	0x00	RX ULPDET resulted in boot in ULPCD mode
[21:21]	WAKEUP_RX_ULP	r-	0x00	Indicates if VEN is masked due to wakeup with rx_ulp. This bit is cleared with ULPDET_WKUP_ VEN_MASK_CLR
[20:20]	BOOT_SPI	r-	0x00	Bootup Reason
[19:19]	BOOT_I2C	r-	0x00	Bootup Reason
[18:18]	BOOT_I3C	r-	0x00	Bootup Reason
[17:17]	BOOT_HSU	r-	0x00	Bootup Reason
[16:16]	BOOT_GPIO3	r-	0x00	Bootup Reason
[15:15]	BOOT_GPIO2	r-	0x00	Bootup Reason
[14:14]	BOOT_GPIO1	r-	0x00	Bootup Reason
[13:13]	BOOT_GPIO0	r-	0x00	Bootup Reason
[12:12]	BOOT_LPDET	r-	0x00	Bootup Reason
[11:11]	BOOT_RX_ULPDET	r-	0x00	Bootup Reason
[10:10]	RESERVED	r-	0x00	reserved
[9:9]	RESERVED	r-	0x00	reserved
[8:8]	RESERVED	r-	0x00	reserved
[7:7]	BOOT_PVDDLDO_ OVERCURRENT	r-	0x00	Bootup Reason
[6:6]	BOOT_VDDIO_LOSS	r-	0x00	Bootup Reason
[5:5]	BOOT_VDDIO_START	r-	0x00	Bootup Reason this is valid if STBY/SUSPEND entered with VDDIO LOSS
[4:4]	BOOT_WUC	r-	0x00	Bootup Reason
[3:3]	BOOT_TEMP	r-	0x00	Bootup Reason

Table 189. PCRM_SYS_BOOT1_STS (0xC6) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[2:2]	RESERVED	r-	0x00	reserved
[1:1]	RESERVED	r-	0x00	reserved
[0:0]	BOOT_POR	r-	0x00	Bootup Reason

9.14.2.41 PCRM_SYS_STBY1_CTRL (0xC7)

This register provides control of standby and suspend configurations.

Table 190. PCRM_SYS_STBY1_CTRL (0xC7) register bit description

Bit	Symbol	Access	Value	Description
[31:23]	RESERVED	r-	0x00	reserved
[22:22]	STBY_GPIO0_POLARITY	rw	0x00	Standby/Suspend Wakeup polarity configuration 0: default active high , 1: active low
[21:21]	STBY_GPIO1_POLARITY	rw	0x00	Standby/Suspend Wakeup polarity configuration 0: default active high , 1: active low
[20:20]	STBY_GPIO2_POLARITY	rw	0x00	Standby/Suspend Wakeup polarity configuration 0: default active high , 1: active low
[19:19]	STBY_GPIO3_POLARITY	rw	0x00	Standby/Suspend Wakeup polarity configuration 0: default active high , 1: active low
[18:17]	STBY_VOLT	rw	0x00	Select Voltage in standby and hard power down mode : 00b = 1V1 ; 01b = 1V0; 10b = 0V9 ; 11b = 0V9
[16:16]	CLR_RST_STS	rw	0x00	Clears Reset reason status register values in PCRM_SYS_BOOT3_STS_REG
[15:6]	WUC_VALUE	rw	0x00	Wakeup Timer count down Value (10 bits counter; LFO CLK / 1024 = 371Hz.)
[5:4]	RESERVED	r-	0x00	reserved
[3:3]	CLR_BOOT_REGS	rw	0x00	Clears STBY_PREV_REASON values in the PCRM_SYS_BOOT1_STS_REG and BOOT_REASON values and in PCRM_SYS_BOOT2_STS_REG
[2:1]	RESERVED	r-	0x00	reserved
[0:0]	STBY_REQ_WFI	rw	0x00	standby entry with WFI

9.14.2.42 PCRM_SYS_ULPCD_CTRL (0xC8)

This register provides settings for ULPCD entry.

Table 191. PCRM_SYS_ULPCD_CTRL (0xC8) register bit description

Bit	Symbol	Access	Value	Description
[31:1]	RESERVED	r-	0x00	reserved
[0:0]	NFC_ULPCD_ENTRY_REQ	rw	0x00	NFC ULPCD Mode Entry Request (From NFC FW)

9.14.2.43 PCRM_SYS_STBY_CTRL (0xC9)

This register provides settings for STANDBY entry.

Table 192. PCRM_SYS_STBY_CTRL (0xC9) register bit description

Bit	Symbol	Access	Value	Description
[31:1]	RESERVED	r-	0x00	reserved
[0:0]	NFC_STBY_ENTRY_REQ	-w	0x00	NFC Standby Mode Entry Request (From NFC FW)

9.14.2.44 PCRM_SYS_STBY_CFG (0xCA)

This register provides the control to configure wakeup sources from standby/suspend mode.

Table 193. PCRM_SYS_STBY_CFG (0xCA) register bit description

Bit	Symbol	Access	Value	Description
[31:26]	RESERVED	r-	0x00	reserved
[25:25]	SUSPEND_EN_USB	rw	0x00	suspend mode enable with USB
[24:18]	I23C_ADDR	rw	0x00	I2C I3C address for wakeup
[17:17]	STBY_EN_VDDIO_START	rw	0x00	Enables VDDIO start detect wakeup, Note: This bit and STBY_EN_VDDIO_LOSS is mutually exclusive
[16:16]	RESERVED	rw	0x00	reserved
[15:15]	STBY_EN_CTAUX	rw	0x00	Enables CTAUX interface
[14:14]	STBY_EN_VDDIO_LOSS	rw	0x00	Enables VDDIO loss detect wakeup
[13:13]	RESERVED	rw	0x00	reserved
[12:12]	STBY_EN_GPIO0	rw	0x00	Enables GPIO0 wakeup
[11:11]	STBY_EN_GPIO1	rw	0x00	Enables GPIO1 wakeup
[10:10]	STBY_EN_GPIO2	rw	0x00	Enables GPIO2 wakeup
[9:9]	STBY_EN_GPIO3	rw	0x00	Enables GPIO3 wakeup
[8:6]	RESERVED	r-	0x00	reserved
[5:5]	STBY_EN_PVDDLDO_ OVERCURRENT	rw	0x00	Enables PVDDLDO Overcurrent indication as wakeup reason
[4:4]	STBY_EN_TEMP	rw	0x00	Enables Temperature variation wakeup
[3:3]	STBY_EN_LPDET	rw	0x00	Enables RF Level Detector wakeup (LPDET based)
[2:2]	STBY_EN_RF_ULPDET	rw	0x00	Enables RF Level Detector wakeup (ULPDET based)
[1:1]	STBY_EN_HOSTIF	rw	0x00	Enables wakeup from Host Interface pin activity
[0:0]	STBY_EN_WUC	rw	0x00	Enables Wakeup Timer wakeup

9.14.2.45 PCRM_CLIF_ANA_AGC_RXPROT_CTRL (0xCB)

This register provides the configuration of HFATT value during LPCD calibration and detection.

Table 194. PCRM_CLIF_ANA_AGC_RXPROT_CTRL (0xCB) register bit description

Bit	Symbol	Access	Value	Description
[31:06]	RESERVED	r-	0x00	reserved

Table 194. PCRM_CLIF_ANA_AGC_RXPROT_CTRL (0xCB) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[5:0]	RX_AGC_HFATT_CTRL	rw	0x00	HF attenuator control in low power mode

9.14.2.46 PCRM_LPDET_FSM_CTRL2 (0xCC)

This register provides configuration for LPDET.

Table 195. PCRM_LPDET_FSM_CTRL2 (0xCC) register bit description

Bit	Symbol	Access	Value	Description
[31:21]	RESERVED	r-	0x00	reserved
[20:18]	LPDET_RECOVERY_COUNT_LIMIT	rw	0x00	Clock recovery check time duration (counted in N+1 LFO clock cycle => reg=0 means 1 clock cycle) / max is 8 LFO cycles
[17:9]	LPDET_RECOVERY_COUNT_MAX	rw	0x00	Maximum clock recovery counter value to enable wake-up from RF field (RFLD function) - based on carrier frequency
[8:0]	LPDET_RECOVERY_COUNT_MIN	rw	0x00	Minimum clock recovery counter value to enable wake-up from RF field (RFLD function) - based on carrier frequency

9.14.2.47 PCRM_LPDET_FSM_CTRL1 (0xCD)

This register provides extended configuration for LPDET.

Table 196. PCRM_LPDET_FSM_CTRL1 (0xCD) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x00	reserved
[30:30]	BYPASS_LPDET_FSM	rw	0x00	Bypass the LPDET_FSM control and allows to directly control LPDET from PCRM registers
[29:29]	RUN_LPDET	rw	0x00	Run LPDET FSM in any power mode
[28:27]	VCM_COUNT	rw	0x00	VCM LFO cycle count
[26:26]	LPDET_FSM_EN	rw	0x00	Enables the LPDET_FSM to run constantly (used for RFLD function during polling loops) in Standby mode
[25:25]	LPDET_ONESHOT_RUN	rw	0x00	Enables the LPDET module once (used for collision checks)
[24:17]	LPDET_COUNT_MAX	rw	0x00	Maximum LPDET counter value to enable Clock recovery frequency check - based on carrier frequency / 2
[16:9]	LPDET_COUNT_MIN	rw	0x00	Minimum LPDET counter value to enable Clock recovery frequency check - based on carrier frequency / 2
[8:8]	LPDET_ADD_DELAY_EN	rw	0x00	Minimum LPDET counter value to enable Clock recovery frequency check - based on carrier frequency / 2
[7:0]	LPDET_T5_COUNT	rw	0x01	Defines the LPDET_FSM T5 (wait time) min=1 / max=(to be reviewed)

9.14.2.48 PCRM_CLIF_ANA_XTAL (0xCE)

This register provides XTAL control configurations.

Table 197. PCRM_CLIF_ANA_XTAL (0xCE) register bit description

Bit	Symbol	Access	Value	Description
[31:29]	RESERVED	r-	0x00	reserved
[28:27]	XTAL_SLICER_PSM	rw	0x00	sets the XTAL slicer driving strength
[26:26]	XTAL_PKDET_MON_EN	rw	0x00	enable signal for monitoring XTAL outputs
[25:16]	TEMP	rw	0x00	Temperature information for the CLIF main PLL. Post processed from BIST GPADC datas trunk to 4 bits => 5% accuracy
[15:15]	XTAL_AUTO_EN	rw	0x00	Enable XTAL automatic start when RF field detection event is triggered (RFLD function)
[14:13]	XTAL_AMP_SEL	rw	0x00	target level for amplitude regulation loop
[12:7]	XTAL_AMP_CTRL	rw	0x00	Oscillation Amplitude control
[6:6]	XTAL_OVER_BOOST_EN	rw	0x01	Enable BOOST mode ; more GM
[5:5]	XTAL_CLKFLAG_EN	rw	0x00	CLKFLAG enable
[4:4]	XTAL_SLICER_EN	rw	0x00	Enable Slicer
[3:3]	XTAL_PKDET_EN	rw	0x00	Enable for XTAL peak detector
[2:2]	XTAL_AMP_REG_AUTO_EN	rw	0x00	Enable analog automatic amplitude regulation
[1:1]	XTAL_BYPASS_EN	rw	0x00	Bypass GM Buffer
[0:0]	XTAL_EN	rw	0x00	Enable signal for XTAL Oscillator

9.14.2.49 PCRM_PMU_ANA_VEN_MON (0xCF)

This register provides configuration of VEN pin control.

Table 198. PCRM_PMU_ANA_VEN_MON (0xCF) register bit description

Bit	Symbol	Access	Value	Description
[31:16]	RESERVED	r-	0x00	reserved
[15:4]	VEN_OFF_HPD_ENTRY_LIMIT_TIME	rw	0x0FF	Counter time limit before going to OFF/HPD state when VEN goes low
[3:0]	NFC_RESET_LIMIT_TIME	rw	0xF	Counter time limit before reseting NFC core

9.14.2.50 PCRM_PMU_ANA_VBAT_MON (0xD0)

This register provides VBAT monitor control.

Table 199. PCRM_PMU_ANA_VBAT_MON (0xD0) register bit description

Bit	Symbol	Access	Value	Description
[31:12]	RESERVED	r-	0x00	reserved
[11:11]	VBAT_MON_FSM_EN	rw	0x00	Enable the vbat monitor fsm
[10:10]	VBAT_MON_CMD_DIS	rw	0x00	Disable turn off command from VBAT monitor FSM; use mainly for debug purpose.

Table 199. PCRM_PMU_ANA_VBAT_MON (0xD0) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[9:0]	VBAT_FSM_OFF_LOOP_TIME	rw	0x03	Timing between 2 Vbat monitoring (based on LFO_clk cycles)

9.14.2.51 PCRM_PMU_ANA_TEMP_SNS_CTRL (0xD1)

This register provides the temperature warning selection for PMU and NFC.

Table 200. PCRM_PMU_ANA_TEMP_SNS_CTRL (0xD1) register bit description

Bit	Symbol	Access	Value	Description
[31:4]	RESERVED	r-	0x00	reserved
[3:2]	NFC_OVER_TEMP_SEL	rw	0x00	NFC Thermal warning detection threshold value (00b: disabled / 01b: 114 C / 10b: 125 C / 11b: 130 C)
[1:0]	PMU_OVER_TEMP_SEL	rw	0x00	PMU Thermal warning detection threshold value (00b: disabled / 01b: 114 C / 10b: 125 C / 11b: 130 C)

9.14.2.52 PCRM_PMU_ANA_VMON_CTRL (0xD2)

This register provides the monitor configuration for VUP, VDDC, VHV and VBAT.

Table 201. PCRM_PMU_ANA_VMON_CTRL (0xD2) register bit description

Bit	Symbol	Access	Value	Description
[31:7]	RESERVED	r-	0x00	reserved
[6:6]	VMON_VUP_THRESH_SEL	rw	0x00	Voltage monitor VUP threshold (0: 2.4V falling edge 1: 3.2V falling edge)
[5:5]	VMON_VUP_EN	rw	0x00	Voltage monitor VUP enable
[4:4]	RESERVED	r-	0x00	reserved
[3:3]	VMON_VDDC_EN	rw	0x00	Voltage monitor VDDC enable
[2:2]	VMON_VHV_EN	rw	0x00	Voltage monitor VHV enable
[1:1]	VMON_VBAT_THRESH_SEL	rw	0x00	Voltage monitor VBAT threshold (0: 2.4V falling edge 1: 2.5V rising edge)
[0:0]	VMON_VBAT_EN	rw	0x00	Voltage monitor VBAT enable

9.14.2.53 PCRM_CFG_OFFPLUS (0xD3)

Reserved for future use.

Table 202. PCRM_CFG_OFFPLUS (0xD3) register bit description

Bit	Symbol	Access	Value	Description
[31:0]	RESERVED	r-	0x00	reserved

9.14.2.54 PCRM_PAD_AUX_3 (0xD4)

This register provides settings for AUX_3 pin.

Table 203. PCRM_PAD_AUX_3 (0xD4) register bit description

Bit	Symbol	Access	Value	Description
[31:6]	RESERVED	r-	0x00	reserved
[5:4]	AUX_3_SLEW_RATE	rw	0x00	Selects Driver Strength for AUX_3
[3:2]	AUX_3_PUPD	rw	0x01	Enables PullUp/Down for AUX_3 (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
[1:1]	AUX_3_EN_OUT	rw	0x00	Enables Output driver for AUX_3
[0:0]	AUX_3_EN_IN	rw	0x00	Enables Input Driver for AUX_3

9.14.2.55 PCRM_PAD_AUX_2 (0xD5)

This register provides settings for AUX_2 pin.

Table 204. PCRM_PAD_AUX_2 (0xD5) register bit description

Bit	Symbol	Access	Value	Description
[31:6]	RESERVED	r-	0x00	reserved
[5:4]	AUX_2_SLEW_RATE	rw	0x00	Selects Driver Strength for AUX_2
[3:2]	AUX_2_PUPD	rw	0x01	Enables PullUp/Down for AUX_2 (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
[1:1]	AUX_2_EN_OUT	rw	0x00	Enables Output driver for AUX_2
[0:0]	AUX_2_EN_IN	rw	0x00	Enables Input Driver for AUX_2

9.14.2.56 PCRM_PAD_AUX_1 (0xD6)

This register provides settings for AUX_1 pin.

Table 205. PCRM_PAD_AUX_1 (0xD6) register bit description

Bit	Symbol	Access	Value	Description
[31:6]	RESERVED	r-	0x00	reserved
[5:4]	AUX_1_SLEW_RATE	rw	0x00	Selects Driver Strength for AUX_1
[3:2]	AUX_1_PUPD	rw	0x01	Enables PullUp/Down for AUX_1 (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
[1:1]	AUX_1_EN_OUT	rw	0x00	Enables Output driver for AUX_1
[0:0]	AUX_1_EN_IN	rw	0x00	Enables Input Driver for AUX_1

9.14.2.57 PCRM_SYS_SUSPEND_CTRL (0xD7)

This register provides configuration for SUSPEND entry.

Table 206. PCRM_SYS_SUSPEND_CTRL (0xD7) register bit description

Bit	Symbol	Access	Value	Description
[31:1]	RESERVED	r-	0x00	reserved
[0:0]	NFC_SUSPEND_ENTRY_REQ	-w	0x00	Suspend mode request entry configuration

9.14.2.58 PCRM_PAD_SPIM_MISO (0xD8)

This register provides settings for SPIM_MISO pin.

Table 207. PCRM_PAD_SPIM_MISO (0xD8) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x00	reserved
[16:16]	SPIM_MISO_ENABLE	rw	0x00	If set them SPIM_MISO unit output is driving the GPIO
[15:6]	RESERVED	r-	0x00	reserved
[5:4]	SPIM_MISO_SLEW_RATE	rw	0x00	Selects Driver Strength for SPIM_MISO
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	SPIM_MISO_EN_OUT	rw	0x00	Enables Output driver for SPIM_MISO
[0:0]	SPIM_MISO_EN_IN	rw	0x00	Enables Input Driver for SPIM_MISO

9.14.2.59 PCRM_PAD_SPIM_MOSI (0xD9)

This register provides settings for SPIM_MOSI pin.

Table 208. PCRM_PAD_SPIM_MOSI (0xD9) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x00	reserved
[16:16]	SPIM_MOSI_ENABLE	rw	0x00	If set them SPIM_MOSI unit output is driving the GPIO
[15:6]	RESERVED	r-	0x00	reserved
[5:4]	SPIM_MOSI_SLEW_RATE	rw	0x00	Selects Driver Strength for SPIM_MOSI
[3:2]	SPIM_MOSI_PUPD	rw	0x01	Enables PullUp/Down for SPIM_MOSI (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up

Table 208. PCRM_PAD_SPIM_MOSI (0xD9) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[1:1]	SPIM_MOSI_EN_OUT	rw	0x00	Enables Output driver for SPIM_MOSI
[0:0]	SPIM_MOSI_EN_IN	rw	0x00	Enables Input Driver for SPIM_MOSI

9.14.2.60 PCRM_PAD_SPIM_SCLK (0xDA)

This register provides settings for SPIM_SCLK pin.

Table 209. PCRM_PAD_SPIM_SCLK (0xDA) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x00	reserved
[16:16]	SPIM_SCLK_ENABLE	rw	0x00	If set them SPIM_SCLK unit output is driving the GPIO
[15:6]	RESERVED	r-	0x00	reserved
[5:4]	SPIM_SCLK_SLEW_RATE	rw	0x00	Selects Driver Strength for SPIM_SCLK
[3:2]	SPIM_SCLK_PUPD	rw	0x01	Enables PullUp/Down for SPIM_SCLK (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	SPIM_SCLK_EN_OUT	rw	0x00	Enables Output driver for SPIM_SCLK
[0:0]	SPIM_SCLK_EN_IN	rw	0x00	Enables Input Driver for SPIM_SCLK

9.14.2.61 PCRM_PAD_SPIM_SSN (0xDB)

This register provides settings for SPIM_SSN pin.

Table 210. PCRM_PAD_SPIM_SSN (0xDB) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x00	reserved
[16:16]	SPIM_SSN_ENABLE	rw	0x00	If set them SPIM_SSN unit output is driving the GPIO
[15:6]	RESERVED	r-	0x00	reserved
[5:4]	SPIM_SSN_SLEW_RATE	rw	0x00	Selects Driver Strength for SPIM_SSN
[3:2]	SPIM_SSN_PUPD	rw	0x01	Enables PullUp/Down for SPIM_SSN (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	SPIM_SSN_EN_OUT	rw	0x00	Enables Output driver for SPIM_SSN

Table 210. PCRM_PAD_SPIM_SSN (0xDB) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[0:0]	SPIM_SSN_EN_IN	rw	0x00	Enables Input Driver for SPIM_SSN

9.14.2.62 PCRM_PAD_I2CM_SCL (0xDC)

This register provides settings for I2CM_SCL pin.

Table 211. PCRM_PAD_I2CM_SCL (0xDC) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x00	reserved
[16:16]	I2CM_SCL_ENABLE	rw	0x00	If set them I2CM_SCL unit output is driving the GPIO
[15:8]	RESERVED	r-	0x00	reserved
[7:7]	I2CM_SCL_ECS	rw	0x00	Enables Pull-up current source for I2CM_SCL (I2C_SCL)
[6:6]	I2CM_SCL_EGP	rw	0x00	Enables GPIO mode (0: I2C mode; 1: GPIO mode) for I2CM_SCL (I2C_SCL)
			0b	I2C mode
			1b	GPIO mode
[5:5]	I2CM_SCL_FSEL	rw	0x00	Selects Input Filter value for I2C mode (0: 50ns; 1: 10ns) for I2CM_SCL (I2C_SCL)
			0b	50ns
			1b	10ns
[4:4]	I2CM_SCL_SLEW_RATE	rw	0x00	Selects Driver Strength / Speed mode (0: Low speed GPIO / SF and FP I2C mode; 1: Medium speed GPIO / HS I2C mode) on I2CM_SCL (I2C_SCL)
			0b	Low speed GPIO / SF and FP I2C mode
			1b	Medium speed GPIO / HS I2C mode
[3:2]	I2CM_SCL_PUPD	rw	0x01	Enables PullUp/Down for I2CM_SCL (I2C_SCL) (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	I2CM_SCL_EN_OUT	rw	0x00	Enables Output driver for I2CM_SCL (I2C_SCL)
[0:0]	I2CM_SCL_EN_IN	rw	0x00	Enables Input Driver for I2CM_SCL (I2C_SCL)

9.14.2.63 PCRM_PAD_I2CM_SDA (0xDD)

This register provides settings for I2CM_SDA pin.

Table 212. PCRM_PAD_I2CM_SDA (0xDD) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x00	reserved
[16:16]	I2CM_SDA_ENABLE	rw	0x00	If set them I2CM_SDA unit output is driving the GPIO
[15:8]	RESERVED	r-	0x00	reserved
[7:7]	I2CM_SDA_ECS	rw	0x00	Enables Pull-up current source for I2CM_SDA (I2C_SDA)
[6:6]	I2CM_SDA_EGP	rw	0x00	Enables GPIO mode (0: I2C mode; 1: GPIO mode)for I2CM_SDA (I2C_SDA)
			0b	I2C mode
			1b	GPIO mode
[5:5]	I2CM_SDA_FSEL	rw	0x00	Selects Input Filter value for I2C mode (0: 50ns; 1: 10ns) for I2CM_SDA (I2C_SDA)
			0b	50ns
			1b	10ns
[4:4]	I2CM_SDA_SLEW_RATE	rw	0x00	Selects Driver Strength / Speed mode (0: Low speed GPIO / SF and FP I2C mode; 1: Medium speed GPIO / HS I2C mode) on I2CM_SDA (I2C_SDA)
			0b	Low speed GPIO / SF and FP I2C mode
			1b	Medium speed GPIO / HS I2C mode
[3:2]	I2CM_SDA_PUPD	rw	0x01	Enables PullUp/Down for I2CM_SDA (I2C_SDA) (00b: Weak Pull-Down; 01b: No Pull; 10b: Bus Keeper; 11b: Weak Pull-Up)
			00b	Weak Pull-Down
			01b	No Pull
			10b	Bus Keeper
			11b	Weak Pull-Up
[1:1]	I2CM_SDA_EN_OUT	rw	0x00	Enables Output driver for I2CM_SDA (I2C_SDA)
[0:0]	I2CM_SDA_EN_IN	rw	0x00	Enables Input Driver for I2CM_SDA (I2C_SDA)

9.14.2.64 PCRM_PAD_CTAUX_IO (0xDE)

This register provides settings for CT_AUX_IO pin.

Table 213. PCRM_PAD_CTAUX_IO (0xDE) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x00	reserved
[16:16]	IO_AUX_ENABLE	rw	0x00	If set the CT_AUX IP is driving this pad, otherwise GPIO mode is active.
[15:7]	RESERVED	r-	0x00	reserved

Table 213. PCRM_PAD_CTAUX_IO (0xDE) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[6:6]	IO_AUX_ZIF_SEL	rw	0x00	Select whether ZI or ZIF pad pin shall be used (0:ZI, 1= ZIF)
			00b	ZI
			01b	ZIF
[5:5]	IO_AUX_INDEF	rw	0x00	Defines receiver output state when receiver is disabled.
[4:4]	IO_AUX_EHS	rw	0x00	Output Driver Speed for CT_AUX_IO (0: Slow, 1:Fast)
			00b	Slow
			01b	Fast
[3:3]	IO_AUX_ENQN	rw	0x00	Quasi-bidirectional mode control for CT_AUX_IO (0: Disabled, 1: Enabled)
			00b	Disabled
			01b	Enabled
[2:2]	IO_AUX_EPUN	rw	0x01	Enables weak pullup for CT_AUX_IO (Active Low)
[1:1]	IO_AUX_EPD	rw	0x00	Enables weak pulldown for CT_AUX_IO
[0:0]	IO_AUX_ENZI	rw	0x01	Enables Receiver for CT_AUX_IO (Active Low)

9.14.2.65 PCRM_PAD_CTAUX_CLK (0xDF)

This register provides settings for CT_AUX_CLK pin.

Table 214. PCRM_PAD_CTAUX_CLK (0xDF) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x00	reserved
[16:16]	CLK_AUX_ENABLE	rw	0x00	If set the CT_AUX IP is driving this pad, otherwise GPIO mode is active.
[15:7]	RESERVED	r-	0x00	reserved
[6:6]	CLK_AUX_ZIF_SEL	rw	0x00	Select whether ZI or ZIF pad pin shall be used (0:ZI, 1= ZIF)
			00b	ZI
			01b	ZIF
[5:5]	CLK_AUX_INDEF	rw	0x00	Defines receiver output state when receiver is disabled.
[4:4]	CLK_AUX_EHS	rw	0x00	Output Driver Speed for CT_AUX_CLK (0: Slow, 1:Fast)
			00b	Slow
			01b	Fast
[3:3]	CLK_AUX_ENQN	rw	0x00	Quasi-bidirectional mode control for CT_AUX_CLK (0: Disabled, 1: Enabled)
			00b	Disabled

Table 214. PCRM_PAD_CTAUX_CLK (0xDF) register bit description*...continued*

Bit	Symbol	Access	Value	Description
			01b	Enabled
[2:2]	CLK_AUX_EPUN	rw	0x01	Enables weak pullup for CT_AUX_CLK (Active Low)
[1:1]	CLK_AUX_EPD	rw	0x00	Enables weak pulldown for CT_AUX_CLK
[0:0]	CLK_AUX_ENZI	rw	0x01	Enable Receiver for CT_AUX_CLK (Active Low)

9.14.2.66 PCRM_PAD_CTAUX_INT (0xE0)

This register provides settings for CT_AUX_INT pin.

Table 215. PCRM_PAD_CTAUX_INT (0xE0) register bit description

Bit	Symbol	Access	Value	Description
[31:17]	RESERVED	r-	0x00	reserved
[16:16]	INT_AUX_ENABLE	rw	0x00	If set the CT_AUX IP is driving this pad, otherwise GPIO mode is active.
[15:7]	RESERVED	r-	0x00	reserved
[6:6]	INT_AUX_ZIF_SEL	rw	0x00	Select whether ZI or ZIF pad pin shall be used (0:ZI, 1= ZIF)
			00b	ZI
			01b	ZIF
[5:5]	INT_AUX_INDEF	rw	0x00	Defines receiver output state when receiver is disabled.
[4:4]	INT_AUX_EHS	rw	0x00	Output Driver Speed for CT_AUX_INT (0: Slow, 1:Fast)
			00b	Slow
			01b	Fast
[3:3]	INT_AUX_ENQN	rw	0x00	Quasi-bidirectional mode control for CT_AUX_INT (0: Disabled, 1 : Enabled)
			00b	Disabled
			01b	Enabled
[2:2]	INT_AUX_EPUN	rw	0x01	Enables weak pullup for CT_AUX_INT (Active Low)
[1:1]	INT_AUX_EPD	rw	0x00	Enables weak pulldown for CT_AUX_INT
[0:0]	INT_AUX_ENZI	rw	0x01	Enable Receiver for CT_AUX_INT (Active Low)

9.14.2.67 PCRM_CLIF_ULPDET_DISABLE (0xE1)

This register provides configuration to disable ULPDET.

Table 216. PCRM_CLIF_ULPDET_DISABLE (0xE1) register bit description

Bit	Symbol	Access	Value	Description
[31:1]	RESERVED	r-	0x00	reserved
[0:0]	RX_ULPDET_DISABLE	rw	0x00	Write '1' and sequentially write '0' will disable RX ULPDET function.

9.14.2.68 PCRM_CLIF_ULPDET_ENABLE (0xE2)

This register provides configuration to enable ULPDET.

Table 217. PCRM_CLIF_ULPDET_ENABLE (0xE2) register bit description

Bit	Symbol	Access	Value	Description
[31:1]	RESERVED	r-	0x00	reserved
[0:0]	RX_ULPDET_ENABLE	rw	0x00	Write '1' and sequentially write '0' will enable RX ULPDET function

9.14.2.69 PCRM_ANA_USBPLL_MODE (0xE3)

This register provides configuration for USB PLL.

Table 218. PCRM_ANA_USBPLL_MODE (0xE3) register bit description

Bit	Symbol	Access	Value	Description
[31:6]	RESERVED	r-	0x00	reserved
[5:5]	USBPLL_BYPASS_PDIV2	rw	0x00	Bypass of the divide by 2 divider in the post divider.
[4:4]	USBPLL_DIRECTO	rw	0x00	Bypass of the post-divider
[3:3]	USBPLL_DIRECTI	rw	0x00	Bypass of the pre-divider
[2:2]	USBPLL_BYPASS	rw	0x00	Bypass of the PLL (input clock to output clock)
[1:1]	USBPLL_CLKEN	rw	0x00	Enable of the output clock of the PLL
[0:0]	USBPLL_POWER_ENABLE	rw	0x00	Power enable input of the PLL (active high)

9.14.2.70 PCRM_ANA_USBPLL_DIV (0xE4)

This register provides configuration of USB PLL clock divisor settings.

Table 219. PCRM_ANA_USBPLL_DIV (0xE4) register bit description

Bit	Symbol	Access	Value	Description
[31:29]	RESERVED	r-	0x00	reserved
[28:24]	USBPLL_PDIV	rw	0x05	Post divider ratio (P-divider)
[23:8]	USBPLL_MDIV	rw	0xB1	Feedback divider ratio (M-divider)
[7:0]	USBPLL_NDIV	rw	0x0A	Predivider ratio (N-divider)

9.14.2.71 PCRM_ULPCD_CTRL3 (0xE5)

This register provides configuration for ULPCD.

Table 220. PCRM_ULPCD_CTRL3 (0xE5) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	LOAD	rw	0x00	Load ULPCD control signal to PCRM-AON
[30:29]	RESERVED	r-	0x00	reserved
[28:28]	ULP_STANDBY	rw	0x00	Ultra Low Power Standby
[27:27]	RESERVED	r-	0x00	reserved
[26:16]	RSSI_REFERENCE	rw	0x00	Relative Signal Strength Reference Level

Table 220. PCRM_ULPCD_CTRL3 (0xE5) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[15:15]	RESERVED	r-	0x00	reserved
[14:10]	RSSI_THRESHOLD	rw	0x00	Relative signal Strenght Threshold Level
[9:8]	RSSI_SAMPLES	rw	0x00	Number of RSSI samples
[7:7]	RESERVED	r-	0x00	reserved
[6:0]	RSSI_NSPL	rw	0x00	RSSI NSPL for LP GPADC

9.14.2.72 PCRM_ULPCD_CTRL2 (0xE6)

This register provides extended configuration for ULPCD.

Table 221. PCRM_ULPCD_CTRL2 (0xE6) register bit description

Bit	Symbol	Access	Value	Description
[31:23]	RESERVED	r-	0x00	reserved
[22:19]	ULPCD_VCM_TRIM	rw	0x00	VCM Trim value
[18:18]	ULPCD_GPIO3_ABORT_ POLARITY	rw	0x00	ULPCD GPIO3 abort polarity
[17:17]	ULPCD_GPIO3_ABORT_EN	rw	0x00	ULPCD GPIO3 abort enable
[16:16]	ULPCD_CALIBRATION	rw	0x00	ULPCD calibration enable
[15:15]	RESERVED	rw	0x00	reserved
[14:14]	VBAT_THRESH_SEL	rw	0x00	VBAT threshold select
[13:13]	VBAT_EN	rw	0x00	VBAT enable
[12:12]	VEN_INTERNAL	rw	0x00	VEN internal
[11:8]	ULPCD_SPARE	rw	0x00	SPARE register for retention
[7:7]	RESERVED	r-	0x00	reserved
[6:4]	XTAL_NOVERLAP_TRIMMING	rw	0x5	XTAL No-overlap trimming
[3:0]	ULFO_TRIM	rw	0x00	ULFO trim value

9.14.2.73 PCRM_ULPCD_CTRL1 (0xE7)

This register provides extended configuration of ULPCD.

Table 222. PCRM_ULPCD_CTRL1 (0xE7) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	BYPASS_VBAT_MON_CHECK_ AT_BOOT	rw	0x00	reserved
[30:30]	TX_SUPPLY_INTERNAL	rw	0x00	1: Internal TX supply, 0: External TX supply
[29:26]	RFON_GUARD_TIME	rw	0x00	RFON guard time: Trfon_guard_time = (RFON_ GUARD_TIME + 2) * Tlfo
[25:24]	TX_EN_DRV_DELAY	rw	0x00	TX enable driver delay: Ttx_enable_driver_delay = {5, 10, 15, 20} * Tlfo for TX_EN_DRV_DELAY = {0, 1, 2, 3}

Table 222. PCRM_ULPCD_CTRL1 (0xE7) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[23:22]	TX_EN_DELAY	rw	0x01	TX enable delay: Ttx_enable_delay = {10, 16, 23, 30} * Tlfo for TX_EN_DELAY = {0, 1, 2, 3}
[21:21]	RESERVED	rw	0x01	reserved
[20:16]	TX_SET_GS_PN_TX12	rw	0x1F	TX Set
[15:15]	LDO_VDDPA_CURRENT_SENSE_EN	rw	0x00	LDO VDDPA Current sense enable
[14:9]	LDO_VDDPA_VOUT_SEL	rw	0x00	LDO VDDPA VOUT select
[8:8]	LDO_VDDPA_LIMITER_EN	rw	0x00	LDO VDDPA limiter enable
[7:7]	LDO_VDDPA_OVERCURRENT_EN	rw	0x00	LDO VDDPA overcurrent enable
[6:6]	LDO_VDDPA_CURMIN_EN	rw	0x00	LDO VDDPA CURMIN enable
[5:0]	RX_AGC_HFATT_CTRL	rw	0x00	RX AGC HF Attenuator control

9.14.2.74 PCRM_ULPCD_CTRL0 (0xE8)

This register provides extended configuration of ULPCD.

Table 223. PCRM_ULPCD_CTRL0 (0xE8) register bit description

Bit	Symbol	Access	Value	Description
[31:29]	RESERVED	r-	0x00	reserved
[28:27]	XTAL_OVER_BOOST_DELAY	rw	0x02	XTAL over boost delay: Txtal_over_boost_delay = {10, 16, 23, 30} * Tlfo for XTAL_OVER_BOOST_DELAY = {0, 1, 2, 3}
[26:23]	XTAL_SLICER_DELAY	rw	0x08	XTAL Slicer delay: Txtal_slicer_delay = 66 + (XTAL_SLICER_DELAY * 4) * Tlfo
[22:22]	XTAL_OVER_BOOST_EN	rw	0x01	XTAL over boost delay enable
[21:16]	XTAL_AMP_CTRL	rw	0x19	XTAL control
[15:12]	RESERVED	r-	0x00	reserved
[11:0]	ULPCD_WKUP_TIME	rw	0x00	Wakeup Timer Reload Value: Tulpcd_wkup_time = ULPCD_WKUP_TIME * Tulfo

9.14.2.75 PCRM_HP_ULPCD_STS (0xE9)

This register provides status of ULPCD configuration loaded to low-power registers before starting ULPCD.

Table 224. PCRM_HP_ULPCD_STS (0xE9) register bit description

Bit	Symbol	Access	Value	Description
[31:1]	RESERVED	r-	0x00	reserved
[0:0]	BUSY	r-	0x00	ULPCD register file data transfer in progress

9.14.2.76 PCRM_PMU_ANA_SMPS_CTRL (0xEA)

This register provides configuration for DC-DC boost onboard.

Table 225. PCRM_PMU_ANA_SMPS_CTRL (0xEA) register bit description

Bit	Symbol	Access	Value	Description
[31:30]	RESERVED	r-	0x00	reserved
[29:27]	SMPS_MAXDT_SEL	rw	0x00	SMPS max duty cycle value, valid when SMPS_ MAX_DTC_BYPASS is set
[26:26]	SMPS_MAXDT_SEL_BYPASS	rw	0x00	SMPS max duty cycle lookup table bypass
[25:24]	SMPS_GM	rw	0x00	SMPS Gm set up
[23:22]	SMPS_RSENSE	rw	0x00	SMPS Rsense set up
[21:20]	SMPS_SOFT_START	rw	0x01	SMPS Soft Start set up
[19:17]	SMPS_SAWTOOTHGEN	rw	0x00	SMPS Sawtooth generator set up
[16:14]	RESERVED	r-	0x00	reserved
[13:12]	SMPS_PROT_UNDERSHOOT_ VTH	rw	0x00	SMPS
[11:10]	SMPS_REG_SPARE_0	rw	0x00	SMPS
[9:7]	SMPS_PID	rw	0x00	SMPS PID filter set up
[6:1]	SMPS_VDDBOOST_VOUT_SEL	rw	0x00	SMPS Ouput voltage selection
[0:0]	SMPS_EN	rw	0x00	SMPS enable

9.14.2.77 PCRM_ULPCD_CTRL4 (0xEB)

This register provides configuration for ULPCD.

Table 226. PCRM_ULPCD_CTRL4 (0xEB) register bit description

Bit	Symbol	Access	Value	Description
[31:28]	ULPCD_LP_SPARE	rw	0x00	Spare register control/status between PCRM_AON and PCRM_LP
[27:20]	RESERVED	r-	0x00	reserved
[19:18]	ULPCD_GPADC_START_HIGH_ TIME	rw	0x00	Width of START. 0: 2CLK, 1: 3CLK, 2: 5CLK, 3: 9CLK
[17:16]	ULPCD_GPADC_RST_DIS_TO_ START_TIME	rw	0x00	GPADC RST de-assertion to GPADC START assertion delay. 0: 3CLK, 1: 4CLK, 2: 6CLK, 3: 10CLK
[15:14]	ULPCD_GPADC_EN_TO_RST_ DIS_TIME	rw	0x00	GPADC EN to GPADC RST de-assertion delay. 0: 1CLK, 1: 2 CLK, 2: 4CLK, 3: 8CLK
[13:12]	ULPCD_GPADC_RST_SET_TO_ EN_TIME	rw	0x00	GPADC RST assertion to GPADC EN time. 0: 1CLK, 1: 2 CLK, 2: 3CLK, 3: 4CLK
[11:10]	ULPCD_CLKDET_CHK_DELAY_ WAIT_MULT	rw	0x00	CLKDET check delay wait multiplier. 0: 12'd1140 1: 12'd3188
[9:6]	ULPCD_TESTBUS_MUX_SEL	rw	0x00	Testbus MUX select
[5:5]	ULPCD_TESTBUS_EN	rw	0x00	Enable ULPCD testbus
[4:4]	ULPCD_FUNC_DEBUG_MODE	rw	0x00	ULPCD Functional Debug mode enable
[3:3]	ULPCD_GPADC_SHIFT	rw	0x00	ULPCD GPADC shift
[2:1]	ULPCD_XTAL_SLICER_PSM	rw	0x00	Set XTAL slicer driving strength

Table 226. PCRM_ULPCD_CTRL4 (0xEB) register bit description*...continued*

Bit	Symbol	Access	Value	Description
[0:0]	ULPCD_XTAL_BYPASS_EN	rw	0x00	XTAL bypass enable

9.14.2.78 PCRM_ANA_USBPLL_STS (0xEC)

This register provides status of USB PLL settings.

Table 227. PCRM_ANA_USBPLL_STS (0xEC) register bit description

Bit	Symbol	Access	Value	Description
[31:5]	RESERVED	r-	0x00	reserved
[4:4]	USBPLL_FR	r-	0x00	Free running detector output (active high)
[3:3]	USBPLL_PACK	r-	0x00	USB_PLL Post-Divider Ratio Change Acknowledge
[2:2]	USBPLL_NACK	r-	0x00	Pre-divider ratio change acknowledge output
[1:1]	USBPLL_MACK	r-	0x00	Feedback divider ratio change acknowledge output
[0:0]	USBPLL_LOCK	r-	0x00	Lock detector output (active high)

9.14.2.79 PCRM_ANA_USBPLL_CTRL (0xED)

This register provides USBPLL control.

Table 228. PCRM_ANA_USBPLL_CTRL (0xED) register bit description

Bit	Symbol	Access	Value	Description
[31:7]	RESERVED	r-	0x00	reserved
[6:6]	USBPLL_LIMUP_OFF	rw	0x00	Up limiter control pin
[5:5]	USBPLL_FRM_CLOCKSTABLE	rw	0x00	Free running mode clock stable control input
[4:4]	USBPLL_PREQ	rw	0x00	USB_PLL Post-Divider Ratio Change Request
[3:3]	USBPLL_NREQ	rw	0x00	USB_PLL Pre-Divider Ratio Change Request
[2:2]	USBPLL_MREQ	rw	0x00	USB_PLL Feedback Divider Ratio Change Request
[1:1]	USBPLL_FRM	rw	0x00	Free running mode control input
[0:0]	USBPLL_SKEW_EN	rw	0x00	USB_PLL Skew Mode

9.14.2.80 PCRM_ANA_USBPLL_BW (0xEE)

This register provides USBPLL settings for bandwidth selection.

Table 229. PCRM_ANA_USBPLL_BW (0xEE) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	USBPLL_BAND_DIRECT	rw	0x00	Bandwidth adjustment pin to modify the bandwidth of the PLL directly
[30:15]	RESERVED	r-	0x00	reserved
[14:9]	USBPLL_SELI	rw	0x2D	Bus to select the bandwidth
[8:4]	USBPLL_SELP	rw	0x1F	Bus to select the bandwidth
[3:0]	USBPLL_SELR	rw	0x00	Bus to select the bandwidth

9.14.2.81 PCRM_CLIF_DAC (0xEF)

This register provides the configuration required for antenna tuning DAC.

Table 230. PCRM_CLIF_DAC (0xEF) register bit description

Bit	Symbol	Access	Value	Description
[31:28]	RESERVED	r-	0x00	reserved
[27:24]	TUNING_DAC_2_OFFSET_CTRL	rw	0x06	x111b=2V, x110b=3V, x100b=3.45V, x000b=3.8V
[23:17]	TUNING_DAC_2_CTRL	rw	0x00	Output voltage of DAC2 according to 1/128 *(TUNING_DAC_2_CTRL) * (Range in V)
[16:16]	TUNING_DAC_2_PD	rw	0x0	0=DAC Turned off, 1=DAC enabled
[15:12]	RESERVED	r-	0x00	reserved
[11:8]	TUNING_DAC_1_OFFSET_CTRL	rw	0x06	x111b=2V, x110b=3V, x100b=3.45V, x000b=3.8V
[7:1]	TUNING_DAC_1_CTRL	rw	0x00	Output voltage of DAC1 according to 1/128 *(TUNING_DAC_1_CTRL) * (Range in V)
[0:0]	TUNING_DAC_1_PD	rw	0x0	0=DAC Turned off, 1=DAC enabled

9.14.2.82 PCRM_HP_SYS_CLK_EN (0xF0)

This register provides clock enable for various peripherals controlled by application.

Table 231. PCRM_HP_SYS_CLK_EN (0xF0) register bit description

Bit	Symbol	Access	Value	Description
[31:25]	RESERVED	r-	0x00	reserved
[24:24]	CT_AUX_IF_APB_CLK_ENABLE	rw	0x00	Enables clock source for CT_AUX_IF_APB
[23:23]	CT_AUX_IF_CLK_ENABLE	rw	0x00	Enables clock source for CT_AUX_IF
[22:22]	LP_UART_CLK_ENABLE	rw	0x00	Enables clock source for LP UART
[21:21]	HS_UART_CLK_ENABLE	rw	0x00	Enables clock source for LP UART
[20:20]	PWM_CLK_ENABLE	rw	0x00	Enables clock source for PWM unit
[19:19]	PWM_45M_CLK_ENABLE	rw	0x00	Enables clock source for PWM unit
[18:14]	RESERVED	rw	0x00	reserved
[13:13]	USB_APB_CLK_ENABLE	rw	0x00	Enables clock source for USB APB
[12:12]	USB_CLK_ENABLE	rw	0x00	Enables clock source for USB
[11:11]	SPIM_F_CLK_ENABLE	rw	0x00	Enables clock source for SPIM-H CLOCK
[10:10]	SPIM_H_CLK_ENABLE	rw	0x00	Enables clock source for SPIM-F CLOCK
[9:9]	I2CM_APB_CLK_ENABLE	rw	0x00	Enables clock source for I2CM APB
[8:8]	I2CM_CLK_ENABLE	rw	0x00	Enables clock source for I2CM
[7:7]	CRC_CLK_ENABLE	rw	0x00	Enables clock source for CRC
[6:6]	HOSTIF_APB_CLK_ENABLE	rw	0x00	Enables clock source for HostIF_APB
[5:5]	HOSTIF_CLK_ENABLE	rw	0x00	Enables clock source for HOSTIF
[4:4]	TIMERS_CLK_ENABLE	rw	0x00	Enables clock source for TIMERS

Table 231. PCRM_HP_SYS_CLK_EN (0xF0) register bit description...*continued*

Bit	Symbol	Access	Value	Description
[3:0]	RESERVED	rw	0x00	reserved

9.14.2.83 PCRM_SYS_CLK_MUX_SEL (0xF1)

This register provides clock selection for CLIF and contact interface.

Table 232. PCRM_SYS_CLK_MUX_SEL (0xF1) register bit description

Bit	Symbol	Access	Value	Description
[3:13]	RESERVED	r-	0x00	reserved
[1:12]	CLIF_CLK_SRC_SEL_A0	rw	0x00	ceres option to select ceres A0 or B0 cclif clock
[1:7]	RESERVED	r-	0x00	reserved
[6:6]	CTIF_CLK_SRC_SEL	rw	0x00	contact interface clock selection (0;27.12 Mhz 1: USBPLL div/2)
[5:0]	RESERVED	r-	0x00	Selects the source clock for the GPADC (0:HFO/4, 1: clk_27.12MHx clock source from CLIF ANA).

9.14.3 EEPROM configuration description

The settings done in EEPROM are used for basic configuration which does not change frequently. Typically it is performed once during trimming or configuration of a product. The EEPROM has a limited number of erase/write cycles that can be performed. This means, that configurations that change frequently must be performed in standard registers which do not keep their value during reset and power off.

This section describes the EEPROM configuration of the PN7642.

Writing to the EEPROM has to be performed with Read-Modify-Write for all memory addresses which contain RFU bits.

The detailed description of the EEPROM is available in the User API documentation.

9.14.3.1 EEPROM configuration for power, TXLDO, XTAL and Clocks

This section provides the configuration of diffrent EEPROM paramters for the system.

9.14.3.1.1 List of EEPROM configuration parameters for power, TXLDO, XTAL and Clocks

Table 233. List of EEPROM configuration parameters for power, TXLDO, XTAL and Clocks

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
DCDC_PWR_CONFIG (0x0000)	PN76_USER_PMU->PwrConfig	0x0000	0	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
DCDC_CONFIG (0x0001)	PN76_USER_PMU->Dcdc Config	0x0001	1	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TXLDO_CONFIG (0x0002)	PN76_USER_PMU->Txldo Config	0x0002	2	4	E_PN76_EEPROM_SECURE_LIB_CONFIG
TXLDO_VDDPA_CONFIG (0x0006)	PN76_USER_PMU->TxldoStart Vddpa	0x0006	6	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

Table 233. List of EEPROM configuration parameters for power, TXLDO, XTAL and Clocks*...continued*

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
TXLDO_VDDPA_MAX_RDR (0x0007)	PN76_USER_PMU->TxLdoVddpaMaxRdr	0x0007	7	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TXLDO_VDDPA_MAX_CARD (0x0008)	PN76_USER_PMU->TxLdoVddpaMaxCard	0x0008	8	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
BOOST_DEFAULT_VOLTAGE (0x0009)	PN76_USER_PMU->BoostDefaultVoltage	0x0009	9	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
XTAL_CONFIG (0x000F)	PN76_CLKGEN->bXtalConfig	0x000F	15	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
XTAL_TIMEOUT (0x0010)	PN76_CLKGEN->bXtalTimeOut	0x0010	16	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
CLK_INPUT_FREQ (0x0011)	PN76_RF_CLOCK_CFG->bPLLClkInputFrq	0x0011	17	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
XTAL_CHECK_DELAY (0x0012)	PN76_RF_CLOCK_CFG->bXtalCheckDelay	0x0012	18	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

9.14.3.1.2 DCDC_PWR_CONFIG (0x0000)

Configuration for power.

Table 234. DCDC_PWR_CONFIG (0x0000)

Function	bit	Values	Description
DC-DC usage in card mode	[7]	0x00	DC-DC is not powered and set to bypass
		0x01	DC-DC is powered and not bypassed
DC-DC usage in reader mode	[6]	0x00	DC-DC is not powered and set to bypass
		0x01	DC-DC is powered and not bypassed
RFU	[5]		Do not touch. Default value is 0x01
VUP input voltage	[4:0]	0x00	Not connected or 0 V
		0x01	No DC-DC and internal VDDPA_LDO: VUP supplied by VBAT / VBATPWR (pin VUP_TX connected to VBAT/VBATPWR)
		0x02	Internal DC-DC: with auto by pass and variable boost w.r.t VDDPA (internal DPC controls VDDBOOST): DC-DC goes into pass through mode when the VDDPA goes below 3.3 V. When VDDPA is greater than 3.3 V, the DC-DC is configured to boost voltage in range of 3.3 V to 6 V. Internal DC-DC: with fixed VDDBOOST
		0x05 - 0x09	RFU
		0x10	No DC-DC and internal VDDPA_LDO: VUP supplied by external LDO (not connected to VBAT)

9.14.3.1.3 DCDC_CONFIG (0x0001)

DCDC Configuration

Table 235. DCDC_CONFIG (0x0001)

Function	bit	Values	Description
RFU	[7:5]		Reserved
DC-DC pass through feature	[4]	0x00	DC-DC pass through feature is not supported (Vout = 0v or +5v)
		0x01	DC-DC pass through feature is supported (Vout = 0v or +5v)
DC-DC for LPCD (Not ULPCD)	[3]	0x00	Use of DC-DC for LPCD disabled (Not ULPCD)
		0x01	Use of DC-DC for LPCD enabled (Not ULPCD)
RFU	[2:0]		Reserved

9.14.3.1.4 TXLDO_CONFIG (0x0002)

Table 236. TXLDO_CONFIG (0x0002)

Function	bit	Values	Description
RFU	[31:2]		Reserved
Overcurrent protection	[1]	0x00	Overcurrent protection feature disabled
		0x01	Overcurrent protection feature enabled
Enable Tx-LDO	[0]	0x00	TxLDO is disabled. No voltage output of the TXLDO
		0x01	TxLDO is enabled. Regulated voltage output of the TXLDO

9.14.3.1.5 TXLDO_VDDPA_CONFIG (0x0006)

Table 237. TXLDO_VDDPA_CONFIG (0x0006)

Function	bit	Values	Description
VDDPA voltage level	[7:0]	0x00 - 0x2A	Value 0 indicates 1.50 V. Further VDDPA voltage would be: 1.50+0.10*this parameter value (in Volt). Maximum value of 0x2A indicates 5.70 V. 0x00: 1V50 0x01: 1V60 0x02: 1V70 0x03: 1V80 0x04: 1V90 0x05: 2V00 0x06: 2V10 0x07: 2V20 0x08: 2V30 0x09: 2V40 0x0A: 2V50 0x0B: 2V60 0x0C: 2V70 0x0D: 2V80 0x0E: 2V90 0x0F: 3V00 0X10: 3V10 0x11: 3V20 0x12: 3V30 0x13: 3V40 0x14: 3V50 0x15: 3V60 0x16: 3V70 0x17: 3V80 0x18: 3V90 0x19: 4V00 0x1A: 4V10 0x1B: 4V20 0x1C: 4V30

Table 237. TXLDO_VDDPA_CONFIG (0x0006)

Function	bit	Values	Description
			0x1D: 4V40 0x1E: 4V50 0x1F: 4V60 0x20: 4V70 0x21: 4V80 0x22: 4V90 0x23: 5V00 0x24: 5V10 0x25: 5V20 0x26: 5V30 0x27: 5V40 0x28: 5V50 0x29: 5V60 0x2A: 5V70

9.14.3.1.6 TXLDO_VDDPA_MAX_RDR (0x0007)

Table 238. TXLDO_VDDPA_MAX_RDR (0x0007)

Function	bit	Values	Description
VDDPA max voltage level	[7:0]	0x00 - 0x2A	Value 0 indicates 1.50 V. Further VDDPA voltage would be 1.50+0.10*this parameter value. Maximum value of 0x2A indicates for 5.70 V 0x00: 1V50 0x01: 1V60 0x02: 1V70 0x03: 1V80 0x04: 1V90 0x05: 2V00 0x06: 2V10 0x07: 2V20 0x08: 2V30 0x09: 2V40 0x0A: 2V50 0x0B: 2V60 0x0C: 2V70 0x0D: 2V80 0x0E: 2V90 0x0F: 3V00 0X10: 3V10 0x11: 3V20 0x12: 3V30 0x13: 3V40 0x14: 3V50 0x15: 3V60 0x16: 3V70 0x17: 3V80 0x18: 3V90 0x19: 4V00 0x1A: 4V10 0x1B: 4V20 0x1C: 4V30 0x1D: 4V40 0x1E: 4V50 0x1F: 4V60 0x20: 4V70 0x21: 4V80 0x22: 4V90 0x23: 5V00 0x24: 5V10 0x25: 5V20 0x26: 5V30 0x27: 5V40 0x28: 5V50 0x29: 5V60 0x2A: 5V70

9.14.3.1.7 TXLDO_VDDPA_MAX_CARD (0x0008)

Table 239. TXLDO_VDDPA_MAX_CARD (0x0008)

Function	bit	Values	Description
VDDPA max voltage level	[7:0]	0x00 - 0x2A	Value 0 indicates 1.50 V. Further VDDPA voltage would be 1.50+0.10*this parameter value. Maximum value of 0x2A indicates for 5.70 V 0x00: 1V50 0x01: 1V60 0x02: 1V70 0x03: 1V80 0x04: 1V90 0x05: 2V00 0x06: 2V10 0x07: 2V20 0x08: 2V30 0x09: 2V40 0x0A: 2V50 0x0B: 2V60 0x0C: 2V70 0x0D: 2V80 0x0E: 2V90 0x0F: 3V00 0X10: 3V10 0x11: 3V20 0x12: 3V30 0x13: 3V40 0x14: 3V50 0x15: 3V60 0x16: 3V70 0x17: 3V80 0x18: 3V90 0x19: 4V00 0x1A: 4V10 0x1B: 4V20 0x1C: 4V30 0x1D: 4V40 0x1E: 4V50 0x1F: 4V60 0x20: 4V70 0x21: 4V80 0x22: 4V90 0x23: 5V00 0x24: 5V10 0x25: 5V20 0x26: 5V30 0x27: 5V40 0x28: 5V50 0x29: 5V60 0x2A: 5V70

9.14.3.1.8 BOOST_DEFAULT_VOLTAGE (0x0009)

Table 240. BOOST_DEFAULT_VOLTAGE (0x0009)

Function	bit	Values	Description
VDDBOOST output voltage	[7:0]	0x00 - 0x1D	Value 0 indicates 3.1 V. Further VDDBOOST voltage would be 3.10+0.10*this parameter value. Maximum value of 0x1D indicates for 6.00 V 0x00: 3.1 V 0x01: 3.2 V 0x02: 3.3 V 0x03: 3.4 V 0x04: 3.5 V 0x05: 3.6 V 0x06: 3.7 V 0x07: 3.8 V 0x08: 3.9 V 0x09: 4.0 V 0x0A: 4.1 V 0x0B: 4.2 V 0x0C: 4.3 V 0x0D: 4.4 V 0x0E: 4.5 V 0x0F: 4.6 V 0x10: 4.7 V 0x11: 4.8 V 0x12: 4.9 V 0x13: 5.0 V 0x14: 5.1 V 0x15: 5.2 V 0x16: 5.3 V 0x17: 5.4 V 0x18: 5.5 V 0x19: 5.6 V 0x1A: 5.7 V 0x1B: 5.8 V 0x1C: 5.9 V 0x1D: 6.0 V
		Other values	RFU

9.14.3.1.9 XTAL_CONFIG (0x000F)

Configuration for the XTAL startup procedure

Table 241. XTAL_CONFIG (0x000F)

Function	bit	Values	Description
RFU	[7:1]		RFU
XTAL startup procedure	[0]	0x00	disable Crystal recalibration start after wake-up
		0x01	enable Crystal recalibration start after wake-up

9.14.3.1.10 XTAL_TIMEOUT (0x0010)

Timeout for XTAL to be ready

Table 242. XTAL_TIMEOUT (0x0010)

Function	bit	Values	Description
Configuration for XTAL startup procedure	[7:0]		Timeout for XTAL to be ready (in *128us). This configuration does not speed up the boot time.

9.14.3.1.11 CLK_INPUT_FREQ (0x0011)

Configuration for the PLL input clock frequency

Table 243. CLK_INPUT_FREQ (0x0011)

Function	bit	Values	Description
RFU	[7:4]		RFU
PLL clock configuration	[3:0]	0x00	8MHz
		0x01	12MHz
		0x02	16MHz
		0x03	24MHz
		0x04	32MHz
		0x05	48MHz
		0x06	RFU
		0x07	22.5MHz HFO
		0x08	XTAL 27.12 MHz
		others	RFU

9.14.3.1.12 XTAL_CHECK_DELAY (0x0012)

Table 244. XTAL_CHECK_DELAY (0x0012)

Function	bit	Values	Description
RFRetry_numberU	[7:5]		Max Number of retries before a clock error is raised
Interval	[4:0]		Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18.8 us). This is the time to try to lock the PLL, a stable crystal clock is required for locking. If the PLL is not locked, a next retry to lock the PLL will be done after this interval. This value can be used to optimize the startup time dependent on the crystal characteristics. This is important, e.g., for optimization of the LPCD and ULPCD.

9.14.3.1.13 VDDPA_DISCHARGE (0x050D)

enable/disable fast VDDPA Discharge

Table 245. VDDPA_DISCHARGE (0x050D)

Function	bits	Values	Description
RFU	[7:1]		Reserved
EnableFast VDDPADischarge	[0]	0x00	Disables fast discharge of VDDPA by setting VDDPA=5.7 and then to 1.5 V, during RF OFF
		0x01	Enables fast discharge of VDDPA by setting VDDPA=5.7 and then to 1.5 V, during RF OFF (default)

9.14.3.2 RM_TX_SHAPING - TX wave shaping for passive reader mode

This section provides the TX shaping for different type of cards in passive reader mode.

9.14.3.2.1 TX wave shaping for TypeA passive reader mode for all baud-rates.

This section provides the TX shaping for TypeA passive reader mode.

9.14.3.2.1.1 RESIDUAL_AMPL_LEVEL_A106 (0x0014)

Residual amplitude level for A106

Table 246. RESIDUAL_AMPL_LEVEL_A106 (0x0014)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.1.2 EDGE_TYPE_A106 (0x0015)

Edge type for A106

Table 247. EDGE_TYPE_A106 (0x0015)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.1.3 EDGE_STYLE_A106 (0x0016)

Time constant Edge style configuration for A106

Table 248. EDGE_STYLE_A106 (0x0016)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ A106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ A106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.1.4 EDGE_LENGTH_A106 (0x0017)

Edge length for A106

Table 249. EDGE_LENGTH_A106 (0x0017)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.1.5 RESIDUAL_AMPL_LEVEL_A212 (0x0018)

Table 250. RESIDUAL_AMPL_LEVEL_A212 (0x0018)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.1.6 EDGE_TYPE_A212 (0x0019)

Table 251. EDGE_TYPE_A212 (0x0019)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.1.7 EDGE_STYLE_A212 (0x001A)

Table 252. EDGE_STYLE_A212 (0x001A)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ A212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ A212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.1.8 EDGE_LENGTH_A212 (0x001B)

Table 253. EDGE_LENGTH_A212 (0x001B)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.1.9 RESIDUAL_AMPL_LEVEL_A424 (0x001C)

Table 254. RESIDUAL_AMPL_LEVEL_A424 (0x001C)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.1.10 EDGE_TYPE_A424 (0x001D)

Table 255. EDGE_TYPE_A424 (0x001D)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.1.11 EDGE_STYLE_A424 (0x001E)

Table 256. EDGE_STYLE_A424 (0x001E)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A424 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ A424 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A424 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ A424 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.1.12 EDGE_LENGTH_A424 (0x001F)

Table 257. EDGE_LENGTH_A424 (0x001F)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.1.13 RESIDUAL_AMPL_LEVEL_A848 (0x0020)

Table 258. RESIDUAL_AMPL_LEVEL_A848 (0x0020)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.1.14 EDGE_TYPE_A848 (0x0021)

Table 259. EDGE_TYPE_A848 (0x0021)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.1.15 EDGE_STYLE_A848 (0x0022)

Table 260. EDGE_STYLE_A848 (0x0022)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A848 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ A848 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A848 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ A848 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.1.16 EDGE_LENGTH_A848 (0x0023)

Table 261. EDGE_LENGTH_A848 (0x0023)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.2 TX wave shaping for Type B passive reader mode for all baud-rates.

This section provides the TX shaping for Type B passive reader mode.

9.14.3.2.2.1 RESIDUAL_AMPL_LEVEL_B106 (0x0024)

Table 262. RESIDUAL_AMPL_LEVEL_B106 (0x0024)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.2.2 EDGE_TYPE_B106 (0x0025)

Table 263. EDGE_TYPE_B106 (0x0025)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.2.3 EDGE_STYLE_B106 (0x0026)

Table 264. EDGE_STYLE_B106 (0x0026)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_B106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ B106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_B106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ B106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.2.4 EDGE_LENGTH_B106 (0x0027)

Table 265. EDGE_LENGTH_B106 (0x0027)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.2.5 RESIDUAL_AMPL_LEVEL_B212 (0x0028)

Table 266. RESIDUAL_AMPL_LEVEL_B212 (0x0028)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.2.6 EDGE_TYPE_B212 (0x0029)

Table 267. EDGE_TYPE_B212 (0x0029)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.2.7 EDGE_STYLE_B212 (0x002A)

Table 268. EDGE_STYLE_B212 (0x002A)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_B212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ B212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_B212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ B212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.2.8 EDGE_LENGTH_B212 (0x002B)

Table 269. EDGE_LENGTH_B212 (0x002B)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.2.9 RESIDUAL_AMPL_LEVEL_B424 (0x002C)

Table 270. RESIDUAL_AMPL_LEVEL_B424 (0x002C)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.2.10 EDGE_TYPE_B424 (0x002D)

Table 271. EDGE_TYPE_B424 (0x002D)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.2.11 EDGE_STYLE_B424 (0x002E)

Table 272. EDGE_STYLE_B424 (0x002E)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_B424 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ B424 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_B424 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ B424 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.2.12 EDGE_LENGTH_B424 (0x002F)

Table 273. EDGE_LENGTH_B424 (0x002F)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.2.13 RESIDUAL_AMPL_LEVEL_B848 (0x0030)

Table 274. RESIDUAL_AMPL_LEVEL_B848 (0x0030)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.2.14 EDGE_TYPE_B848 (0x0031)

Table 275. EDGE_TYPE_B848 (0x0031)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.2.15 EDGE_STYLE_B848 (0x0032)

Table 276. EDGE_STYLE_B848 (0x0032)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_B848 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ B848 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_B848 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ B848 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.2.16 EDGE_LENGTH_B848 (0x0033)

Table 277. EDGE_LENGTH_B848 (0x0033)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.3 TX wave shaping for Type F passive reader mode for all baud-rates.

This section provides the TX shaping for Type F passive reader mode.

9.14.3.2.3.1 RESIDUAL_AMPL_LEVEL_F212 (0x0034)

Table 278. RESIDUAL_AMPL_LEVEL_F212 (0x0034)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.3.2 EDGE_TYPE_F212 (0x0035)

Table 279. EDGE_TYPE_F212 (0x0035)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.3.3 EDGE_STYLE_F212 (0x0036)

Table 280. EDGE_STYLE_F212 (0x0036)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_F212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_F212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.3.4 EDGE_LENGTH_F212 (0x0037)

Table 281. EDGE_LENGTH_F212 (0x0037)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.3.5 RESIDUAL_AMPL_LEVEL_F424 (0x0038)

Table 282. RESIDUAL_AMPL_LEVEL_F424 (0x0038)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.3.6 EDGE_TYPE_F424 (0x0039)

Table 283. EDGE_TYPE_F424 (0x0039)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.3.7 EDGE_STYLE_F424 (0x003A)

Table 284. EDGE_STYLE_F424 (0x003A)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_F424 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F424 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_F424 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F424 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.3.8 EDGE_LENGTH_F424 (0x003B)

Table 285. EDGE_LENGTH_F424 (0x003B)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.4 TX wave shaping for Type V (ISO15693) passive reader mode for all baud-rates.

This section provides the TX shaping for Type V (ISO15693) passive reader mode.

9.14.3.2.4.1 RESIDUAL_AMPL_LEVEL_V10_26 (0x004C)

Table 286. RESIDUAL_AMPL_LEVEL_V10_26 (0x004C)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.4.2 EDGE_TYPE_V10_26 (0x004D)

Table 287. EDGE_TYPE_V10_26 (0x004D)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.4.3 EDGE_STYLE_V10_26 (0x004E)

Table 288. EDGE_STYLE_V10_26 (0x004E)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V10_26 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ V10_26 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V10_ 26 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ V10_26 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.4.4 EDGE_LENGTH_V10_26 (0x004F)

Table 289. EDGE_LENGTH_V10_26 (0x004F)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.4.5 RESIDUAL_AMPL_LEVEL_V10_53 (0x0050)

Table 290. RESIDUAL_AMPL_LEVEL_V10_53 (0x0050)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.4.6 EDGE_TYPE_V10_53 (0x0051)

Table 291. EDGE_TYPE_V10_53 (0x0051)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.4.7 EDGE_STYLE_V10_53 (0x0052)

Table 292. EDGE_STYLE_V10_53 (0x0052)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V10_53 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ V10_53 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V10_ 53 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ V10_53 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.4.8 EDGE_LENGTH_V10_53 (0x0053)

Table 293. EDGE_LENGTH_V10_53 (0x0053)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.4.9 RESIDUAL_AMPL_LEVEL_V10_106 (0x0054)

Table 294. RESIDUAL_AMPL_LEVEL_V10_106 (0x0054)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.4.10 EDGE_TYPE_V10_106 (0x0055)

Table 295. EDGE_TYPE_V10_106 (0x0055)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.4.11 EDGE_STYLE_V10_106 (0x0056)

Table 296. EDGE_STYLE_V10_106 (0x0056)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V10_106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V10_106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V10_106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V10_106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.4.12 EDGE_LENGTH_V10_106 (0x0057)

Table 297. EDGE_LENGTH_V10_106 (0x0057)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.4.13 RESIDUAL_AMPL_LEVEL_V10_212 (0x0058)

Table 298. RESIDUAL_AMPL_LEVEL_V10_212 (0x0058)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.4.14 EDGE_TYPE_V10_212 (0x0059)

Table 299. EDGE_TYPE_V10_212 (0x0059)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.4.15 EDGE_STYLE_V10_212 (0x005A)

Table 300. EDGE_STYLE_V10_212 (0x005A)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V10_212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V10_212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V10_212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V10_212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.4.16 EDGE_LENGTH_V10_212 (0x005B)

Table 301. EDGE_LENGTH_V10_212 (0x005B)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.4.17 RESIDUAL_AMPL_LEVEL_V100_26 (0x003C)

Table 302. RESIDUAL_AMPL_LEVEL_V100_26 (0x003C)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.4.18 EDGE_TYPE_V100_26 (0x003D)

Table 303. EDGE_TYPE_V100_26 (0x003D)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.4.19 EDGE_STYLE_V100_26 (0x003E)

Table 304. EDGE_STYLE_V100_26 (0x003E)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_26 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_26 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_26 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_26 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.4.20 EDGE_LENGTH_V100_26 (0x003F)

Table 305. EDGE_LENGTH_V100_26 (0x003F)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.4.21 RESIDUAL_AMPL_LEVEL_V100_53 (0x0040)

Table 306. RESIDUAL_AMPL_LEVEL_V100_53 (0x0040)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.4.22 EDGE_TYPE_V100_53 (0x0041)

Table 307. EDGE_TYPE_V100_53 (0x0041)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.4.23 EDGE_STYLE_V100_53 (0x0042)

Table 308. EDGE_STYLE_V100_53 (0x0042)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_53 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_53 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_53 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_53 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.4.24 EDGE_LENGTH_V100_53 (0x0043)

Table 309. EDGE_LENGTH_V100_53 (0x0043)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.4.25 RESIDUAL_AMPL_LEVEL_V100_106 (0x0044)

Table 310. RESIDUAL_AMPL_LEVEL_V100_106 (0x0044)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.4.26 EDGE_TYPE_V100_106 (0x0045)

Table 311. EDGE_TYPE_V100_106 (0x0045)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.4.27 EDGE_STYLE_V100_106 (0x0046)

Table 312. EDGE_STYLE_V100_106 (0x0046)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.4.28 EDGE_LENGTH_V100_106 (0x0047)

Table 313. EDGE_LENGTH_V100_106 (0x0047)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.4.29 RESIDUAL_AMPL_LEVEL_V100_212 (0x0048)

Table 314. RESIDUAL_AMPL_LEVEL_V100_212 (0x0048)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.4.30 EDGE_TYPE_V100_212 (0x0049)

Table 315. EDGE_TYPE_V100_212 (0x0049)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.4.31 EDGE_STYLE_V100_212 (0x004A)

Table 316. EDGE_STYLE_V100_212 (0x004A)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.4.32 EDGE_LENGTH_V100_212 (0x004B)

Table 317. EDGE_LENGTH_V100_212 (0x004B)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.5 TX wave shaping for ISO18000 p3m3 passive reader mode for all baud-rates.

This section provides the TX shaping for ISO18000 p3m3 passive reader mode.

9.14.3.2.5.1 RESIDUAL_AMPL_LEVEL_180003M3_TARI9P44 (0x0060)

Table 318. RESIDUAL_AMPL_LEVEL_180003M3_TARI9P44 (0x0060)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.5.2 EDGE_TYPE_180003M3_TARI9P44 (0x0061)

Table 319. EDGE_TYPE_180003M3_TARI9P44 (0x0061)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.5.3 EDGE_STYLE_180003M3_TARI9P44 (0x0062)

Table 320. EDGE_STYLE_180003M3_TARI9P44 (0x0062)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_ 180003M3_TARI9P44 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ 180003M3_TARI9P44 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_ 180003M3_TARI9P44 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ 180003M3_TARI9P44 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.5.4 EDGE_LENGTH_180003M3_TARI9P44 (0x0063)

Table 321. EDGE_LENGTH_180003M3_TARI9P44 (0x0063)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.5.5 RESIDUAL_AMPL_LEVEL_180003M3_TARI18P88 (0x005C)

Table 322. RESIDUAL_AMPL_LEVEL_180003M3_TARI18P88 (0x005C)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.5.6 EDGE_TYPE_180003M3_TARI18P88 (0x005D)

Table 323. EDGE_TYPE_180003M3_TARI18P88 (0x005D)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.5.7 EDGE_STYLE_180003M3_TARI18P88 (0x005E)

Table 324. EDGE_STYLE_180003M3_TARI18P88 (0x005E)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_ 180003M3_TARI18P8 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ 180003M3_TARI18P8 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_ 180003M3_TARI18P8 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ 180003M3_TARI18P8 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.5.8 EDGE_LENGTH_180003M3_TARI18P88 (0x005F)

Table 325. EDGE_LENGTH_180003M3_TARI18P88 (0x005F)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.2.6 TX wave shaping for B-Prime passive reader mode for all baud-rates.

This section provides the TX shaping for B-Prime passive reader mode.

9.14.3.2.6.1 RESIDUAL_AMPL_LEVEL_B_PRIME106 (0x0064)

Table 326. RESIDUAL_AMPL_LEVEL_B_PRIME106 (0x0064)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.2.6.2 EDGE_TYPE_B_PRIME106 (0x0065)

Table 327. EDGE_TYPE_B_PRIME106 (0x0065)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.2.6.3 EDGE_STYLE_B_PRIME106 (0x0066)

Table 328. EDGE_STYLE_B_PRIME106 (0x0066)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_B_ PRIME106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_B_ PRIME106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_B_ PRIME106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_B_ PRIME106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.2.6.4 EDGE_LENGTH_B_PRIME106 (0x0067)

Table 329. EDGE_LENGTH_B_PRIME106 (0x0067)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.3 DPC Settings

This section provides the settings related to DPC configuration

9.14.3.3.1 DPC_CONFIG (0x0068)

DPC configuration

Table 330. DPC_CONFIG (0x0068)

Function	bit	Values	Description
RFU	[7:3]		RFU
DPC in Active target mode	[2]		DPC configuration in active target mode
		0x00	disabled

Table 330. DPC_CONFIG (0x0068)*...continued*

Function	bit	Values	Description
		0x01	enabled
DPC in Active initiator mode	[1]		DPC configuration in active initiator mode
		0x00	disabled
		0x01	enabled
DPC in Reader/Passive Initiator mode	[0]		DPC configuration in Reader/ Passive Initiator mode
		0x00	disabled
		0x01	enabled

9.14.3.3.2 DPC_TARGET_CURRENT (0x0069)

DPC configuration unloaded VDDPA target current in mA

Table 331. DPC_TARGET_CURRENT (0x0069)

Function	bit	Values	Description
DPC in Active target mode	[15:0]		VDDPA target current in mA. The target current +/- hysteresis defines the limiting maximum current for the DPC.

Note: This configuration shall not exceed 350 mA - hysteresis.

Note: The resulting current that is driven by the transmitter can be further reduced based on the current reduction lookup table entries.

9.14.3.3.3 DPC_HYSTERESIS_LOADING (0x006B)

The hysteresis (**bHysteresis** and **bHysteresis_Unloading**) together with the target current (**wTargetCurrent**) defines the current limit, at which the DPC automatically decreases or raises the VDDPA. The VDDPA is automatically reduced, as soon as the current exceeds the **wTargetCurrent + bHysteresis**, and the VDDPA is automatically increased again, as soon as the current is below **wTargetCurrent** # **bHysteresis_Unloading**.

Table 332. DPC_HYSTERESIS_LOADING (0x006B)

Function	bit	Values	Description
DPC hysteresis loading	[7:0]		Absolute difference to current Target Current in mA that triggers a DPC update event during loading.

Note: If the hysteresis is configured too small, it might cause an oscillation of the transmitted field.

Note: In most application, the default values work well and do not need to be modified.

9.14.3.3.4 DPC_ALGO_INTERVAL (0x006C)

Table 333. DPC_ALGO_INTERVAL (0x006C)

Function	bit	Values	Description
algointerval	[15:0]	1ms	DPC algorithm time interval between two consecutive current checks, unit = 128/13,56MHz (~9.44us) Default = 1ms

9.14.3.3.5 DPC_HYSTERESIS_UNLOADING (0x006E)

Table 334. DPC_HYSTERESIS_UNLOADING (0x006E)

Function	bit	Values	Description
DPC hysteresis unloading	[7:0]		Absolute difference to current Target Current in mA that triggers a DPC update event during unloading.

9.14.3.3.6 DPC_TXLDOVDDPALow (0x006F)

Table 335. DPC_TXLDOVDDPALow (0x006F)

Function	bit	Values	Description
TXLDOVDDPALow	[7:0]		VDDPA Low Limit for RDON

9.14.3.3.7 DPC_TXGSN (0x0070)

TXGSN configuration.

Table 336. DPC_TXGSN (0x0070)

Function	bit	Values	Description
DPC hysterisis loading	[7:0]	Less than 20	resistance = 10 Ohm / (tx1_gsn + 1)
		more than or equal 20	20: resistance = 0.5 Ohm

9.14.3.3.8 DPC_RDON_CONTROL (0x0071)

Table 337. DPC_RDON_CONTROL (0x0071)

Function	bit	Values	Description
VDDPA low limit control	[7:0]	0x00	Disabled
		0x01	RdON Control
		0x02	PWM control
		Others	RFU

9.14.3.3.9 DPC_InitialRDOn_RFOn (0x0072)

Table 338. DPC_InitialRDOn_RFOn (0x0072)

Function	bit	Values	Description
DPC_InitialRDOn_RFOn	[7:0]		Initial GSP TX1/TX2 value during FieldON

9.14.3.3.10 DPC_TXLDO_MAX_DROPOUT (0x0073)

Table 339. DPC_TXLDO_MAX_DROPOUT (0x0073)

Function	bit	Values	Description
DPC_TXLDO_MAX_DROPOUT	[15:0]	0xE10*	Maximum allowed voltage drop in milliVolts in the TxLDO, between `VUP` and `VDDPA`, if DPC is enabled. ***Note:*** *`VDDPA` does not go below `(VUP – DPC_TXLDO_MAX_DROPOUT)`, even if the loading requires a lower `VDDPA`.*

Table 339. DPC_TXLDO_MAX_DROPOUT (0x0073)

Function	bit	Values	Description
			Default = E10h = 3600 mV

9.14.3.3.11 DPC_GUARD_TIME (0x0079)

Table 340. DPC_GUARD_TIME (0x0079)

Function	bit	Values	Description
algointerval	[7:0]		DPC guard time configuration. Guard time before tx. 1unit = 1us.

The DPC regulation is done once before TX and once after RX.

The guard time parameter is the time between DPC regulation completion and TX start.

The guard time parameter is the time between RX stop and DPC regulation start.

The guard time is always enabled for TX

Note: Recommendation is not to modify the default value.

9.14.3.3.12 DPC_ENABLE_DURING_FDT (0x007A)

DPC regulation enable during FDT.

Table 341. DPC_ENABLE_DURING_FDT (0x007A)

Function	bit	Values	Description
Disable DPC during FDT	[7:0]	0x00	DPC disabled during FDT (debug purpose only)
		0x01	DPC enabled during FDT (recommendation)
		others	RFU

9.14.3.3.13 DPC_GUARD_TIME_AFTER_RX (0x007B)

Enable DPC with guard time after RX

Table 342. DPC_GUARD_TIME_AFTER_RX (0x007B)

Function	bit	Values	Description
Enable DPC guard time after RX	[7:0]	0x00	DPC disabled after RX (debug purpose only)
		0x01	DPC enabled after RX (recommendation)
		others	RFU

9.14.3.3.14 DPC Lookup table entries

Table 343. DPC lookup table entries

Entry	Address	Function	bit	Values	Description
ENTRY 0 for 1V5	0x7D	This below details are for entry 0. Similar is for all other entries.			
		Target current reduction	[31:24]		Byte 0. Target current reduction in mA (unsigned)
		AWC amp mod change	[23:16]		Byte 1. Relative change of modulated amplitude level (signed)

Table 343. DPC lookup table entries*...continued*

Entry	Address	Function	bit	Values	Description
		AWC edge time constant for ASK100	[15:8]		Byte 2. Target current reduction in mA (unsigned)
			[15:12]		ASK100, Relative change of rising edge time constant (signed)
			[11:8]		ASK100, Relative change of falling edge time constant (signed)
		AWC edge time constant for ASK100	[7:0]		Byte 2. Target current reduction in mA (unsigned)
			[7:4]		ASK10, Relative change of rising edge time constant (signed)
			[3:0]		ASK10, Relative change of falling edge time constant (signed)
ENTRY_01 for 1.60V	0x0081	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_02 for 1.70V	0x0085	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_03 for 1.80V	0x0089	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_04 for 1.90V	0x008D	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_05 for 2.00V	0x0091	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_06 for 2.10V	0x0095	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_07 for 2.20V	0x0099	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_08 for 2.30V	0x009D	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_09 for 2.40V	0x00A1	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_10 for 2.50V	0x00A5	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_11 for 2.60V	0x00A9	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_12 for 2.70V	0x00AD	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_13 for 2.80V	0x00B1	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_14 for 2.90V	0x00B5	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_15 for 3.00V	0x00B9	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_16 for 3.10V	0x00BD	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_17 for 3.20V	0x00C1	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_18 for 3.30V	0x00C5	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_19 for 3.40V	0x00C9	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_20 for 3.50V	0x00CD	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_21 for 3.60V	0x00D1	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_22 for 3.70V	0x00D5	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_23 for 3.80V	0x00D9	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_24 for 3.90V	0x00DD	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_25 for 4.00V	0x00E1	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_26 for 4.10V	0x00E5	Byte and bit-fields description, refer to ENTRY_0 .			

Table 343. DPC lookup table entries*...continued*

Entry	Address	Function	bit	Values	Description
ENTRY_27 for 4.20V	0x00E9	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_28 for 4.30V	0x00ED	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_29 for 4.40V	0x00F1	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_30 for 4.50V	0x00F5	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_31 for 4.60V	0x00F9	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_32 for 4.70V	0x00FD	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_33 for 4.80V	0x0101	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_34 for 4.90V	0x0105	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_35 for 5.00V	0x0109	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_36 for 5.10V	0x010D	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_37 for 5.20V	0x0111	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_38 for 5.30V	0x0115	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_39 for 5.40V	0x0119	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_40 for 5.50V	0x011D	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_41 for 5.60V	0x0121	Byte and bit-fields description, refer to ENTRY_0 .			
ENTRY_42 for 5.70V	0x0125	Byte and bit-fields description, refer to ENTRY_0 .			

9.14.3.4 ARC Settings for passive reader modes

This section provides the ARC settings for Reader Mode TX wave shaping configuration

9.14.3.4.1 ARC_SETTINGS_BARCCONFIG (0x0129)

ARC settings configuration.

Table 344. ARC_SETTINGS_BARCCONFIG (0x0129)

Function	bit	Values	Description
ARC settings configuration	[7]	0x00	ARC algorithm is disabled.
		0x01	ARC algorithm is enabled.
	[6:3]		RFU
	[2:0]		Number of entries in ARC table
		0x00	one entry
		0x01	two entries
		0x02	three entries
		0x03	four entries
		0x04	five entries
		others	RFU

9.14.3.4.2 ARC_SETTINGS_WARCVDDPA (0x012B)

VDDPA settings.

Table 345. ARC_SETTINGS_WARCVDDPA (0x012B)

Function	byte	Values	Description
VDDPA settings	[4]	See below note	VDDPA range_index 4: if VDDPA voltage between VDDPA_3 to ARC_VDDPA_4
	[3]		VDDPA range_index 3: if VDDPA voltage between VDDPA_2 to ARC_VDDPA_3 - 0.1
	[2]		VDDPA_range_index 2: if VDDPA voltage between VDDPA_1 to ARC_VDDPA_2 - 0.1
	[1]		VDDPA_range_index 1: if VDDPA voltage between VDDPA_0 to (ARC_VDDPA_1 - 0.1)
	[0]		VDDPA_range_index 0: if VDDPA voltage between 1.5 to (VDDPA_0 - 0.1)

Note:for above settings, value of 0x00 indicates for 1V50, 0x01 indicates for 1V60. Further increase with 100mV and value of 0x2A corresponds to 5V70.

9.14.3.4.3 ARC_SETTINGS_WRMARCA_106 (0x0130)

ARC table settings for reader mode Type A 106kbps

Table 346. ARC_SETTINGS_WRMARCA_106 (0x0130)

Function	byte	bits	Values	Description
RM_RX_ARC_0	[9:8]	[15]		ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'.
			0x00	ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used.
			0x01	ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used.
		[14]		ARC enable/disable
			0x00	ARC disabled for this technology and baudrate
			0x01	ARC enabled for this technology and baudrate
		[13:10]		RFU
		[9]		Enable the IIR filter
		[8:7]		MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)
		[6:0]		DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_1	[7:6]	[15]		ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'.

Table 346. ARC_SETTINGS_WRMARCA_106 (0x0130)*...continued*

Function	byte	bits	Values	Description
			0x00	ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used.
			0x01	ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used.
		[14]		RFU
		[13:10]		RFU
		[9]		Enable the IIR filter
		[8:7]		MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)
		[6:0]		DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_2	[5:4]	[15]		ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'.
			0x00	ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used.
			0x01	ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used.
		[14]		RFU
		[13:10]		RFU
		[9]		Enable the IIR filter
		[8:7]		MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)
		[6:0]		DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_3	[3:2]	[15]		ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'.
			0x00	ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used.
			0x01	ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used.
		[14]		RFU
		[13:10]		RFU
		[9]		Enable the IIR filter

Table 346. ARC_SETTINGS_WRMARCA_106 (0x0130)*...continued*

Function	byte	bits	Values	Description
		[8:7]		MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)
		[6:0]		DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_4	[1:0]	[15]		ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'.
			0x00	ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used.
			0x01	ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used.
		[14]		RFU
		[13:10]		RFU
		[9]		Enable the IIR filter
		[8:7]		MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)
		[6:0]		DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

9.14.3.4.4 ARC_SETTINGS_TABLE for other technologies

Table 347. ARC_SETTINGS_TABLE for other technologies

Technology	Address	Function	Byte	Description
ARC_SETTINGS_A_212	0x13A-0x143	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_A_424	0x144-0x14D	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_A_848	0x14E-0x157	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.

Table 347. ARC_SETTINGS_TABLE for other technologies*...continued*

Technology	Address	Function	Byte	Description
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_B_106	0x158-0x161	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_B_212	0x162-0x16B	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_B_424	0x16C-0x175	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_B_848	0x176-0x17F	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_F_424	0x180-0x189	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_F_424	0x18A-0x193	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_V_6P6	0x19E-0x1A7	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.

Table 347. ARC_SETTINGS_TABLE for other technologies*...continued*

Technology	Address	Function	Byte	Description
ARC_SETTINGS_V_26	0x19E-0x1A7	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_V_53	0x1A8-0x1B1	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_V_106	0x1B2-0x1BB	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_V_212	0x1BC-0x1C5	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_180003M3_SC424_4MAN	0x1C6-1CF	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_180003M3_SC424_2MAN	0x1D0-1D9	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_180003M3_SC848_4MAN	0x1DA-0x1E3	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_180003M3_SC848_2MAN	0x1E4-0x1ED	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.

Table 347. ARC_SETTINGS_TABLE for other technologies*...continued*

Technology	Address	Function	Byte	Description
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_AI_106	0x1EE-0x1F7	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_AI_212	0x1F8-0x201	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.
ARC_SETTINGS_AI_424	0x202-0x20B	RM_RX_ARC_0	[9:8]	Refer to RM_RX_ARC_0.
		RM_RX_ARC_1	[7:6]	Refer to RM_RX_ARC_1.
		RM_RX_ARC_2	[5:4]	Refer to RM_RX_ARC_2.
		RM_RX_ARC_3	[3:2]	Refer to RM_RX_ARC_3.
		RM_RX_ARC_4	[1:0]	Refer to RM_RX_ARC_4.

9.14.3.4.5 ARC_RM_A106_FDT (0x051B)

Table 348. ARC_RM_A106_FDT (0x051B)

Function	Address	Bytesn	Bits	Value	Description
RM_RX_ARC_FDT_0	0x51B	[1:0]	Settings for RM_RX_ARC_FDT_0		
			[15]	0x00	ARC settings apply always
				0x01	ARC settings applicable during FDT
			[14]	0x00	ARC Disabled for this Tech and Baudrate
				0x01	ARC Enabled for this Tech and Baudrate
				NOTE	This bit is RFU for RM_RX_ARC_FDT_1, RM_RX_ARC_FDT_2, RM_RX_ARC_FDT_3, RM_RX_ARC_FDT_4.
			[13:10]		RFU. Reserved.
			[9]		Enable the IIR filter.
			[8:7]		MF_GAIN (ths value will be applied to the SIGPR_RM_

Table 348. ARC_RM_A106_FDT (0x051B)*...continued*

Function	Address	Bytesn	Bits	Value	Description
					TECH register, applies as soon as the ARC is enabled)
			[6:0]		DPC_ SIGNAL_DETECT_TH_ OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_FDT_1	0x51D	[3:2]	Settings for RM_RX_ARC_FDT_1. Bit definitions is same as that of RM_RX_ARC_FDT_0		
RM_RX_ARC_FDT_2	0x51F	[5:4]	Settings for RM_RX_ARC_FDT_2. Bit definitions is same as that of RM_RX_ARC_FDT_0		
RM_RX_ARC_FDT_3	0x521	[7:6]	Settings for RM_RX_ARC_FDT_3. Bit definitions is same as that of RM_RX_ARC_FDT_0		
RM_RX_ARC_FDT_4	0x523	[9:8]	Settings for RM_RX_ARC_FDT_4. Bit definitions is same as that of RM_RX_ARC_FDT_0		

9.14.3.5 RSSI configuration parameters (applicable for card emulation)

9.14.3.5.1 EEPROM_APC_RSSI_LIST

List of RSSI settings for card emulation only

Table 349. List of RSSI settings for card emulation only

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
RSSI_TIMER (0x020C)	PN76_APC_RSSI->bRssiTimer	0x020C	524	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
RSSI_TIMER_FIRST_PERIOD (0x020E)	PN76_APC_RSSI->bRssiTimerFirstPeriod	0x020E	526	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
RSSI_CTRL_00_AB (0x0210)	PN76_APC_RSSI->bRssiCtrl_00_AB	0x0210	528	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
RSSI_NB_ENTRIES_AB (0x0211)	PN76_APC_RSSI->bRssiNbEntriesAB	0x0211	529	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
RSSI_THRESHOLD_AB entries table	PN76_APC_RSSI->wRssiThresholdAB_01	0x0212-0x271	530	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
RSSI_CTRL_00_F (0x0272)	PN76_APC_RSSI->bRssiCtrl_00_F	0x0272	626	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
RSSI_NB_ENTRIES_F (0x0273)	PN76_APC_RSSI->bRssiNbEntriesF	0x0273	627	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
RSSI_THRESHOLD_F entries table	PN76_APC_RSSI->wRssiThresholdF_01	0x0274-0x2D3	628	2	E_PN76_EEPROM_SECURE_LIB_CONFIG

9.14.3.5.2 RSSI_TIMER (0x020C)

RSSI timer

Table 350. RSSI_TIMER (0x020C)

Function	bits	Values	Description
RSSI_TIMER	[15:0]		RSSI timer. Default: 423d.

9.14.3.5.3 RSSI_TIMER_FIRST_PERIOD (0x020E)

First period duration after Rf field ON.

Table 351. RSSI_TIMER_FIRST_PERIOD (0x020E)

Function	bits	Values	Description
RSSI	[15:0]		First period duration after Rffield ON. Unit is 128/ fc (106kHz) if set to 0 it means feature is not used 0D2 => ~2ms

9.14.3.5.4 RSSI_CTRL_00_AB (0x0210)

RSSI control.

Table 352. RSSI_CTRL_00_AB (0x0210)

Function	bits	Values	Description
RSSI	[7:6]		Reserved
	[5:0]		(APC_ID_REF_AB) ID of APC_TX entry that is equiv to RSSI = 0 (for Type AB)

9.14.3.5.5 RSSI_NB_ENTRIES_AB (0x0211)

For Initial RF ON, CEA and CEB.

Table 353. RSSI_NB_ENTRIES_AB (0x0211)

Function	bits	Values	Description
RSSI	[7:5]		Reserved
	[4:0]		Number of entries in RSSI look up table (it refers to RSSI_ENTRY_AB_01 to RSSI_ENTRY_AB_18);

9.14.3.5.6 RSSI_THRESHOLD_PHASE_TABLE for Type-A and Type-B

Table 354. RSSI_THRESHOLD_PHASE_TABLE for Type-A and Type-B

Entry	Address	Function	bit	Values	Description
RSSI_THRESHOLD_AB_01	0x212	RSSI	Threshold value for APC algorithm for TypeA and TypeB **Note:** dwRssiEntryAB_00 = 0 (not in EEPROM) Signed phase compensation with 1/4 degree resolution: 16 bits signed value (using complement of 2)		
			[15:13]		Reserved
			[12:0]		RSSI Value
RSSI_PHASE_AB_01	0x214	RSSI	[15:0]		Phase compensation value for APC algorithm for TypeA and TypeB. Signed phase compensation with 1/4 degree resolution:16 bits signed value (using complement of 2)

Table 354. RSSI_THRESHOLD_PHASE_TABLE for Type-A and Type-B*...continued*

Entry	Address	Function	bit	Values	Description
RSSI_THRESHOLD_AB_02	0x0216	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_02	0x0218	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_03	0x021A	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_03	0x021C	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_04	0x021E	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_04	0x0220	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_05	0x0222	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_05	0x0224	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_06	0x0226	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_06	0x0228	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_07	0x022A	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_07	0x022C	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_08	0x022E	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_08	0x0230	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_09	0x0232	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_09	0x0234	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_0A	0x0236	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_0A	0x0238	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_0B	0x023A	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_0B	0x023C	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_0C	0x023E	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_0C	0x0240	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_0D	0x0242	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_0D	0x0244	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_0E	0x0246	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_0E	0x0248	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_0F	0x024A	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_0F	0x024C	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_10	0x024E	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_10	0x0250	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_11	0x0252	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_11	0x0254	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_12	0x0256	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_12	0x0258	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_13	0x025A	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_13	0x025C	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			

Table 354. RSSI_THRESHOLD_PHASE_TABLE for Type-A and Type-B*...continued*

Entry	Address	Function	bit	Values	Description
RSSI_THRESHOLD_AB_14	0x025E	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_14	0x0260	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_15	0x0262	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_15	0x0264	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_16	0x0266	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_16	0x0268	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_17	0x026A	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_17	0x026C	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSI_THRESHOLD_AB_18	0x026E	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
RSSI_PHASE_AB_18	0x0270	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			

9.14.3.5.7 RSSI_CTRL_00_F (0x0272)

Table 355. RSSI_CTRL_00_F (0x0272)

Function	bits	Values	Description
RSSI	[7:6]		Reserved
	[5:0]		(APC_ID_REF_AB) ID of APC_TX entry that is equiv to RSSI = 0 (for Type F)

9.14.3.5.8 RSSI_NB_ENTRIES_F (0x0273)

Table 356. RSSI_NB_ENTRIES_F (0x0273)

Function	bits	Values	Description
RSSI	[7:5]		Reserved
	[4:0]		Number of entries in RSSI look up table (it refers to RSSI_ENTRY_F_01 to RSSI_ENTRY_F_18);

9.14.3.5.9 RSSI_THRESHOLD_PHASE_TABLE for Type-F

Table 357. RSSI_THRESHOLD_PHASE_TABLE for Type-F

Entry	Address	Function	bit	Values	Description
RSSI_THRESHOLD_F_01	0x276	RSSI	Threshold value for APC algorithm for TypeF **Note:** dwRssiEntryF_00 = 0 (not in EEPROM) Signed phase compensation with 1/4 degree resolution: 16 bits signed value (using complement of 2)		
			[15:13]		Reserved
			[12:0]		RSSI Value
RSSI_PHASE_F_01	0x276	RSSI	[15:0]		Phase compensation value for APC algorithm for TypeF. Signed phase compensation with 1/4 degree resolution:16 bits signed value (using complement of 2)
RSSI_THRESHOLD_F_02	0x0278	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			

Table 357. RSSI_THRESHOLD_PHASE_TABLE for Type-F*...continued*

Entry	Address	Function	bit	Values	Description
RSSI_PHASE_F_02	0x027A	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_03	0x027C	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_03	0x027E	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_04	0x0280	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_04	0x0282	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_05	0x0284	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_05	0x0286	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_06	0x0288	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_06	0x028A	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_07	0x028C	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_07	0x028E	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_08	0x0290	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_08	0x0292	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_09	0x0294	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_09	0x0296	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_0A	0x0298	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_0A	0x029A	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_0B	0x029C	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_0B	0x029E	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_0C	0x02A0	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_0C	0x02A2	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_0D	0x02A4	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_0D	0x02A6	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_0E	0x02A8	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_0E	0x02AA	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_0F	0x02AC	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_0F	0x02AE	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_10	0x02B0	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_10	0x02B2	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_11	0x02B4	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_11	0x02B6	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_12	0x02B8	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_12	0x02BA	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_13	0x02BC	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_13	0x02BE	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_14	0x02C0	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			

Table 357. RSSI_THRESHOLD_PHASE_TABLE for Type-F*...continued*

Entry	Address	Function	bit	Values	Description
RSSI_PHASE_F_14	0x02C2	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_15	0x02C4	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_15	0x02C6	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_16	0x02C8	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_16	0x02CA	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_17	0x02CC	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_17	0x02CE	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSI_THRESHOLD_F_18	0x02D0	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
RSSI_PHASE_F_18	0x02D2	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			

9.14.3.6 RSSI APC algorithm table output settings TX_PARAM_ENTRY_TABLE. Applicable only for card emulation.

APC TX_PARAM_ENTRY for ID.

Table 358. TX_PARAM_ENTRY_00_ID (0x02D4)

Entry ID	Address	Function	bits	Values	Description
ENTRY_00_ID	0x2D4	Driver count	[7]		Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT):
				0x00	Dual driver
				0x01	Single driver
		BPSK mode	[6]		BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE):
				0x00	Dual driver
				0x01	Single driver
		ID	[5:0]		ID
ENTRY_00_Tx1	0x2D5	RFU	[7:6]		Reserved
		PMU VDDPA setting	[5:0]		VDDPA(v) = (val*10)+1,5 0x00 = 1.50 V ... 0x2Ah = 5.70 V
ENTRY_00_Tx2	0x2D6	Scaling factor	[7:0]		Scaling factor for TX1 and TX2
ENTRY_01_ID	0x02D7	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_01_TX1	0x02D8	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_01_TX2	0x02D9	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_02_ID	0x02DA	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_02_TX1	0x02DB	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_02_TX2	0x02DC	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_03_ID	0x02DD	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_03_TX1	0x02DE	For bit-field values, refer to ENTRY_00_TX1 above			

Table 358. TX_PARAM_ENTRY_00_ID (0x02D4)*...continued*

Entry ID	Address	Function	bits	Values	Description
ENTRY_03_TX2	0x02DF	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_04_ID	0x02E0	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_04_TX1	0x02E1	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_04_TX2	0x02E2	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_05_ID	0x02E3	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_05_TX1	0x02E4	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_05_TX2	0x02E5	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_06_ID	0x02E6	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_06_TX1	0x02E7	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_06_TX2	0x02E8	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_07_ID	0x02E9	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_07_TX1	0x02EA	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_07_TX2	0x02EB	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_08_ID	0x02EC	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_08_TX1	0x02ED	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_08_TX2	0x02EE	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_09_ID	0x02EF	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_09_TX1	0x02F0	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_09_TX2	0x02F1	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_0A_ID	0x02F2	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_0A_TX1	0x02F3	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_0A_TX2	0x02F4	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_0B_ID	0x02F5	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_0B_TX1	0x02F6	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_0B_TX2	0x02F7	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_0C_ID	0x02F8	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_0C_TX1	0x02F9	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_0C_TX2	0x02FA	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_0D_ID	0x02FB	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_0D_TX1	0x02FC	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_0D_TX2	0x02FD	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_0E_ID	0x02FE	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_0E_TX1	0x02FF	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_0E_TX2	0x0300	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_0F_ID	0x0301	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_0F_TX1	0x0302	For bit-field values, refer to ENTRY_00_TX1 above			

Table 358. TX_PARAM_ENTRY_00_ID (0x02D4)*...continued*

Entry ID	Address	Function	bits	Values	Description
ENTRY_0F_TX2	0x0303	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_10_ID	0x0304	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_10_TX1	0x0305	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_10_TX2	0x0306	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_11_ID	0x0307	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_11_TX1	0x0308	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_11_TX2	0x0309	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_12_ID	0x030A	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_12_TX1	0x030B	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_12_TX2	0x030C	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_13_ID	0x030D	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_13_TX1	0x030E	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_13_TX2	0x030F	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_14_ID	0x0310	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_14_TX1	0x0311	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_14_TX2	0x0312	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_15_ID	0x0313	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_15_TX1	0x0314	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_15_TX2	0x0315	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_16_ID	0x0316	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_16_TX1	0x0317	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_16_TX2	0x0318	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_17_ID	0x0319	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_17_TX1	0x031A	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_17_TX2	0x031B	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_18_ID	0x031C	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_18_TX1	0x031D	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_18_TX2	0x031E	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_19_ID	0x031F	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_19_TX1	0x0320	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_19_TX2	0x0321	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_1A_ID	0x0322	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_1A_TX1	0x0323	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_1A_TX2	0x0324	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_1B_ID	0x0325	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_1B_TX1	0x0326	For bit-field values, refer to ENTRY_00_TX1 above			

Table 358. TX_PARAM_ENTRY_00_ID (0x02D4)*...continued*

Entry ID	Address	Function	bits	Values	Description
ENTRY_1B_TX2	0x0327	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_1C_ID	0x0328	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_1C_TX1	0x0329	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_1C_TX2	0x032A	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_1D_ID	0x032B	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_1D_TX1	0x032C	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_1D_TX2	0x032D	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_1E_ID	0x032E	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_1E_TX1	0x032F	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_1E_TX2	0x0330	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_1F_ID	0x0331	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_1F_TX1	0x0332	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_1F_TX2	0x0333	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_20_ID	0x0334	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_20_TX1	0x0335	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_20_TX2	0x0336	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_21_ID	0x0337	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_21_TX1	0x0338	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_21_TX2	0x0339	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_22_ID	0x033A	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_22_TX1	0x033B	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_22_TX2	0x033C	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_23_ID	0x033D	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_23_TX1	0x033E	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_23_TX2	0x033F	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_24_ID	0x0340	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_24_TX1	0x0341	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_24_TX2	0x0342	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_25_ID	0x0343	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_25_TX1	0x0344	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_25_TX2	0x0345	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_26_ID	0x0346	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_26_TX1	0x0347	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_26_TX2	0x0348	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_27_ID	0x0349	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_27_TX1	0x034A	For bit-field values, refer to ENTRY_00_TX1 above			

Table 358. TX_PARAM_ENTRY_00_ID (0x02D4)*...continued*

Entry ID	Address	Function	bits	Values	Description
ENTRY_27_TX2	0x034B	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_28_ID	0x034C	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_28_TX1	0x034D	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_28_TX2	0x034E	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_29_ID	0x034F	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_29_TX1	0x0350	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_29_TX2	0x0351	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_2A_ID	0x0352	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_2A_TX1	0x0353	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_2A_TX2	0x0354	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_2B_ID	0x0355	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_2B_TX1	0x0356	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_2B_TX2	0x0357	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_2C_ID	0x0358	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_2C_TX1	0x0359	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_2C_TX2	0x035A	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_2D_ID	0x035B	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_2D_TX1	0x035C	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_2D_TX2	0x035D	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_2E_ID	0x035E	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_2E_TX1	0x035F	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_2E_TX2	0x0360	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_2F_ID	0x0361	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_2F_TX1	0x0362	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_2F_TX2	0x0363	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_30_ID	0x0364	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_30_TX1	0x0365	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_30_TX2	0x0366	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_31_ID	0x0367	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_31_TX1	0x0368	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_31_TX2	0x0369	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_32_ID	0x036A	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_32_TX1	0x036B	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_32_TX2	0x036C	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_33_ID	0x036D	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_33_TX1	0x036E	For bit-field values, refer to ENTRY_00_TX1 above			

Table 358. TX_PARAM_ENTRY_00_ID (0x02D4)*...continued*

Entry ID	Address	Function	bits	Values	Description
ENTRY_33_TX2	0x036F	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_34_ID	0x0370	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_34_TX1	0x0371	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_34_TX2	0x0372	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_35_ID	0x0373	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_35_TX1	0x0374	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_35_TX2	0x0375	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_36_ID	0x0376	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_36_TX1	0x0377	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_36_TX2	0x0378	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_37_ID	0x0379	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_37_TX1	0x037A	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_37_TX2	0x037B	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_38_ID	0x037C	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_38_TX1	0x037D	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_38_TX2	0x037E	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_39_ID	0x037F	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_39_TX1	0x0380	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_39_TX2	0x0381	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_3A_ID	0x0382	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_3A_TX1	0x0383	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_3A_TX2	0x0384	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_3B_ID	0x0385	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_3B_TX1	0x0386	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_3B_TX2	0x0387	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_3C_ID	0x0388	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_3C_TX1	0x0389	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_3C_TX2	0x038A	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_3D_ID	0x038B	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_3D_TX1	0x038C	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_3D_TX2	0x038D	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_3E_ID	0x038E	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_3E_TX1	0x038F	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_3E_TX2	0x0390	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_3F_ID	0x0391	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_3F_TX1	0x0392	For bit-field values, refer to ENTRY_00_TX1 above			

Table 358. TX_PARAM_ENTRY_00_ID (0x02D4)*...continued*

Entry ID	Address	Function	bits	Values	Description
ENTRY_3F_TX2	0x0393	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_40_ID	0x0394	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_40_TX1	0x0395	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_40_TX2	0x0396	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_41_ID	0x0397	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_41_TX1	0x0398	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_41_TX2	0x0399	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_42_ID	0x039A	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_42_TX1	0x039B	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_42_TX2	0x039C	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_43_ID	0x039D	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_43_TX1	0x039E	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_43_TX2	0x039F	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_44_ID	0x03A0	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_44_TX1	0x03A1	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_44_TX2	0x03A2	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_45_ID	0x03A3	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_45_TX1	0x03A4	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_45_TX2	0x03A5	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_46_ID	0x03A6	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_46_TX1	0x03A7	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_46_TX2	0x03A8	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_47_ID	0x03A9	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_47_TX1	0x03AA	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_47_TX2	0x03AB	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_48_ID	0x03AC	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_48_TX1	0x03AD	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_48_TX2	0x03AE	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_49_ID	0x03AF	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_49_TX1	0x03B0	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_49_TX2	0x03B1	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_4A_ID	0x03B2	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_4A_TX1	0x03B3	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_4A_TX2	0x03B4	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_4B_ID	0x03B5	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_4B_TX1	0x03B6	For bit-field values, refer to ENTRY_00_TX1 above			

Table 358. TX_PARAM_ENTRY_00_ID (0x02D4)...*continued*

Entry ID	Address	Function	bits	Values	Description
ENTRY_4B_TX2	0x03B7	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_4C_ID	0x03B8	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_4C_TX1	0x03B9	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_4C_TX2	0x03BA	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_4D_ID	0x03BB	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_4D_TX1	0x03BC	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_4D_TX2	0x03BD	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_4E_ID	0x03BE	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_4E_TX1	0x03BF	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_4E_TX2	0x03C0	For bit-field values, refer to ENTRY_00_TX2 above			

9.14.3.7 Autocol configuration settings.

Autocol configuration settings.

9.14.3.7.1 List of Autocoll configuration settings

List of Autocoll configuration settings

Table 359. List of Autocoll configuration settings

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
RF_DEBOUNCE_TIMEOUT (0x03C4)	PN76_AUTOCOLL_CFG->bRfDebounceTimeout	0x03C4	964	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
SENSE_RES (0x03C5)	PN76_AUTOCOLL_CFG->bSensRes	0x03C5	965	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
NFC_ID1 (0x03C7)	PN76_AUTOCOLL_CFG->bNfcID1	0x03C7	967	3	E_PN76_EEPROM_SECURE_LIB_CONFIG
SEL_RES (0x03CA)	PN76_AUTOCOLL_CFG->bSelRes	0x03CA	970	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
FELICA_POLLRES (0x03CB)	PN76_AUTOCOLL_CFG->bPollRes	0x03CB	971	18	E_PN76_EEPROM_SECURE_LIB_CONFIG
RANDOM_UID_ENABLE (0x03DD)	PN76_AUTOCOLL_CFG->bRandomUIDEnable	0x03DD	989	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

9.14.3.7.2 RF_DEBOUNCE_TIMEOUT (0x03C4)

Debounce timeout

Table 360. RF_DEBOUNCE_TIMEOUT (0x03C4)

Function	bits	Values	Description
DEBOUNCE_TIMEOUT	[7:0]		Timeout used after the RF detection during the AUTOCOLL to detect if there is a glitch or continuous RF. Value is entered in 1 micro seconds.

9.14.3.7.3 SENSE_RES (0x03C5)

Response to ReqA / ATQA in order byte 0, byte 1.

Table 361. SENSE_RES (0x03C5)

Function	bits	Values	Description
Response to ReqA / ATQA	[15:0]		ATQA in order byte 0, byte 1
	[15:8]		Byte1 value
	[7:0]		Byte0 value

9.14.3.7.4 NFC_ID1 (0x03C7)

Response to ReqA / ATQA in order byte 0, byte 1

Table 362. NFC_ID1 (0x03C7)

Function	bits	Values	Description
UID address generation	[31:0]		If Random UID is disabled (EEPROM address 0x2CB), the content of these addresses is used to generate a Fixed UID. The order is byte 0, Byte 1, Byte 2; Byte3 - which is the first NFCID1 byte - is fixed to 08h, the check byte is calculated automatically.
	[31:24]	0x08	Byte3 value
	[23:16]		Byte2 value
	[15:8]		Byte1 value
	[7:0]		Byte0 value

9.14.3.7.5 SEL_RES (0x03CA)

Response to Select : SAK.

Table 363. SEL_RES (0x03CA)

Function	bits	Values	Description
Response to Select	[7:0]		Response to Select : SAK

9.14.3.7.6 FELICA_POLLRES (0x03CB)

Response to Select : SAK

Table 364. FELICA_POLLRES (0x03CB)

Function	byte	bits	Values	Description
Felica Poll response	[1:0]	[15:0]	0x01FE	FeliCa polling response. Shall be the same value.
	[7:2]	[47:0]		FeliCa polling response. NFCID2 (6 bytes).
	[15:8]	[63:0]		FeliCa polling response. PAD (8 bytes).
	[17:16]	[15:0]		FeliCa polling response. System code (2 bytes).

9.14.3.7.7 RANDOM_UID_ENABLE (0x03DD)

Random UID enable

Table 365. RANDOM_UID_ENABLE (0x03DD)

Function	bits	Values	Description
Random UID enable	[7:1]		Reserved
	[0]	0x00	Use UID stored in EEPROM
		0x01	Randomly generate the UID in which the first byte is fixed and the remaining 3 bytes are random A new random number is generated after each RF-OFF to RF-ON.

9.14.3.8 LPCD related configuration parameters

9.14.3.8.1 EEPROM_LPCD_SETTINGS_LIST

List of LPCD related configuration settings

Table 366. List of LPCD related configuration settings

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
EEPR1OM_LPCD_SETTINGS_AVG_SAMPLES	PN76_LPCD_SETTINGS->avg_samples	0x03DE	990	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPCD_RSSI_TARGET (0x03E0)	PN76_LPCD_SETTINGS->lpcd_rssi_target	0x03E0	992	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPCD_RSSI_HYST (0x03E2)	PN76_LPCD_SETTINGS->lpcd_rssi_hyst	0x03E2	994	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPCD_CONFIG (0x03E3)	PN76_LPCD_SETTINGS->wConfig	0x03E3	995	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPCD_THRESHOLD (0x03E6)	PN76_LPCD_SETTINGS->lpcd_threshold_coarse	0x03E6	998	4	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPCD_WAIT_RX_SETTLE (0x03F7)	PN76_LPCD_SETTINGS->wWaitRxSettle	0x03F7	1015	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPCD_VDDPA (0x03FB)	PN76_LPCD_SETTINGS->bTxLdoVddpa	0x03FB	1019	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPCD_CHECK_PERIOD (0x03FC)	PN76_LPCD_SETTINGS->wCheckPeriod	0x03FC	1020	2	E_PN76_EEPROM_SECURE_LIB_CONFIG

9.14.3.8.2 LPCD_AVG_SAMPLES (0x03DE)

Number of samples used for averaging

Table 367. LPCD_AVG_SAMPLES (0x03DE)

Function	bits	Values	Description
Random UID enable	[7:3]		Reserved

Table 367. LPCD_AVG_SAMPLES (0x03DE)*...continued*

Function	bits	Values	Description
LPCD_AVG_SAMPLES	[2:0]		Defines how many samples of the I and Q values are used for the averaging. Average samples in power of 2.
		0x00	1 sample
		0x01	2 samples
		0x02	4 samples
		0x03	8 samples
		0x04	16 samples
		0x05	32 samples
		0x06	64 samples
		0x07	RFU

9.14.3.8.3 LPCD_RSSI_TARGET (0x03E0)

Table 368. LPCD_RSSI_TARGET (0x03E0)

Function	bits	Values	Description
LPCD_RSSI_TARGET	[15:0]		Value to be set in register DGRM_RSSI_REG_ DGRM_RSSI_TARGET. Typically the same values from the Type A106 LOAD_RF_CONFIGURATION API (DGRM_RSSI register) are used.

9.14.3.8.4 LPCD_RSSI_HYST (0x03E2)

Table 369. LPCD_RSSI_HYST (0x03E2)

Function	bits	Values	Description
LPCD_RSSI_HYST	[7:0]		Value to be set in CLIF_DGRM_RSSI_REG_ DGRM_RSSI_HYST Typically the same values from the Type A106 LOAD_RF_CONFIGURATION API (DGRM_RSSI register) are used.

9.14.3.8.5 LPCD_CONFIG (0x03E3)

Number of samples used for averaging

Table 370. LPCD_CONFIG (0x03E3)

Function	bits	Values	Description
RFU	[15:6]		Reserved
LPCD_CONFIG	[5]	0x00	Disables feature Immediate RF OFF before TXLDO shutdown to save power
		0x01	Enables feature Immediate RF OFF before TXLDO shutdown to save power. For this feature, Enable VDDPA fast discharge must be enabled.
	[4]	0x00	Disables VDDPA fast discharge.
		0x01	Enable VDDPA fast discharge.

Table 370. LPCD_CONFIG (0x03E3)*...continued*

Function	bits	Values	Description
	[3]	0x00	Enable single driver
		0x01	Enable both drivers
	[2:0]		Acquisition channels
		0x00-0x01	RFU
		0x02	Magnitude
		0x03	I and Q
		0x04	M, I and Q
		0x05-0x07	RFU

9.14.3.8.6 LPCD_THRESHOLD (0x03E6)

LPCD threshold type depends upon the LPCD_CONFIG[2:0] value in Table 370

For 'I and Q' mode: 1st threshold = I ch; 2nd threshold = Q ch.

Table 371. LPCD_THRESHOLD (0x03E6)

Function	bits	Values	Description
LPCD Q channel threshold	[31:16]		ADC LSB granularity of threshold depends of avg_samples_meas value:
		0x00	unit 1
		0x01	unit 1/2
		0x02	unit 1/4
		0x03	unit 1/8
		0x04	unit 1/16
		0x05	unit 1/32
		Other	Reserved
LPCD I channel threshold	[15:0]		ADC LSB granularity of threshold depends of avg_samples_meas value:
		0x00	unit 1
		0x01	unit 1/2
		0x02	unit 1/4
		0x03	unit 1/8
		0x04	unit 1/16
		0x05	unit 1/32
		Other	Reserved

Note: If the difference between the measured value and the reference is greater than the threshold on either channels, then a card is detected.

9.14.3.8.7 LPCD_WAIT_RX_SETTLE (0x03F7)

Delay between FieldOn and starting ADC data averaging.

Table 372. LPCD_WAIT_RX_SETTLE (0x03F7)

Function	bits	Values	Description
LPCD DELAY	[15:0]		Delay between FieldOn and starting ADC data averaging. Value in us, default 14h = 20us

9.14.3.8.8 LPCD_VDDPA (0x03FB)

VDDPA voltage when DCDC (internal or external) or external power source is used to feed TXLDO.

Table 373. LPCD_VDDPA (0x03FB)

Function	bits	Values	Description
VDDPA voltage LPCD DELAY	[7:0]		TXLDO output voltage.
		0x00-0x2A	resultant voltage would be: 1V50 + this value * 0.10) 0x00: 1V50 0x01: 1V60 0x02: 1V70 0x03: 1V80 0x04: 1V90 0x05: 2V00 0x06: 2V10 0x07: 2V20 0x08: 2V30 0x09: 2V40 0x0A: 2V50 0x0B: 2V60 0x0C: 2V70 0x0D: 2V80 0x0E: 2V90 0x0F: 3V00 0X10: 3V10 0x11: 3V20 0x12: 3V30 0x13: 3V40 0x14: 3V50 0x15: 3V60 0x16: 3V70 0x17: 3V80 0x18: 3V90 0x19: 4V00 0x1A: 4V10 0x1B: 4V20 0x1C: 4V30 0x1D: 4V40 0x1E: 4V50 0x1F: 4V60 0x20: 4V70 0x21: 4V80 0x22: 4V90 0x23: 5V00

Table 373. LPCD_VDDPA (0x03FB)*...continued*

Function	bits	Values	Description
			0x24: 5V10 0x25: 5V20 0x26: 5V30 0x27: 5V40 0x28: 5V50 0x29: 5V60 0x2A: 5V70
		Others	Reserved

9.14.3.8.9 LPCD_CHECK_PERIOD (0x03FC)

Timer value defining standby duration before calibration and reference measurement in LPCD single mode(Mode 4)

Table 374. LPCD_CHECK_PERIOD (0x03FC)

Function	bits	Values	Description
LPCD DELAY	[15:0]		2.63ms resolution, default 0x26 = ~100ms

9.14.3.9 CORRECTION_ENTRY_TABLE TX wave shaping for proprietary correction configuration

Table 375. CORRECTION_ENTRY_TABLE

Entry	Address	Function	bit	Values	Description
CORRECTION_ENTRY 0 for 1V5	0x042B	PROP_CORRECTION_ENTRY	[15:8]		Correction applied for ASK10 Range would be -128 to +127.
			[7:0]		Correction applied for ASK100. Range would be -128 to +127.
CORRECTION_ENTRY1 for 1.60V	0x042D	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY2 for 1.70V	0x042F	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY3 for 1.80V	0x0431	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY4 for 1.90V	0x0433	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY5 for 2.00V	0x0435	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY6 for 2.10V	0x0437	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY7 for 2.20V	0x0439	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY8 for 2.30V	0x043B	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY9 for 2.40V	0x043D	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			

Table 375. CORRECTION_ENTRY_TABLE*...continued*

Entry	Address	Function	bit	Values	Description
CORRECTION_ENTRY10 for 2.50V	0x043F	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY11 for 2.60V	0x0441	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY12 for 2.70V	0x0443	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY13 for 2.80V	0x0445	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY14 for 2.90V	0x0447	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY15 for 3.00V	0x0449	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY16 for 3.10V	0x044B	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY17 for 3.20V	0x044D	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY18 for 3.30V	0x044F	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY19 for 3.40V	0x0451	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY20 for 3.50V	0x0453	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY21 for 3.60V	0x0455	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY22 for 3.70V	0x0457	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY23 for 3.80V	0x0459	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY24 for 3.90V	0x045B	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY25 for 4.00V	0x045D	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY26 for 4.10V	0x045F	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY27 for 4.20V	0x0461	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY28 for 4.30V	0x0463	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY29 for 4.40V	0x0465	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY30 for 4.50V	0x0467	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY31 for 4.60V	0x0469	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			

Table 375. CORRECTION_ENTRY_TABLE*...continued*

Entry	Address	Function	bit	Values	Description
CORRECTION_ENTRY32 for 4.70V	0x046B	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY33 for 4.80V	0x046D	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY34 for 4.90V	0x046F	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY35 for 5.00V	0x0471	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY36 for 5.10V	0x0473	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY37 for 5.20V	0x0475	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY38 for 5.30V	0x0477	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY39 for 5.40V	0x0479	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY40 for 5.50V	0x047B	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY41 for 5.60V	0x047D	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			
CORRECTION_ENTRY42 for 5.70V	0x047F	Byte and bit-fields description, refer to CORRECTION_ENTRY_0			

9.14.3.10 TX_SHAPING_RTRANS_FTRANS_TABLE TX wave shaping for proprietary correction configuration for rising edge and falling edges. (0x0481)

9.14.3.10.1 TX_SHAPING_RTRANS_FTRANS_1 (0x0481)

The rising Transition register values loaded when Proprietary TX Shaping configuration is set in the RM_TECHNO_TX_SHAPING table to use proprietary TX shaping.

Table 376. TX_SHAPING_RTRANS_FTRANS_1 (0x0481)

Function	Address	Bytes	Bits	Description
RTRANS0	0x0481	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS1	0x0485	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS2	0x0489	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS3	0x048D	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
FTRANS0	0x0491	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS1	0x0495	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge

Table 376. TX_SHAPING_RTRANS_FTRANS_1 (0x0481)*...continued*

Function	Address	Bytes	Bits	Description
FTRANS2	0x0499	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS3	0x049D	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge

9.14.3.10.2 TX_SHAPING_RTRANS_FTRANS_2 (0x4A1)

The rising Transition register values loaded when Proprietary TX Shaping configuration is set in the RM_TECHNO_TX_SHAPING table to use proprietary TX shaping.

Table 377. TX_SHAPING_RTRANS_FTRANS_2 (0x4A1)

Function	Address	Bytes	Bits	Description
RTRANS0	0x4A1	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS1	0x04A5	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS2	0x04A9	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS3	0x04AD	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
FTRANS0	0x04B1	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS1	0x04B5	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS2	0x04B9	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS3	0x04BD	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge

9.14.3.10.3 TX_SHAPING_RTRANS_FTRANS_3 (0x04C1)

The rising Transition register values loaded when Proprietary TX Shaping configuration is set in the RM_TECHNO_TX_SHAPING table to use proprietary TX shaping.

Table 378. TX_SHAPING_RTRANS_FTRANS_3 (0x04C1)

Function	Address	Bytes	Bits	Description
RTRANS0	0x04C1	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS1	0x04C5	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS2	0x04C9	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS3	0x04CD	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
FTRANS0	0x04D1	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge

Table 378. TX_SHAPING_RTRANS_FTRANS_3 (0x04C1)*...continued*

Function	Address	Bytes	Bits	Description
FTRANS1	0x04D5	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS2	0x04D9	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS3	0x04DD	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge

9.14.3.10.4 TX_SHAPING_RTRANS_FTRANS_1 (0x04E1)

The rising Transition register values loaded when Proprietary TX Shaping configuration is set in the RM_TECHNO_TX_SHAPING table to use proprietary TX shaping.

Table 379. TX_SHAPING_RTRANS_FTRANS_1 (0x04E1)

Function	Address	Bytes	Bits	Description
RTRANS0	0x04E1	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS1	0x04E5	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS2	0x04E9	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS3	0x04ED	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
FTRANS0	0x04F1	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS1	0x04F5	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS2	0x04F9	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS3	0x04FD	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge

9.14.3.11 TX driver NOV (non-overlap) settings configuration.

9.14.3.11.1 EEPROM_TX_DRIVER_NOV_LIST

List of NOV configuration parameters

Table 380. List of NOV configuration parameters

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
NOV_CFG_CAL (0x0501)	PN76_TX_DRIVER_NOV->Cfg NovCal	0x0501	1281	1	EEPROM_SECURE_LIB_ CONFIG
NOV_CAL_VAL1 (0x0502)	PN76_TX_DRIVER_NOV- >VddpaCalVal1	0x0502	1282	1	EEPROM_SECURE_LIB_ CONFIG
NOV_CAL_VAL2 (0x0503)	PN76_TX_DRIVER_NOV- >VddpaCalVal2	0x0503	1283	1	EEPROM_SECURE_LIB_ CONFIG

Table 380. List of NOV configuration parameters*...continued*

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
NOV_CAL_THRESHOLD (0x0504)	PN76_TX_DRIVER_NOV->Cfg Threshold	0x0504	1284	1	EEPROM_SECURE_LIB_CONFIG
NOV_CAL_OFFSET1 (0x0505)	PN76_TX_DRIVER_NOV->UserOffsets1	0x0505	1285	4	EEPROM_SECURE_LIB_CONFIG
NOV_CAL_OFFSET2 (0x0509)	PN76_TX_DRIVER_NOV->UserOffsets2	0x0509	1289	4	EEPROM_SECURE_LIB_CONFIG

9.14.3.11.2 NOV_CFG_CAL (0x0501)

NOV calibration type

Table 381. NOV_CFG_CAL (0x0501)

Function	bits	Values	Description
RFU	[7:2]		Reserved
NOV_CALIBRATION_TYPE	[1:0]	0x00	No calibration performed, needs to be updated to 01 or 10 before the first RF on of the chip is performed.
		0x01	Enable FW calibration after every cold boot.
		0x02	Use calibration value coming from EEPROM NOV_CAL_VAL1, NOV_CAL_VAL2 (Default)
		0x03	RFU

9.14.3.11.3 NOV_CAL_VAL1 (0x0502)

Table 382. NOV_CAL_VAL1 (0x0502)

Function	bits	Values	Description
VDDPACALVAL1	[7:0]	0x03	(1.8 V)
		0x0D	(2.8V)

9.14.3.11.4 NOV_CAL_VAL2 (0x0503)

Table 383. NOV_CAL_VAL2 (0x0503)

Function	bits	Values	Description
VDDPACALVAL2	[7:0]	0x15	(3.6 V)
		0x24	(5.1V)

9.14.3.11.5 NOV_CAL_THRESHOLD (0x0504)

Table 384. NOV_CAL_THRESHOLD (0x0504)

Function	bits	Values	Description
VDDPACALVAL2	[7:0]	0x08	(2.3 V)
		0x16	(3.7V)

9.14.3.11.6 NOV_CAL_OFFSET1 (0x0505)

Table 385. NOV_CAL_OFFSET1 (0x0505)

Function	bits	Values	Description
RFU	[31:29]		Reserved
VDDAPA MIN	[28:24]		Group#1 (VDDPA min to CfgThreshold), offset_2l(1)
	[23:21]		Reserved
	[20:16]		Group#1 (VDDPA min to CfgThreshold), offset_2l(0)
	[15:13]		Reserved
	[12:08]		Group#1 (VDDPA min to CfgThreshold), offset_3l_p2
	[07:05]		Reserved
	[04:00]		Group#1 (VDDPA min to CfgThreshold), offset_3l

9.14.3.11.7 NOV_CAL_OFFSET2 (0x0509)

Table 386. NOV_CAL_OFFSET2 (0x0509)

Function	bits	Values	Description
RFU	[31:29]		Reserved
VDDAPA MAX	[28:24]		Group#1 (VDDPA max to CfgThreshold), offset_2l(1)
	[23:21]		Reserved
	[20:16]		Group#1 (VDDPA max to CfgThreshold), offset_2l(0)
	[15:13]		Reserved
	[12:08]		Group#1 (VDDPA max to CfgThreshold), offset_3l_p2
	[07:05]		Reserved
	[04:00]		Group#1 (VDDPA max to CfgThreshold), offset_3l

9.14.3.12 Active reader mode TX wave shaping configuration

This section provides the active reader mode TX wave shaping configuration settings.

9.14.3.12.1 RESIDUAL_AMPL_LEVEL_ACTIVE_A106 (0X050E)

Table 387. RESIDUAL_AMPL_LEVEL_ACTIVE_A106 (0X050E)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.12.2 EDGE_TYPE_ACTIVE_A106 (0X050F)

Table 388. EDGE_TYPE_ACTIVE_A106 (0X050F)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.12.3 EDGE_STYLE_ACTIVE_A106 (0X0510)

Table 389. EDGE_STYLE_ACTIVE_A106 (0X0510)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	

Table 389. EDGE_STYLE_ACTIVE_A106 (0X0510)*...continued*

Function	bit	Values	Description
			For Firmware based shaping (bEdgeType_A106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ A106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_ A106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.12.4 EDGE_LENGTH_ACTIVE_A106 (0X0511)

Table 390. EDGE_LENGTH_ACTIVE_A106 (0X0511)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.12.5 RESIDUAL_AMPL_LEVEL_ACTIVE_F212 (0X0512)

Table 391. RESIDUAL_AMPL_LEVEL_ACTIVE_F212 (0X0512)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.12.6 EDGE_TYPE_ACTIVE_F212 (0X0513)

Table 392. EDGE_TYPE_ACTIVE_F212 (0X0513)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels

Table 392. EDGE_TYPE_ACTIVE_F212 (0X0513)*...continued*

Function	bit	Values	Description
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.12.7 EDGE_STYLE_ACTIVE_F212 (0X0514)

Table 393. EDGE_STYLE_ACTIVE_F212 (0X0514)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_F212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	

Table 393. EDGE_STYLE_ACTIVE_F212 (0X0514)*...continued*

Function	bit	Values	Description
			For Firmware based shaping (bEdgeType_F212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.12.8 EDGE_LENGTH_ACTIVE_F212 (0X0515)

Table 394. EDGE_LENGTH_ACTIVE_F212 (0X0515)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.12.9 RESIDUAL_AMPL_LEVEL_ACTIVE_F424 (0X0516)

Table 395. RESIDUAL_AMPL_LEVEL_ACTIVE_F424 (0X0516)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0% carrier
		0xFF	100% carrier

9.14.3.12.10 EDGE_TYPE_ACTIVE_F424 (0X0517)

Table 396. EDGE_TYPE_ACTIVE_F424 (0X0517)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction

Table 396. EDGE_TYPE_ACTIVE_F424 (0X0517)*...continued*

Function	bit	Values	Description
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

9.14.3.12.11 EDGE_STYLE_ACTIVE_F424 (0X0518)

Table 397. EDGE_STYLE_ACTIVE_F424 (0X0518)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_F424 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F424 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_F424 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F424 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.3.12.12 EDGE_LENGTH_ACTIVE_F424 (0X0519)

Table 398. EDGE_LENGTH_ACTIVE_F424 (0X0519)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.3.13 Settings related to NFCLD and RFLD. For Card Mode Dynamic LMA settings(0x011D)

9.14.3.13.1 EEPROM_MEASURED_LMA_RSSI_LIST

List of Settings related to NFCLD and RFLD. For Card Mode Dynamic LMA settings.

Table 399. List of Settings related to NFCLD and RFLD. For Card Mode Dynamic LMA settings.

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
LMA_RSSI_INTERPOLATED_RSSI (0x0530)	PN76_MEASURED_LMA_RSSI->wMeasuredInterpolatedRSSI	0x0530	1328	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
LMA_RSSI_FIELD_STRENGTH (0x0532)	PN76_MEASURED_LMA_RSSI->bMeasuredFieldStrength	0x0532	1330	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

9.14.3.13.2 LMA_RSSI_INTERPOLATED_RSSI (0x0530)

Table 400. LMA_RSSI_INTERPOLATED_RSSI (0x0530)

Function	bits	Values	Description
LMA_RSSI_INTERPOLATED_RSSI	[15:0]		Measured Interpolated RSSI (16 bit, in little-endian format). Each count indicates a value of 1/2048 mV.

9.14.3.13.3 LMA_RSSI_FIELD_STRENGTH (0x0532)

Table 401. LMA_RSSI_FIELD_STRENGTH (0x0532)

Function	bits	Values	Description
LMA_RSSI_FIELD_STRENGTH	[7:0]		Field strength (8 bits, 1/16 A/m LSB) used for b MeasuredLMA and wMeasuredInterpolatedRSSI.

9.14.3.14 Global TX_SHAPING configuration

This section provides configuration global TX waveform shaping settings.

9.14.3.14.1 EEPROM_RM_GLOBAL_TX_SHAPING_LIST

List of Settings related TX_SHAPING configuration.

Table 402. List of Settings related TX_SHAPING configuration.

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
TX_SHAPING_CONIFG (0x058C)	PN76_RM_GLOBAL_TX_SHAPING->bConfig	0x058C	1420	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TX_INV_RM (0x058D)	PN76_RM_GLOBAL_TX_SHAPING->bTX_INV_RM	0x058D	1421	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TX_CLK_MODE_1 (0x058E)	PN76_RM_GLOBAL_TX_SHAPING->bCLK_MODE_1	0x058E	1422	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TX_CLK_MODE_2 (0x058F)	PN76_RM_GLOBAL_TX_SHAPING->bCLK_MODE_2	0x058F	1423	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
GSN_MOD_RM (0x0590)	PN76_RM_GLOBAL_TX_SHAPING->bGSN_MOD_RM	0x0590	1424	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
GSN_CW_RM (0x0591)	PN76_RM_GLOBAL_TX_SHAPING->bGSN_CW_RM	0x0591	1425	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
GSP_RM (0x0592)	PN76_RM_GLOBAL_TX_SHAPING->bGSP_RM	0x0592	1426	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TX_FRCZERO_THR (0x0593)	PN76_RM_GLOBAL_TX_SHAPING->bTX_FRCZERO_THR	0x0593	1427	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
SIGNAL_SCALING_CONFIG (0x0594)	PN76_RM_GLOBAL_TX_SHAPING->bSignalScaling Config	0x0594	1428	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TX_PH_SHIFT_DIV10 (0x0595)	PN76_RM_GLOBAL_TX_SHAPING->bTX_PH_SHIFT_DIV10	0x0595	1429	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TX_PH_SHIFT_MOD10 (0x0596)	PN76_RM_GLOBAL_TX_SHAPING->bTX_PH_SHIFT_MOD10	0x0596	1430	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

9.14.3.14.2 TX_SHAPING_CONIFG (0x058C)

PWM scheme for RM

Table 403. TX_SHAPING_CONIFG (0x058C)

Function	bits	Values	Description
RFU	[7:1]		Reserved
PWM scheme for RM	[0]	0x00	defining 3-levels for drivers TX1/2 - required for balanced antenna (default)
		0x01	defining 2-levels for drivers TX1/2 - required for single ended antenna

9.14.3.14.3 TX_INV_RM (0x058D)

Transmitter configuration

Table 404. TX_INV_RM (0x058D)

Function	bits	Values	Description
RFU	[7:6]		Reserved
TX1 output configuration	[5]	0x00	TX1 non-inverted output (output zero remains zero)
		0x01	TX1 inverted output (common mode operation, output zero becomes one)
TX2 output configuration	[4]	0x00	TX2 non-inverted output (output zero remains zero)
		0x01	TX2 inverted output (common mode operation, output zero becomes one)
RFU	[3:2]		Reserved
TX1 phase shift configuration	[1]	0x00	TX1 no phase shift, 0 deg
		0x01	TX1 phase shifted by 180 deg
TX2 phase shift configuration	[0]	0x00	TX2 no phase shift, 0 deg
		0x01	TX2 phase shifted by 180 deg

9.14.3.14.4 TX_CLK_MODE_1 (0x058E)

Transmitter configuration

Table 405. TX_CLK_MODE_1 (0x058E)

Function	bits	Values	Description
RFU	[7]		Reserved
CLK_MODE_CW_RM	[6:4]		CLK_MODE_CW_RM
RFU	[3]		Reserved
CLK_MODE_MOD_RM	[2:0]		CLK_MODE_MOD_RM

9.14.3.14.5 TX_CLK_MODE_2 (0x058F)

CLK_MODE configuration

Table 406. TX_CLK_MODE_2 (0x058F)

Function	bits	Values	Description
RFU	[7]		Reserved
CLK_MODE_DEFAULT	[6:4]		CLK_MODE_DEFAULT
RFU	[3]		Reserved
CLK_MODE_TRANS_RM	[2:0]		CLK_MODE_TRANS_RM

9.14.3.14.6 GSN_MOD_RM (0x0590)

GSN_MOD_RM configuration

Table 407. GSN_MOD_RM (0x0590)

Function	bits	Values	Description
RFU	[7:5]		Reserved
GSN_MOD_RM	[4:0]		GSN_MOD_RM

9.14.3.14.7 GSN_CW_RM (0x0591)

GSN_CW_RM configuration

Table 408. GSN_CW_RM (0x0591)

Function	bits	Values	Description
RFU	[7:5]		Reserved
GSN_CW_RM	[4:0]		GSN_CW_RM

9.14.3.14.8 GSP_RM (0x0592)

GSP_RM configuration

Table 409. GSP_RM (0x0592)

Function	bits	Values	Description
RFU	[7:5]		Reserved
GSP_RM	[4:0]		GSP_RM

9.14.3.14.9 TX_FRCZERO_THR (0x0593)

CLIF_SS_TX_CFG_REG configuration

Table 410. TX_FRCZERO_THR (0x0593)

Function	bits	Values	Description
RFU	[7]		Reserved
CLIF_SS_TX_CFG_REG	[6:0]		Defining CLIF_SS_TX_CFG_REG[12:6]

9.14.3.14.10 SIGNAL_SCALING_CONFIG (0x0594)

Global TX_SS_TARGET_SCALE configuration

Table 411. SIGNAL_SCALING_CONFIG (0x0594)

Function	bits	Values	Description
Global TX_SS_TARGET_SCALE	[7:0]		Global TX_SS_TARGET_SCALE configuration for debugging purposes

9.14.3.14.11 TX_PH_SHIFT_DIV10 (0x0595)

Global TX_SS_TARGET_SCALE configuration

Table 412. TX_PH_SHIFT_DIV10 (0x0595)

Function	bits	Values	Description
RFU	[7:5]		Reserved
CLIF_ANACTRL_TX_CONFIG_REG	[4:0]		CLIF_ANACTRL_TX_CONFIG_REG.TX_PH_SHIFT_DIV10

9.14.3.14.12 TX_PH_SHIFT_MOD10 (0x0596)

Global CLIF_ANACTRL_TX_CONFIG_REG.TX_PH_SHIFT_MOD10 configuration

Table 413. TX_PH_SHIFT_MOD10 (0x0596)

Function	bits	Values	Description
RFU	[7:4]		Reserved
CLIF_ANACTRL_TX_CONFIG_REG.TX_PH_SHIFT_MOD10	[3:0]		CLIF_ANACTRL_TX_CONFIG_REG.TX_PH_SHIFT_MOD10

9.14.3.15 Settings for encryption/decryption of keys storage for Symmetric and Asymmetric private keys

This section provides the derivation messages for different operations on application keys.

9.14.3.15.1 APP_ENCRY_DECRY_KEY_DERIV_MSG (0x0550)

Table 414. APP_ENCRY_DECRY_KEY_DERIV_MSG (0x0550)

Function	bytes	Values	Description
abCustEncrDecrDerivMsg	[23:0]		Derivation message for encryption/decryption for Master Keys for interfacing with Mbed.

9.14.3.15.2 APP_ENCRY_KEY_DERIV_MSG_ASYMM_KEY (0x568)

Table 415. APP_ENCRY_KEY_DERIV_MSG_ASYMM_KEY (0x568)

Function	bytes	Values	Description
adwDerivMsgEncDecKeyForAsym	[23:0]		Derivation message for encrypting/decrypting the storing/retrieving of Asymm private key.

9.14.3.16 RFLD and NFCLD settings

9.14.3.16.1 EEPROM_RFLD_NFCLD_SETTINGS_LIST

List of settings related to RFLD and NFCLD

Table 416. List of settings related to RFLD and NFCLD

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
NFCLD_ONOFF_THRESHOLD (0x0597)	PN76_EXT_RF_DETECTION_HW->dwNFCLD_OnOff Threshold	0x0597	1431	4	E_PN76_EEPROM_SECURE_LIB_CONFIG
NFCLD_ONOFF_MASKTIME (0x059B)	PN76_EXT_RF_DETECTION_HW->dwNFCLD_OnOffMask Time	0x059B	1435	4	E_PN76_EEPROM_SECURE_LIB_CONFIG
NFCLD_ON_THRESHOLD (0x05BF)	PN76_EXT_RF_DETECT_INT_INPUT->wNFCLD_OnThreshold	0x05BF	1471	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
NFCLD_OFF_THRESHOLD (0x05C1)	PN76_EXT_RF_DETECT_INT_INPUT->wNFCLD_OffThreshold	0x05C1	1473	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPDET_ON_THRESHOLD (0x05C3)	PN76_EXT_RF_DETECT_INT_INPUT->wLPDET_OnThreshold	0x05C3	1475	2	E_PN76_EEPROM_SECURE_LIB_CONFIG

Table 416. List of settings related to RFLD and NFCLD*...continued*

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
NFCLD_RFLD_VALID (0x05C5)	PN76_EXT_RF_DETECT_INT_INPUT->wNFCLD_RFLD_Valid_Bit	0x05C5	1477	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

9.14.3.16.2 NFCLD_ONOFF_THRESHOLD (0x0597)

NFCLD_ON_OFF_THRESHOLD

Note: Value can be overwritten if writing tags A098, A09E or A01F (depends on feature controls: NFCLD interpolation, APC/RX enhancements).

Table 417. NFCLD_ONOFF_THRESHOLD (0x0597)

Function	bits	Values	Description
NFCLD_ON_OFF_THRESHOLD	[31:16]		RF Field OFF Threshold
	[15:0]		RF Field ON Threshold

9.14.3.16.3 NFCLD_ONOFF_MASKTIME (0x059B)

NFCLD_ON_OFF_MASKTIME

Table 418. NFCLD_ONOFF_MASKTIME (0x059B)

Function	bits	Values	Description
RFU	[31:20]		Reserved.
NFCLD_ON_OFF_MASKTIME	[19:15]		Masking time OFF = 10us
	[14:0]		Masking time ON = 300us

9.14.3.16.4 NFCLD_ON_THRESHOLD (0x05BF)

Table 419. NFCLD_ON_THRESHOLD (0x05BF)

Function	bits	Values	Description
RF Field ON Threshold	[15:0]		RF Field ON Threshold; Code resolution: (1/2048) Vpp @ Vrrsi.

9.14.3.16.5 NFCLD_OFF_THRESHOLD (0x05C1)

Table 420. NFCLD_OFF_THRESHOLD (0x05C1)

Function	bits	Values	Description
RF Field OFF Threshold	[15:0]		RF Field ON Threshold; Code resolution: (1/2048) Vpp @ Vrrsi.

9.14.3.16.6 LPDET_ON_THRESHOLD (0x05C3)

Table 421. LPDET_ON_THRESHOLD (0x05C3)

Function	bits	Values	Description
LPDET ON Threshold	[15:0]		Code Resolution (1/2048)Vpp at Vrssi 14 = 10mVpp.

Note:value can be overwritten if writing tags A098 or A09E (depends on feature controls: APC/RX enhancements)

9.14.3.16.7 NFCLD_RFLD_VALID (0x05C5)

Table 422. NFCLD_RFLD_VALID (0x05C5)

Function	bits	Values	Description
RFU	[7:1]		Resreved.
NFCLD_RFLD_VALID	[0:0]		If this bit is set to 1 then the NFCLD Threshold and RFLD Threshold is a valid data and calibration wont be done gain till this bit is cleared and POR is issued.

9.14.3.17 ULPCD related settings

This section provides the ULPCD related configuration settings

9.14.3.17.1 EEPROM_ULPCD_LIST

List of ULPCD related configuration settings

Table 423. List of ULPCD related configuration settings

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
ULPCD_VDDPA_CTRL (0638)	PN76_ULPCD_CONFIG->Vddpa_Ctrl	0x0638	1592	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
ULPCD_AGC_HFATT_CTRL (063A)	PN76_ULPCD_CONFIG->Agc_Hfatt_Ctrl	0x063A	1594	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
ULPCD_TIMING_CTRL (063B)	PN76_ULPCD_CONFIG->Timing_Ctrl	0x063B	1595	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
ULPCD_VOLTAGE_CTRL (063D)	PN76_ULPCD_CONFIG->Voltage_Ctrl	0x063D	1597	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
ULPCD_RSSI_GUARD_TIME (0640)	PN76_ULPCD_SETTINGS->brssi_nsp	0x0640	1600	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
ULPCD_RSSI_SAMPLE_CFG (0641)	PN76_ULPCD_SETTINGS->brssi_no_samples	0x0641	1601	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
ULPCD_THRESH_LVL (0642)	PN76_ULPCD_SETTINGS->bthresh_lvl	0x0642	1602	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
ULPCD_GPIO3 (0643)	PN76_ULPCD_SETTINGS->bpolarity	0x0643	1603	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

9.14.3.17.2 ULPCD_VDDPA_CTRL (0638)

VDDPA control during ULPCD

Table 424. ULPCD_VDDPA_CTRL (0638)

Function	bits	Values	Description
RFU	[15:9]		Reserved

Table 424. ULPCD_VDDPA_CTRL (0638)*...continued*

Function	bits	Values	Description
VDDPA control	[8:3]		TXLDO output voltage during ULPCD polling. Value 0x00 --> 1V50, 0x01 --> 1V60.. with 0.10 voltage increment till value of 0x2A --> 5V70.
RFU	[2:0]		Reserved

9.14.3.17.3 ULPCD_AGC_HFATT_CTRL (063A)

VDDPA control during ULPCD

Table 425. ULPCD_AGC_HFATT_CTRL (063A)

Function	bits	Values	Description
AGC_HFATT_CTRL	[7:0]	—	The value to be used during ULPCD. This value must be set to a value read from CLIF_RXCTRL_STATUS register during ULPCD calibration process.

9.14.3.17.4 ULPCD_TIMING_CTRL (063B)

ULPCD timing control

Table 426. ULPCD_TIMING_CTRL (063B)

Function	bits	Values	Description
RFON_GUARD_TIME	[7:4]		RFON guard time: (RFON_GUARD_TIME + 2) * LFO-Freq (380 kHz) Guard time: Time between RF-ON and first sampling of data
RFU	[3:0]		Reserved

9.14.3.17.5 ULPCD_VOLTAGE_CTRL (063D)

ULPCD voltage control

Table 427. ULPCD_VOLTAGE_CTRL (063D)

Function	bits	Values	Description
RFU	[7:2]		Reserved
TX_SUPPLY by VUP_TX	[1]	0x00	VUP externally supplied (2.8 V to 6.0 V)
		0x01	VUP supplied by PN7642 itself (pin VUP_TX connected to VBAT/VBATPWR)
RFU	[0]		Reserved

9.14.3.17.6 ULPCD_RSSI_GUARD_TIME (0640)

Number of RSSI Samples which are internally averaged.

Table 428. ULPCD_RSSI_GUARD_TIME (0640)

Function	bits	Values	Description
RFU	[7]		Reserved

Table 428. ULPCD_RSSI_GUARD_TIME (0640)*...continued*

Function	bits	Values	Description
ULPCD RSSI sampling guard time	[6:0]		This is the time between consecutive RSSI samples.

Note: *Range - 0 - 127 micro seconds The GPADC RSSI acquisition time can be calculated with T= (ROUNDS * (brssi_nsp + 30 + 3.5) + 11.5) * Tclkgpadc*

9.14.3.17.7 ULPCD_RSSI_SAMPLE_CFG (0641)

Number of RSSI Samples which are internally averaged

Table 429. ULPCD_RSSI_SAMPLE_CFG (0641)

Function	bits	Values	Description
RFU	[7:2]		Reserved
number of RSSI Samples	[1:0]	0x00	4 rounds
		0x01	8 rounds
		0x02	16 rounds
		0x03	32 rounds

9.14.3.17.8 ULPCD_THRESH_LVL (0642)

RSSI Threshold level.

Note: If the difference between the measured RSSI value and the reference (which is derived during calibration) is greater than the threshold, then a card is detected.

Table 430. ULPCD_THRESH_LVL (0642)

Function	bits	Values	Description
RFU	[7:5]		Reserved
RSSI Threshold level	[4:0]		0 - 31

9.14.3.17.9 ULPCD_GPIO3 (0643)

GPIO3 abort polarity configuration

Note: If PN7642 is using the ULPCD, GPIO3 cannot be used for any other purpose than aborting the ULPCD.

Table 431. ULPCD_GPIO3 (0643)

Function	bits	Values	Description
RFU	[7:1]		Reserved
RSSI Threshold level	[0]	0x00	low-level aborts ULPCD
		0x01	high-level aborts ULPCD

9.14.3.18 TEMPERATURE related settings

This section provides the configuration of Temperature warning settings.

9.14.3.18.1 EEPROM_TEMP_WARNING_LIST

List of settings for Temperature related cut-offs and notifications

Table 432. List of settings for Temperature related cut-offs and notifications

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
TEMP_WARNING (0x0648)	PN76_USER_SMU_CONFIG->bTempWarning	0x0648	1608	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
ENABLE_GPIO0_ON_OVERTEMP (0x0649)	PN76_USER_SMU_CONFIG->bEnableGpio0OnOverTemp	0x0649	1609	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

9.14.3.18.2 TEMP_WARNING (0x0648)

Table 433. TEMP_WARNING (0x0648)

Function	bits	Values	Description
PMU high threshold	[7:6]	0x00	Disabled
		0x01	114 degC
		0x02	125 degC
		0x03	130 degC
PMU low threshold	[5:4]	0x00	Disabled
		0x01	114 degC
		0x02	125 degC
		0x03	130 degC
CLIF high threshold	[3:2]	0x00	Disabled
		0x01	114 degC
		0x02	125 degC
		0x03	130 degC
CLIF low threshold	[1:0]	0x00	Disabled
		0x01	114 degC
		0x02	125 degC
		0x03	130 degC

9.14.3.18.3 ENABLE_GPIO0_ON_OVERTEMP (0x0649)

Enable over temperature indication through GPIO0

Table 434. ENABLE_GPIO0_ON_OVERTEMP (0x0649)

Function	bits	Values	Description
RFU	[7:1]		Reserved
Gpio0 temp indication	[0]	0x00	temperature event indication through GPIO0 is disabled.
		0x01	temperature event indication through GPIO0 is enabled.

10 Limiting values

Table 435. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(VUP\_TX)}$	supply voltage on pin VUP_TX	-	-0.3	6.3	V
$V_{DD(VBAT)}$	supply voltage on pin VBAT	-	-0.3	5.8	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO	on pin VDDIO, power supply for host interface and GPIOs	-0.3	3.8	V
$V_{DD(GPIO\_x)}$	input voltage on pin used as GPIO	-	-0.3	3.8	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA	maximum limiting values for $I_{DD(VDDPA)}$ and $T_{j(max)}$ not violated	-	6.0	V
$V_{i(RXP)}$	input voltage on pin RXP	-	-0.3	+ 2.0	V
$V_{i(RXN)}$	input voltage on pin RXN	-	-0.3	+ 2.0	V
V_{ESD}	electrostatic discharge voltage	human body model (HBM)[1]	-2000	2000	V
		charge device model (CDM)[2]	-500	+500	V
$T_{j(max)}$	junction temperature	-	-	125	°C
T_{stg}	storage temperature	no supply voltage applied	-55	+150	°C

[1] According to ANSI/ESDA/JEDEC JS-001
[2] According to ANSI/ESDA/JEDEC JS-002

Stress above one or more of the limiting values may cause permanent damage to the device or limit the lifetime.

Product might not behave according to specification.

11 Characteristics

This chapter describes the electrical characteristics for the usage of the product.

Functionality according to this specification and compliancy to referred standards is guaranteed if the device is operated within the limits.

For further information, refer to the PQP (product qualification package) which summarizes the results of the characterization and qualification performed.

11.1 Thermal characteristics

Table 436. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB, transmitter output current up to 350 mA	-40	+25	+85	°C
		in still air with exposed pins soldered on a 4 layer JEDEC PCB, TX current = 120 mA @ VDDPA=3.6 V	-40	+25	+105	°C

Table 437. Thermal characteristics VFBGA64 package

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB, package VFBGA64	53	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	-	22	K/W

Table 438. Junction Temperature

Symbol	Parameter	Conditions	Min	Max	Unit
T_{j_max}	maximum junction temperature	-	-	+125	°C

Table 439. Thermal Shutdown Temperature

Symbol	Parameter	Conditions	Typ	Unit
$T_{shutdown}$	shutdown of chip due to high temperature detected by temp sensor	-	125	°C

11.2 Static characteristics

Table 440. Supply voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(VBAT\_PWR)}$	supply voltage on pin VBAT_PWR (DC-DC input pin)	DC-DC disabled	2.4	-	5.5	V
		DC-DC enabled	2.8	-	4.8	V
$V_{DD(VUP\_TX)}$	supply voltage on pin VUP_TX (TX_LDO input pin)	Remark: If DC-DC is used, its output $V_{DD(BOOST)}$ Min is limited to 3.1 V	2.4	-	6.0	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA (input of the transmitter power amplifier)	-	1.5	-	5.7	V
$V_{DD(VBAT)}$	supply voltage on pin VBAT (analog and digital supply)	VBAT >= VDDIO	2.4	-	5.5	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO (supply for host interface and GPIOs)	typical 1.8 V interface supply voltage	1.62	-	1.98	V
		typical 3.3 V interface supply voltage	2.4	-	3.6	V
$V_{I(RXP)}$	input voltage on pin RXP	-	-0.5	-	1.8	V
$V_{I(RXN)}$	input voltage on pin RXN	-	-0.5	-	1.8	V
$V_{O(LDO)}$	LDO output voltage on pin PVDD_LDO		3	3.4	3.6	V

Note: The voltage on pin VDDIO must always be smaller or equal to the voltage on pin VBAT.

Note: *$V_{O(LDO)}$ is designed to supply only the peripherals of the chip. It is not allowed to use this output to supply any other "off chip" components by this output.*

Table 441. Current consumption in active mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(VBAT)}$	system supply		-	-	20	mA
$I_{DD(VDDIO)}$		This current depends on the output current of peripherals. At no time, the sum of the maximum output currents shall exceed $I_{DD(VDDIO)}$ max	-	-	30	mA
$I_{DD(BOOST\_IN)}$	DC-DC boost supply	average input current	-	-	1.0	A
		peak input current (short peak)	-	-	1.7	A
$I_{DD(VUP\_TX)}$	input supply for transmitter LDO	-	-	-	350	mA
$I_{DD(VDDPA)}$	RF power amplifier (transmitter) current	supplied via VUP_TX (TX_LDO active)	-	-	350	mA

Table 441. Current consumption in active mode*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		supplied without DC-DC and without TXLDO active	-	-	400	mA
$I_{DD(PVDD\_OUT)}$	maximum supply current of PVDD_LDO	for pin PVDD_OUT	-	-	30	mA

Table 442. Current consumption during power-saving modes

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OFF\ Plus\ Mode\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in OFF Plus mode	25 °C ambient operating temperature	-	5	-	µA
$I_{OFF\ Plus\ ULFO\ Mode\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in OFF Plus mode, ULFO active (ULPCD during RF-OFF)	25 °C ambient operating temperature	-	5	-	µA
$I_{hard\ power\ down\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in hard Power-down mode	25 °C ambient operating temperature	-	40	105	µA
$I_{standby\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in Standby mode	25 °C ambient operating temperature	-	45	110	µA
$I_{suspend\ (VBAT)}$	supply current on pin VBAT in suspend mode	25 °C ambient operating temperature	-	2.5	-	mA
$I_{ULPCD\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in ULPCD (Ultra Low-Power Card Detection) mode	25 °C ambient operating temperature, VBAT supply voltage 3.3 V, antenna matching 50 R, 3.3 V antenna supply voltage, 3x RF-on per second	-	22	-	µA
$I_{LPCD\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in LPCD (Enhanced Low-Power Card Detection with highest sensitivity) mode, without DC-DC used	25 °C ambient operating temperature, VBAT supply voltage 3.3 V, antenna matching 50 R, 3.3 V antenna supply voltage, 3x RF-on per second	-	240	-	µA

Table 443. Overcurrent detection function

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(VUP\_TX)}$	current of overcurrent detection becoming active	-	450	550	650	mA

This is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

Table 444. VEN pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$	0.7 * $V_{DD(VDDIO)}$	-	$V_{DD(VDDIO)}$	V
V_{IL}	LOW-level input voltage		0	-	0.3 * $V_{DD(VDDIO)}$	V
I_{IH}	HIGH-level input current	$V_I = V_{DD(VBAT)}$	-	-	1	µA
I_{IL}	LOW-level input current	V_I = 0 V	-1	-	-	µA
C_i	input capacitance		-	5	-	pF
$t_{(ULPCD\_abort)}$	VEN time required to abort ULPCD		5	-	-	ms

Table 445. GPIO input / output pins (GPIO_0 - 5, SWDIO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$; 1.62 <= VDDIO <= 1.98 or 2.4 <= VDDIO <= 3.6	0.65x VDDIO	-	VDDIO+0.5	V
V_{IL}	LOW-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$; 1.62 <= VDDIO <= 1.98 or 2.4 <= VDDIO <= 3.6	- 0.5	-	0.35 × VDDIO	V
V_{OH}	HIGH-level output voltage	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	VDDIO - 0.4	-	VDDIO	V
V_{OH}	LOW-level output voltage	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	0	-	0.4	V
I_{OH}	HIGH-level output current	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-	-	3	mA
I_{OL}	LOW-level output current	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-	-	3	mA
I_{IH}	HIGH-level input current	2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-	-	1	µA
I_{IL}	LOW-level input current	2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-1	-	-	µA
R_{PU}	Weak pullup resistor		40	50	62	kΩ
R_{PD}	Weak pulldown resistor		40	50	62	kΩ
C_L	Load capacitance		-	-	20	pF
C_{IN}	Input capacitance		-	-	5	pF
I_{OSH}	Short circuit current output high	1.62 <= VDDIO <= 1.98	-	-	16	mA
I_{OSH}	Short circuit current output high	2.4 <= VDDIO <= 3.6	-	-	44	mA

Table 446. GPIO output pins (UART_RX, SPI_MISO, SPIM_MISO, IRQ, PWM 0-3, AUX_1, AUX_2, AUX_3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	VDDIO - 0.4	-	VDDIO	V
V_{OH}	LOW-level output voltage	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	0	-	0.4	V
I_{OH}	HIGH-level output current	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-	-	3	mA
I_{OL}	LOW-level output current	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-	-	3	mA
R_{PU}	Weak pullup resistor		40	50	62	kΩ
R_{PD}	Weak pulldown resistor		40	50	62	kΩ
C_L	load capacitance		-	-	20	pF

Table 447. GPIO input pins (DWL_REQ, SWD_CLK, HOST_IF_SEL0, HOST_IF_SEL1, AD1, UART_CTS, SPI_SCK, UART_RTS, SPI_NSS, I^2C_ADR_BIT_0, I^3C_ADR_BIT_0, UART_TX, I^2C_ADR_BIT_1, I^3C_ADR_BIT_1, SPI_MOSI, SPIM_MOSI, SPIM_SCLK, SPIM_NSS)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$; 1.62 <= VDDIO <= 1.98 or 2.4 <= VDDIO <= 3.6	0.65x VDDIO	-	VDDIO+0.5	V
V_{IL}	LOW-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$; 1.62 <= VDDIO <= 1.98 or 2.4 <= VDDIO <= 3.6	- 0.5	-	0.35 × VDDIO	V
I_{IH}	HIGH-level input current	2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-	-	1	µA
I_{IL}	LOW-level input current	2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-1	-	-	µA
R_{PU}	Weak pullup resistor		40	50	62	kΩ
R_{PD}	Weak pulldown resistor		40	50	62	kΩ
C_{IN}	input capacitance		-	-	5	pF

Table 448. XTAL1, XTAL2 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(p-p)}$	peak-to-peak input voltage	-	0.4	-	1.65	V
I_{IH}	HIGH-level input current	VI= 1.65 V, no power saving, active mode	-	-	5	µA

Table 448. XTAL1, XTAL2 pins *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IL}	LOW-level input current	VI = 0 V, no power saving, active mode	-	-	1	µA
δ	duty cycle	-	35	-	65	%
$C_{i(CLK1)}$	input capacitance on pin CLK1	VDD = 1.8 V, VDC = 0.65 V, VAC = 0.9 V (p-p)	-	1	-	pF
$C_{i(CLK2)}$	input capacitance on pin CLK2	VDD = 1.8 V, VDC = 0.65 V, VAC = 0.9 V (p-p)	-	1	-	pF

Table 449. RXp, RXn pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(dyn)}$	dynamic input voltage		-	-	1.8	V
C_i	input capacitance		-	1	-	pF
Z_i	input impedance from RXN, RXP pins to VMID	Reader, card, and P2P modes	-	-	15	kΩ

Table 450. TX1, TX2 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(VDDPA)}$=5.0 V; with internal VDDPA LDO	-	$V_{DD(VDDPA)}$ -150 mV	$V_{DD(VDDPA)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(VDDPA)}$=5.0 V;with internal VDDPA LDO	0	200	-	m

Table 451. VTUNE0 and VTUNE1 output pins (Tuning DAC)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{O_max}	HIGH-level maximum output voltage	connected to a variable capacitor (varicap), VDDIO = 3.3 V	-	$V_{DD(VDDIO)}$	3.65	V
V_{O_min}	LOW-level minimum output voltage	connected to a variable capacitor (varicap)	- 0.3	0	200	mV
	DAC resolution		-	-	8	bits
C_{O_LOAD}	output capacitance load of pin		0	-	4	nF

Table 452. USB pins (ATX_C (USB D+) ATX_D (USB D-))

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OZ}	OFF-state output current	0 V < Vi < 3.3 V	-10	-	10	µA

Table 452. USB pins (ATX_C (USB D+) ATX_D (USB D-))*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DI}	Differential input sensitivity voltage	(D+) - (D-)	0.2	-	-	V
V_{CM}	Differential common mode voltage range	Includes V_{DI} range	0.8	-	2.5	V
$V_{th(rs)se}$	Single-ended receiver switching threshold voltage		0.8	-	2	V
V_L	low-level input voltage		0.8	-	-	V
V_{IH}	high-level input voltage		-	-	2	V
V_{OH}	high-level output voltage		3	3.3	3.6	pF
C_{trans}	transceiver capacitance	Pin to GND	-	15	-	
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	28	-	44	Ω
V_{CRS}	output signal crossover voltage		1.3	-	2	V

Table 453. I2C / I3C input pins (ATX_B pin (I^2C (SCL), I^3C (SCL))

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	high-level input voltage		0.65 x $V_{DD(VDDIO)}$	-	$V_{DD(VDDIO)}$ + 0.5	V
V_{IL}	low-level input voltage		0.5	-	0.35 x $V_{DD(VDDIO)}$	V
I_{IH}	high-level input current		-	-	1	µA
I_{IL}	low-level input current		-1	-	-	µA
C_{IN}	input capacitance		-	-	5	pF

Table 454. I2C / I3C output pins (ATX_A pin (I^2C (SDA), I^3C (SDA))

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	high-level output voltage	$V_{DD(VDDIO)}$ = 1.62, 1.8, 1.98: I2C (I_{OH} = 14.5 mA)	0.3 x $V_{DD(VDDIO)}$	-	0.7 x $V_{DD(VDDIO)}$	V
V_{OL}	low-level output voltage	$V_{DD(VDDIO)}$ = 1.62, 1.8, 1.98: I2C (I_{OL} = 6 mA)	0	-	0.4	V
V_{OH}	high-level output voltage	$V_{DD(VDDIO)}$ = 2.4, 3.3, 3.6: I2C (I_{OH} = 13.6 mA)	0.3 x $V_{DD(VDDIO)}$	-	0.7 x $V_{DD(VDDIO)}$	V
V_{OL}	low-level output voltage	$V_{DD(VDDIO)}$ = 2.4, 3.3, 3.6: I2C (I_{OL} = 11.5 mA)	0	-	0.4	V
I_{OH}	high-level output current	$V_{DD(VDDIO)}$ = 1.62, 1.8, 1.98: I2C At 0.3 × VDDE < VOH < 0.7 × VDDE	3	-	14.5	mA
I_{OL}	low-level output current	$V_{DD(VDDIO)}$ = 1.62, 1.8, 1.98: I2C At VOL = 0.4 V	6	-	-	mA
I_{OH}	high-level output current	$V_{DD(VDDIO)}$ = 2.4, 3.3, 3.6: I2C At 0.3 × VDDE < VOH < 0.7 × VDDE	3.5	-	13.6	mA
I_{OL}	low-level output current	$V_{DD(VDDIO)}$ = 2.4, 3.3, 3.6: I2C At VOL = 0.4 V	11.5	-	-	mA
C_L	load capacitance		-	-	20	pF

Table 455. ISO AUX pins (ISO_INT_AUX, ISO_IO_AUX, ISO_CLK_AUX)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	high-level input voltage		0.65 x $V_{DD(VDDIO)}$	-	$V_{DD(VDDIO)}$	V
V_{IL}	low-level input voltage		0	-	0.35 x $V_{DD(VDDIO)}$	V

Table 455. ISO AUX pins (ISO_INT_AUX, ISO_IO_AUX, ISO_CLK_AUX)*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HYS}	input hysteresis voltage		0.05 x $V_{DD(VDDIO)}$	-	-	V
V_{OH}	high-level output voltage by “medium” pullup (only in “quasi-bidirectional” mode)	IOH = –20 µA	0.7 x $V_{DD(VDDIO)}$	-	-	V
V_{OH2}	high-level output voltage by strong pullup	IOH = –0.1 mA	$V_{DD(VDDIO)}$ - 0.2	-	-	V
V_{OL}	low-level output voltage	IOL = 1.0 mA	-	-	0.3	V
V_{OL2}	low-level output voltage	IOL = 0.75 mA; 1.8 V	-	-	0.15 x $V_{DD(VDDIO)}$	V
C_{IN}	Input capacitance		-	-	5	pF

11.3 Timing characteristics

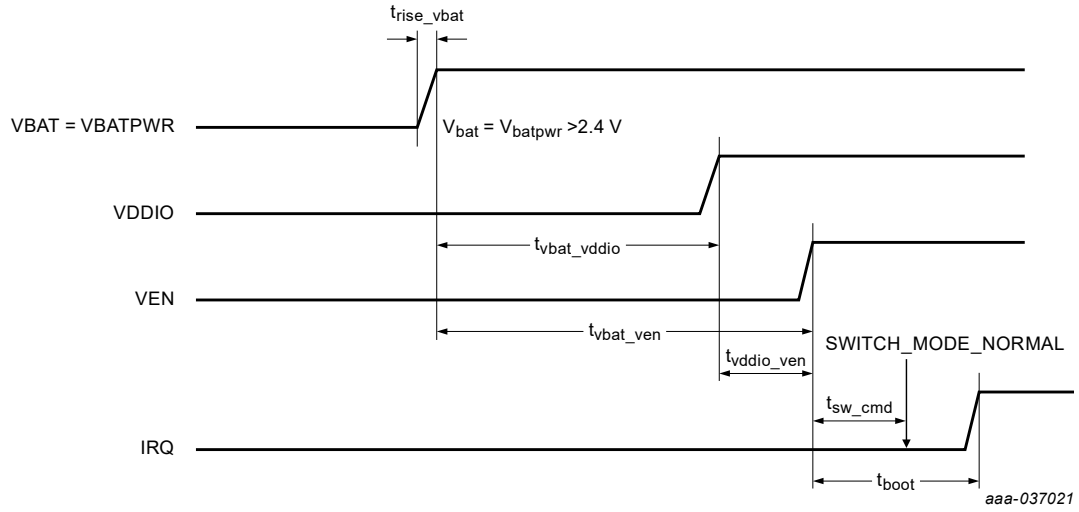


Figure 29. Startup timing

After VEN reset and tswcmd are lapsed, SWITCH_MODE_NORMAL command shall be issued to enter normal mode of operation. Recommended value of tswcmd = 500 µs.

Table 456. Power supply connection timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rise_vbat}	VBAT supply ramp	VEN = Low	0	-	2.75	V/µs
t_{vbat_vddio}	time between ramping up VBAT and ramping VDDIO	vddio condition: VBAT>2.4 V, VDDIO supply	0	500	1000	ms

Table 456. Power supply connection timing *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		(External), hpd_off_sel = x				
t_{vbat_ven}	time between ramping VBAT and VEN	vddio condition: VBAT>2.4 V, VDDIO supply (External), hpd_off_sel = x	0	500.5	1001	ms
t_{boot}	start-up time[1]	vddio condition: VBAT>2.4 V, VDDIO supply (External), hpd_off_sel = x	3.2	3.27	dependent on configuration of XTAL_CHECK_DELAY (0013h) in EEPROM. This configuration can be used to optimize the boot time for crystals which allow a fast settling. This allows to optimize the average current consumption during ULPCD and LPCD. default EEPROM configuration: 3.4	ms

[1] (PN7642 ready to receive commands on the host interface). For ULPCD and LPCD, the PN7642 indicates the ability to receive commands from a host by raising an IDLE IRQ.

Table 457. Pulse length

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(VEN)}$	on Pin VEN, pulse width to reset the chip or exit from ULPCD / Hard power down State	-	5	-	-	ms
$t_{(wake-up)}$	on pin GPIOx, pulse width to wake up	-	1	-	-	µs
$t_{VEN(GPIO)}$	time from VEN high to GPIO's available for use	-	100	-	-	ms

Table 458. SPI interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCKL}	SCK LOW time	33.3	-	-	ns
t_{SCKH}	SCK HIGH time	33.3	-	-	ns
$t_{h(SCKH-D)}$	SCK HIGH to data input hold time	16.65	-	-	ns
$t_{su(D-SCKH)}$	data input to SCK HIGH set-up time	16.65	-	-	ns
$t_{h(SCKL-Q)}$	SCK LOW to data output hold time	-	-	25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NTS HIGH time	0	-	-	ns

Table 458. SPI interface*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
t_{NSSH}	NTS HIGH time	33.3	-	-	ns

Table 459. Timing characteristics for GPIO, UART (GPIO Low Speed), PWM (GPIO Low Speed)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	VDDIO = 1.8 V; high speed	0.8	-	1.9	ns
		VDDIO = 3.3 V; high speed	0.6	-	1.5	ns
		VDDIO = 1.8 V; fast speed	1.2	-	3.3	ns
		VDDIO = 3.3 V; fast speed	0.8	-	1.9	ns
		VDDIO = 1.8 V; medium speed	2	-	4.6	ns
		VDDIO = 3.3 V; medium speed	1.4	-	2.9	ns
		VDDIO = 1.8 V; low speed	20	-	43	ns
		VDDIO = 3.3 V; low speed	15	-	28	ns
t_f	fall time	VDDIO = 1.8 V; high speed	0.8	-	1.9	ns
		VDDIO = 3.3 V; high speed	0.6	-	1.5	ns
		VDDIO = 1.8 V; fast speed	1.2	-	3.3	ns
		VDDIO = 3.3 V; fast speed	0.8	-	1.9	ns
		VDDIO = 1.8 V; medium speed	2	-	4.6	ns
		VDDIO = 3.3 V; medium speed	1.4	-	2.9	ns
		VDDIO = 1.8 V; low speed	15	-	25	ns
		VDDIO = 3.3 V; low speed	14	-	21	ns

Table 460. Timing characteristics for ATX_, ATX_B in I^2C configuration

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	VDDIO = 1.8 V; high speed - input	18	-	35	ns

Table 460. Timing characteristics for ATX_, ATX_B in I^2C configuration*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		VDDIO = 3.3 V; high speed - input	17	-	39	ns
		VDDIO = 1.8 V; standard, fast, fast+ speed - input	68	-	120	ns
		VDDIO = 3.3 V; standard, fast, fast+ speed - input	66	-	115	ns
		VDDIO = 1.8 V; high-speed clock - output	14	-	40	ns
		VDDIO = 3.3 V; high-speed clock - output	11	-	35	ns
		VDDIO = 1.8 V; high-speed data - output	25	-	90	ns
		VDDIO = 3.3 V; high-speed data - output	15	-	90	ns
t_f	fall time	VDDIO = 1.8 V; high speed - input	18	-	35	ns
		VDDIO = 3.3 V; high speed - input	17	-	30	ns
		VDDIO = 1.8 V; standard, fast, fast+ speed - input	70	-	125	ns
		VDDIO = 3.3 V; standard, fast, fast+ speed - input	67	-	120	ns
		VDDIO = 1.8 V; high-speed clock - output	15	-	35	ns
		VDDIO = 3.3 V; high-speed clock - output	13.5	-	28	ns
		VDDIO = 1.8 V; high-speed data - output	15	-	35	ns

Table 460. Timing characteristics for ATX_, ATX_B in I^2C configuration*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		VDDIO = 3.3 V; high-speed data - output	13.5	-	28	ns

Table 461. RF_ON command timing following a previous RF_OFF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(RF\_OFF-RF\_ON)}$	RF_ON command timing	guard time between command sends for RF_OFF and command send for RF_ON, capacitors on transmitter must be fully de-charged before RF_ON command is sent	5.1	5.6	-	ms

Table 462. I^2C timing specification: Standard, Fast Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	Load capacitance < 400 pF	0	-	0.4	MHz
t_{SU} START	Set-up time for a (repeated) START condition	Load capacitance < 400 pF	600	-	-	ns
t_{HD} START	hold time of a (repeated) START condition	Load capacitance < 400 pF	600	-	-	ns
t_{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 400 pF	1.3	-	-	µs
t_{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 400 pF	600	-	-	ns
t_{SU} DATA	DATA set-up time	Load capacitance < 400 pF	100	-	-	ns
t_{HD} DATA	DATA hold-up time	Load capacitance < 400 pF	0	-	900	ns

Table 462. I^2C timing specification: Standard, Fast Mode*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tr_{DA}	Rise time of SDA	Load capacitance < 400 pF	30	-	250	ns
tf_{DA}	Fall time of SDA	Load capacitance < 400 pF	30	-	250	ns

Table 463. I^2C timing specification: High-Speed Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	Load capacitance < 100 pF	0	-	3.4	MHz
t_{SU} START	Set-up time for a (repeated) START condition	Load capacitance < 100 pF	160	-	-	ns
t_{HD} START	hold time of a (repeated) START condition	Load capacitance < 100 pF	160	-	-	ns
t_{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 100 pF	160	-	-	ns
t_{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 100 pF	60	-	-	ns
t_{SU} DATA	DATA set-up time	Load capacitance < 100 pF	10	-	-	ns
t_{HD} DATA	DATA hold-up time	Load capacitance < 100 pF	0	-	-	ns
tr_{DA}	Rise time of SDA	Load capacitance < 100 pF	10	-	80	ns
tf_{DA}	Fall time of SDA	Load capacitance < 100 pF	10	-	80	ns

Table 464. I^2C timing specification: Fast + High-Speed-Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	Load capacitance < 100 pF	0	-	1	MHz

Table 464. I^2C timing specification: Fast + High-Speed-Mode*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SU} START	Set-up time for a (repeated) START condition	Load capacitance < 100 pF	260	-	-	ns
t_{HD} START	hold time of a (repeated) START condition	Load capacitance < 100 pF	260	-	-	ns
t_{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 100 pF	500	-	-	ns
t_{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 100 pF	260	-	-	ns
t_{SU} DATA	DATA set-up time	Load capacitance < 100 pF	50	-	-	ns
t_{HD} DATA	DATA hold-up time	Load capacitance < 100 pF	0	-	-	ns
tr_{DA}	Rise time of SDA	Load capacitance < 100 pF	-	-	120	ns
tf_{DA}	Fall time of SDA	Load capacitance < 100 pF	-	-	120	ns

Table 465. Timing characteristics for I^3C interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LOW}	Low period of SCL clock		200	-	-	ns
t_{HIGH}	High period of SCL clock		-	-	41	ns
tf_{DA}	Fall time of SDA		t_{CF}	-	12	ns
t_{CAS}	Clock after START (S) condition	ENTAS0	38.4 nano	-	1 µ	s
		ENTAS1			100 µ	s
		ENTAS2			2 mill	s
		ENTAS3			50 mill	s
t_{CBP}	Clock before STOP (P) condition		t_{CAS}min / 2	-	-	s
t_{AVAL}	BUS available condition		1	-	-	ns

Table 465. Timing characteristics for I^3C interface*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{IDLE}	BUS IDLE condition		1	-	-	ms
t_{MMLock}	Time Internal where new Controller must not drive SDA LOW		t_{AVAL}min	-	-	us

Table 466. Timing characteristics for USB interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %	4	-	20	ns
t_f	fall time	10 % to 90 %	4	-	20	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f	-	-	10	%
V_{CRS}	output signal crossover voltage		1.3	-	2	V
t_{FEOPT}	source SE0 interval of EOP	T = 25 °C	160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	T = 25 °C	-2	-	+5	ns
t_{JR1}	receiver jitter to next transition	T = 25 °C	-18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %; T = 25 °C	-9	-	+9	ns
t_{FEOPR}	receiver SE0 interval of EOP	must accept as EOP; T = 25 °C	82	-	-	ns

Table 467. Timing characteristics ISO AUX interface (ISO_INT_AUX, ISO_IO_AUX, ISO_CLK_AUX)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	output rise time at IO	VDDIO = 1.8 V; EHS = L	50	-	125	ns
	output rise time at IO	VDDIO = 3.3 V; EHS = L	32	-	86	ns
	output rise time at IO	VDDIO = 1.8 V; EHS = H	25	-	63	ns
	output rise time at IO	VDDIO = 3.3 V; EHS = H	16	-	43	ns

Table 467. Timing characteristics ISO AUX interface (ISO_INT_AUX, ISO_IO_AUX, ISO_CLK_AUX)*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	input rise time at IO	VDDIO = 1.8 V	1.2	-	3.2	ns
	input rise time at IO	VDDIO = 3.3 V	1.2	-	3.2	ns
t_f	output fall time at IO	VDDIO = 1.8 V; EHS = L	11	-	31	ns
	output fall time at IO	VDDIO = 3.3 V; EHS = L	8	-	22	ns
	output fall time at IO	VDDIO = 1.8 V; EHS = H	9	-	25	ns
	output fall time at IO	VDDIO = 3.3 V; EHS = H	6	-	16	ns
	input fall time at IO	VDDIO = 1.8 V	0.9	-	2.3	ns
	input fall time at IO	VDDIO = 3.3 V	0.9	-	2.3	ns

11.4 Clock input

Table 468. Crystal requirements for ISO/IEC14443 compliant operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{xtal}	crystal frequency	ISO/IEC compliancy	-	27.12	-	MHz
delta f_{xtal}	crystal frequency accuracy	for full RF operating range	-40	-	+40	ppm
ESR	equivalent series resistance	-	10	30	100	Ω
C_L	load capacitance	-	6	8	10	pF
$t_{startup}$	crystal startup time	-	-	-	1	ms
P_{xtal}	crystal power dissipation	-	-	-	100	µW

Table 469. Frequency requirements for a direct clock input (no crystal)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	ISO/IEC compliancy	-	24	-	MHz
			-	32	-	
			-	48	-	
delta f_{clk}	clock frequency accuracy	for full RF operating range	-40	-	+40	ppm
φ_n	phase noise	input phase noise floor at 100 kHz offset	-	- 150	-145	dBc/Hz

Table 469. Frequency requirements for a direct clock input (no crystal) ***...continued***

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
φ_n	phase noise	input phase noise floor at 1 MHz offset	-	- 152	-149	dBc/Hz
V_i	Input voltage boundary	sinus signal	0	-	1.8	V
$V_{i(p-p)}$	peak-to-peak Input voltage	sinus signal	0.4	-	1.8	V
$V_{i(clk)}$	clock input voltage	square signal	0	-	1.8 +/-10%	V

11.5 EEPROM characteristics

Table 470. EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$N_{endu(W)}$	write endurance	at ambient temperature T_a = +25 °C	100	-	-	K cycles
t_{ret}	retention time	at ambient temperature T_a =+25 °C	25	-	-	years

12 Package outline

12.1 VFBGA64 package

Table 471. Package outline VFBGA64 (SOT1307-2)

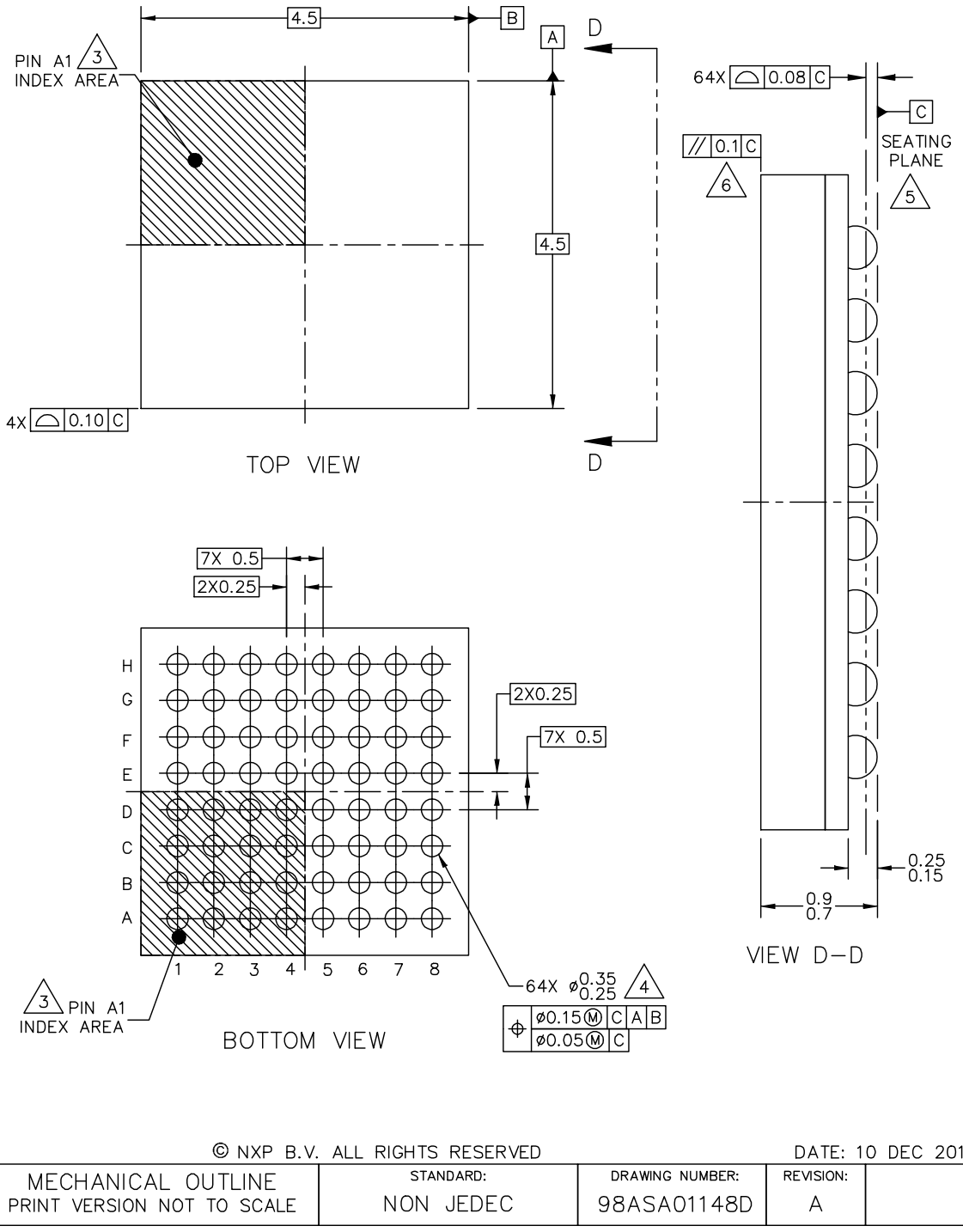


Figure 30. Package outline VFBGA64 (SOT1307-2)

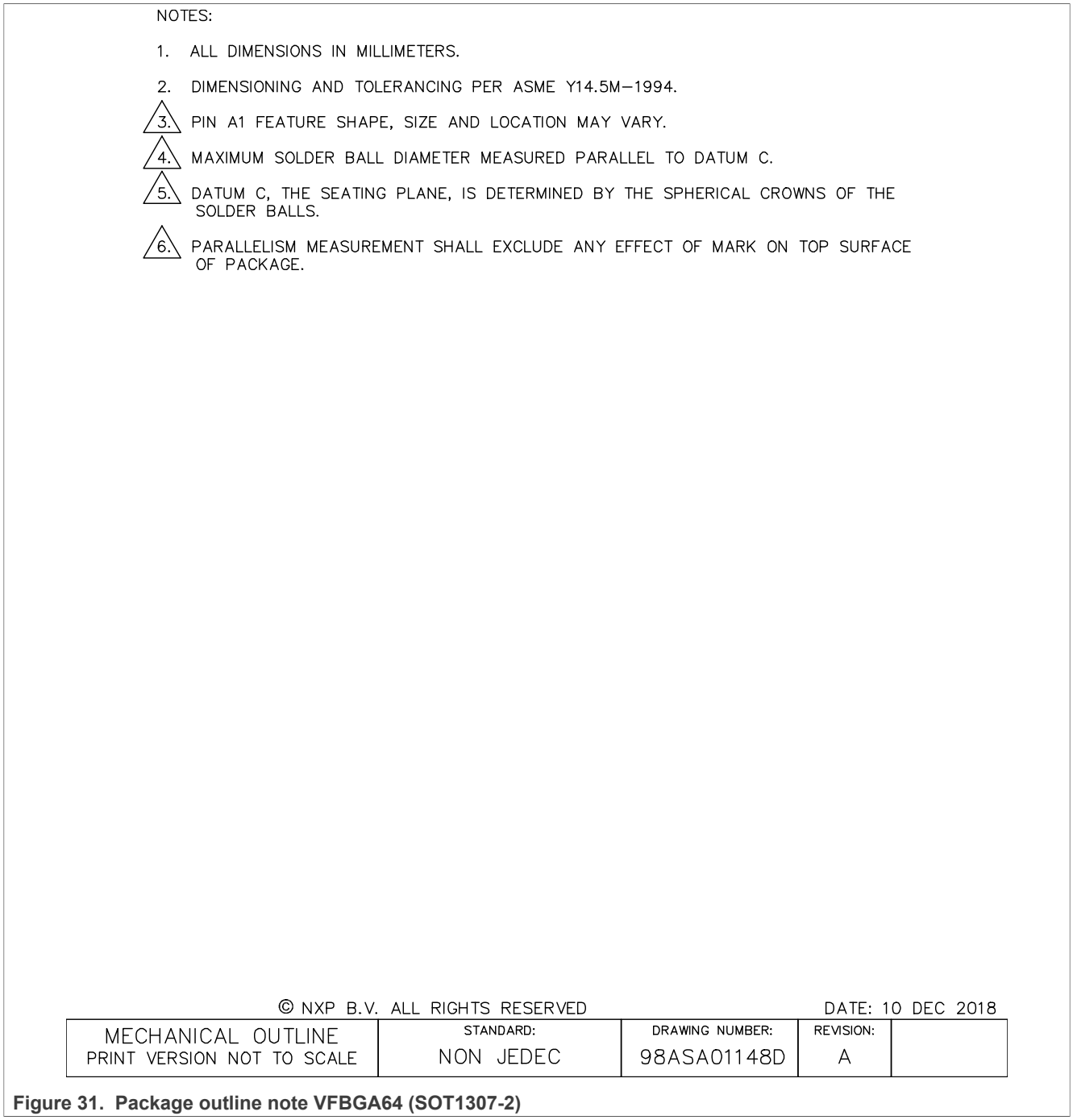


Figure 31. Package outline note VFBGA64 (SOT1307-2)

13 Package marking

13.1 Package marking drawing VFBGA64

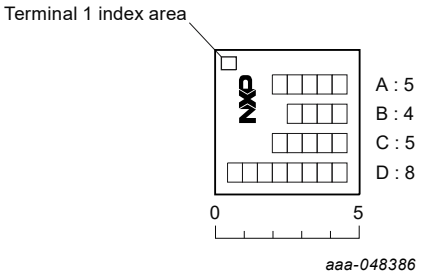


Figure 32. VFBGA64 Package 4 line marking

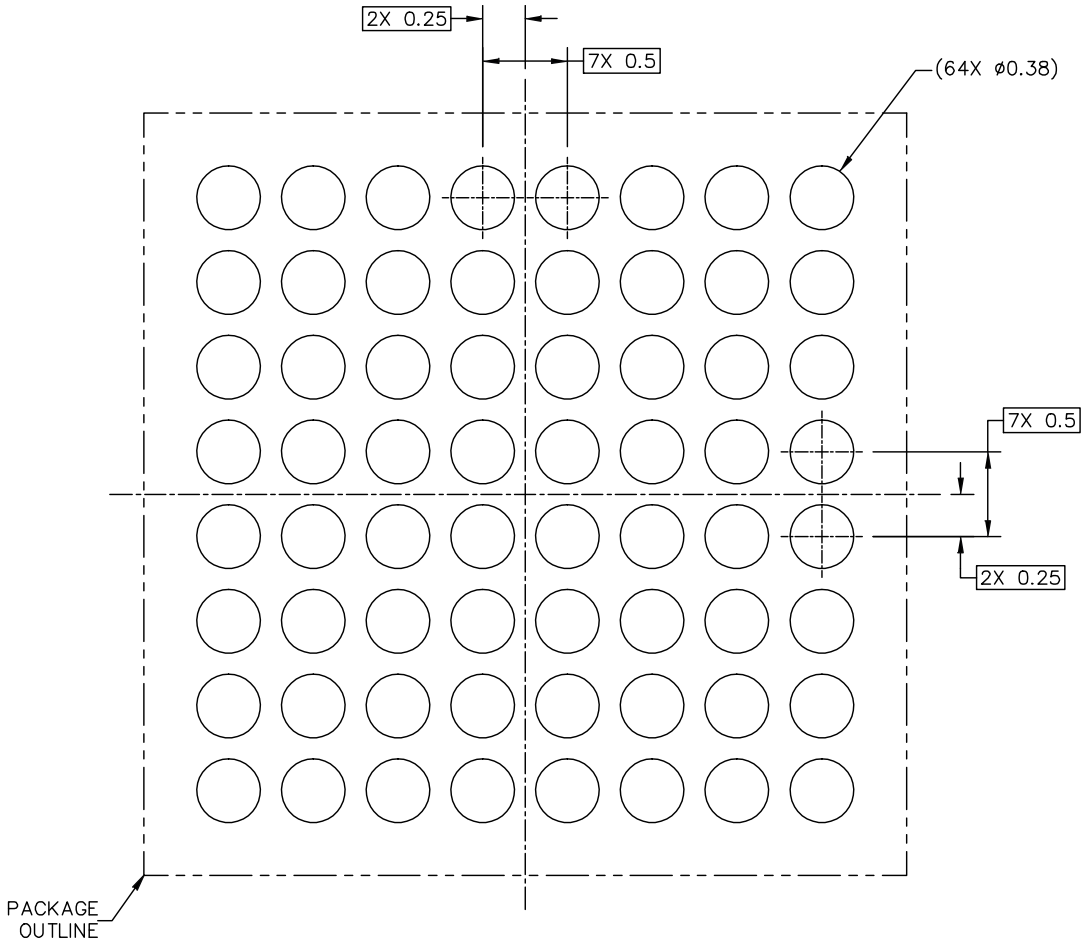
Line A: 5 characters; e.g. "7642" for PN7642

Line B: Firmware version programmed during production

Line C: 5 characters; contains the DB ID and AS ID

Line D: 8 characters; stDYYWW(X) - contains information assembly center, date code, and maturity level (“X” = engineering samples, “ “ = released product)

14 Reflow soldering footprint VFBGA64



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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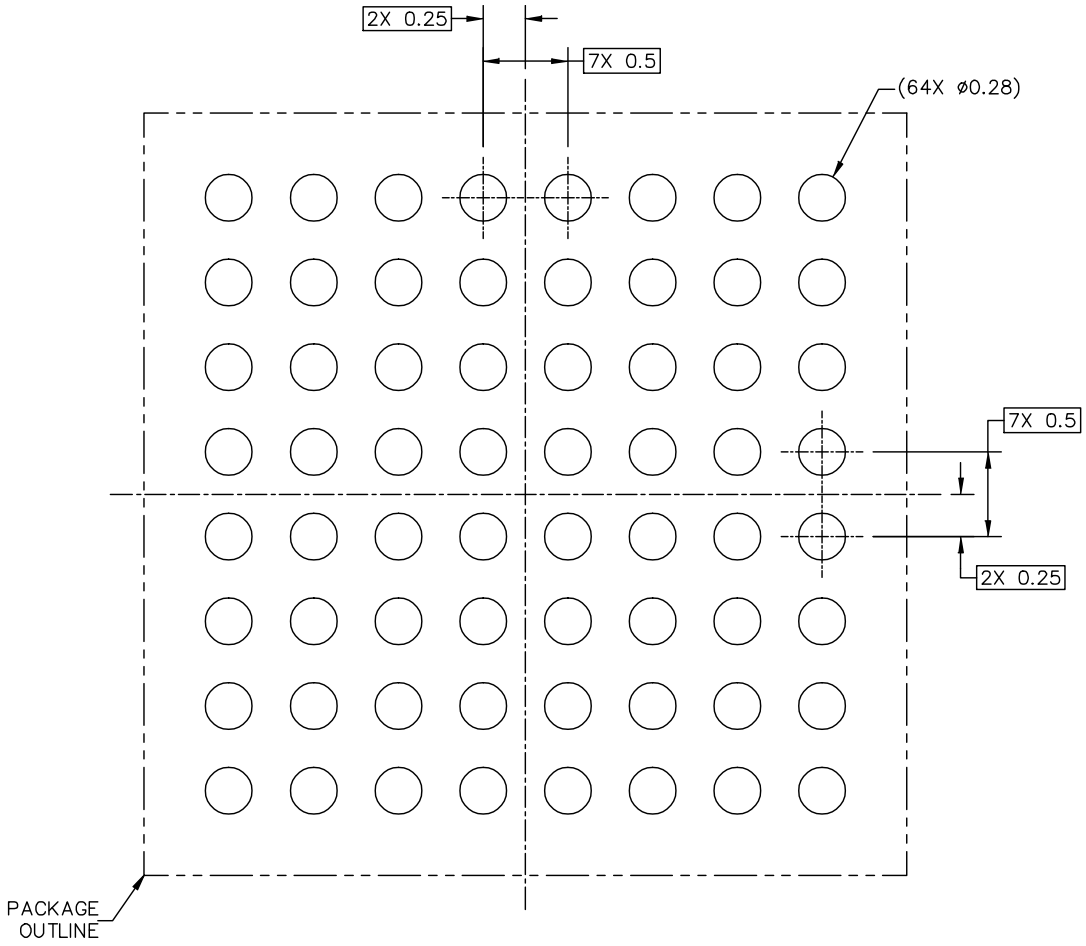
DATE: 10 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01148D	REVISION: A	

Figure 33. Reflow soldering footprint part1 for VFBGA64 (SOT1307-2)



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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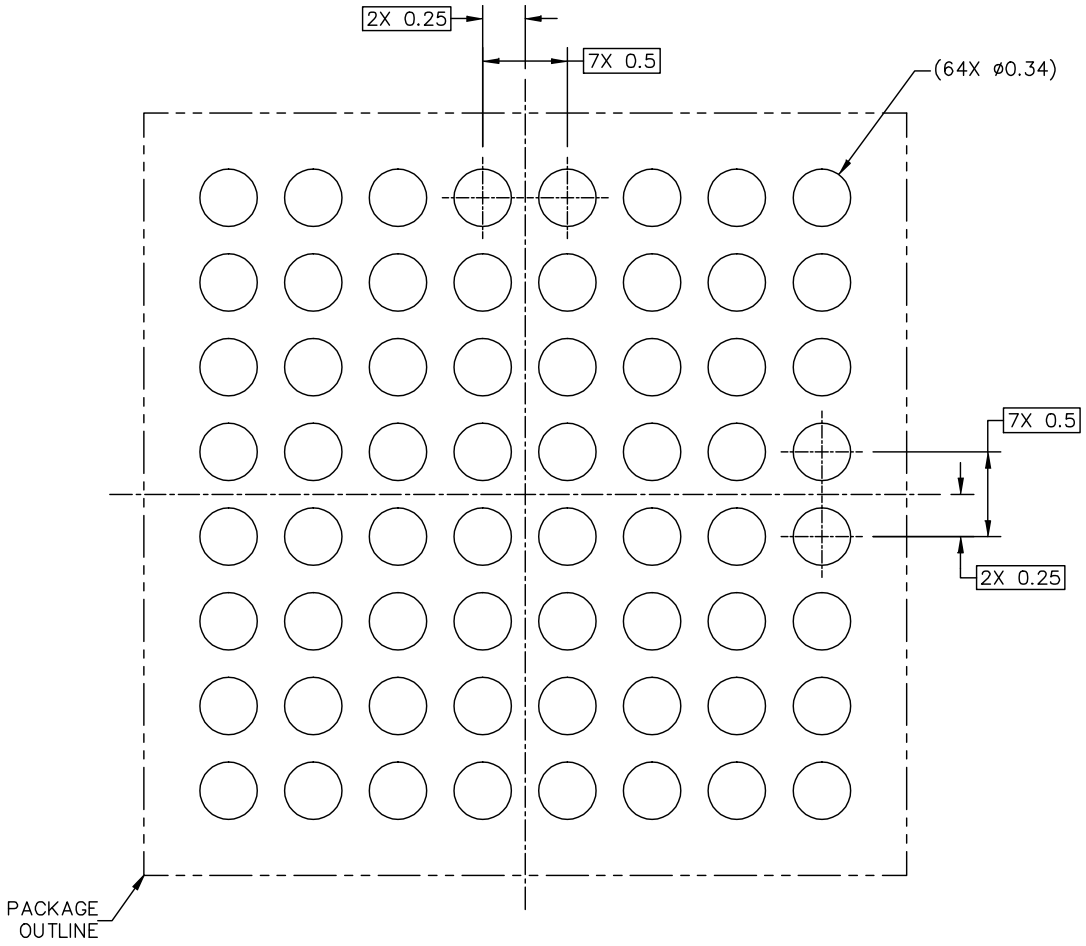
DATE: 10 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01148D	REVISION: A	

Figure 34. Reflow soldering footprint part2 for VFBGA64 (SOT1307-2)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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DATE: 10 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01148D	REVISION: A	

Figure 35. Reflow soldering footprint part3 for VFBGA64 (SOT1307-2)

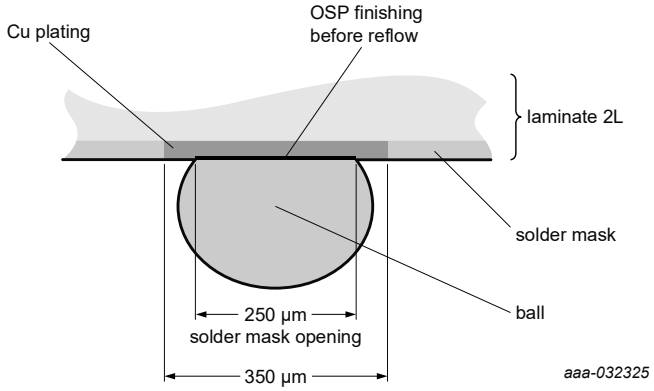

Figure 36. Soldering and footprint representative illustration for VFBGA64 (SOT1307-2)

15 Surface mount reflow soldering

For information on surface mount, reflow soldering and component handling please refer to the related application note.

This application note provides guidelines for the board mounting and handling of NXP Semiconductor packages:

https://www.nxp.com/docs/en/application-note/AN10365.pdf

16 Handling information

Moisture Sensitivity Level (MSL) evaluation has been performed according to *SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C)*.

An MSL corresponds to a certain out-of-bag time (or floor life). If semiconductor packages are removed from their sealed dry-bags and not soldered within their out-of-bag time, they must be baked prior to reflow soldering, in order to remove any moisture that might have soaked into the package.

For MSL3:

168h out-of-pack floor life at maximum ambient temperature, conditions < 30 °C / 60 % RH.

For MSL2:

- 1 year out-of-pack floor life at maximum ambient temperature, conditions < 30 °C° / 60 % RH.

For MSL1:

- No out-of-pack floor live spec. required. Conditions: <30 °C° / 85 % RH.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.
Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

17 Abbreviations

Table 472. Abbreviations

Acronym	Description
AA	audio accelerator
ADC	analog-to-digital converter
AGC	automatic gain control
AHB	advanced high-performance bus
AHB-Lite	advanced high-performance bus (single-controller implementation)
AHB bus	advanced high-performance bus
APB	advanced peripheral bus
API	application programming interface
ARC	adaptive receiver control
Arm	Advanced RISC Machine
AWC	adaptive waveshape control
BBA	baseband amplifier
BOD	brownout detection
CITO	controller input target output (previously master input slave output)
CLIF	contactless interface
COTI	controller output target input (previously master output slave input)
CPU	central processing unit
CRC	cyclic redundancy check
CTR	current transfer ratio
CTS	clear to send
DAC	digital-to-analog converter
DC-DC	switch-mode voltage regulator which uses an inductor to store and transfer energy to the output, used for a power supply voltage conversion. PN7642 integrates a step-up/boost converter
DDR	double data rate
DMA	direct memory access
DPC	dynamic power control
ECC	elliptic curve cryptography
EEPROM	electrically erasable programmable read-only memory
EMC	electromagnetic compatibility
EMD	electromagnetic disturbance
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macro
EOF	end-of-frame
Fm+	Fast-mode Plus
FSM	finite state machine

Table 472. Abbreviations...*continued*

Acronym	Description
GND	Ground
GPIO	general-purpose input output
HID	human interface device
HPD	hard power down
HW	hardware
IC	Integrated Circuit
IIR	infinite impulse response
IrDA	Infrared Data Association
IAP	In-Application Programming
ISP	In-System Programming
I/O	input/output
I/Q	in-phase/quadrature-phase
JEDEC	Joint Electron Device Engineering Council
LDO	low dropout regulator
LPCD	low-power card detection
LPUART	Low-Power Universal Asynchronous Receiver / Transmitter
LSB	least significant bit
LSByte	least significant byte
MISO	SPI interface controller in target out
MSL	moisture sensitivity level
MOSI	SPI interface controller out target In
NFC	near-field communication
NRZ	non-return-to-zero
NSS	SPI interface active-low target-select signal
NTS	not target select (previously not slave select)
NVIC	nested vectored interrupt controller
OS	operating system
OTP	one time programmable
PCB	printed-circuit board
PC	personal computer
PCD	power card detection
PICC	proximity inductive coupling card
PLL	phase-locked loop
PMU	power management unit
PWM	pulse width modulation
RAM	random-access memory

Table 472. Abbreviations...*continued*

Acronym	Description
RF	radio frequency
RNG	random number generator
ROM	read-only memory
RSA	Rivest, Shamir, and Adleman public key cryptosystem
RSSI	receiver signal strength indicator
RTOS	real-time operating system
RTS	request to send
SCK	SPI interface serial clock
SCL	I^2C interface serial clock
SDA	serial data
SMPS	switch mode power supply
SPI	serial peripheral interface
SRAM	static random-access memory
SWD	serial wire debug
TFT	display technology: thin-film transistor-display
TX	transmit
UART	universal asynchronous receiver transmitter
UID	Unique identifier of a card, used during anti-collision sequence to select one out of multiple cards.
ULPCD	ultra low-power card detection
USB	universal serial bus
VREF	voltage reference

18 References

[1] Specification – Apple Enhanced Contactless Polling Specification: Version 1.1.
[2] User manual – UM11905 PN76 instruction manual (link)

19 Revision history

Table 473. Revision history

Document ID	Release date	Data sheet status	Supersedes
PN7642 v.3.2	06 May 2024	Product data sheet	PN7642 v.3.1
Modifications:	• Table 22 "Supply voltage range configuration": updated DCDC_PWR_CONFIG (EEPROM) configuration. **NFC Sub System** • Section 9.4.3 "Dynamic power control (DPC)": updated Figure 7 "System overview: DPC, AWC, and ARC". **CLIF registers** • Added the description of registers included in PN7642 FW v02.02 and above: – Section 9.14.1.79 "LPCD_CALIBRATE_CTRL (0x50)" – Section 9.14.1.80 "IQ_CHANNEL_VALS (0x51)" – Section 9.14.1.81 "CALIBRATE_STATUS (0x53)" **PRCM registers** • Section 9.14.2.40 "PCRM_SYS_BOOT1_STS (0xC6)": updated. • Section 9.14.2.14 "PCRM_PMU_ANA_VBAT_MON2 (0xAC)": updated. **EEPROM registers** • Section 9.14.3.17.3 "ULPCD_AGC_HFATT_CTRL (063A)": added EEPROM configuration. • Table 233 "List of EEPROM configuration parameters for power, TXLDO, XTAL and Clocks": updated. • Updated the description of registers for PN7642 FW v02.02 and above: – Section 9.14.3.1.5 "TXLDO_VDDPA_CONFIG (0x0006)" – Section 9.14.3.1.7 "TXLDO_VDDPA_MAX_CARD (0x0008)" – Section 9.14.3.1.6 "TXLDO_VDDPA_MAX_RDR (0x0007)" – Section 9.14.3.1.8 "BOOST_DEFAULT_VOLTAGE (0x0009)" – Section 9.14.3.3.10 "DPC_TXLDO_MAX_DROPOUT (0x0073)"		
PN7642 v.3.1	21 June 2023	Product data sheet	PN7642 v.3.0
Modifications:	• Firmware versions: PN7642EV/C101 added • Section 5 "Ordering information": updated • Section 13.1 "Package marking drawing VFBGA64": updated • Register and EEPROM description updated		
PN7642 v.3.0	14 March 2023	Product data sheet	PN7642 v.1.2
Modifications:	• Data sheet status changed to product data sheet, security status changed to public		
PN7642 v.1.2	8 November 2022	Objective data sheet	PN7642 v.1.1
Modifications:	• Product name "PN76 family" changed into PN7642 throughout the document • Section 2.2 "Product comparison": updated		
PN7642 v.1.1	10 October 2022	Objective data sheet	PN7642 v.1.0
Modifications:	• Entry for HFQNF40 deleted • The replacement of "master/slave" by "controller/target" in this document follows the recommendation of the NXP - I^2C and JEDEC SPI standards organizations. • Section 9.4.6 "Energy-saving card detection" and subchapters added • Section 2.2 "Product comparison": updated • Section 9.3.5.4 "On-chip flash memory map": updated • Section 5 "Ordering information": updated		
PN7642 v.1.0	27 September 2022	Objective data sheet	-

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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Tables

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Contents

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