

# S32G3

## S32G3 Data Sheet

Rev. 2 — 02/2023

Data Sheet: Technical Data

- This document provides electrical specifications for S32G3.
- For functional characteristics and the programming model, see S32G3 Reference Manual.



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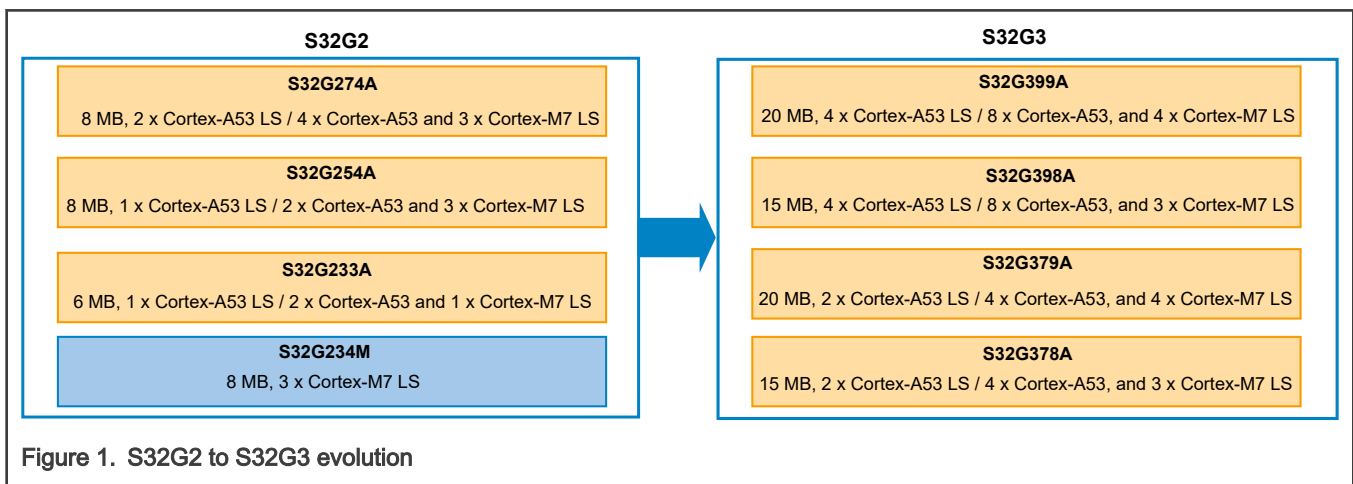
# 1 Introduction

## 1.1 Overview

S32G3 is a family of high-performance vehicle network processors that combine controller area network (CAN), local interconnect network (LIN), and FlexRay networking with high data rate Ethernet networking. It also combines a functional safe-core infrastructure with MPU cores and includes high-level security features. The S32G3 chips are pin-for-pin compatible with S32G2 chips, providing over 2x performance and over 2x system RAM.

**Table 1. S32G3 family key enhancements**

| Feature                      | Enhancements  |
|------------------------------|---|
| Compute performance          | Up to 2.6 x increase in applications performance (doubling Cortex-A53 cores @ 1.3x frequency) |
| Real-time memory             | Increase SRAM from 6 MB / 8 MB to 15 MB / 20 MB   |
| Real-time performance        | Additional pair of Cortex-M7 lockstep cores   |
| Ethernet interface bandwidth | Increased speed from 1 Gbps to 2.5 Gbps on two SGMII interfaces                               |
| Ethernet packet routing      | Performance target increase from 2 Gbps@64B to 3 Gbps@64B                                     |



S32G3 family includes the following variants:

- S32G399A
- S32G398A
- S32G379A
- S32G378A

This document primarily represents the features offered by the superset S32G399A. To compare the features of the S32G3 family variants, see [Feature comparison](#).

## 1.2 Applications

Combining ASIL D safety, hardware security, high-performance real-time and application processing and network acceleration, this chip targets applications that includes:

- Service-oriented gateways and domain controllers
- Safety processor for ADAS and autonomous driving
- High-performance central compute nodes

- FOTA masters controlling secure software image downloads and their distribution to the ECUs in the network
- Security services and key management
- Smart antennas

## 2 Block diagram

The following is the block diagram for S32G399A, the superset chip in the S32G3 family.

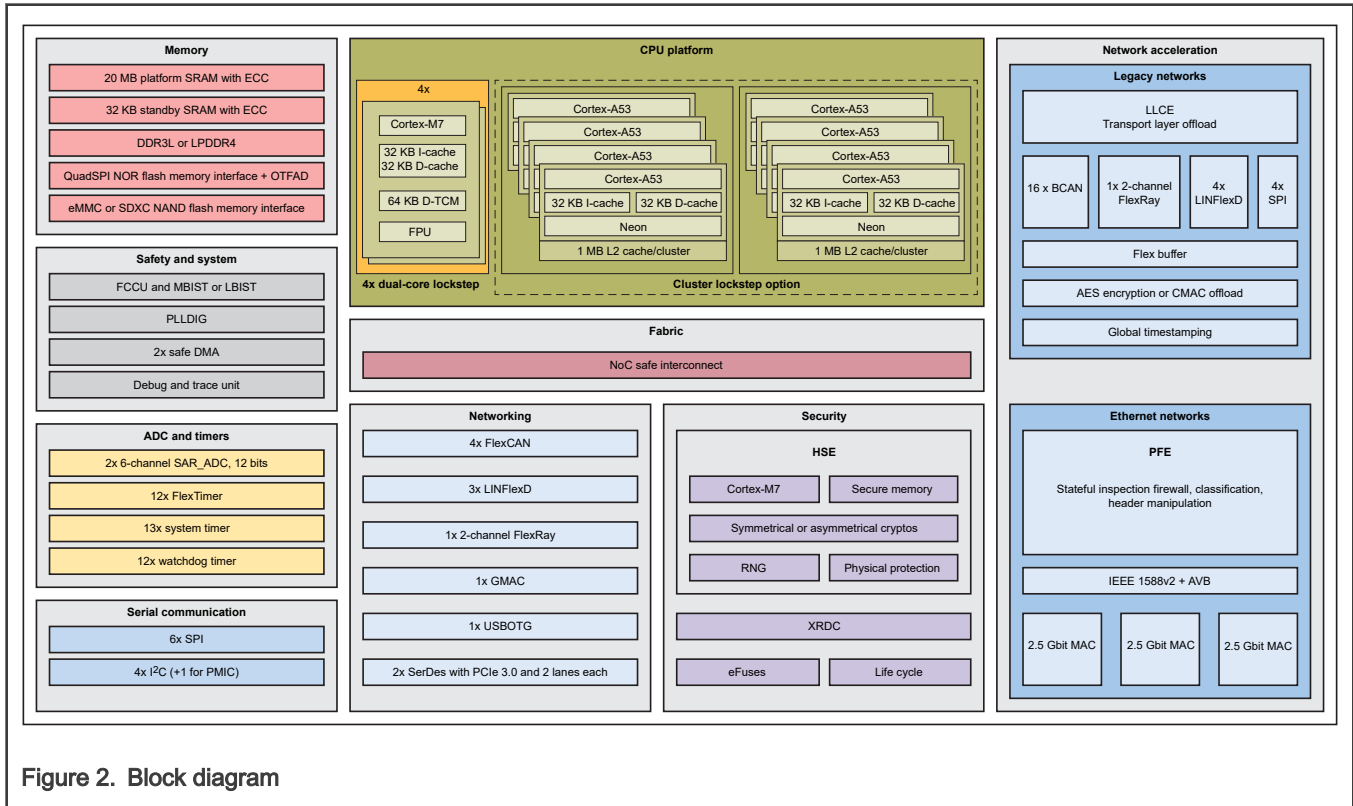


Figure 2. Block diagram

## 3 Feature comparison

This table compares the features of the chips in the S32G3 family.

Table 2. S32G3 feature list and supported functionality

| Feature                        | S32G399A  | S32G398A                              | S32G379A   | S32G378A   |
|--------------------------------|---|---------------------------------------|--|--|
| <b>Compute and bus modules</b> |   |                                       |  |  |
| Applications CPUs              | 4 x Cortex-A53 LS<br>(8 x Cortex-A53)               | 4 x Cortex-A53 LS<br>(8 x Cortex-A53) | 2 x Cortex-A53 LS<br>(4 x Cortex-A53) <sup>1</sup> | 2 x Cortex-A53 LS<br>(4 x Cortex-A53) <sup>1</sup> |
| Real-time CPUs                 | 4 x Cortex-M7 LS                                    | 3 x Cortex-M7 LS <sup>2</sup>         | 4 x Cortex-M7 LS                                   | 3 x Cortex-M7 LS <sup>2</sup>                      |
| Cortex-A53                     |   |                                       |  |  |
| L1 cache                       | 32 KB I-cache and 32 KB D-cache per Cortex-A53 core |                                       |  |  |
| L2 cache                       | 1 MB per cluster                                    |                                       |  |  |

Table continues on the next page...

Table 2. S32G3 feature list and supported functionality (continued)

| Feature                      | S32G399A   | S32G398A           | S32G379A | S32G378A           |
|------------------------------|--|--------------------|----------|--------------------|
| Cache coherency interconnect | Supported  |                    |          |                    |
| Interrupt controller         | GIC-500  |                    |          |                    |
| Maximum frequency            | Up to 1.3 GHz  |                    |          |                    |
| Functional safety            | Configurable ASIL D lockstep clusters and two ASIL B independent clusters                |                    |          |                    |
| <b>Cortex-M7</b>             |  |                    |          |                    |
| L1 cache                     | 32 KB I-cache and 32 KB D-cache per Cortex-M7  |                    |          |                    |
| Cache coherency interconnect | Not supported  |                    |          |                    |
| Interrupt controller         | 4 x NVIC   |                    |          |                    |
| Maximum frequency            | 400 MHz  |                    |          |                    |
| Functional safety            | Dual-core lockstep   |                    |          |                    |
| DTCM                         | 64 KB per Cortex-M7  |                    |          |                    |
| <b>System modules</b>        |  |                    |          |                    |
| DMA                          | 2x safe eDMA (supporting lockstep) with 32 channels per eDMA                             |                    |          |                    |
| DMAMUX                       | 128 inputs per DMA   |                    |          |                    |
| Debug: Run control           | Arm CoreSight JTAG (IEEE 1149.1)   |                    |          |                    |
| Debug: Trace                 | 4-lane Aurora  |                    |          |                    |
| SWT instances                | 12   |                    |          |                    |
| STM instances                | 13   |                    |          |                    |
| <b>Memory modules</b>        |  |                    |          |                    |
| Internal RAM                 | 20 MB  | 15 MB <sup>3</sup> | 20 MB    | 15 MB <sup>3</sup> |
| RAM ports                    | 16 (four groups of four ports each), and ports in each group are interleaved at 64 bytes |                    |          |                    |
| DRAM                         | DDR3L and LPDDR4 – up to 4 GB  |                    |          |                    |
| DRAM PHY                     | x32  |                    |          |                    |
| QuadSPI instances            | 1  |                    |          |                    |
| uSDHC instances              | 1  |                    |          |                    |
| Fuses                        | 8 KB bank  |                    |          |                    |
| Standby SRAM with ECC        | 32 KB  |                    |          |                    |
| <b>Security modules</b>      |  |                    |          |                    |
| Security subsystem           | HSE_H  |                    |          |                    |

Table continues on the next page...

Table 2. S32G3 feature list and supported functionality (continued)

| Feature                                   | S32G399A   | S32G398A | S32G379A | S32G378A |
|---|--|----------|----------|----------|
| Resource isolation                        | XRDC supporting 16 domains                                   |          |          |          |
| Arm TrustZone                             | Supported  |          |          |          |
| Life cycle                                | Supported  |          |          |          |
| Secure debug                              | Supported  |          |          |          |
| <b>Communication interface modules</b>    |  |          |          |          |
| Communication acceleration                | LLCE   |          |          |          |
| CAN with flexible data rate               | 16 in LLCE and 4 outside LLCE                                |          |          |          |
| FlexRay 2.1 (dual-channel) instances      | 1 in LLCE and 1 outside LLCE                                 |          |          |          |
| LINFlexD instances                        | 4 in LLCE and 3 outside LLCE                                 |          |          |          |
| Ethernet acceleration                     | PFE  |          |          |          |
| Ethernet MAC                              | 3 in PFE and 1 outside PFE                                   |          |          |          |
| Ethernet interface                        | MII, RMII, RGMII, SGMII                                      |          |          |          |
| PCIe controller                           | 2x Gen3 controllers (X1, X2 modes)                           |          |          |          |
| SerDes subsystem                          | Four lanes (configurable PCIe and SGMII)                     |          |          |          |
| USBOTG instances                          | 1, supporting USB 2.0 and a ULPI interface                   |          |          |          |
| I <sup>2</sup> C instances                | 4 + 1 for power management integrated circuits (PMIC)        |          |          |          |
| SPI instances                             | 4 (in LLCE, can be enabled with firmware) and 6 outside LLCE |          |          |          |
| CRC instances                             | 1  |          |          |          |
| <b>Generic modules</b>                    |  |          |          |          |
| PIT instances                             | 2  |          |          |          |
| SAR_ADC instances                         | 12-bit 2 x 6 channels  |          |          |          |
| FTM instances                             | 2 x 6 channels   |          |          |          |
| CTU instances                             | 1  |          |          |          |
| SEMA42 instances                          | 1  |          |          |          |
| <b>Clocking, power, and reset modules</b> |  |          |          |          |
| FIRC frequency                            | 48 MHz   |          |          |          |
| SIRC frequency                            | 32 KHz   |          |          |          |
| FXOSC frequency                           | 20-40 MHz  |          |          |          |
| PLLDIG instances                          | 5  |          |          |          |
| Low-power mode                            | Supported  |          |          |          |

*Table continues on the next page...*

Table 2. S32G3 feature list and supported functionality (continued)

| Feature                               | S32G399A   | S32G398A | S32G379A | S32G378A |
|---------------------------------------|--|----------|----------|----------|
| RTC                                   | 1 with API function  |          |          |          |
| Wake-up                               | 24 wake-up sources   |          |          |          |
| <b>Miscellaneous</b>                  |  |          |          |          |
| Package specifications and dimensions | 525 flip-chip plastic ball-grid array; 19 mm x 19mm x 0.8 mm |          |          |          |

1. Cortex-A53\_2 and Cortex-A53\_3 have been defeatured in cluster 0 and cluster 1.
2. Cortex-M7\_2 has been defeatured. See the System RAM Controller chapter of the S32G3 Reference Manual for details.
3. SRAM (12, 13, 14, 15) i.e., the highest address range (0x34F0\_0000–0x353F\_FFFF) associated to Cortex-M7\_2 have been defeatured. See the System RAM Controller chapter of the S32G3 Reference Manual for details on internal RAM support across the family.

## 4 Ordering information

### S32G3 Part Numbering\*

Production Part Number

|     |       |  |
|-----|-------|--|
| S32 | 1-3   | Product brand and Status                       |
| G   | 4     | Product line                                   |
| 3   | 5     | Family   |
| 9   | 6     | MPU performance identifier                     |
| 9   | 7     | MCU performance identifier and system RAM size |
| A   | 8     | Product type                                   |
| S   | 9     | Chip configuration                             |
| C   | 10    | Arm core speeds                                |
| K0  | 11-12 | Fab and mask revision                          |
| V   | 13    | Temperature (T <sub>A</sub> ) range            |
| UC  | 14-15 | Package code                                   |
| R   | 16    | Shipping method                                |

|   |  |   |
|---|--|---|
| <b>1<sup>st</sup> 2<sup>nd</sup>, 3<sup>rd</sup> Characters</b><br>Product brand and status<br><br>P32 = Prototype chip<br>S32 = Qualified device       | <b>4<sup>th</sup> Character</b><br>Product line<br>G = Gateway   | <b>9<sup>th</sup> Character</b><br>Chip configuration<br>A = Standard chip<br>S = Premium security chip   |
| <b>5<sup>th</sup> Character</b><br>Family<br>3 = S32G3 family   | <b>6<sup>th</sup> Character</b><br>MPU performance identifier<br>7 – 4x Cortex-A53<br>9 – 8x Cortex-A53                | <b>10<sup>th</sup> Character</b><br>Arm core speeds<br>A = 400 MHz (Cortex-M7), 1000 MHz (Cortex-A53)<br>B = 400 MHz (Cortex-M7), 1100 MHz (Cortex-A53)<br>C = 400 MHz (Cortex-M7), 1300 MHz (Cortex-A53) |
| <b>7<sup>th</sup> Character</b><br>MCU performance identifier and system RAM size<br>8 = 3x Cortex-M7 and 15 MB SRAM<br>9 = 4x Cortex-M7 and 20 MB SRAM | <b>8<sup>th</sup> Character</b><br>Product type<br>A = MCU + MPU   | <b>11<sup>th</sup> and 12<sup>th</sup> Characters</b><br>Fab and mask revision<br>K = TSMC fab<br>x = Mask revision (0 = first mask revision)   |
| <b>14<sup>th</sup> and 15<sup>th</sup> Characters</b><br>Package code<br>UC = 525 FC-PBGA, 19x19mm, 0.8mm pitch   | <b>13<sup>th</sup> Character</b><br>Temperature (T <sub>A</sub> ) range<br>C = -40 °C to 85 °C<br>V = -40 °C to 105 °C | <b>16<sup>th</sup> Character</b><br>Shipping method<br>T = Tray<br>R = Reel   |

|                      | S32G378A | S32G379A | S32G398A | S32G399A |
|----------------------|----------|----------|----------|----------|
| ARM Cortex-M7 Cores  | 3        | 4        | 3        | 4        |
| ARM Cortex-A53 Cores | 4        | 4        | 8        | 8        |
| System RAM Size      | 15 MB    | 20 MB    | 15 MB    | 20 MB    |

\*Contact NXP sales representative for part numbers

Figure 3. Ordering information



## 5 Electrostatic Discharge (ESD) Characteristics

The following table gives the ESD ratings and test conditions for the device.

**Table 3. Electrostatic Discharge (ESD) Characteristics**

| Symbol | Description                                       | Min | Typ | Max  | Unit | Condition | Spec Number |
|--------|---|-----|-----|------|------|-----------|-------------|
| —      | ESD Human Body Model (HBM) <sup>1, 2, 3</sup>     | —   | —   | 2000 | V    | All pins  | —           |
| —      | ESD Charged Device Model (CDM) <sup>1, 3, 4</sup> | —   | —   | 250  | V    | All pins  | —           |

1. Device failure is defined as: "If after exposure to ESD pulses, the device does not meet the device specification requirements."
2. This parameter is tested in conformity with AEC-Q100-002
3. All ESD testing conforms with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
4. This parameter is tested in conformity with AEC-Q100-011.

## 6 Absolute Max Ratings

This table defines the absolute maximum ratings for the device in terms of reliability characteristics. Absolute maximum rating specifications are stress ratings only, and functional operation is not guaranteed under these conditions. Functional operating conditions are given in the Operating Conditions section of this document.

**NOTE**

All specifications associated with VIN are measured at the SoC pin.

**Table 4. Absolute Max Ratings**

| Symbol                   | Description  | Min  | Typ | Max  | Unit | Condition | Spec Number |
|--------------------------|--|------|-----|------|------|-----------|-------------|
| VDD                      | Core voltage Supply <sup>1, 2</sup>                  | -0.3 | —   | 0.96 | V    | —         | —           |
| VSS                      | Ground Supply <sup>1</sup>                           | -0.3 | —   | 0.3  | V    | —         | —           |
| VDD_STBY                 | Standby domain supply voltage <sup>1, 2</sup>        | -0.3 | —   | 0.96 | V    | —         | —           |
| VDD_LV_PLL_AUR           | Aurora PLL digital voltage supply <sup>1, 2</sup>    | -0.3 | —   | 0.96 | V    | —         | —           |
| VDD_LV_PLL_DDR0          | DDR0 PLL digital voltage supply <sup>1, 2</sup>      | -0.3 | —   | 0.96 | V    | —         | —           |
| VDD_VP_PCIE <sub>n</sub> | PCIE0/1 core voltage supply (n=0, 1) <sup>1, 2</sup> | -0.3 | —   | 0.96 | V    | —         | —           |
| VDD_FIRC                 | FIRC high voltage supply <sup>1, 3</sup>             | -0.3 | —   | 2.16 | V    | —         | —           |
| VDD_EFUSE                | EFUSE high voltage supply <sup>1, 3</sup>            | -0.3 | —   | 2.16 | V    | —         | —           |

*Table continues on the next page...*

**Table 4. Absolute Max Ratings (continued)**

| Symbol          | Description   | Min  | Typ | Max  | Unit | Condition                | Spec Number |
|-----------------|---|------|-----|------|------|--------------------------|-------------|
| VDD_IO_x        | GPIO 3.3V supply <sup>1, 4</sup>                    | -0.3 | —   | 4    | V    | —                        | —           |
| VDD_IO_A        | GPIO A 3.3V supply <sup>1, 4</sup>                  | -0.3 | —   | 4    | V    | —                        | —           |
| VDD_IO_B        | GPIO B 3.3V supply <sup>1, 4</sup>                  | -0.3 | —   | 4    | V    | —                        | —           |
| VDD_IO_GMAC0    | GMAC0 I/O voltage supply <sup>1, 4</sup>            | -0.3 | —   | 4    | V    | —                        | —           |
| VDD_IO_GMAC1    | GMAC1 I/O voltage supply <sup>1, 4</sup>            | -0.3 | —   | 4    | V    | —                        | —           |
| VDD_IO_QSPI     | QSPI A I/O voltage supply <sup>1, 3</sup>           | -0.3 | —   | 2.16 | V    | —                        | —           |
| VDD_IO_SDHC     | uSDHC / QSPI B I/O voltage supply <sup>1, 4</sup>   | -0.3 | —   | 4    | V    | —                        | —           |
| VDD_IO_CLKOUT   | CLKOUT 1.8V I/O supply <sup>1, 3</sup>              | -0.3 | —   | 2.16 | V    | —                        | —           |
| VDD_IO_AUR      | Aurora 1.8V I/O supply <sup>1, 3</sup>              | -0.3 | —   | 2.16 | V    | —                        | —           |
| VDD_IO_DDR0     | DDR0 I/O voltage supply <sup>1</sup>                | -0.3 | —   | 2.16 | V    | —                        | —           |
| VDD_IO_USB      | USB I/O voltage supply <sup>1, 4</sup>              | -0.3 | —   | 4    | V    | —                        | —           |
| VDD_IO_STBY     | Standby domain I/O voltage supply <sup>1, 4</sup>   | -0.3 | —   | 4    | V    | —                        | —           |
| VDD_VREF        | Supply detector high voltage supply <sup>1, 3</sup> | -0.3 | —   | 2.16 | V    | —                        | —           |
| VDD_ADC         | ADC voltage supply <sup>1, 3</sup>                  | -0.3 | —   | 2.16 | V    | Reference to VSS_<br>ADC | —           |
| VSS_ADC         | ADC ground supply <sup>1</sup>                      | -0.3 | —   | 0.3  | V    | Reference to VSS         | —           |
| VDD_HV_PLL      | PLL high voltage supply <sup>1, 3</sup>             | -0.3 | —   | 2.16 | V    | —                        | —           |
| VDD_HV_PLL_AUR  | Aurora PLL high voltage supply <sup>1, 3</sup>      | -0.3 | —   | 2.16 | V    | —                        | —           |
| VDD_HV_PLL_DDR0 | DDR PLL voltage supply <sup>1, 3</sup>              | -0.3 | —   | 2.16 | V    | —                        | —           |
| VDD_DDR0        | DDR0 high voltage supply <sup>1, 3</sup>            | -0.3 | —   | 2.16 | V    | DDR PHY PLL              | —           |

*Table continues on the next page...*

Table 4. Absolute Max Ratings (continued)

| Symbol                   | Description  | Min              | Typ | Max              | Unit | Condition              | Spec Number |
|--------------------------|--|------------------|-----|------------------|------|------------------------|-------------|
| VDD_FXOSC                | FXOSC high voltage supply <sup>1, 3</sup>                          | -0.3             | —   | 2.16             | V    | Reference to VSS_FXOSC | —           |
| VSS_FXOSC                | FXOSC ground supply <sup>1</sup>                                   | -0.3             | —   | 0.3              | V    | Reference to VSS       | —           |
| VEXTAL                   | FXOSC EXTAL input voltage range <sup>1, 3, 5</sup>                 | -0.3             | —   | 2.16             | V    | —                      | —           |
| VXTAL                    | FXOSC XTAL input voltage range <sup>1, 3, 5</sup>                  | -0.3             | —   | 2.16             | V    | —                      | —           |
| VDD_IO_PCIE <sub>n</sub> | PCIe0/1 high voltage supply (n=0, 1) <sup>1, 3</sup>               | -0.3             | —   | 2.16             | V    | —                      | —           |
| VDD_TMU                  | Thermal Monitoring Unit (TMU) high voltage supply <sup>1, 3</sup>  | -0.3             | —   | 2.16             | V    | —                      | —           |
| VREFH_ADC                | ADC reference high voltage <sup>1, 3</sup>                         | -0.3             | —   | 2.16             | V    | Reference to VREFL_ADC | —           |
| VREFL_ADC                | ADC reference low voltage <sup>1</sup>                             | -0.3             | —   | 0.3              | V    | Reference to VSS       | —           |
| VAD_INPUT                | ADC input voltage range <sup>1, 6, 7</sup>                         | VSS_AD<br>C -0.6 | —   | VDD_AD<br>C +0.5 | V    | —                      | —           |
| VIN                      | GPIO input voltage range <sup>1, 8, 9, 10</sup>                    | VSS - 0.3        | —   | VDD_IO_ * + 0.3  | V    | —                      | —           |
| IINJ_D                   | Maximum DC current injection digital I/O pin <sup>1, 11</sup>      | -3               | —   | 3                | mA   | —                      | —           |
| IINJ_A                   | Maximum DC current injection analog input pin <sup>1, 6, 12</sup>  | -1               | —   | 1                | mA   | —                      | —           |
| IINJ_LVDS                | Max LVDS RX or TX pin injection current <sup>1, 13</sup>           | 0                | —   | 100              | uA   | —                      | —           |
| IINJ_LVDS                | Max LVDS RX or TX pin injection current <sup>1</sup>               | 0                | —   | 100              | uA   | —                      | —           |
| IMAXSEG                  | Maximum RMS current per GPIO supply domain (VDD_IO_*) <sup>1</sup> | —                | —   | 140              | mA   | —                      | —           |
| TSTG                     | Storage temperature range <sup>1</sup>                             | -55              | —   | 150              | C    | —                      | —           |

Table continues on the next page...

Table 4. Absolute Max Ratings (continued)

| Symbol      | Description  | Min  | Typ | Max  | Unit | Condition  | Spec Number |
|-------------|--|------|-----|------|------|--|-------------|
| TSDR        | Maximum solder temperature <sup>1, 14</sup>            | —    | —   | 260  | C    | Pb free  | —           |
| MSL         | Moisture Sensitivity Level <sup>1, 15</sup>            | —    | —   | 3    | —    | —  | —           |
| V_OS_US_10  | Voltage at 10 % of t <sub>SIGNAL</sub> <sup>16</sup>   | -0.4 | —   | 3.7  | V    | 3.3V, See "SoC-pin overshoot/undershoot voltage for each GPIO pad type" figure below | —           |
| V_OS_US_7p5 | Voltage at 7.50 % of t <sub>SIGNAL</sub> <sup>16</sup> | -0.5 | —   | 3.8  | V    | 3.3V, See "SoC-pin overshoot/undershoot voltage for each GPIO pad type" figure below | —           |
| V_OS_US_2p5 | Voltage at 2.50 % of t <sub>SIGNAL</sub> <sup>16</sup> | -0.6 | —   | 3.9  | V    | 3.3V, See "SoC-pin overshoot/undershoot voltage for each GPIO pad type" figure below | —           |
| V_OS_US_1p6 | Voltage at 1.60 % of t <sub>SIGNAL</sub> <sup>16</sup> | -0.7 | —   | 4    | V    | 3.3V, See "SoC-pin overshoot/undershoot voltage for each GPIO pad type" figure below | —           |
| V_OS_US_10  | Voltage at 10 % of t <sub>SIGNAL</sub> <sup>17</sup>   | -0.7 | —   | 2.31 | V    | 1.8V, See "SoC-pin overshoot/undershoot voltage for each GPIO pad type" figure below | —           |

1. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device. See the operating conditions table for functional specifications.
2. Allowed 0.88V – 0.96V for 60 seconds cumulative over lifetime with no operating restrictions, 2.0 hours cumulative over lifetime with device in reset, at maximum T<sub>j</sub> = 125 °C
3. Allowed 1.92V - 2.16V for 60 seconds cumulative over lifetime with no operating restrictions, 2.6 hours cumulative over lifetime with device in reset, at maximum T<sub>j</sub> = 125 °C
4. Allowed 3.52V - 4.0V for 60 seconds cumulative over lifetime with no operating restrictions, 2.6 hours cumulative over lifetime with device in reset, at maximum T<sub>j</sub> = 125 °C
5. VEXTAL/ VXTAL (min) is for powered condition. VEXTAL/VXTAL (min) can be lower in unpowered condition.
6. Allowed for a cumulative duration of 50 hours operation over the lifetime of the device at maximum T<sub>j</sub>, with VDD\_ADC <= 1.92V, VSS\_ADC = 0V. Allowed for unlimited duration if the device is unpowered.
7. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage equals the supply plus the voltage drop across the internal ESD diode from I/O pin to supply.
8. Absolute maximum DC VIN levels for a powered device are 3.82V and 2.22V, for 3.3V and 1.8V domains, respectively. For powered devices when VIN ≥ VDD\_IO\*, VIN must simultaneously follow the constraint that VIN-VDD\_IO\* ≤ 0.3V for the DC case. For unpowered devices, the allowed VIN max level is +0.9V. Unpowered devices must simultaneously follow IINJ\_D unpowered current injection constraints.
9. Absolute minimum DC VIN level for a powered device is -0.3V. For unpowered devices, the allowed VIN min level is -0.9V. Unpowered devices must simultaneously follow IINJ\_D unpowered current injection constraints.
10. DC case limit. Overshoot/Undershoot beyond this range is allowed, but only for the limited durations as constrained by temporal percentages of t<sub>SIGNAL</sub>.
11. IINJ\_D specifications are per pin for an unpowered condition of the associated supply. The maximum simultaneous injection per supply is 30mA.

- 12. Non-disturb of ADC channels during current injection cannot be guaranteed. The degradation in channel performance cannot be specified due to the dynamic operation of the ADC input mux and potential for varying charge distribution. For the max +/-1mA DC injection quoted here, VAD\_INPUT would be +0.5/-0.6V relative to VREFH\_ADC/VREFL\_ADC at max Tj. ADC Output of the channel into which injection occurs will saturate depending on the direction of injection and for the channels not subject to current injection Offset error would be -12 LSB to 6 LSB and TUE would be -12 LSB to 8 LSB.
- 13. Applies exclusively to ZipWire and does not apply to Aurora. Allowed for a cumulative of 14 hours over the life of the part. The voltage on the RX or TX pin must not exceed 2.16 V at any time during the power-cycling or normal operation.
- 14. Solder profile per IPC/JEDEC J-STD-020D.
- 15. Moisture sensitivity per JEDEC test method A112.
- 16. For AC Signals in a 3.3V supply domain, if  $VDD\_IO \leq 3.3V$ , max VIN overshoot is limited to  $VDD\_IO+20\%$ . If  $VDD\_IO > 3.3V$ , then max VIN overshoot is limited to 4V.
- 17. For AC Signals in a 1.8V supply domain, max VIN overshoot is limited to  $VDD\_IO+20\%$  for 10% of tSIGNAL.

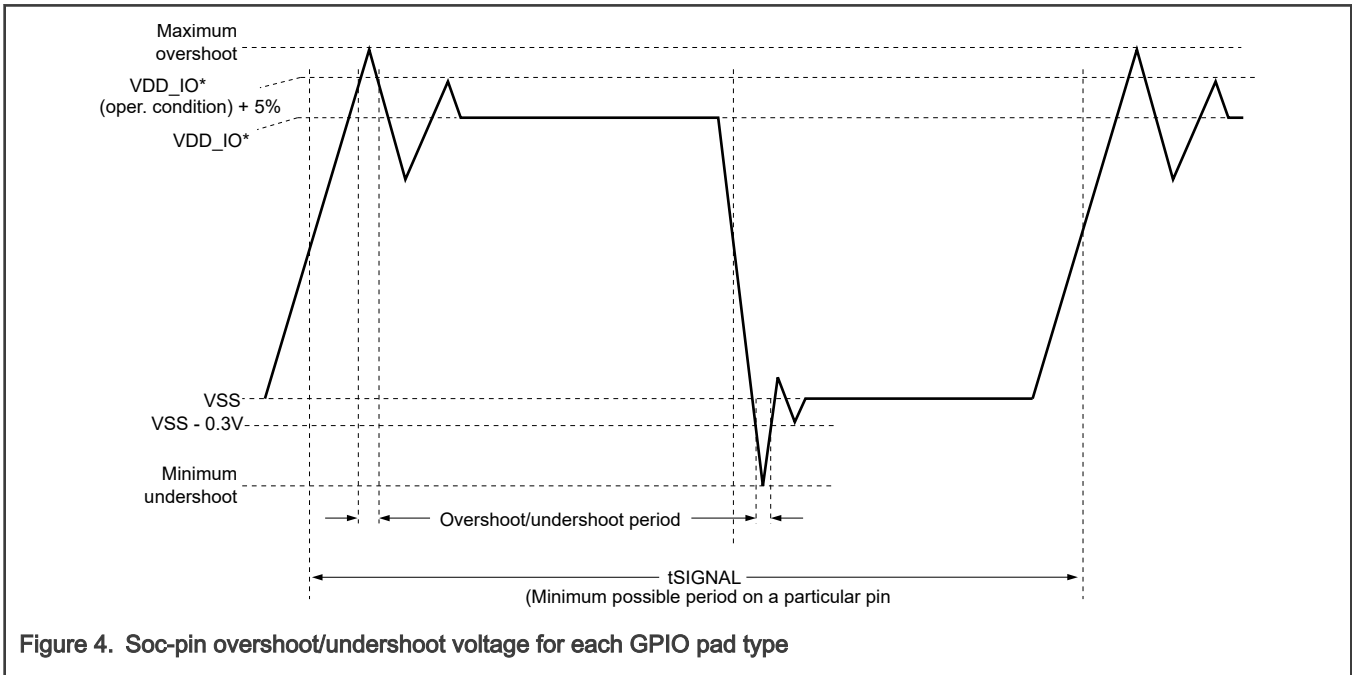


Figure 4. Soc-pin overshoot/undershoot voltage for each GPIO pad type

## 7 Operating conditions

### 7.1 Operating Conditions

The following table describes the functional operating conditions for the device, and for which all specifications in this datasheet are valid, except where explicitly noted. Device behavior is not guaranteed for operation outside of the conditions in this table.

**NOTE**

$\Delta VDD^*$  specifications are applicable to the supplies mentioned in the condition column when the device is not in standby mode. VDD\_IO\_B, VDD\_IO\_QSPI and VDD\_DDR0 may stay powered in standby mode as applicable to the group.

**NOTE**

All specifications associated with VIN are measured at the SoC pin.

**Table 5. Operating Conditions**

| Symbol          | Description   | Min  | Typ | Max  | Unit | Condition | Spec Number |
|-----------------|---|------|-----|------|------|-----------|-------------|
| fSYS_A53        | Cortex-A53 core operating frequency <sup>1, 2</sup> | —    | —   | 1311 | MHz  | —         | —           |
| fSYS_CM7        | Cortex-M7 core operating frequency <sup>1, 2</sup>  | —    | —   | 400  | MHz  | —         | —           |
| fSYS_PFE_PE     | PFE PE operating frequency <sup>1, 2</sup>          | —    | —   | 600  | MHz  | —         | —           |
| Tj              | Junction Temperature Range <sup>1, 3, 4</sup>       | -40  | —   | 125  | C    | —         | —           |
| Ta              | Ambient Temperature Range <sup>1, 4</sup>           | -40  | —   | 105  | C    | —         | —           |
| VDD             | Core voltage Supply <sup>1</sup>                    | 0.75 | 0.8 | 0.87 | V    | —         | —           |
| VSS             | Ground Supply <sup>1</sup>                          | —    | 0   | —    | V    | —         | —           |
| VDD_STBY        | Standby domain supply voltage <sup>1, 5</sup>       | 0.75 | 0.8 | 0.87 | V    | —         | —           |
| VDD_LV_PLL_AUR  | Aurora PLL digital voltage supply <sup>1</sup>      | 0.75 | 0.8 | 0.87 | V    | —         | —           |
| VDD_LV_PLL_DDR0 | DDR0 PLL digital voltage supply <sup>1</sup>        | 0.75 | 0.8 | 0.87 | V    | —         | —           |
| VDD_VP_PCIE0    | PCIE0/1 core voltage supply <sup>1, 6</sup>         | 0.75 | 0.8 | 0.87 | V    | —         | —           |
| VDD_IO_A        | GPIO A 3.3V supply <sup>1</sup>                     | 3.08 | 3.3 | 3.52 | V    | —         | —           |
| VDD_IO_B        | GPIO B 3.3V supply <sup>1, 7</sup>                  | 3.08 | 3.3 | 3.52 | V    | —         | —           |
| VDD_IO_GMAC0    | GMAC0 I/O voltage supply <sup>1</sup>               | 1.68 | 1.8 | 1.92 | V    | 1.8V      | —           |
| VDD_IO_GMAC0    | GMAC0 I/O voltage supply <sup>1</sup>               | 3.08 | 3.3 | 3.52 | V    | 3.3V      | —           |
| VDD_IO_GMAC1    | GMAC1 I/O voltage supply <sup>1</sup>               | 1.68 | 1.8 | 1.92 | V    | 1.8V      | —           |
| VDD_IO_GMAC1    | GMAC1 I/O voltage supply <sup>1</sup>               | 3.08 | 3.3 | 3.52 | V    | 3.3V      | —           |
| VDD_IO_QSPI     | QuadSPI A I/O voltage supply <sup>1, 8</sup>        | 1.68 | 1.8 | 1.92 | V    | 1.8V      | —           |

*Table continues on the next page...*

**Table 5. Operating Conditions (continued)**

| Symbol          | Description                                      | Min   | Typ  | Max  | Unit | Condition                  | Spec Number |
|-----------------|--|-------|------|------|------|----------------------------|-------------|
| VDD_IO_SDHC     | uSDHC / QSPI B I/O voltage supply <sup>1</sup>   | 1.68  | 1.8  | 1.92 | V    | 1.8V                       | —           |
| VDD_IO_SDHC     | uSDHC I/O voltage supply <sup>1</sup>            | 3.08  | 3.3  | 3.52 | V    | 3.3V                       | —           |
| VDD_IO_CLKOUT   | CLKOUT 1.8V I/O supply <sup>1</sup>              | 1.68  | 1.8  | 1.92 | V    | —                          | —           |
| VDD_IO_AUR      | Aurora 1.8V I/O supply <sup>1</sup>              | 1.68  | 1.8  | 1.92 | V    | Aurora LVDS Tx + ref clock | —           |
| VDD_IO_STBY     | Standby domain I/O voltage supply <sup>1,7</sup> | 3.08  | 3.3  | 3.52 | V    | —                          | —           |
| VDD_IO_USB      | USB I/O voltage supply <sup>1</sup>              | 1.68  | 1.8  | 1.92 | V    | 1.8V                       | —           |
| VDD_IO_USB      | USB I/O voltage supply <sup>1</sup>              | 3.08  | 3.3  | 3.52 | V    | 3.3V                       | —           |
| VDD_IO_DDR0     | DDR3L I/O voltage supply <sup>1</sup>            | 1.283 | 1.35 | 1.45 | V    | —                          | —           |
| VDD_IO_DDR0     | LPDDR4 I/O voltage supply <sup>1</sup>           | 1.06  | 1.1  | 1.17 | V    | —                          | —           |
| δVDD_IO_DDR0    | DDR3L I/O supply ripple voltage <sup>1</sup>     | -5    | —    | 5    | %    | —                          | —           |
| δVDD_IO_DDR0    | LPDDR4 I/O supply ripple voltage <sup>1</sup>    | -2.5  | —    | 2.5  | %    | —                          | —           |
| VDD_DDR0        | DDR0 high voltage supply <sup>1</sup>            | 1.68  | 1.8  | 1.92 | V    | —                          | —           |
| VDD_FIRC        | FIRC high voltage supply <sup>1</sup>            | 1.68  | 1.8  | 1.92 | V    | —                          | —           |
| VDD_VREF        | PMC high voltage supply <sup>1</sup>             | 1.68  | 1.8  | 1.92 | V    | —                          | —           |
| VDD_EFUSE       | EFUSE high voltage supply <sup>1,9,10,11</sup>   | 1.68  | 1.8  | 1.92 | V    | —                          | —           |
| VDD_ADC         | ADC high voltage supply <sup>1</sup>             | 1.68  | 1.8  | 1.92 | V    | —                          | —           |
| VDD_HV_PLL      | PLL high voltage supply <sup>1</sup>             | 1.68  | 1.8  | 1.92 | V    | —                          | —           |
| VDD_HV_PLL_AUR  | Aurora PLL high voltage supply <sup>1</sup>      | 1.68  | 1.8  | 1.92 | V    | —                          | —           |
| VDD_HV_PLL_DDR0 | DDR PLL voltage supply <sup>1</sup>              | 1.68  | 1.8  | 1.92 | V    | —                          | —           |

*Table continues on the next page...*

Table 5. Operating Conditions (continued)

| Symbol                   | Description   | Min       | Typ | Max            | Unit | Condition   | Spec Number |
|--------------------------|---|-----------|-----|----------------|------|---|-------------|
| $\delta$ VDD_HV_PLL_DDR0 | DDR PLL supply ripple voltage <sup>1</sup>                                    | -2.5      | —   | 2.5            | %    | —   | —           |
| VDD_FXOSC                | FXOSC high voltage supply <sup>1</sup>  | 1.68      | 1.8 | 1.92           | V    | —   | —           |
| VDD_IO_PCIEn             | PCIE0/1 high voltage supply <sup>1, 6</sup>                                   | 1.68      | 1.8 | 1.92           | V    | —   | —           |
| VDD_TMU                  | Thermal Monitoring Unit (TMU) high voltage supply <sup>1</sup>                | 1.68      | 1.8 | 1.92           | V    | —   | —           |
| VREFH_ADCn               | ADC reference high voltage (n=0, 1) <sup>1</sup>                              | 1.68      | 1.8 | 1.92           | V    | —   | —           |
| VIN_33                   | 3.3V GPIO input voltage range <sup>1, 12, 13, 14</sup>                        | VSS - 0.3 | —   | VDD_IO_* + 0.3 | V    | —   | —           |
| VIN_18                   | 1.8V GPIO input voltage range <sup>1, 12, 13, 14</sup>                        | VSS - 0.3 | —   | VDD_IO_* + 0.3 | V    | —   | —           |
| $\Delta$ VDD             | 0.8V supply voltage differential <sup>1, 15</sup>                             | -25       | —   | 25             | mV   | Applies to all 0.8V supplies on the device.   | —           |
| $\Delta$ VDD_HV_18_IO    | 1.8V I/O supply voltage differential group <sup>1, 15</sup>                   | -25       | —   | 25             | mV   | Applies to VDD_IO_QSPI, VDD_IO_SDHC, VDD_IO_GMAC0, VDD_IO_GMAC1, VDD_IO_USB   | —           |
| $\Delta$ VDD_HV_18_ANA   | 1.8V analog supply voltage differential group <sup>1, 9, 10, 11, 15, 16</sup> | -25       | —   | 25             | mV   | Applies to VDD_IO_CLKOUT, VDD_IO_AUR, VDD_TMU, VREFH_ADC*, VDD_ADC, VDD_HV_PLL*, VDD_VREF, VDD_FXOSC, VDD_FIRC, VDD_EFUSE, VDD_DDR0, VDD_IO_PCIE0, VDD_IO_PCIE1 | —           |
| $\Delta$ VDD_HV_33_IO    | 3.3V I/O supply voltage differential group <sup>1, 15</sup>                   | -25       | —   | 25             | mV   | VDD_IO_A, VDD_IO_B  | —           |
| $\Delta$ VSS_HV_18       | 1.8V supply ground voltage differential <sup>1, 15</sup>                      | -25       | —   | 25             | mV   | Applies to VSS, VREFL_ADCn, VSS_ADC, VSS_FXOSC  | —           |

Table continues on the next page...



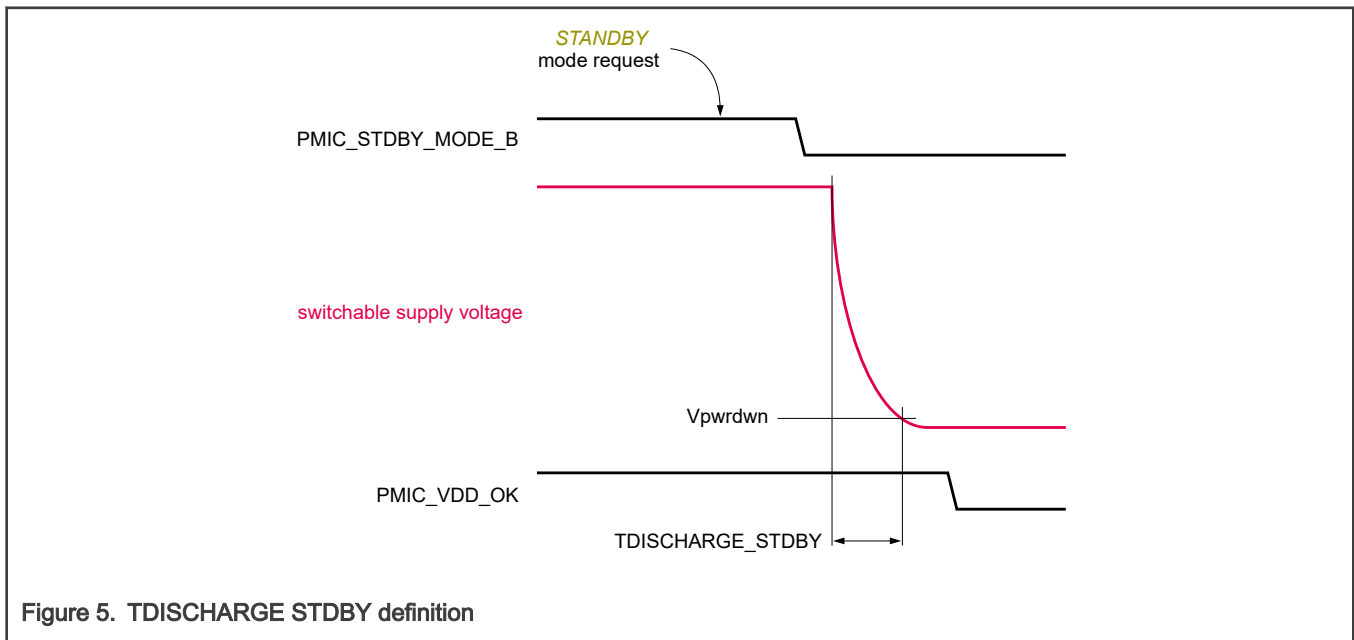
Table 5. Operating Conditions (continued)

| Symbol           | Description  | Min                | Typ | Max                | Unit   | Condition  | Spec Number |
|------------------|--|--------------------|-----|--------------------|--------|--|-------------|
| VRAMP_LV         | LV supply voltage ramp-up rate <sup>1, 17</sup>              | 0.001              | —   | 24                 | V / ms | Applies to 0.8V supplies                                     | —           |
| VRAMP_HV         | HV supply voltage ramp-up rate <sup>1</sup>                  | 0.001              | —   | 24                 | V / ms | Applies to 1.8V supplies and DDR I/O supplies.               | —           |
| VRAMP_HV_33_IO   | 3.3V I/O supply voltage ramp-up rate <sup>1</sup>            | 0.001              | —   | 50                 | V / ms | Applies to 3.3V I/O supplies.                                | —           |
| TDISCHARGE_STDBY | Supply discharge time during Standby mode entry <sup>1</sup> | 100                | —   | —                  | us     | Applies to all switchable supplies during Standby mode entry | —           |
| VAD_INPUT        | ADC input voltage range <sup>1, 18</sup>                     | VSS_AD<br>C - 0.35 | —   | VDD_AD<br>C + 0.25 | V      | —  | —           |
| IINJ_D           | GPIO Input DC Injection Current <sup>1, 19</sup>             | -3                 | —   | 3                  | mA     | Unpowered  | —           |
| IINJ_D           | GPIO Input DC Injection Current <sup>1, 20</sup>             | 0                  | —   | 5                  | uA     | Powered  | —           |
| IINJ_A           | SAR ADC Input DC Injection Current <sup>1, 21</sup>          | -20                | —   | 20                 | uA     | —  | —           |
| IMAXSEG          | Maximum RMS current per GPIO supply domain <sup>1</sup>      | —                  | —   | 120                | mA     | —  | —           |

- The operating conditions in this table apply as required conditions for all other specifications in this document, unless explicitly noted as an exception in another section of this document.
- The stated maximum operating frequency must be observed when using the PLL with frequency modulation enabled. Center-spread modulation is supported in cases where the nominal operating frequency plus half the modulation depth is less than the stated maximum frequency.
- Lifetime operation at T<sub>j</sub> max not guaranteed. Standard automotive temperature profile assumed for performance and reliability guarantees.
- The junction temperature (T<sub>j</sub>) range specification cannot be violated. The ambient temperature shown in the table, is a rough indicative value, for a typical system. Customers must ensure there is an appropriate thermal solution in their system to keep T<sub>j</sub> within the spec range
- The operating voltage range applies when the device is not in standby mode.
- Both PCIe supplies must ramp for the SerDes PHY to safely power up into its reset state. Until both supplies are ramped, the SerDes PHY will be in an undefined state.
- A minimum of 2.91V is supported on this supply when the device is in low-power standby mode if it is kept powered during this mode.
- The device supports QSPI interface to 3.3V memories on the QSPI B bank, which is multiplexed with uSDHC functions on the VDD\_IO\_SDHC supply. QSPI A signals on VDD\_IO\_QSPI are limited to 1.8V.
- The VDD\_EFUSE supply must be maintained within specification during fuse programming. Failure to do this may result in improper functionality of the device after fuse programming.
- Refer to the Power Sequencing section for the relationship of VDD\_EFUSE powering up/down relative to the core, high-voltage, and I/O supplies.
- VDD\_EFUSE must be grounded when not actively programming the fuses. This supply is not required to be powered for fuse reads. See device hardware design guidelines document for more details.

12. For AC signals, allowed max  $V_{IN} \leq VDD\_IO^*$  for lifetime operation. If AC overshoot beyond  $VDD\_IO^*$  occurs, then refer to the Abs Max duration constraints as a function of the amount of overshoot. For DC signals  $\geq VDD\_IO$ ,  $V_{IN}-VDD\_IO^* \leq 0.3V$  is allowed for lifetime operation.
13. The min DC  $V_{IN}$  level for a powered device is  $-0.3V$ . If AC undershoot below  $-0.3V$  occurs, then refer to the Abs Max duration constraints as a function of the amount of undershoot.
14. DC case limit. Overshoot/Undershoot beyond this range is allowed, but only for the limited durations as constrained by temporal percentages of t SIGNAL.
15. The "voltage differential" refers to the difference between the lowest and highest voltages across all supplies within the supply group as defined under Condition column.
16. VREFH\_ADCn allows a differential voltage of  $\pm 100mV$ .
17. On slow ramps, the RESET\_B pin may be observed to be asserted multiple times during the supply ramping. In order to prevent these pulses from being propagated into the system, it is recommended that the PMIC drives RESET\_B low during supply ramp or whenever POR\_B is asserted.
18. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage equals the supply plus the voltage drop across the internal ESD diode from I/O pin to supply.
19. IINJ\_D specifications are per pin for an unpowered condition of the associated supply. The maximum simultaneous injection per supply is 30mA.
20. You must ensure that neither IINJ nor VIN specs are violated. Negligible DC injection currents are expected to flow during normal powered operation.
21. The SAR ADC electrical specifications are not guaranteed during any period when the operating injection current limit is violated. These specifications are at maximum  $T_j$  and  $VREFH\_ADC=1.8V$ ; the injected current will reduce with reduced  $T_j$ .

The device hardware design guidelines document summarizes mandatory board design rules in table "Decaps and Ferrite Bead requirement" and section "PDN (Power Delivery Network) Guidelines".



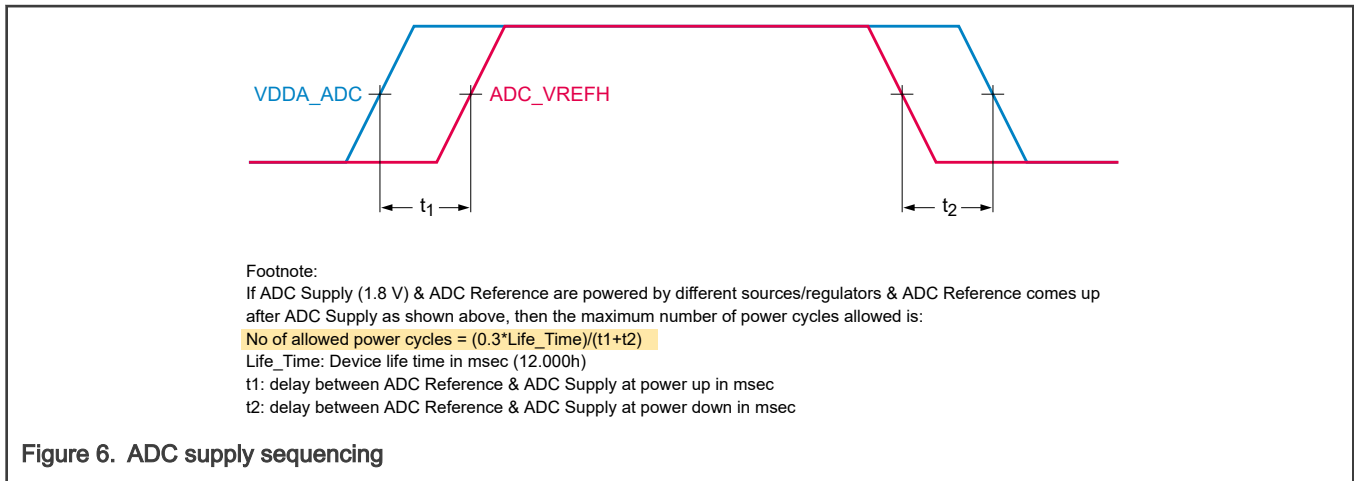


Figure 6. ADC supply sequencing

## 7.2 Clock frequency ranges

The following table gives the frequency range minimum and maximums to use when programming the clock dividers on the device.

Table 6. Clock frequency ranges

| Symbol              | Description                           | Min | Typ | Max   | Unit | Condition          | Spec Number |
|---------------------|---------------------------------------|-----|-----|-------|------|--------------------|-------------|
| fA53_CORE_DIV2_CLK  | Cortex-A53 core div2 clock frequency  | 24  | —   | 655.5 | MHz  | A53_CORE_DIV2_CLK  | —           |
| fA53_CORE_DIV10_CLK | Cortex-A53 core div10 clock frequency | 4.8 | —   | 131.1 | MHz  | A53_CORE_DIV10_CLK | —           |
| fLBIST_CLK          | LBIST[7:0] clock frequency            | —   | —   | 50    | MHz  | LBIST_CLK[7:0]     | —           |
| fXBAR_CLK           | XBAR clock frequency                  | 24  | —   | 400   | MHz  | XBAR_CLK           | —           |
| fXBAR_2X_CLK        | XBAR 2X clock frequency               | 48  | —   | 800   | MHz  | XBAR_2X_CLK        | —           |
| fXBAR_DIV2_CLK      | XBAR div2 clock frequency             | 12  | —   | 200   | MHz  | XBAR_DIV2_CLK      | —           |
| fXBAR_DIV3_CLK      | XBAR div3 clock frequency             | 8   | —   | 133   | MHz  | XBAR_DIV3_CLK      | —           |
| fXBAR_DIV4_CLK      | XBAR div4 clock frequency             | 6   | —   | 100   | MHz  | XBAR_DIV4_CLK      | —           |
| fXBAR_DIV6_CLK      | XBAR div6 clock frequency             | 4   | —   | 66.7  | MHz  | XBAR_DIV6_CLK      | —           |
| fDAPB_CLK           | Debug clock frequency                 | —   | —   | 133   | MHz  | fDAPB_CLK          | —           |
| fFRAY_CHI           | FlexRay CHI clock frequency           | —   | —   | 133   | MHz  | —                  | —           |

Table continues on the next page...

Table 6. Clock frequency ranges (continued)

| Symbol             | Description                          | Min | Typ | Max   | Unit | Condition         | Spec Number |
|--------------------|--------------------------------------|-----|-----|-------|------|-------------------|-------------|
| fSERDES_REF_CLK    | SERDES reference clock frequency     | 100 | —   | 125   | MHz  | SERDES_REF_CLK    | —           |
| fPER_CLK           | Peripheral clock frequency           | —   | —   | 80    | MHz  | PER_CLK           | —           |
| fFTM_0_REF_CLK     | FlexTimer 0 external clock frequency | —   | —   | 20    | MHz  | FTM_0_REF_CLK     | —           |
| fFTM_1_REF_CLK     | FlexTimer 1 external clock frequency | —   | —   | 20    | MHz  | FTM_1_REF_CLK     | —           |
| fFLEXRAY_PE_CLK    | FlexRay PE clock frequency           | —   | —   | 40    | MHz  | FLEXRAY_PE_CLK    | —           |
| fCAN_PE_CLK        | CAN PE clock frequency               | 40  | —   | 80    | MHz  | CAN_PE_CLK        | —           |
| fLIN_BAUD_CLK      | LIN baud clock frequency             | —   | —   | 133   | MHz  | LIN_BAUD_CLK      | —           |
| fLINFLEXD_CLK      | LIN clock frequency                  | —   | —   | 66.7  | MHz  | LINFLEXD_CLK      | —           |
| fGMAC_TS_CLK       | GMAC timestamp clock frequency       | 5   | —   | 200   | MHz  | GMAC_TS_CLK       | —           |
| fGMAC_0_TX_CLK     | GMAC_0 transmit clock frequency      | 2.5 | —   | 125   | MHz  | GMAC_0_TX_CLK     | —           |
| fGMAC_0_RX_CLK     | GMAC_0 receive clock frequency       | 2.5 | —   | 125   | MHz  | GMAC_0_RX_CLK     | —           |
| fGMAC_0_REF_CLK    | GMAC_0 reference clock frequency     | —   | —   | 50    | MHz  | GMAC_0_REF_CLK    | —           |
| fPFE_MAC_0_TX_CLK  | PFE MAC_0 transmit clock frequency   | 2.5 | —   | 312.5 | MHz  | PFE_MAC_0_TX_CLK  | —           |
| fPFE_MAC_0_RX_CLK  | PFE MAC_0 receive clock frequency    | 2.5 | —   | 312.5 | MHz  | PFE_MAC_0_RX_CLK  | —           |
| fPFE_MAC_0_REF_CLK | PFE MAC_0 reference clock frequency  | —   | —   | 50    | MHz  | PFE_MAC_0_REF_CLK | —           |
| fPFE_MAC_1_TX_CLK  | PFE MAC_1 transmit clock frequency   | 2.5 | —   | 312.5 | MHz  | PFE_MAC_1_TX_CLK  | —           |
| fPFE_MAC_1_RX_CLK  | PFE MAC_1 receive clock frequency    | 2.5 | —   | 312.5 | MHz  | PFE_MAC_1_RX_CLK  | —           |

*Table continues on the next page...*

Table 6. Clock frequency ranges (continued)

| Symbol             | Description                         | Min | Typ | Max   | Unit | Condition                      | Spec Number |
|--------------------|-------------------------------------|-----|-----|-------|------|--------------------------------|-------------|
| fPFE_MAC_1_REF_CLK | PFE MAC_1 reference clock frequency | —   | —   | 50    | MHz  | PFE_MAC_1_REF_CLK              | —           |
| fPFE_MAC_2_TX_CLK  | PFE MAC_2 transmit clock frequency  | 2.5 | —   | 312.5 | MHz  | PFE_MAC_2_TX_CLK               | —           |
| fPFE_MAC_2_RX_CLK  | PFE MAC_2 receive clock frequency   | 2.5 | —   | 312.5 | MHz  | PFE_MAC_2_RX_CLK               | —           |
| fPFE_MAC_2_REF_CLK | PFE MAC_2 reference clock frequency | —   | —   | 50    | MHz  | PFE_MAC_2_REF_CLK              | —           |
| fSPI_CLK           | SPI clock frequency                 | 10  | —   | 100   | MHz  | SPI_CLK                        | —           |
| fQSPI_2X_CLK       | QSPI 2X clock frequency             | —   | —   | 400   | MHz  | QSPI_2X_CLK - DDR 200MHz       | —           |
| fQSPI_2X_CLK       | QSPI 2X clock frequency             | —   | —   | 333   | MHz  | QSPI_2X_CLK - DDR 166MHz       | —           |
| fQSPI_2X_CLK       | QSPI 2X clock frequency             | —   | —   | 266   | MHz  | QSPI_2X_CLK - DDR / SDR 133MHz | —           |
| fQSPI_2X_CLK       | QSPI 2X clock frequency             | —   | —   | 208   | MHz  | QSPI_2X_CLK - SDR 104MHz       | —           |
| fQSPI_2X_CLK       | QSPI 2X clock frequency             | —   | —   | 200   | MHz  | QSPI_2X_CLK - SDR 100MHz       | —           |
| fQSPI_2X_CLK       | QSPI 2X clock frequency             | —   | —   | 133   | MHz  | QSPI_2X_CLK - DDR 66MHz        | —           |
| fQSPI_1X_CLK       | QSPI 1X clock frequency             | —   | —   | 200   | MHz  | QSPI_1X_CLK - DDR 200MHz       | —           |
| fQSPI_1X_CLK       | QSPI 1X clock frequency             | —   | —   | 166   | MHz  | QSPI_1X_CLK - DDR 166MHz       | —           |
| fQSPI_1X_CLK       | QSPI 1X clock frequency             | —   | —   | 133   | MHz  | QSPI_1X_CLK - DDR / SDR 133MHz | —           |
| fQSPI_1X_CLK       | QSPI 1X clock frequency             | —   | —   | 104   | MHz  | QSPI_1X_CLK - SDR 104MHz       | —           |
| fQSPI_1X_CLK       | QSPI 1X clock frequency             | —   | —   | 100   | MHz  | QSPI_1X_CLK - SDR 100MHz       | —           |
| fQSPI_1X_CLK       | QSPI 1X clock frequency             | —   | —   | 66    | MHz  | QSPI_1X_CLK - DDR 66MHz        | —           |
| fSDHC_CLK          | uSDHC clock frequency               | —   | —   | 200   | MHz  | SDHC_CLK - DDR HS400           | —           |

Table continues on the next page...

**Table 6. Clock frequency ranges (continued)**

| Symbol       | Description                | Min | Typ | Max | Unit | Condition                  | Spec Number |
|--------------|----------------------------|-----|-----|-----|------|----------------------------|-------------|
| fSDHC_CLK    | uSDHC clock frequency      | 133 | —   | 200 | MHz  | SDHC_CLK - DDR HS400       | —           |
| fSDHC_CLK    | uSDHC clock frequency      | —   | —   | 200 | MHz  | SDHC_CLK - SDR HS200       | —           |
| fSDHC_CLK    | uSDHC clock frequency      | —   | —   | 100 | MHz  | SDHC_CLK - SDR 100MHz      | —           |
| fSDHC_CLK    | uSDHC clock frequency      | —   | —   | 52  | MHz  | SDHC_CLK - DDR / SDR 52MHz | —           |
| fPFE_PE_CLK  | PFE PE clock frequency     | —   | —   | 600 | MHz  | PFE_PE_CLK                 | —           |
| fPFE_SYS_CLK | PFE system clock frequency | —   | —   | 300 | MHz  | PFE_SYS_CLK                | —           |

## 8 Thermal Characteristics

Thermal characteristics are targets based on simulation from preliminary die and package definitions. The specified characteristics are subject to change per final device design and characterization. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

**Table 7. Thermal Resistance**

| Board type <sup>1</sup> | Symbol           | Description   | Value | Unit |
|-------------------------|------------------|---|-------|------|
| JESD51-9, 2s2p          | R <sub>θJA</sub> | Junction to ambient Thermal Resistance              | 15.6  | °C/W |
| JESD51-9, 2s2p          | Ψ <sub>JT</sub>  | Junction to Lid Top Thermal Resistance <sup>2</sup> | 0.3   | °C/W |
| NA                      | R <sub>θJC</sub> | Junction to Case Thermal Resistance <sup>3</sup>    | 0.4   | °C/W |

1. Thermal test board meets JEDEC specification for this package (JESD51-9).
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
3. Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers to the lid surface temperature.

## 9 DC electricals

### 9.1 Total power specifications for 0.8V and 1.8V Analog Domains

The following table contains the individual max and thermal 0.8V power figures for each device in the S32G3 family as well as a 1.8V analog total which applies to all devices. For I/O power specifications please see dedicated I/O table.

Table 8. Total power specifications for 0.8V and 1.8V Analog Domains

| Symbol | Description   | Min | Typ | Max  | Unit | Condition   | Spec Number |
|--------|---|-----|-----|------|------|---|-------------|
| —      | 0.8V Supply Rail<br>Power: S32G399A<br>Max Usecase <sup>1</sup>       | —   | —   | 8.62 | W    | Tj=125C, All 0.8v supplies at 0.8V, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR | —           |
| —      | 0.8V Supply Rail<br>Power: S32G399A<br>Thermal Usecase <sup>2</sup>   | —   | —   | 8.41 | W    | Tj=125C, All 0.8v supplies at 0.8V, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR | —           |
| —      | 0.8V Supply Rail<br>Power: S32G398A<br>Max Usecase <sup>1,3</sup>     | —   | —   | 8.56 | W    | Tj=125C, All 0.8v supplies at 0.8V, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR | —           |
| —      | 0.8V Supply Rail<br>Power: S32G398A<br>Thermal Usecase <sup>2,3</sup> | —   | —   | 8.35 | W    | Tj=125C, All 0.8v supplies at 0.8V, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR | —           |
| —      | 0.8V Supply Rail<br>Power: S32G379A<br>Max Usecase <sup>1,3</sup>     | —   | —   | 8.28 | W    | Tj=125C, All 0.8v supplies at 0.8V, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR | —           |
| —      | 0.8V Supply Rail<br>Power: S32G379A<br>Thermal Usecase <sup>2,3</sup> | —   | —   | 8.08 | W    | Tj=125C, All 0.8v supplies at 0.8V, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR | —           |
| —      | 0.8V Supply Rail<br>Power: S32G378A<br>Max Usecase <sup>1,3</sup>     | —   | —   | 8.22 | W    | Tj=125C, All 0.8v supplies at 0.8V, Sum of VDD,   | —           |

Table continues on the next page...

Table 8. Total power specifications for 0.8V and 1.8V Analog Domains (continued)

| Symbol | Description   | Min | Typ | Max   | Unit | Condition   | Spec Number |
|--------|---|-----|-----|-------|------|---|-------------|
|        |   |     |     |       |      | VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR   |             |
| —      | 0.8V Supply Rail Power: S32G378A Thermal Usecase <sup>2,3</sup> | —   | —   | 8.02  | W    | Tj=125C, All 0.8v supplies at 0.8V, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR   | —           |
| —      | 1.8V Analog Supply Rail power: All devices <sup>4</sup>         | —   | —   | 0.135 | W    | Tj=125C, All 1.8V supplies at 1.8V, Sum of VDD_FXOSC, VDD_HV_PLL_AUR, VDD_HV_PLL_DDR0, VDD_ADC, VREFH_ADC0/1, VDD_FIRC, VDD_VREF, VDD_HV_PLL, VDD_TMU, VDD_DDR0 | —           |

1. Max usecase: This is provided for power supply design. It is the realistic peak power consumption in an application. Shall only be maintained for a very short time (approx. 100us).
2. Thermal usecase: This is provided for designing a thermal solution. This is a realistic maximum sustained usecase which would be maintained for a longer duration.
3. Note that during Self Test execution, the power consumption for this device could exceed the stated spec. The S32G399A device Max Usecase spec will apply for the duration of the self test.
4. 1.8V total does not include additional consumption during a fuse programming operation. See IDD\_EFUSE\_PGM spec for max additional current.

## 9.2 Static power specifications for I/O Domains

The following table contains the static power consumption for each I/O power domain. This data does not include the usage dependent dynamic current of GPIO-pins. To estimate the dynamic GPIO current for a specific use-case, an IO calculator tool is available. For IO calculator, contact your NXP sales representative. The " Device Power and Operating Current Specifications" table contains pre-calculated total I/O power (static + dynamic) for common usecases.

Table 9. Static power specifications for I/O Domains

| Symbol        | Description                      | Min | Typ | Max | Unit | Condition          | Spec Number |
|---------------|----------------------------------|-----|-----|-----|------|--------------------|-------------|
| SPVDD_IO_A    | 3.3V Static Power on VDD_IO_A    | —   | —   | 2.6 | mW   | VDD_IO_A = 3.3V    | —           |
| SPVDD_IO_B    | 3.3V Static Power on VDD_IO_B    | —   | —   | 2.2 | mW   | VDD_IO_B = 3.3V    | —           |
| SPVDD_IO_STBY | 3.3V Static Power on VDD_IO_STBY | —   | —   | 3.1 | mW   | VDD_IO_STBY = 3.3V | —           |

*Table continues on the next page...*



Table 9. Static power specifications for I/O Domains (continued)

| Symbol          | Description                              | Min | Typ | Max   | Unit | Condition            | Spec Number |
|-----------------|--|-----|-----|-------|------|----------------------|-------------|
| SPVDD_IO_SDHC   | 3.3V Static Power on VDD_IO_SDHC         | —   | —   | 159   | mW   | VDD_IO_SDHC = 3.3V   | —           |
| SPVDD_IO_SDHC   | 1.8V Static Power on VDD_IO_SDHC         | —   | —   | 12.1  | mW   | VDD_IO_SDHC = 1.8V   | —           |
| SPVDD_IO_GMAC0  | 3.3V Static Power on VDD_IO_GMAC0        | —   | —   | 150.5 | mW   | VDD_IO_GMAC0 = 3.3V  | —           |
| SPVDD_IO_GMAC0  | 1.8V Static Power on VDD_IO_GMAC0        | —   | —   | 11.4  | mW   | VDD_IO_GMAC0 = 1.8V  | —           |
| SPVDD_IO_GMAC1  | 3.3V Static Power on VDD_IO_GMAC1        | —   | —   | 151.5 | mW   | VDD_IO_GMAC1 = 3.3V  | —           |
| SPVDD_IO_GMAC1  | 1.8V Static Power on VDD_IO_GMAC1        | —   | —   | 11.5  | mW   | VDD_IO_GMAC1 = 1.8V  | —           |
| SPVDD_IO_USB    | 3.3V Static Power on VDD_IO_USB          | —   | —   | 152.6 | mW   | VDD_IO_USB = 3.3V    | —           |
| SPVDD_IO_USB    | 1.8V Static Power on VDD_IO_USB          | —   | —   | 11.4  | mW   | VDD_IO_USB = 1.8V    | —           |
| SPVDD_IO_QSPI   | 1.8V Static Power on VDD_IO_QSPI         | —   | —   | 0.5   | mW   | VDD_IO_QSPI = 1.8V   | —           |
| SPVDD_IO_CLKOUT | 1.8V Static Power on VDD_IO_CLKOUT       | —   | —   | 0.7   | mW   | VDD_IO_CLKOUT = 1.8V | —           |
| SPVDD_IO_PCIE0  | 1.8V Static Power on VDD_IO_PCIE0        | —   | —   | 2.8   | mW   | VDD_IO_PCIE0 = 1.8V  | —           |
| SPVDD_IO_PCIE1  | 1.8V Static Power on VDD_IO_PCIE1        | —   | —   | 2.8   | mW   | VDD_IO_PCIE1 = 1.8V  | —           |
| SPVDD_IO_AUR    | 1.8V Static Power on VDD_IO_AUR          | —   | —   | 0.8   | mW   | VDD_IO_AUR = 1.8V    | —           |
| SPVDD_IO_DDR    | 1.1V Static Power on VDD_IO_DDR - LPDDR4 | —   | —   | 2.4   | mW   | VDD_IO_DDR = 1.1V    | —           |
| SPVDD_IO_DDR    | 1.35V Static Power on VDD_IO_DDR - DDR3L | —   | —   | 2.8   | mW   | VDD_IO_DDR = 1.35V   | —           |

### 9.3 Device Power and Operating Current Specifications

The device power consumption, operating current, and applicable conditions are given in the following table.

**NOTE**

All measurements are at T<sub>j</sub>=125C, unless otherwise specified.

Table 10. Device Power and Operating Current Specifications

| Symbol          | Description  | Min | Typ | Max | Unit | Condition  | Spec Number |
|-----------------|--|-----|-----|-----|------|--|-------------|
| PVDD_STBY       | Standby mode core supply power                             | —   | 58  | —   | uW   | Ta = 25C, VDD_STBY = 0.8V, typical silicon, all pull up/down disabled    | —           |
| PVDD_IO_STBY    | Standby mode I/O supply power <sup>1</sup>                 | —   | 110 | —   | uW   | Ta = 25C, VDD_IO_STBY = 3.0V, typical silicon, all pull up/down disabled | —           |
| IDD_FXOSC       | VDD_FXOSC operating current                                | —   | 0.6 | —   | mA   | 1.8V, 40MHz  | —           |
| IDD_HV_PLL_AUR  | VDD_HV_PLL_AUR operating current                           | —   | 4.3 | —   | mA   | 1.8V, fPLL_VCO = 5GHz  | —           |
| IDD_HV_PLL_DDR0 | VDD_HV_PLL_DDR0 operating current (DDR reference PLL only) | —   | 2   | —   | mA   | fPLL_DDR_PHI0 = 800MHz, fDDR_PLL = 1600MHz, 1.8V                         | —           |
| IDD_ADC         | VDD_ADC operating current                                  | —   | 1.8 | —   | mA   | 1.8V, 2 ADCs @ 1Msps   | —           |
| IDD_ADC         | VDD_ADC operating current                                  | —   | 200 | —   | uA   | 1.8V, Disabled (per ADC)   | —           |
| IVREFH_ADC      | VREFH_ADC operating current                                | —   | 210 | —   | uA   | VREFH_ADC = 1.8V   | —           |
| IDD_FIRC        | VDD_FIRC operating current                                 | —   | 0.6 | —   | mA   | FIRC trimmed frequency (48MHz typical)                                   | —           |
| IDD_VREF        | VDD_VREF operating current                                 | —   | 0.7 | —   | mA   | 1.8V   | —           |
| IDD_HV_PLL      | VDD_HV_PLL operating current                               | —   | 8.9 | —   | mA   | 1.8V, fPLL_VCO = 2GHz, Core / Peripheral/Accelerator PLLs                | —           |
| IDD_EFUSE_PGM   | VDD_EFUSE programming current                              | —   | —   | 140 | mA   | VDD_EFUSE=1.8V, VDD=0.8V   | —           |
| IDD_TMU         | VDD_TMU operating current                                  | —   | 4.6 | —   | mA   | 1.8V, central unit and remote sensors operating                          | —           |
| IDD_DDR0        | VDD_DDR0 operating current                                 | —   | 5.0 | —   | mA   | 1.8V, fPLL_DDR_PHI0 = 800MHz, fDDR_PLL = 1600MHz                         | —           |
| PVDD_IO_PCIEn   | VDD_IO_PCIE0 operating power <sup>2</sup>                  | —   | —   | 76  | mW   | All circuits enabled, VDD_IO_PCIEn=1.8V,                                 | —           |

Table continues on the next page...

Table 10. Device Power and Operating Current Specifications (continued)

| Symbol           | Description                               | Min | Typ   | Max | Unit | Condition   | Spec Number |
|------------------|---|-----|-------|-----|------|---|-------------|
|                  |   |     |       |     |      | Gen3 8Gbps, 2 lanes.<br>Per IP instance   |             |
| PVDD_IO_PCIEn    | VDD_IO_PCIE0 operating power              | —   | —     | 72  | mW   | All circuits enabled, VDD_IO_PCIEn=1.8V, Gen2.1 5Gbps, 2 lanes. Per IP instance   | —           |
| PVDD_IO_PCIEn    | VDD_IO_PCIE0 operating power              | —   | —     | 68  | mW   | All circuits enabled, VDD_IO_PCIEn=1.8V, Gen1.1 2.5Gbps, 2 lanes. Per IP instance   | —           |
| PVDD_IO_PCIEn    | VDD_IO_PCIE0 operating power              | —   | —     | 1.5 | mW   | Powered down state, VDD_IO_PCIEn=1.8V, Per IP instance  | —           |
| PVDD_IO_DDR      | VDD_IO_DDR 100% write operating power     | —   | —     | 625 | mW   | LPDDR4, VDD_IO_DDR = 1.1V, 3200 MT/s, 100% write, 1/2 data lines switching, 60 Ohm transmit termination driving a 60 Ohm load           | —           |
| PVDD_IO_DDR_IDLE | VDD_IO_DDR idle power                     | —   | 55    | —   | mW   | LPDDR4, VDD_IO_DDR = 1.1V, Tj = 25C   | —           |
| PVDD_IO_DDR_RET  | VDD_IO_DDR data retention power           | —   | 0.02  | —   | mW   | LPDDR4, VDD_IO_DDR = 1.1V, Standby mode and DRAM in self-refresh, Tj=25C.   | —           |
| PVDD_IO_DDR_RET  | VDD_IO_DDR data retention power           | —   | 0.030 | —   | mW   | DDR3L, VDD_IO_DDR = 1.35V, Standby mode and DRAM in self-refresh, Tj=25C.   | —           |
| PVDD_IO_DDR      | VDD_IO_DDR 100% write operating power     | —   | —     | 598 | mW   | DDR3L, VDD_IO_DDR = 1.35V, 1600 MT/s, 100% Write operation, 1/2 data lines switching, 60 Ohm transmit termination driving a 60 ohm load | —           |
| PVDD_IO_DDR_IDLE | VDD_IO_DDR idle power                     | —   | 57    | —   | mW   | DDR3L, VDD_IO_DDR = 1.35V, Tj=25C   | —           |
| PVDD_IO_QSPI     | QSPI A I/O voltage supply operating power | —   | 58    | —   | mW   | 1.8V, 200MHz - clocks 100% activity rate, 50% data rate, 1/2 data switching per cycle,  | —           |

Table continues on the next page...

Table 10. Device Power and Operating Current Specifications (continued)

| Symbol          | Description                            | Min | Typ | Max | Unit | Condition  | Spec Number |
|-----------------|--|-----|-----|-----|------|--|-------------|
|                 |  |     |     |     |      | does not include power for other I/O ins on the VDD_IO_QSPI supply. 15.5pF.  |             |
| PVDD_IO_SDHC    | VDD_IO_SDHC operating power            | —   | 128 | —   | mW   | 1.8V, HS400, SD_CLK 100%, SD_D(8) 50%, 1/2 data switching per cycle, does not include power for other I/O pins on the VDD_IO_SDHC supply, 15.5pF                                 | —           |
| PVDD_IO_GMACn   | VDD_IO_GMACn operating power           | —   | 81  | —   | mW   | 1.8V, RGMII 125MHz, 100% clock rate, 50% data rate, 1/2 data switching per cycle, per IP instance, does not include power for other I/O pins on the VDD_IO_GMACn supply. 15.5pF  | —           |
| PVDD_IO_GMACn   | VDD_IO_GMACn operating power           | —   | 292 | —   | mW   | 3.3V, RGMII 125MHz, 100% clock rate, 50% data rate, 1/2 data switching per cycle, per IP instance, does not include power for other I/O pins on the VDD_IO_GMACn supply, 15.5pF. | —           |
| PVDD_IO_USB_TYP | USB I/O voltage supply operating power | —   | 59  | —   | mW   | 1.8V, modem - 8 outputs @60MHz, 50% data rate, 1/2 data switching per cycle, does not include power for other I/O pins on the VDD_IO_USB supply. 15.5pF.                         | —           |
| PVDD_IO_USB_TYP | USB I/O voltage supply operating power | —   | 174 | —   | mW   | 3.3V, modem - 8 outputs @60MHz, 50% data rate, 1/2 data switching per cycle, does not include power for the other I/O pins on the VDD_IO_USB supply. 15.5pF                      | —           |

Table continues on the next page...

**Table 10. Device Power and Operating Current Specifications (continued)**

| Symbol      | Description                               | Min | Typ | Max | Unit | Condition   | Spec Number |
|-------------|---|-----|-----|-----|------|---|-------------|
| PVDD_IO_AUR | Aurora I/O voltage supply operating power | —   | 164 | —   | mW   | 1.8V, 5Gbps on 4 lanes, 50% Activity Rate, 1/2 data switching per cycle | —           |

1. This spec includes the consumption on pins in VDD\_STBY\_IO domain only. See the hardware design guide for more details.
2. This specification can be considered a worst case maximum for any valid 2 x lane SerDes configuration (including PCIe/SGMII or SGMII only modes).

## 10 Power sequencing

### 10.1 Power-up

The following sequence has been validated by NXP and is to be followed when powering up the device. Each supply within a step must be within its specified operating voltage range before the next step in the sequence is started, except as noted below.

1. Set POR\_B input to low value.
2. Ramp up VDD\_IO\_STBY supply.

VDD\_IO\_B can optionally be included with VDD\_IO\_STBY in the first step.

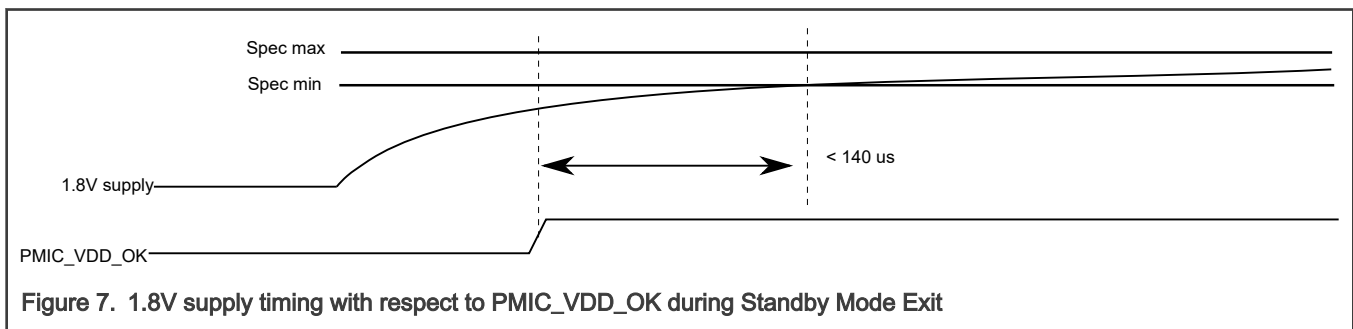
3. Ramp up all GPIO supplies powered to 3.3V.
4. Ramp up all 1.8V supplies including GPIO supplies powered to 1.8V

Step 5 and 6 can commence in the following sequence prior to all 1.8V supplies reaching DC tolerance. Step 5 must still reach DC tolerance before Step 6.

5. Ramp up VDD\_DDR\_IO supply
6. Ramp up all 0.8V supplies
7. Set POR\_B and PMIC\_VDD\_OK inputs to high value once all supplies have reached their specified levels.

**NOTE**

For step 4, it is acceptable for the 1.8V supplies to not yet be within their specified range at the time of asserting the PMIC\_VDD\_OK input when exiting Standby mode if it is ensured that they are within their specified range no later than 140 us after the PMIC\_VDD\_OK input assertion. VDD\_IO\_QSPI (a 1.8V GPIO supply) has the additional option to ramp with step 3 instead of step 4.



**Figure 7. 1.8V supply timing with respect to PMIC\_VDD\_OK during Standby Mode Exit**

**NOTE**

While powering up the device, the VDD\_EFUSE supply pin must be kept powered down. While the device is already powered up, the VDD\_EFUSE supply pin can be powered up/down independent of the other supplies on the device. The VDD\_EFUSE supply pin must be powered down prior to Standby mode entry or, at the latest, powered down together with the other 1.8V supplies during Standby mode entry.

**Table 11. Power-up**

| Symbol   | Description                                       | Min | Typ | Max | Unit | Condition | Spec Number |
|----------|---|-----|-----|-----|------|-----------|-------------|
| Vpwrdown | Maximum voltage on a supply pin in powerdown mode | —   | —   | 100 | mV   | —         | —           |

The power-up sequence on Standby exit is the same except that only the switchable supplies that were powered down during Standby mode are ramped up again, and the POR\_B input is kept high throughout the sequence.

## 10.2 Power-down

When powering down the SoC, it is recommended to use the reverse order from the power-up sequence. If this cannot be achieved, ensure that all supplies are below the Vpwrdown level before powering up again.

## 11 Electromagnetic compatibility (EMC)

EMC measurements to IC-level IEC standards are available from NXP Semiconductor on request.

## 12 GPIO Pads

**Table 12. GPIO Pads**

| Symbol  | Description                           | Min               | Typ | Max               | Unit | Condition       | Spec Number |
|---------|---------------------------------------|-------------------|-----|-------------------|------|-----------------|-------------|
| VIH     | Input high level DC voltage threshold | 0.7 *<br>VDD_IO_* | —   | —                 | V    | 1.8V / 3.3V     | —           |
| VIL     | Input low level DC voltage threshold  | —                 | —   | 0.3 *<br>VDD_IO_* | V    | 1.8V / 3.3V     | —           |
| VOL     | GPIO output low voltage <sup>1</sup>  | —                 | —   | 20% *<br>VDD_IO_* | V    | —               | —           |
| VOH     | GPIO output high voltage <sup>1</sup> | 80% *<br>VDD_IO_* | —   | —                 | V    | —               | —           |
| VHYS_33 | 3.3V GPIO input hysteresis voltage    | 100               | —   | —                 | mV   | Always enabled. | —           |
| ILKG_18 | 1.8V GPIO pad input leakage current   | -17               | —   | 17                | uA   | 1.8V, Tj = 125C | —           |

*Table continues on the next page...*

Table 12. GPIO Pads (continued)

| Symbol       | Description   | Min | Typ | Max   | Unit | Condition  | Spec Number |
|--------------|---|-----|-----|-------|------|--|-------------|
| ILKG_33      | 3.3V GPI / GPIO pad input leakage current           | -30 | —   | 30    | uA   | 3.3V, T <sub>j</sub> = 125C                            | —           |
| ILKG_3318    | 1.8V/3.3V GPIO pad input leakage current (3.3V)     | -50 | —   | 50    | uA   | 3.3V, T <sub>j</sub> = 125C                            | —           |
| ILKG_3318    | 1.8V/3.3V GPIO pad input leakage current (1.8V)     | -17 | —   | 17    | uA   | 1.8V, T <sub>j</sub> = 125C                            | —           |
| CIN_18       | Input capacitance (1.8V GPIO)                       | —   | 6   | 8     | pF   | —  | —           |
| CIN_33       | Input capacitance (3.3V GPI / GPIO)                 | —   | 7   | 11    | pF   | —  | —           |
| CIN_3318     | Input capacitance (1.8V/3.3V GPIO)                  | —   | 7   | 11    | pF   | —  | —           |
| ISLEW        | Input signal slew rate <sup>2</sup>                 | 1   | —   | 4     | V/ns | —  | —           |
| ITR_TF       | Input signal rise/fall time <sup>2,3</sup>          | 0.5 | —   | 2     | ns   | —  | —           |
| TPW_MIN      | Input minimum pulse width                           | 2   | —   | —     | ns   | —  | —           |
| FMAX_IN_18   | 1.8V GPIO maximum input frequency <sup>4</sup>      | —   | —   | 50    | MHz  | CMOS Receiver  | —           |
| FMAX_IN_18   | 1.8V GPIO maximum input frequency <sup>4</sup>      | —   | —   | 208   | MHz  | VREF Receiver  | —           |
| FMAX_IN_3318 | 1.8V/3.3V GPIO maximum input frequency <sup>4</sup> | —   | —   | 208   | MHz  | 1.8V   | —           |
| FMAX_IN_3318 | 1.8V/3.3V GPIO maximum input frequency <sup>4</sup> | —   | —   | 166.7 | MHz  | 3.3V   | —           |
| FMAX_IN_33   | 3.3V GPIO maximum input frequency <sup>4</sup>      | —   | —   | 50    | MHz  | —  | —           |
| IPU_18       | 1.8V GPIO pull up/down resistance                   | 9   | 18  | 23    | kΩ   | pull up @ 0.3 * VDD_HV_IO, pull down @ 0.7 * VDD_HV_IO | —           |
| IPU_33       | 3.3V GPIO pull up/down resistance                   | 9   | 18  | 23    | kΩ   | pull up @ 0.3 * VDD_HV_IO, pull down @ 0.7 * VDD_HV_IO | —           |

Table continues on the next page...

Table 12. GPIO Pads (continued)

| Symbol     | Description  | Min  | Typ  | Max  | Unit       | Condition  | Spec Number |
|------------|--|------|------|------|------------|--|-------------|
| IPU_3318   | 1.8V/3.3V GPIO pull up/down resistance                             | 9    | 18   | 23   | k $\Omega$ | pull up @ 0.3 * VDD_HV_IO, pull down @ 0.7 * VDD_HV_IO | —           |
| RDSON_18   | 1.8V GPIO output impedance (NMOS & PMOS) <sup>5</sup>              | 27.0 | 36.3 | 48.0 | $\Omega$   | SRE[2:0] = xxx, 50% * VDD_IO_*                         | —           |
| RDSON_3318 | 1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 1.8V <sup>5</sup> | 18.0 | 30.0 | 43.0 | $\Omega$   | SRE[2:0] = 000, 50% * VDD_IO_*                         | —           |
| RDSON_3318 | 1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 1.8V <sup>5</sup> | 19.0 | 30.0 | 44.0 | $\Omega$   | SRE[2:0] = 100, 50% * VDD_IO_*                         | —           |
| RDSON_3318 | 1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 1.8V <sup>5</sup> | 21.0 | 33.0 | 49.0 | $\Omega$   | SRE[2:0] = 101, 50% * VDD_IO_*                         | —           |
| RDSON_3318 | 1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 1.8V <sup>5</sup> | 23.0 | 37.5 | 58.0 | $\Omega$   | SRE[2:0] = 110, 50% * VDD_IO_*                         | —           |
| RDSON_3318 | 1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 1.8V <sup>5</sup> | 24.0 | 37.5 | 57.0 | $\Omega$   | SRE[2:0] = 111, 50% * VDD_IO_*                         | —           |
| RDSON_3318 | 1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V <sup>5</sup> | 18.0 | 30.0 | 43.0 | $\Omega$   | SRE[2:0] = 000, 50% * VDD_IO_*                         | —           |
| RDSON_3318 | 1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V <sup>5</sup> | 19.0 | 30.0 | 44.0 | $\Omega$   | SRE[2:0] = 100, 50% * VDD_IO_*                         | —           |
| RDSON_3318 | 1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V <sup>5</sup> | 21.0 | 33.4 | 50.0 | $\Omega$   | SRE[2:0] = 101, 50% * VDD_IO_*                         | —           |
| RDSON_3318 | 1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V <sup>5</sup> | 23.0 | 39.5 | 61.0 | $\Omega$   | SRE[2:0] = 110, 50% * VDD_IO_*                         | —           |

Table continues on the next page...



Table 12. GPIO Pads (continued)

| Symbol     | Description  | Min   | Typ  | Max  | Unit     | Condition                         | Spec Number |
|------------|--|-------|------|------|----------|-----------------------------------|-------------|
| RDSON_3318 | 1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V <sup>5</sup> | 26.0  | 39.5 | 61.0 | $\Omega$ | SRE[2:0] = 111, 50% *<br>VDD_IO_* | —           |
| RDSON_33   | 3.3V GPIO output impedance (NMOS & PMOS) <sup>5</sup>              | 16.5  | 26.5 | 42.0 | $\Omega$ | SRE[2:0] = 000, 50% *<br>VDD_IO_* | —           |
| RDSON_33   | 3.3V GPIO output impedance (NMOS & PMOS) <sup>5</sup>              | 16.5  | 26.5 | 42.0 | $\Omega$ | SRE[2:0] = 100, 50% *<br>VDD_IO_* | —           |
| RDSON_33   | 3.3V GPIO output impedance (NMOS & PMOS) <sup>5</sup>              | 19.2  | 30.5 | 49.5 | $\Omega$ | SRE[2:0] = 101, 50% *<br>VDD_IO_* | —           |
| RDSON_33   | 3.3V GPIO output impedance (NMOS & PMOS) <sup>5</sup>              | 24.5  | 38.0 | 61.5 | $\Omega$ | SRE[2:0] = 110, 50% *<br>VDD_IO_* | —           |
| RDSON_33   | 3.3V GPIO output impedance (NMOS & PMOS) <sup>5</sup>              | 32.0  | 48.0 | 75.5 | $\Omega$ | SRE[2:0] = 111, 50% *<br>VDD_IO_* | —           |
| IOH_18     | 1.8V GPIO output high current <sup>5</sup>                         | -15.0 | —    | -6.0 | mA       | SRE[2:0] = xxx, 80% *<br>VDD_IO_* | —           |
| IOL_18     | 1.8V GPIO output low current <sup>5</sup>                          | 6.0   | —    | 15.0 | mA       | SRE[2:0] = xxx, 20% *<br>VDD_IO_* | —           |
| IOH_3318   | 1.8V/3.3V GPIO output high current at 1.8V <sup>5</sup>            | -22   | —    | -8   | mA       | SRE[2:0] = 000, 80% *<br>VDD_IO_* | —           |
| IOH_3318   | 1.8V/3.3V GPIO output high current at 1.8V <sup>5</sup>            | -21   | —    | -8   | mA       | SRE[2:0] = 100, 80% *<br>VDD_IO_* | —           |
| IOH_3318   | 1.8V/3.3V GPIO output high current at 1.8V <sup>5</sup>            | -19   | —    | -6   | mA       | SRE[2:0] = 101, 80% *<br>VDD_IO_* | —           |
| IOH_3318   | 1.8V/3.3V GPIO output high current at 1.8V <sup>5</sup>            | -17   | —    | -6   | mA       | SRE[2:0] = 110, 80% *<br>VDD_IO_* | —           |
| IOH_3318   | 1.8V/3.3V GPIO output high current at 1.8V <sup>5</sup>            | -17   | —    | -6   | mA       | SRE[2:0] = 111, 80% *<br>VDD_IO_* | —           |
| IOL_3318   | 1.8V/3.3V GPIO output low current at 1.8V <sup>5</sup>             | 8     | —    | 22   | mA       | SRE[2:0] = 000, 20% *<br>VDD_IO_* | —           |

Table continues on the next page...

Table 12. GPIO Pads (continued)

| Symbol   | Description   | Min | Typ | Max | Unit | Condition                         | Spec Number |
|----------|---|-----|-----|-----|------|-----------------------------------|-------------|
| IOL_3318 | 1.8V/3.3V GPIO output low current at 1.8V <sup>5</sup>  | 8   | —   | 21  | mA   | SRE[2:0] = 100, 20% *<br>VDD_IO_* | —           |
| IOL_3318 | 1.8V/3.3V GPIO output low current at 1.8V <sup>5</sup>  | 6   | —   | 20  | mA   | SRE[2:0] = 101, 20% *<br>VDD_IO_* | —           |
| IOL_3318 | 1.8V/3.3V GPIO output low current at 1.8V <sup>5</sup>  | 6   | —   | 18  | mA   | SRE[2:0] = 110, 20% *<br>VDD_IO_* | —           |
| IOL_3318 | 1.8V/3.3V GPIO output low current at 1.8V <sup>5</sup>  | 6   | —   | 17  | mA   | SRE[2:0] = 111, 20% *<br>VDD_IO_* | —           |
| IOH_3318 | 1.8V/3.3V GPIO output high current at 3.3V <sup>5</sup> | -40 | —   | -14 | mA   | SRE[2:0] = 000, 80% *<br>VDD_IO_* | —           |
| IOH_3318 | 1.8V/3.3V GPIO output high current at 3.3V <sup>5</sup> | -40 | —   | -14 | mA   | SRE[2:0] = 100, 80% *<br>VDD_IO_* | —           |
| IOH_3318 | 1.8V/3.3V GPIO output high current at 3.3V <sup>5</sup> | -35 | —   | -10 | mA   | SRE[2:0] = 101, 80% *<br>VDD_IO_* | —           |
| IOH_3318 | 1.8V/3.3V GPIO output high current at 3.3V <sup>5</sup> | -32 | —   | -10 | mA   | SRE[2:0] = 110, 80% *<br>VDD_IO_* | —           |
| IOH_3318 | 1.8V/3.3V GPIO output high current at 3.3V <sup>5</sup> | -32 | —   | -10 | mA   | SRE[2:0] = 111, 80% *<br>VDD_IO_* | —           |
| IOL_3318 | 1.8V/3.3V GPIO output low current at 3.3V <sup>5</sup>  | 15  | —   | 40  | mA   | SRE[2:0] = 000, 20% *<br>VDD_IO_* | —           |
| IOL_3318 | 1.8V/3.3V GPIO output low current at 3.3V <sup>5</sup>  | 15  | —   | 40  | mA   | SRE[2:0] = 100, 20% *<br>VDD_IO_* | —           |
| IOL_3318 | 1.8V/3.3V GPIO output low current at 3.3V <sup>5</sup>  | 13  | —   | 36  | mA   | SRE[2:0] = 101, 20% *<br>VDD_IO_* | —           |
| IOL_3318 | 1.8V/3.3V GPIO output low current at 3.3V <sup>5</sup>  | 12  | —   | 33  | mA   | SRE[2:0] = 110, 20% *<br>VDD_IO_* | —           |
| IOL_3318 | 1.8V/3.3V GPIO output low current at 3.3V <sup>5</sup>  | 11  | —   | 32  | mA   | SRE[2:0] = 111, 20% *<br>VDD_IO_* | —           |

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Table 12. GPIO Pads (continued)

| Symbol  | Description  | Min   | Typ | Max   | Unit | Condition                         | Spec Number |
|---------|--|-------|-----|-------|------|-----------------------------------|-------------|
| IOH_33  | 3.3V GPIO output high current <sup>5</sup>         | -40.1 | —   | -14.0 | mA   | SRE[2:0] = 000, 80% *<br>VDD_IO_* | —           |
| IOH_33  | 3.3V GPIO output high current <sup>5</sup>         | -40.1 | —   | -14.0 | mA   | SRE[2:0] = 100, 80% *<br>VDD_IO_* | —           |
| IOH_33  | 3.3V GPIO output high current <sup>5</sup>         | -36.2 | —   | -12.1 | mA   | SRE[2:0] = 101, 80% *<br>VDD_IO_* | —           |
| IOH_33  | 3.3V GPIO output high current <sup>5</sup>         | -32.0 | —   | -10.3 | mA   | SRE[2:0] = 110, 80% *<br>VDD_IO_* | —           |
| IOH_33  | 3.3V GPIO output high current <sup>5</sup>         | -29.0 | —   | -9.0  | mA   | SRE[2:0] = 111, 80% *<br>VDD_IO_* | —           |
| IOL_33  | 3.3V GPIO output low current <sup>5</sup>          | 14.6  | —   | 39.4  | mA   | SRE[2:0] = 000, 20% *<br>VDD_IO_* | —           |
| IOL_33  | 3.3V GPIO output low current <sup>5</sup>          | 14.6  | —   | 39.4  | mA   | SRE[2:0] = 100, 20% *<br>VDD_IO_* | —           |
| IOL_33  | 3.3V GPIO output low current <sup>5</sup>          | 13.0  | —   | 35.5  | mA   | SRE[2:0] = 101, 20% *<br>VDD_IO_* | —           |
| IOL_33  | 3.3V GPIO output low current <sup>5</sup>          | 11.2  | —   | 32.0  | mA   | SRE[2:0] = 110, 20% *<br>VDD_IO_* | —           |
| IOL_33  | 3.3V GPIO output low current <sup>5</sup>          | 10.0  | —   | 29.0  | mA   | SRE[2:0] = 111, 20% *<br>VDD_IO_* | —           |
| FMAX_18 | 1.8V GPIO maximum output frequency <sup>5, 6</sup> | —     | —   | 208   | MHz  | SRE[2:0] = 000                    | —           |
| FMAX_18 | 1.8V GPIO maximum output frequency <sup>5, 6</sup> | —     | —   | 150   | MHz  | SRE[2:0] = 100                    | —           |
| FMAX_18 | 1.8V GPIO maximum output frequency <sup>5, 6</sup> | —     | —   | 133   | MHz  | SRE[2:0] = 101                    | —           |
| FMAX_18 | 1.8V GPIO maximum output frequency <sup>5, 6</sup> | —     | —   | 100   | MHz  | SRE[2:0] = 110                    | —           |
| FMAX_18 | 1.8V GPIO maximum output frequency <sup>5, 6</sup> | —     | —   | 50    | MHz  | SRE[2:0] = 111                    | —           |
| FMAX_33 | 3.3V GPIO maximum output frequency <sup>5, 6</sup> | —     | —   | 50    | MHz  | SRE[2:0] = 100                    | —           |

Table continues on the next page...

Table 12. GPIO Pads (continued)

| Symbol    | Description   | Min | Typ | Max   | Unit | Condition   | Spec Number |
|-----------|---|-----|-----|-------|------|---|-------------|
| FMAX_33   | 3.3V GPIO maximum output frequency <sup>5, 6</sup>      | —   | —   | 50    | MHz  | SRE[2:0] = 101, reduced slew relative to the SRE[2:0] = 100 setting for the same output load. | —           |
| FMAX_33   | 3.3V GPIO maximum output frequency <sup>5, 6</sup>      | —   | —   | 50    | MHz  | SRE[2:0] = 110  | —           |
| FMAX_33   | 3.3V GPIO maximum output frequency <sup>5, 6</sup>      | —   | —   | 1     | MHz  | SRE[2:0] = 111  | —           |
| FMAX_3318 | 1.8V/3.3V GPIO maximum output frequency <sup>5, 6</sup> | —   | —   | 208   | MHz  | SRE[2:0] = 000, 1.8V  | —           |
| FMAX_3318 | 1.8V/3.3V GPIO maximum output frequency <sup>5, 6</sup> | —   | —   | 166.7 | MHz  | SRE[2:0] = 100, 1.8V  | —           |
| FMAX_3318 | 1.8V/3.3V GPIO maximum output frequency <sup>5, 6</sup> | —   | —   | 150   | MHz  | SRE[2:0] = 101, 1.8V  | —           |
| FMAX_3318 | 1.8V/3.3V GPIO maximum output frequency <sup>5, 6</sup> | —   | —   | 133.3 | MHz  | SRE[2:0] = 110, 1.8V  | —           |
| FMAX_3318 | 1.8V/3.3V GPIO maximum output frequency <sup>5, 6</sup> | —   | —   | 100   | MHz  | SRE[2:0] = 111, 1.8V  | —           |
| FMAX_3318 | 1.8V/3.3V GPIO maximum output frequency <sup>5, 6</sup> | —   | —   | 166.7 | MHz  | SRE[2:0] = 000, 3.3V  | —           |
| FMAX_3318 | 1.8V/3.3V GPIO maximum output frequency <sup>5, 6</sup> | —   | —   | 150   | MHz  | SRE[2:0] = 100, 3.3V  | —           |
| FMAX_3318 | 1.8V/3.3V GPIO maximum output frequency <sup>5, 6</sup> | —   | —   | 133.3 | MHz  | SRE[2:0] = 101, 3.3V  | —           |
| FMAX_3318 | 1.8V/3.3V GPIO maximum output frequency <sup>5, 6</sup> | —   | —   | 100   | MHz  | SRE[2:0] = 110, 3.3V  | —           |
| FMAX_3318 | 1.8V/3.3V GPIO maximum output frequency <sup>5, 6</sup> | —   | —   | 83.3  | MHz  | SRE[2:0] = 111, 3.3V  | —           |

Table continues on the next page...

Table 12. GPIO Pads (continued)

| Symbol     | Description   | Min  | Typ | Max  | Unit | Condition      | Spec Number |
|------------|---|------|-----|------|------|----------------|-------------|
| TR_TF_3318 | 1.8V/3.3V GPIO rise/fall time at 1.8V <a href="#">5, 6, 7</a> | 1.0  | —   | 5.5  | V/ns | SRE[2:0] = 000 | —           |
| TR_TF_3318 | 1.8V/3.3V GPIO rise/fall time at 1.8V <a href="#">5, 6, 7</a> | 1.0  | —   | 5.75 | V/ns | SRE[2:0] = 100 | —           |
| TR_TF_3318 | 1.8V/3.3V GPIO rise/fall time at 1.8V <a href="#">5, 6, 7</a> | 0.75 | —   | 4.75 | V/ns | SRE[2:0] = 101 | —           |
| TR_TF_3318 | 1.8V/3.3V GPIO rise/fall time at 1.8V <a href="#">5, 6, 7</a> | 0.5  | —   | 4.5  | V/ns | SRE[2:0] = 110 | —           |
| TR_TF_3318 | 1.8V/3.3V GPIO rise/fall time at 1.8V <a href="#">5, 6, 7</a> | 0.5  | —   | 4.0  | V/ns | SRE[2:0] = 111 | —           |
| TR_TF_3318 | 1.8V/3.3V GPIO rise/fall time at 3.3V <a href="#">5, 6, 7</a> | 2.0  | —   | 10.5 | V/ns | SRE[2:0] = 000 | —           |
| TR_TF_3318 | 1.8V/3.3V GPIO rise/fall time at 3.3V <a href="#">5, 6, 7</a> | 2.0  | —   | 9.25 | V/ns | SRE[2:0] = 100 | —           |
| TR_TF_3318 | 1.8V/3.3V GPIO rise/fall time at 3.3V <a href="#">5, 6, 7</a> | 1.5  | —   | 9.5  | V/ns | SRE[2:0] = 101 | —           |
| TR_TF_3318 | 1.8V/3.3V GPIO rise/fall time at 3.3V <a href="#">5, 6, 7</a> | 0.75 | —   | 7.5  | V/ns | SRE[2:0] = 110 | —           |
| TR_TF_3318 | 1.8V/3.3V GPIO rise/fall time at 3.3V <a href="#">5, 6, 7</a> | 0.75 | —   | 7.25 | V/ns | SRE[2:0] = 111 | —           |
| TR_TF_18   | 1.8V GPIO rise/fall time <a href="#">5, 6, 7</a>              | 0.75 | —   | 3.75 | V/ns | SRE[2:0] = 000 | —           |
| TR_TF_18   | 1.8V GPIO rise/fall time <a href="#">5, 6, 7</a>              | 0.75 | —   | 3.75 | V/ns | SRE[2:0] = 100 | —           |
| TR_TF_18   | 1.8V GPIO rise/fall time <a href="#">5, 6, 7</a>              | 0.75 | —   | 3.25 | V/ns | SRE[2:0] = 101 | —           |
| TR_TF_18   | 1.8V GPIO rise/fall time <a href="#">5, 6, 7</a>              | 0.75 | —   | 3.25 | V/ns | SRE[2:0] = 110 | —           |
| TR_TF_18   | 1.8V GPIO rise/fall time <a href="#">5, 6, 7</a>              | 0.25 | —   | 3.25 | V/ns | SRE[2:0] = 111 | —           |
| TR_TF_33   | 3.3V GPIO rise/fall time <a href="#">5, 6, 7</a>              | 1.75 | —   | 9.0  | V/ns | SRE[2:0] = 000 | —           |
| TR_TF_33   | 3.3V GPIO rise/fall time <a href="#">5, 6, 7</a>              | 1.90 | —   | 9.0  | V/ns | SRE[2:0] = 100 | —           |
| TR_TF_33   | 3.3V GPIO rise/fall time <a href="#">5, 6, 7</a>              | 1.00 | —   | 8.50 | V/ns | SRE[2:0] = 101 | —           |
| TR_TF_33   | 3.3V GPIO rise/fall time <a href="#">5, 6, 7</a>              | 0.50 | —   | 7.30 | V/ns | SRE[2:0] = 110 | —           |

Table continues on the next page...

Table 12. GPIO Pads (continued)

| Symbol    | Description  | Min  | Typ  | Max | Unit | Condition  | Spec Number |
|-----------|--|------|------|-----|------|--|-------------|
| TR_TF_33  | 3.3V GPIO rise/fall time <sup>5, 6, 7</sup>          | 0.40 | —    | 6.0 | V/ns | SRE[2:0] = 111   | —           |
| WISE_33   | 3.3V GPIO pad indeterminate state end threshold      | —    | 2.35 | —   | V    | See 1.8V and 3.3V GPIO pad detailed behavior diagram below | —           |
| WISE_3318 | 1.8V/3.3V GPIO pad indeterminate state end threshold | —    | 1.53 | —   | V    | See 1.8V/3.3V GPIO pad detailed behavior diagram below     | —           |
| WISE_18   | 1.8V GPIO pad indeterminate state end threshold      | —    | 0.6  | —   | V    | See 1.8V and 3.3V GPIO pad detailed behavior diagram below | —           |

- For current at this voltage see IOL/IOH specs respectively.
- Fastest slew rate and lowest rise/fall time constraint required to meet high-speed interface timing such as QSPI, RGMII, and uSDHC. Slower input transitions can be used for input signals with slow switching rates (<40 MHz).
- The ISLEW has precedence over ITR\_TF if the ITR\_TF violates the implied range for a given ISLEW.
- Input slew rate and rise/fall time limits must be adhered to in conjunction with the max input frequency limits given for proper operation.
- GPIO output transition time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.
- I/O timing specifications are valid for the un-terminated 50ohm transmission line reference load given in the figure below. A lumped 8pF load is assumed at the end of a 5 inch microstrip trace on standard FR4 with approximately 1.5pF/inch. For signals with frequency greater than 63MHz, a maximum 2 inch PCB trace is assumed. For best signal integrity, the series resistance in the transmission line should be matched closely to the selected R<sub>DSO</sub>N of the I/O pad output.
- Rise/fall time specifications are derived from simulation model for the defined operating points (between 20% and 80% of VDD\_HV\_IO level). Actual application rise/fall time should be extracted from IBIS model simulations with the microcontroller models and application PCB.

**NOTE**

In the Standby mode exit case, the rising edge of the PMIC\_VDD\_OK pin determines when the pads enter their 'POR value' state instead of the POR\_B pin.

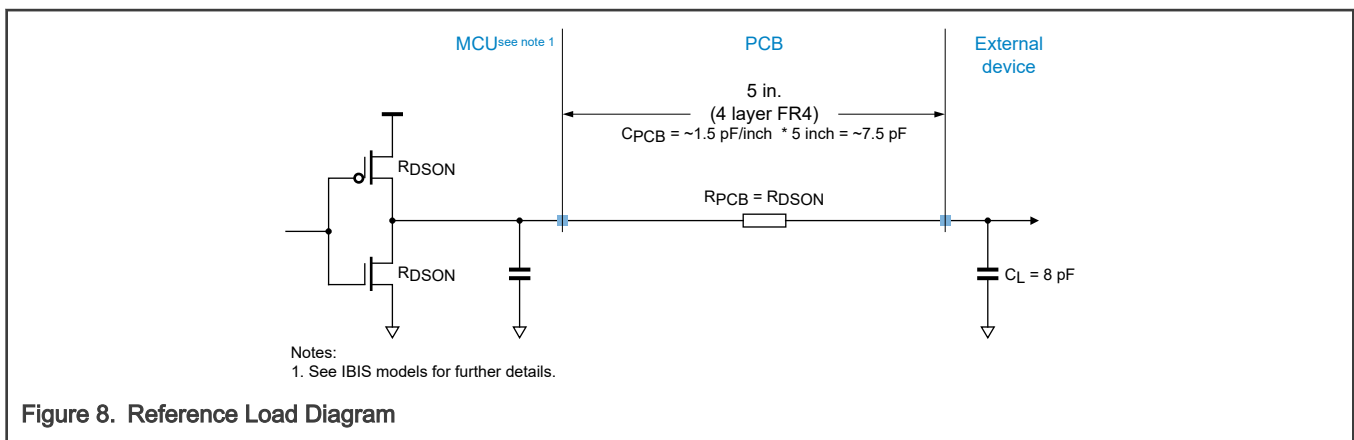


Figure 8. Reference Load Diagram

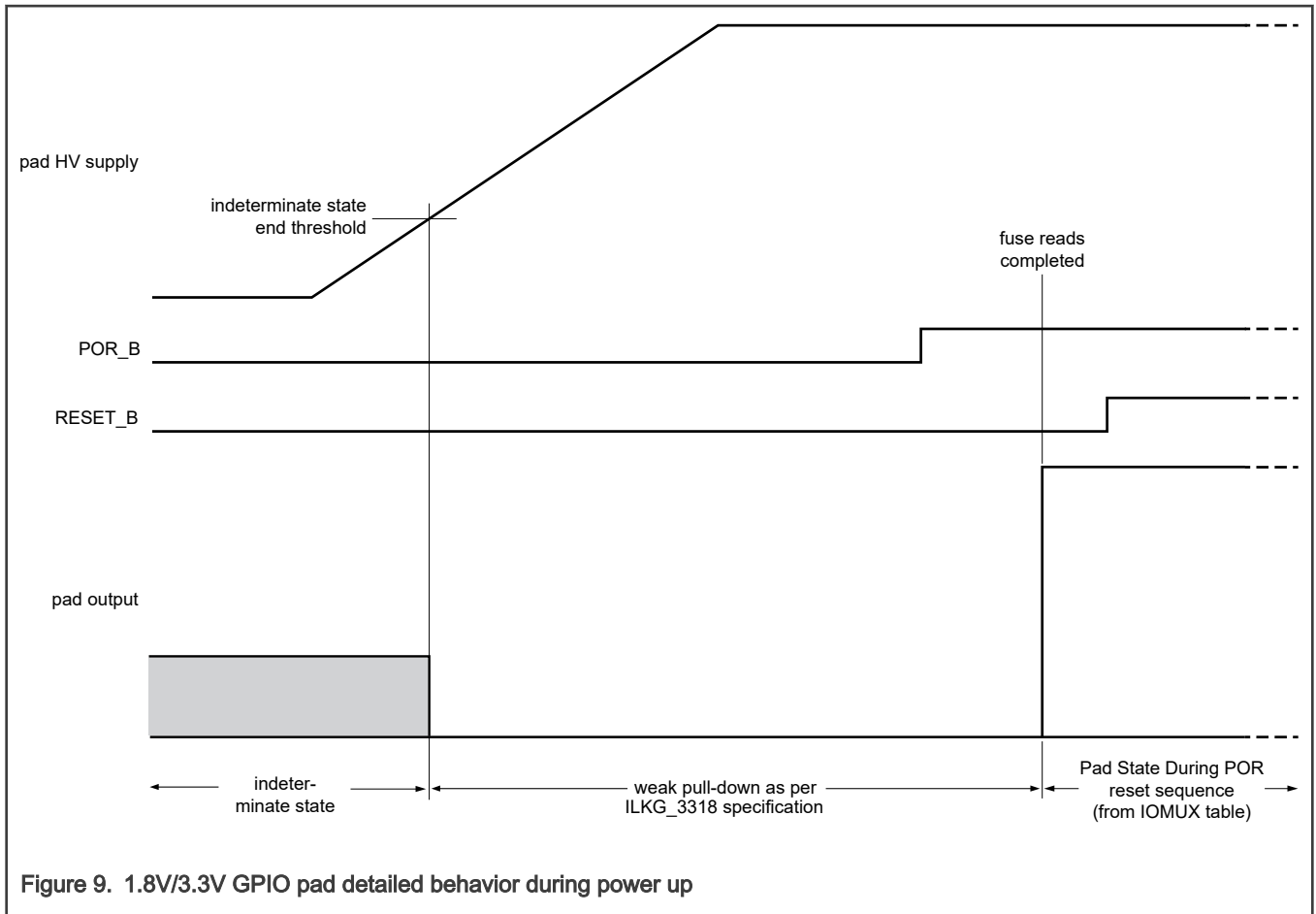
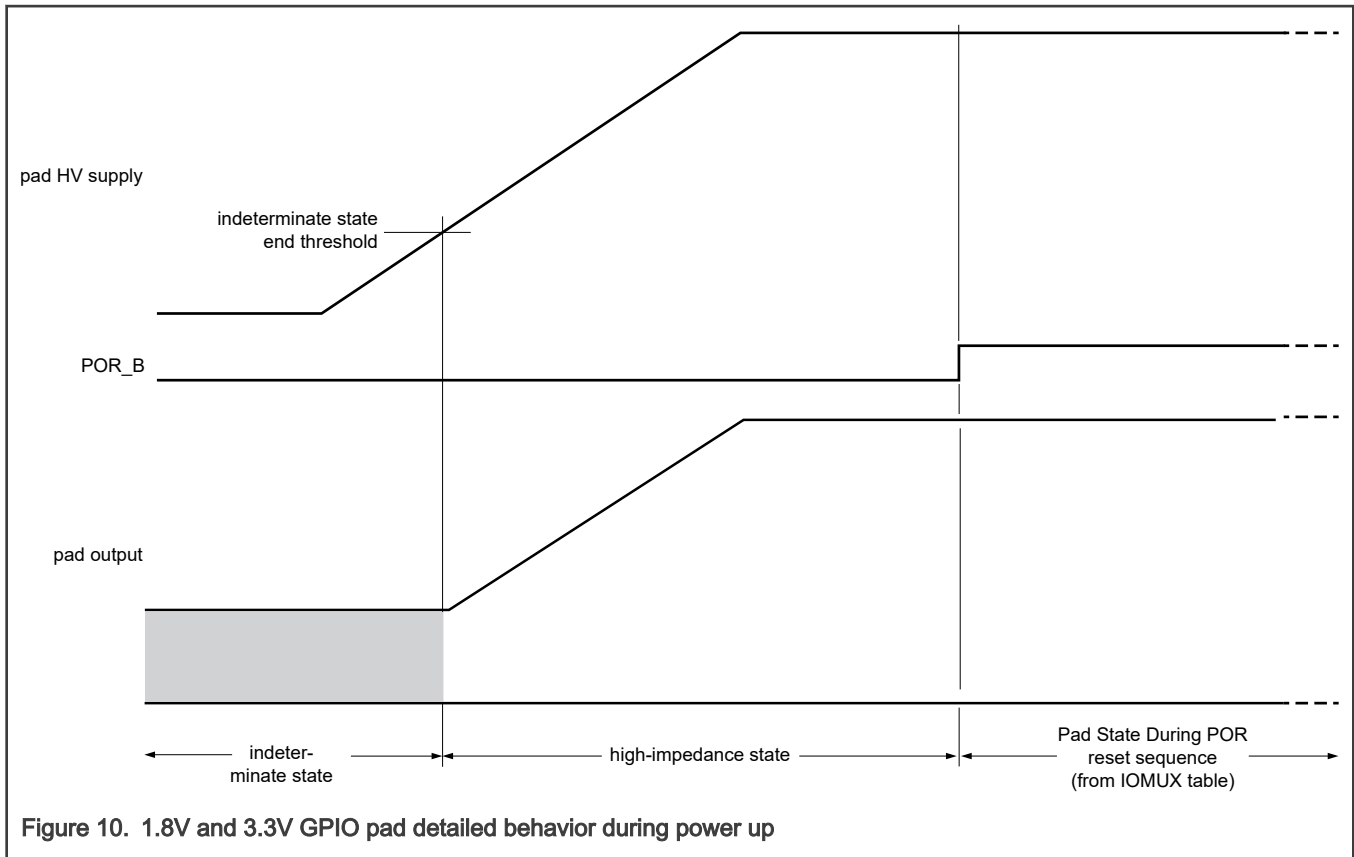


Figure 9. 1.8V/3.3V GPIO pad detailed behavior during power up



The high-impedance state level is shown based on the external pull-up being on the corresponding pad supply.

## 13 Aurora specifications

### 13.1 Aurora Pads

Table 13. Aurora Pads

| Symbol     | Description   | Min  | Typ | Max | Unit | Condition  | Spec Number |
|------------|---|------|-----|-----|------|--|-------------|
| fAURORA    | Data Rate   | 0.05 | —   | 5.0 | Gbps | 100Ω external termination ( Not on board but inside receiver after AC coupling ) | —           |
| IDD_HV_AUR | Transmitter HV supply current consumption (No pre-emphasis)       | 18   | 22  | 31  | mA   | max fAURORA per active transmit lane   | —           |
| IDD_HV_AUR | Transmitter HV supply current consumption (pre-emphasis enabled , | 25   | 30  | 40  | mA   | max fAURORA per active transmit lane   | —           |

Table continues on the next page...



Table 13. Aurora Pads (continued)

| Symbol                 | Description  | Min   | Typ | Max   | Unit       | Condition   | Spec Number |
|------------------------|--|-------|-----|-------|------------|---|-------------|
|                        | pre-emphasis gain=11)  |       |     |       |            |   |             |
| VOD_AURORA_AC          | Transmitter Differential output voltage (end termination) <sup>1, 2, 3</sup>                   | 400   | 600 | 900   | mV         | max fAURORA, 100Ω termination, 100Ω differential transmission line delay, matched network | —           |
| VOD_AURORA_DC          | DC range for the VOD (Transmitter Differential Output Voltage)                                 | 800   | —   | —     | mV         | ipp_obe=1 DC condition  | —           |
| VOD_AURORA_AC_PRE_EMPH | Transmitter Differential output voltage (end termination, preemph=11) <sup>1, 2, 4</sup>       | 600   | 900 | 1200  | mV         | max fAURORA, 100Ω termination, 100Ω differential transmission line delay, matched network | —           |
| VCM_AURORA             | Transmitter Common mode voltage  | 0.775 | —   | 1.025 | V          | —   | —           |
| VCM_LVDS_RX            | Receiver input signal common mode range  | 0.6   | —   | 1.0   | V          | —   | —           |
| VDIFF_LVDS_RX          | Receiver input differential signal   | 400   | —   | —     | mV         | —   | —           |
| CLOAD_AURORA           | Maximum transmission line load ( Lumped Load at any point on Tline )                           | —     | —   | 0.1   | pF         | —   | —           |
| RTERM_AURORA           | Internal termination resistance  | 80    | 100 | 130   | Ohm        | enabled   | —           |
| VSLEW_AURORA           | Differential output slew rate  | —     | 30  | 50    | ps / 200mV | max fAURORA   | —           |
| TSTARTUP_AURORA        | Transmitter startup time (assertion of ipp_obe to common mode settling of differential output) | —     | —   | 500   | ns         | —   | —           |
| TEYE_AURORA            | Valid data region ( Including PLL Jitter for Aurora ) <sup>5</sup>                             | 0.55  | —   | —     | UI         | max fAURORA   | —           |

Table continues on the next page...

Table 13. Aurora Pads (continued)

| Symbol     | Description                                    | Min               | Typ | Max               | Unit | Condition                        | Spec Number |
|------------|--|-------------------|-----|-------------------|------|----------------------------------|-------------|
| VOH_AURORA | Transmitter output high indicator <sup>6</sup> | $VDD\_IO/2 + 0.2$ | —   | —                 | V    | 100Ω termination at receiver end | —           |
| VOL_AURORA | Transmitter output low indicator <sup>6</sup>  | —                 | —   | $VDD\_IO/2 - 0.2$ | V    | 100Ω termination at receiver end | —           |
| PAD_P_BIAS | Pad_p voltage output level when Tx disabled    | —                 | —   | 0.6               | V    | lpp_obe_lv=0 lpp_term_en_lv=0    | —           |
| PAD_N_BIAS | Pad_n voltage output level when Tx disabled    | 1.1               | —   | —                 | V    | lpp_obe_lv=0 lpp_term_en_lv=0    | —           |

- When operating at max speed, there will be losses and differential output will be smaller as against DC condition. Aurora Interface Min differential swing is 400mV which is always guaranteed but the max limit is dependent on board design/ losses. For boards with negligible losses , if differential output (P-N) goes higher than 800mV (Aurora max differential input spec) , user must use “dual termination” scheme as highlighted in the Source Termination Circuit Figure to get the differential swing back within Range. The termination in the source side can be enabled through software in the transmitter pad design. Direct end termination without AC coupling is not allowed.
- Termination scheme as shown in the End Termination Circuit Figure. Direct end termination without AC coupling is not allowed.
- Differential output is with pre-emphasis disabled, and a 10mA output stage current.
- Differential output is with pre-emphasis enabled, and a ~15mA avg output stage current
- UI @ 5Gbps equals 200ps. The valid eye is expected to be > 110ps in width. ISI jitter spec is 20-30ps for the LVDS transmitter across PVT in a delay matched differential transmission line impedance of 100Ω.
- VDD\_IO maps to corresponding supply name on the device.

Termination scheme as shown in “End Termination Circuit” applies to debug tool hardware and is not recommended to be placed on the PC.

Source termination Circuit – Transmitter side 100 ohm termination is present inside the Tx pad and should not be placed on the PCB.

Direct 100 ohm board termination not allowed between AUR\_TXn\_N and AUR\_TXn\_N (n=0,1,2,3). Source termination is only allowed through the internal termination inside LVDS Tx pad.

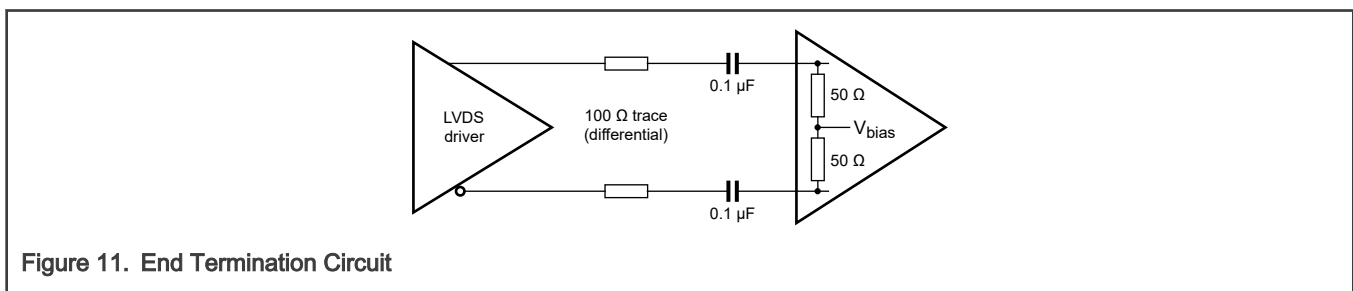


Figure 11. End Termination Circuit

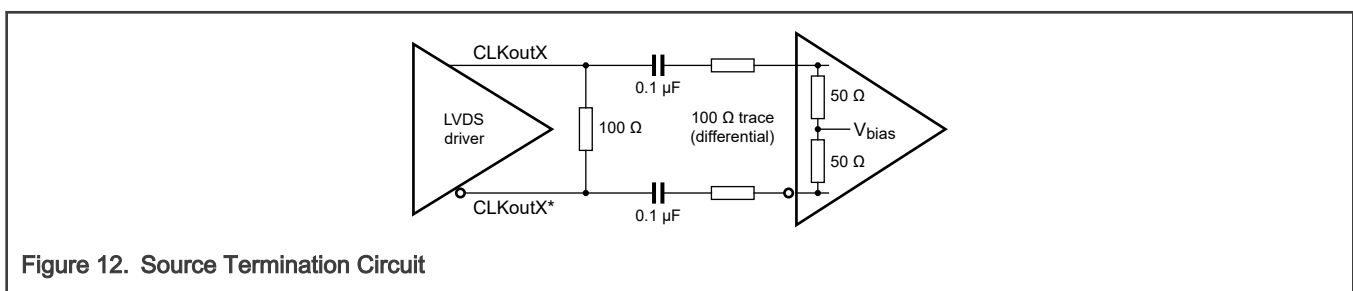


Figure 12. Source Termination Circuit

## 13.2 Aurora Port Timing

The following table gives the Aurora Port interface timing specifications for the device.

Table 14. Aurora Port Timing

| Symbol | Description                              | Min | Typ | Max    | Unit | Condition                      | Spec Number |
|--------|--|-----|-----|--------|------|--------------------------------|-------------|
| BER    | Bit Error Rate                           | —   | —   | 10e-12 | —    | —                              | —           |
| JD     | Transmit line deterministic jitter       | —   | —   | 0.17   | OUI  | data rate <=3.0 Gbps           | —           |
| JD     | Transmit line deterministic jitter       | —   | —   | 0.25   | OUI  | 3.0Gbps < data rate <= 5.0Gbps | —           |
| JT     | Transmit line total jitter               | —   | —   | 0.35   | OUI  | data rate <= 3.0 Gbps          | 2           |
| JT     | Transmit line total jitter               | —   | —   | 0.45   | OUI  | 3.0Gbps < data rate <= 5.0Gbps | 2           |
| SO     | Differential output skew                 | —   | —   | 20     | ps   | —                              | 3           |
| SMO    | Lane to lane output skew                 | —   | —   | 1000   | ps   | —                              | 4           |
| OUI    | Aurora lane unit interval <sup>1,2</sup> | —   | 500 | —      | ps   | 2.0 Gbps                       | 5           |
| OUI    | Aurora lane unit interval <sup>1,2</sup> | —   | 400 | —      | ps   | 2.5 Gbps                       | 5           |
| OUI    | Aurora lane unit interval <sup>1,2</sup> | —   | 333 | —      | ps   | 3.0 Gbps                       | 5           |
| OUI    | Aurora lane unit interval <sup>1,2</sup> | —   | 294 | —      | ps   | 3.4 Gbps                       | 5           |
| OUI    | Aurora lane unit interval <sup>1,2</sup> | —   | 250 | —      | ps   | 4.0 Gbps                       | 5           |
| OUI    | Aurora lane unit interval <sup>1,2</sup> | —   | 200 | —      | ps   | 5.0 Gbps                       | 5           |

1. +/- 100 PPM.

2. The Aurora interface supports data rates of 2.0, 2.5, 3.0, 3.4, 4.0, and 5.0 Gbps.

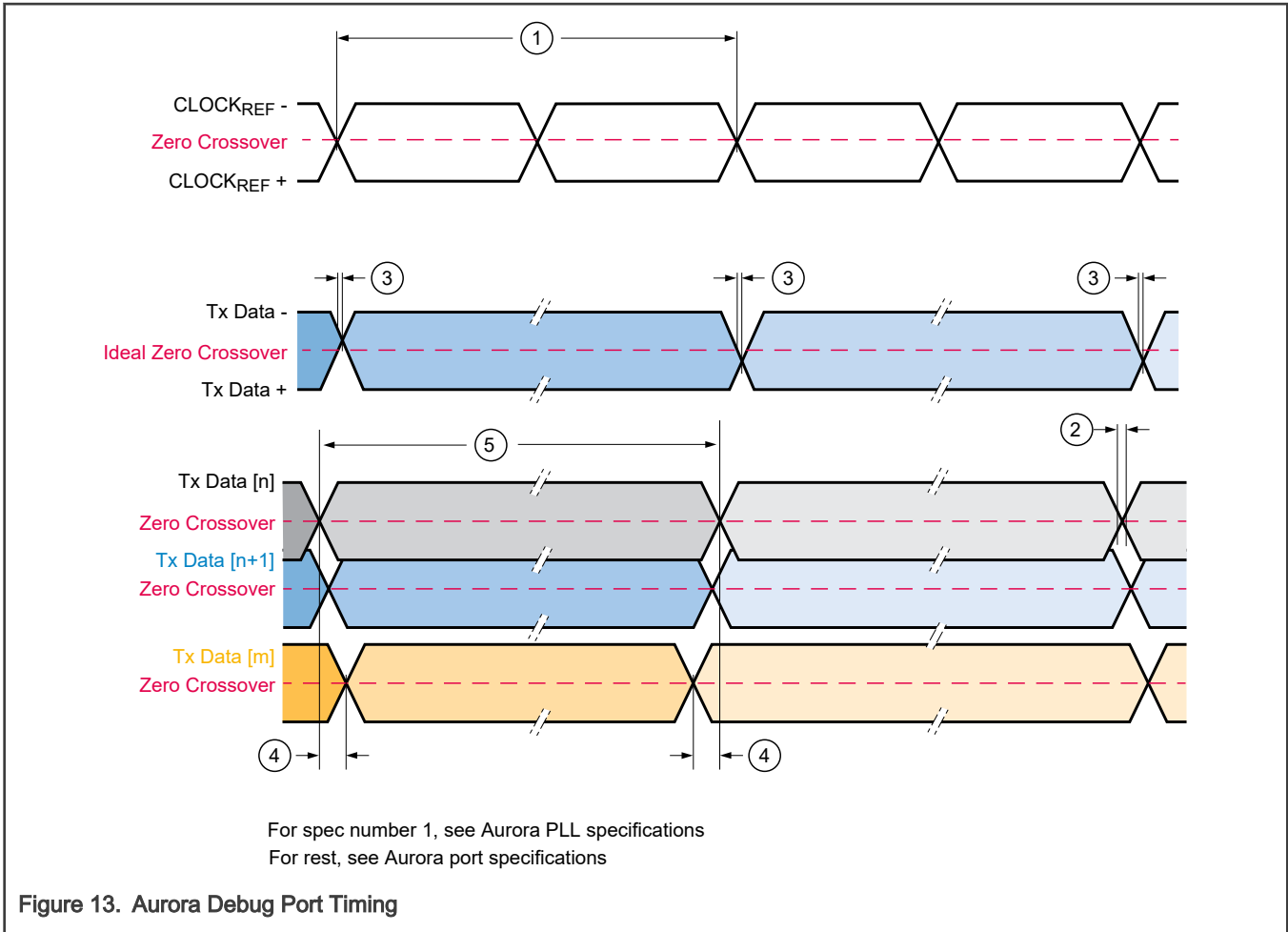


Figure 13. Aurora Debug Port Timing

### 13.3 Aurora PLL

The following table gives the operating frequencies and characteristics of the Aurora PLL. The operating frequencies correspond to the supported Aurora data trace lane speed. The Aurora PLL works from an external 100MHz input reference clock, and achieves a maximum output frequency of 5GHz.

Table 15. Aurora PLL

| Symbol         | Description   | Min | Typ | Max | Unit | Condition | Spec Number |
|----------------|---|-----|-----|-----|------|-----------|-------------|
| fPLL_CLKIN     | Aurora PLL Input Reference Clock Frequency <sup>1, 2, 3</sup> | —   | 100 | —   | MHz  | —         | —           |
| fPLL_CLKIN_PFD | Aurora PLL Phase Detector Clock Frequency <sup>4</sup>        | —   | 100 | —   | MHz  | —         | —           |
| ΔfPLL_CLKIN    | Aurora PLL Input Reference Clock Duty Cycle <sup>1</sup>      | 40  | —   | 60  | %    | —         | —           |

Table continues on the next page...

Table 15. Aurora PLL (continued)

| Symbol       | Description  | Min  | Typ | Max  | Unit | Condition   | Spec Number |
|--------------|--|------|-----|------|------|---|-------------|
| JRCDC        | Reference clock period jitter                          | —    | —   | 5    | ps   | RMS, 0.5MHz - 20MHz   | —           |
| fPLL_VCO     | Aurora PLL VCO Frequency Range                         | 3000 | —   | 5000 | MHz  | —   | —           |
| fPLL_CLKOUT0 | Aurora PLL Output Clock 0 Frequency Range <sup>5</sup> | —    | —   | 5000 | MHz  | 5.0Gbps Aurora lane data rate, VCO frequency divided by 1         | —           |
| fPLL_CLKOUT0 | Aurora PLL Output Clock 0 Frequency Range <sup>5</sup> | —    | —   | 4000 | MHz  | 4.0Gbps Aurora lane data rate, VCO frequency divided by 1         | —           |
| fPLL_CLKOUT0 | Aurora PLL Output Clock 0 Frequency Range <sup>5</sup> | —    | —   | 3400 | MHz  | 3.4Gbps Aurora lane data rate, VCO frequency divided by 1         | —           |
| fPLL_CLKOUT0 | Aurora PLL Output Clock 0 Frequency Range <sup>5</sup> | —    | —   | 3000 | MHz  | 3.0Gbps Aurora lane data rate, VCO frequency divided by 1         | —           |
| fPLL_CLKOUT0 | Aurora PLL Output Clock 0 Frequency Range <sup>5</sup> | —    | —   | 2500 | MHz  | 2.5Gbps Aurora lane data rate, VCO frequency divided by 2.        | —           |
| fPLL_CLKOUT0 | Aurora PLL Output Clock 0 Frequency Range <sup>5</sup> | —    | —   | 2000 | MHz  | 2.0Gbps Aurora lane data rate, VCO frequency divided by 2.        | —           |
| fPLL_CLKOUT0 | Aurora PLL Output Clock 0 Frequency Range              | —    | —   | 500  | MHz  | No tool connected - trace logic clock with FXOSC reference clock. | —           |
| tLOCK        | Aurora PLL Lock Time                                   | —    | —   | 150  | us   | —   | —           |
| PER_jitter   | Aurora PLL Period Jitter                               | -21  | —   | 21   | ps   | fPLL_CLKIN = 100MHz, VCO = 5GHz, fPLL_CLKOUT = 5GHz, 6-sigma      | —           |
| LT_jitter    | Aurora PLL Long Term Jitter                            | -120 | —   | 120  | ps   | Saturated, 6-sigma  | —           |

1. Refer to the LVDS Pad specifications for additional Aurora PLL reference clock electrical specifications. Also see "Aurora Debug Port Timing" figure for fPLL\_CLKIN as spec number 1.
2. 100MHz is the only input reference frequency supported for the Aurora PLL.
3. 40MHz is the only internal input reference frequency supported for the Aurora PLL.
4. It is Aurora PLL Input Reference Clock Frequency after pre-divider.
5. The Aurora PLL is only validated at the frequencies specified within this table - these frequencies correspond to the limited set of Aurora data lane rates that are supported for the device.

## 14 Power Management Controller (PMC)

### 14.1 PMC Bandgap

Table 16. PMC Bandgap

| Symbol     | Description  | Min   | Typ   | Max   | Unit | Condition                           | Spec Number |
|------------|--|-------|-------|-------|------|-------------------------------------|-------------|
| VBG_SCALED | Scaled version of bandgap reference voltage measured by SAR ADC <sup>1</sup> | 1.127 | 1.150 | 1.173 | V    | Both bandgap and buffer are trimmed | —           |

1. ADC conversion error must be included when reading the bandgap reference voltage via the chip ADC.

## 15 Reset

### 15.1 Reset Duration

The durations specified "Reset Duration" table and the corresponding figures refer to standard reset sequences. A reset sequence is no longer standard when it is interrupted by another power-on or destructive reset event, in which case the reset sequence restarts from the beginning of the reset sequence corresponding to that event, and the total duration is the time already spent in reset plus the duration of the new sequence.

The diagrams in this section are not to scale.

Table 17. Reset Duration

| Symbol | Description                         | Min | Typ | Max  | Unit | Condition  | Spec Number |
|--------|-------------------------------------|-----|-----|------|------|--|-------------|
| TFR    | Functional Reset Sequence Duration  | —   | —   | 545  | us   | FIRC_CLK, trimmed                                | —           |
| TDR    | Destructive Reset Sequence Duration | —   | —   | 1370 | us   | FIRC_CLK, trimmed during destructive reset phase | —           |
| POR    | Power On Reset Sequence Duration    | —   | —   | 1500 | us   | FIRC_CLK, trimmed during destructive reset phase | —           |

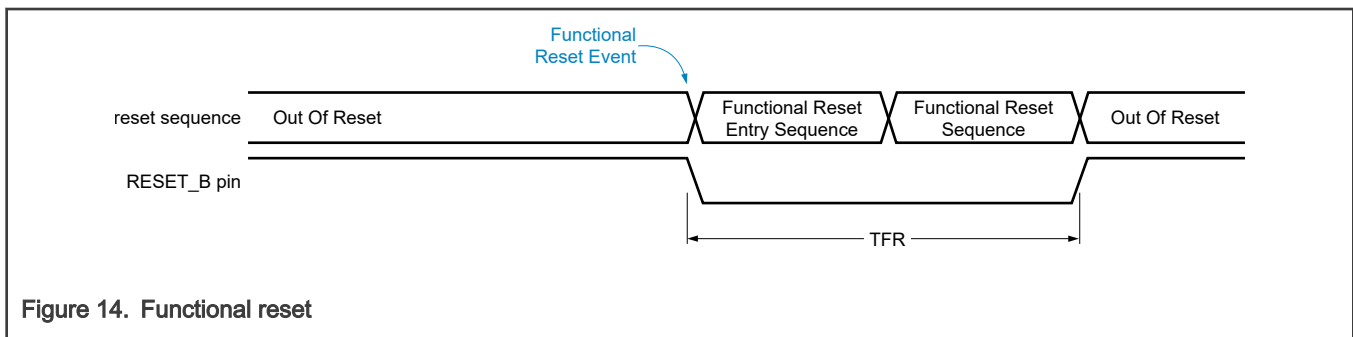
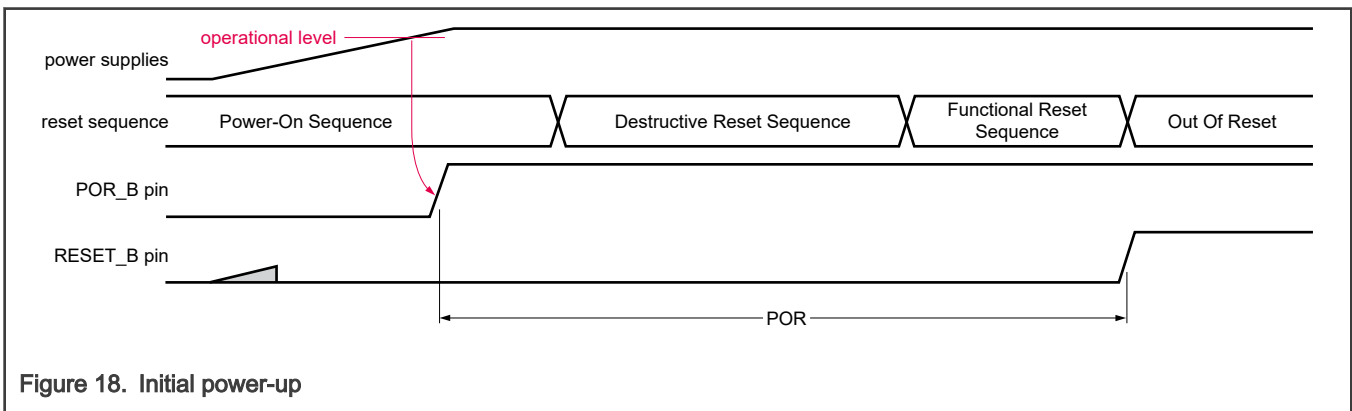
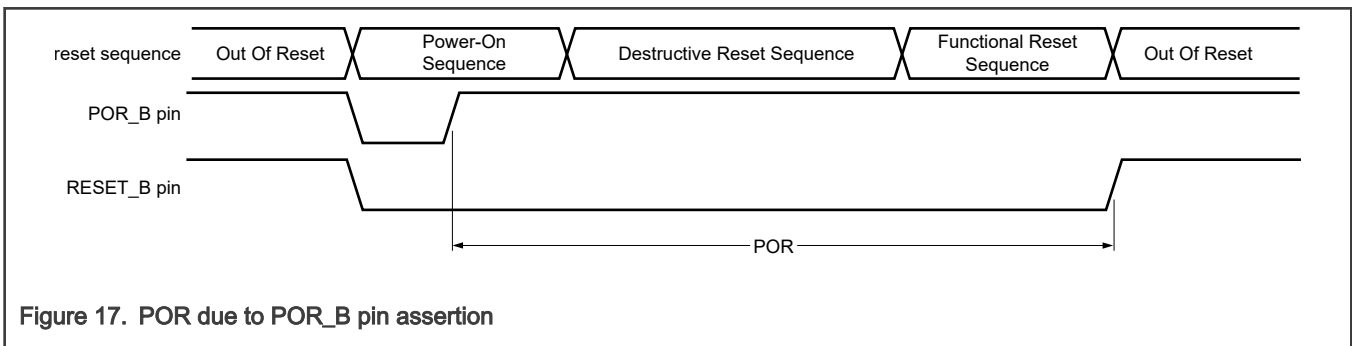
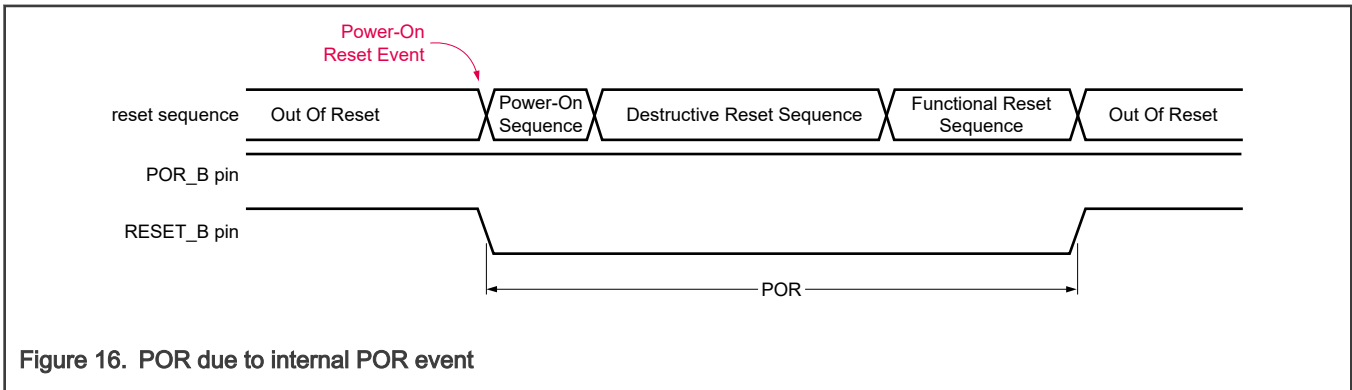
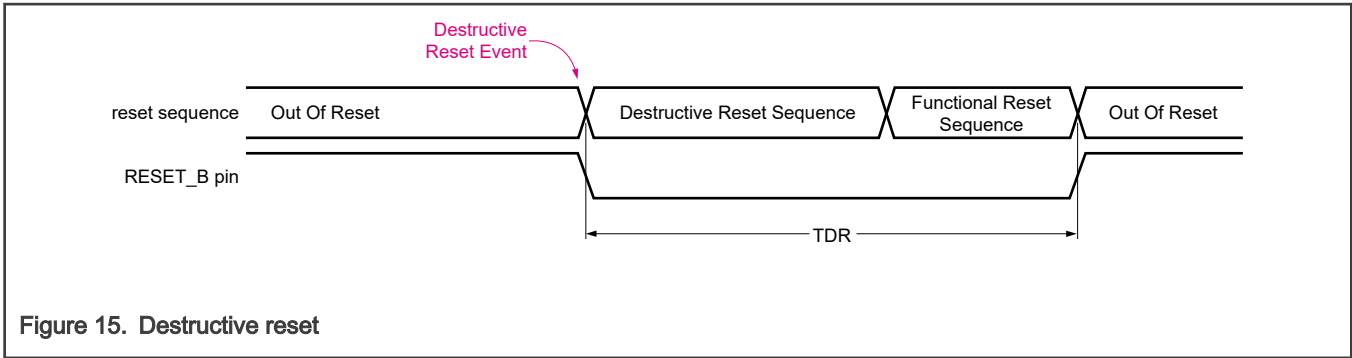


Figure 14. Functional reset



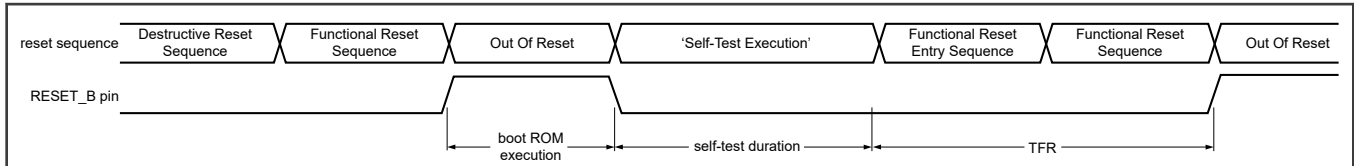


Figure 19. Start-up self-test

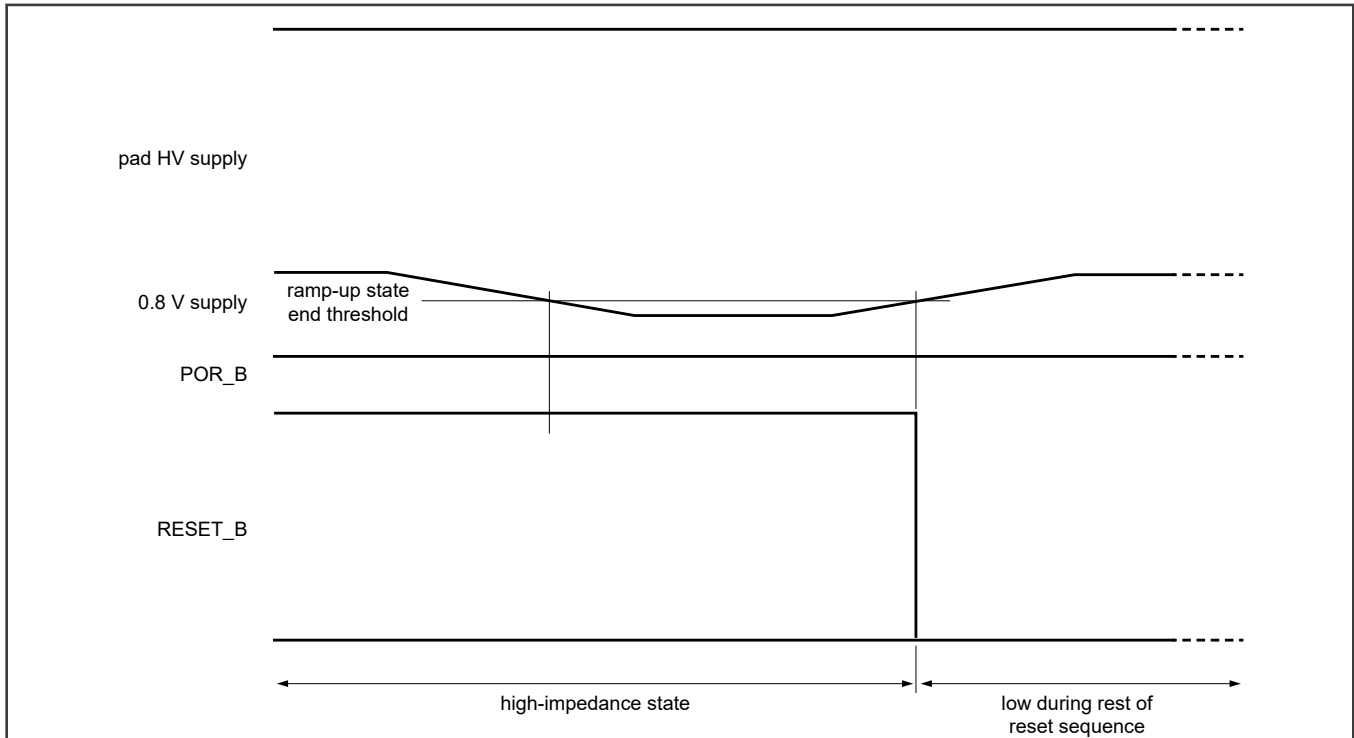
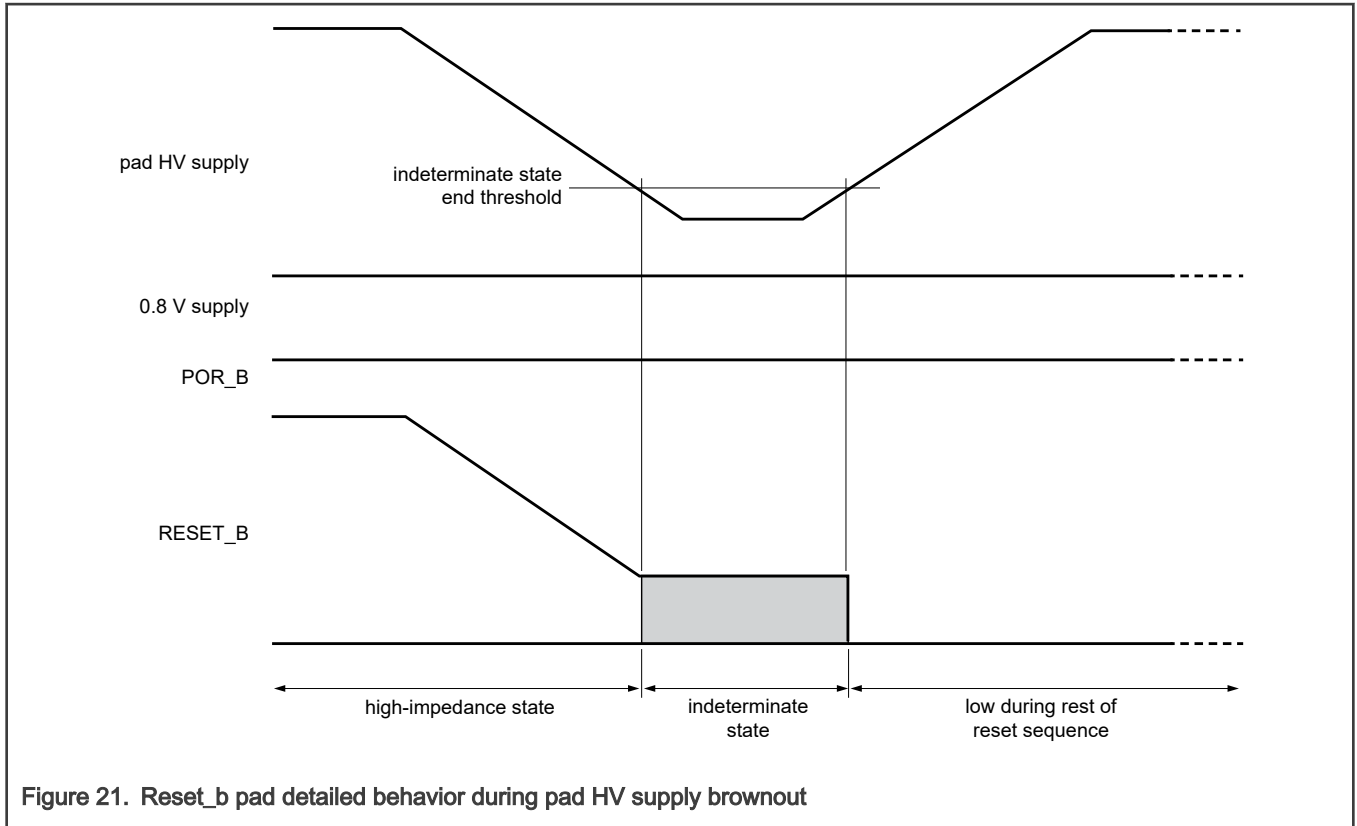
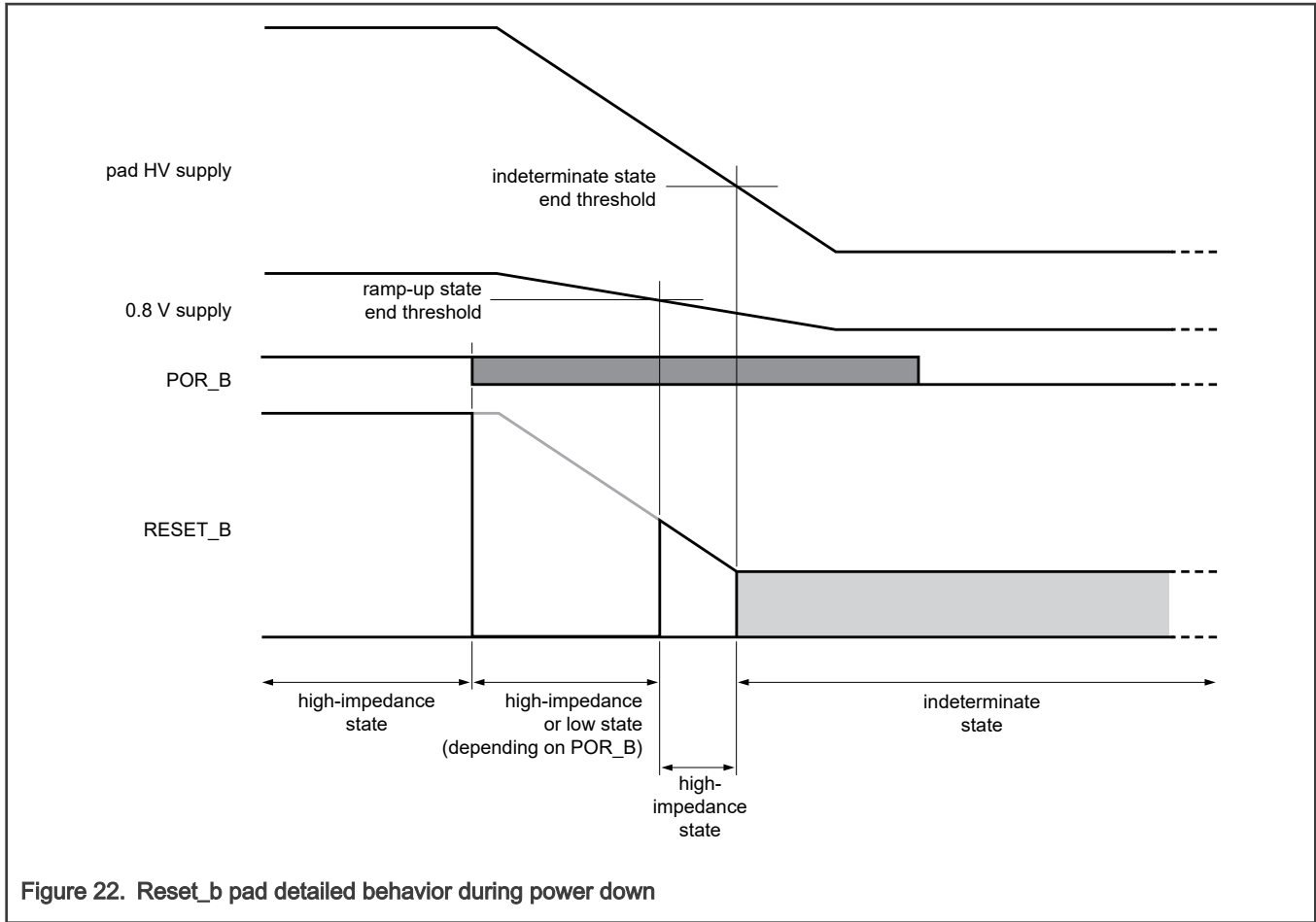


Figure 20. Reset\_b pad detailed behavior during core supply brownout







### 15.2 Reset and Standby related pad electrical characteristics

The following table gives the characteristics of the POR\_B, RESET\_B, PMIC\_STBY\_MODE\_B, and PMIC\_VDD\_OK pads. Values not explicitly listed in this table can be found in the 'GPIO Pads' section.

**Table 18. Reset and Standby related pad electrical characteristics**

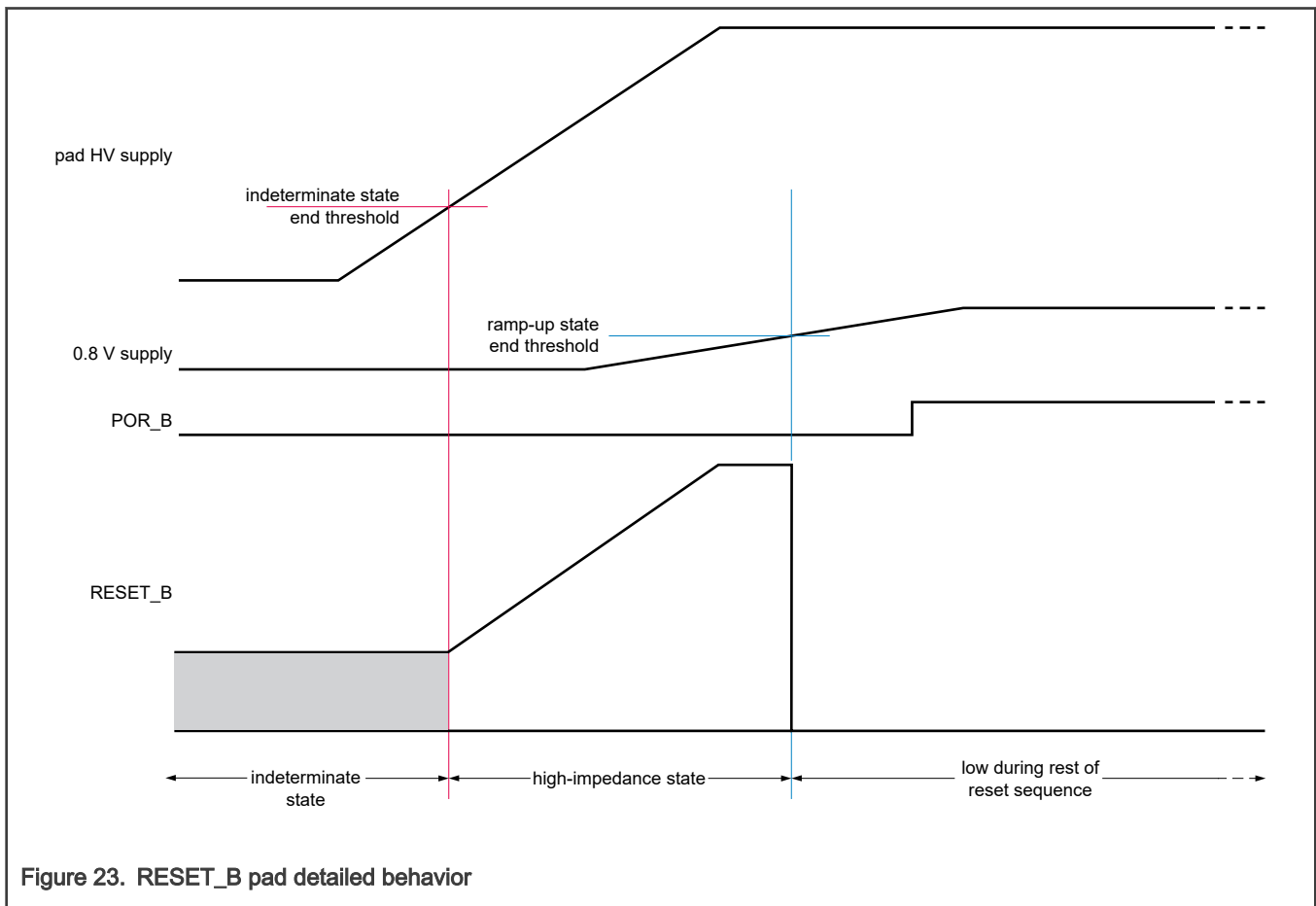
| Symbol        | Description                                   | Min    | Typ  | Max | Unit | Condition                                       | Spec Number |
|---------------|---|--------|------|-----|------|---|-------------|
| ISLEW_POR_B   | POR_B slew rate                               | 30e-06 | —    | 4   | V/ns | —   | —           |
| ISLEW_RESET_B | RESET_B slew rate <sup>1</sup>                | 30e-06 | —    | 4   | V/ns | Noise on RESET_B <100mV peak-peak.              | —           |
| WISE_RESET_B  | RESET_B pad indeterminate state end threshold | —      | 2.35 | —   | V    | See RESET_B pad detailed behavior diagram below | —           |
| VRSE_RESET_B  | RESET_B pad ramp-up state end threshold       | —      | 460  | —   | mV   | See RESET_B pad detailed behavior diagram below | —           |
| WF_RESET_B    | RESET_B input filtered pulse                  | —      | —    | 17  | ns   | —   | —           |

*Table continues on the next page...*

**Table 18. Reset and Standby related pad electrical characteristics (continued)**

| Symbol          | Description                      | Min | Typ | Max | Unit | Condition                 | Spec Number |
|-----------------|----------------------------------|-----|-----|-----|------|---------------------------|-------------|
| WNF_RESET_B     | RESET_B input not filtered pulse | 400 | —   | —   | ns   | —                         | —           |
| MLP_POR_B       | POR_B minimum low pulse          | 5   | —   | —   | us   | —                         | —           |
| MLP_PMIC_VDD_OK | PMIC_VDD_OK minimum low pulse    | 36  | —   | —   | us   | during Standby mode entry | —           |
| MHP_PMIC_VDD_OK | PMIC_VDD_OK minimum high pulse   | 36  | —   | —   | us   | during Standby mode exit  | —           |

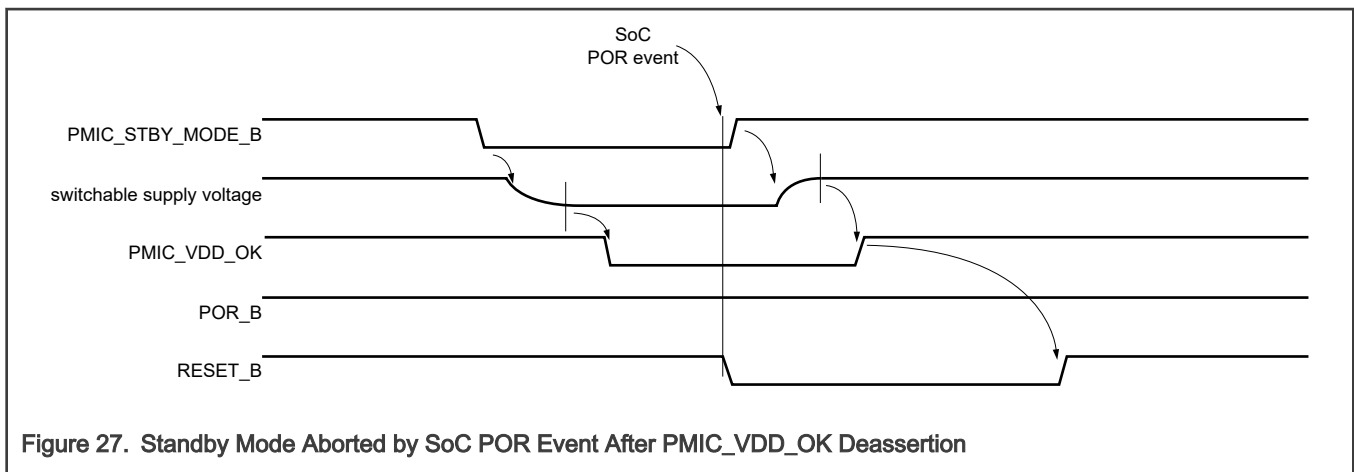
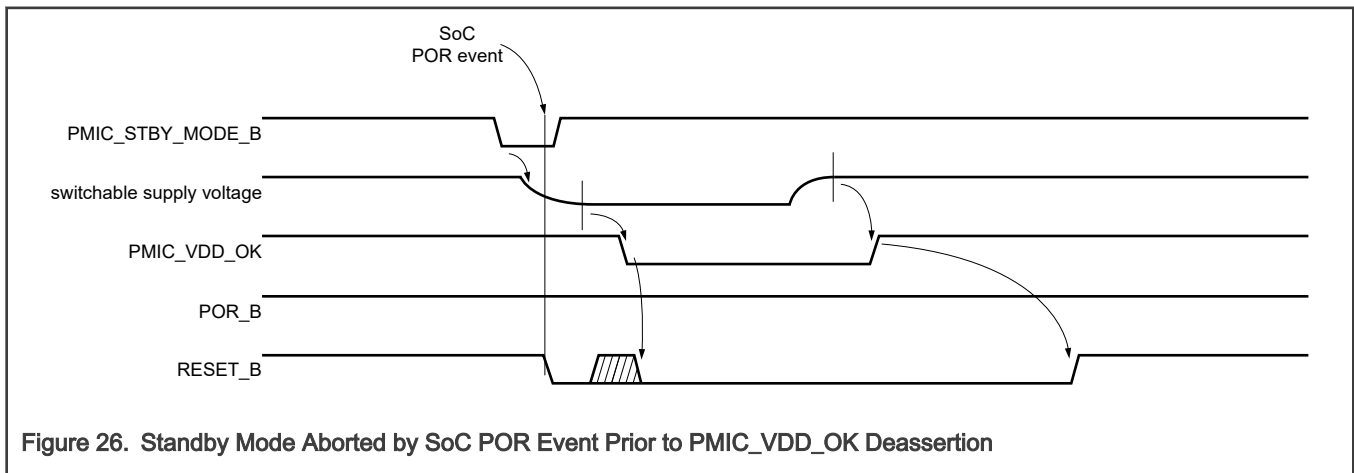
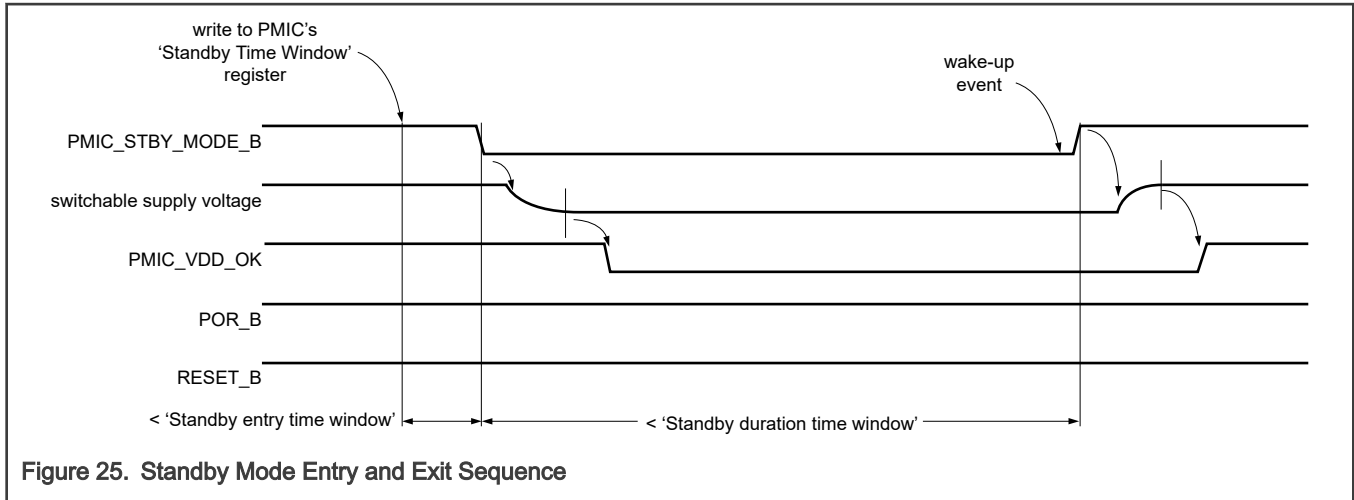
1.  $ISLEW\_RESET\_B(\text{Min}) = \text{MAX}[30\text{e-}06, 0.002 * V_{\text{noise\_p\_p}} * F_{\text{noise}}]$ , where  $V_{\text{noise\_p\_p}}$  is peak-peak noise magnitude (in V) and  $F_{\text{noise}}$  is max noise frequency (in MHz).



**Figure 23. RESET\_B pad detailed behavior**

The RESET\_B pad behavior described in the diagram and the related  $VRSE\_RESET\_B$  parameter spec also apply to the case of core VDD droop after power-up.





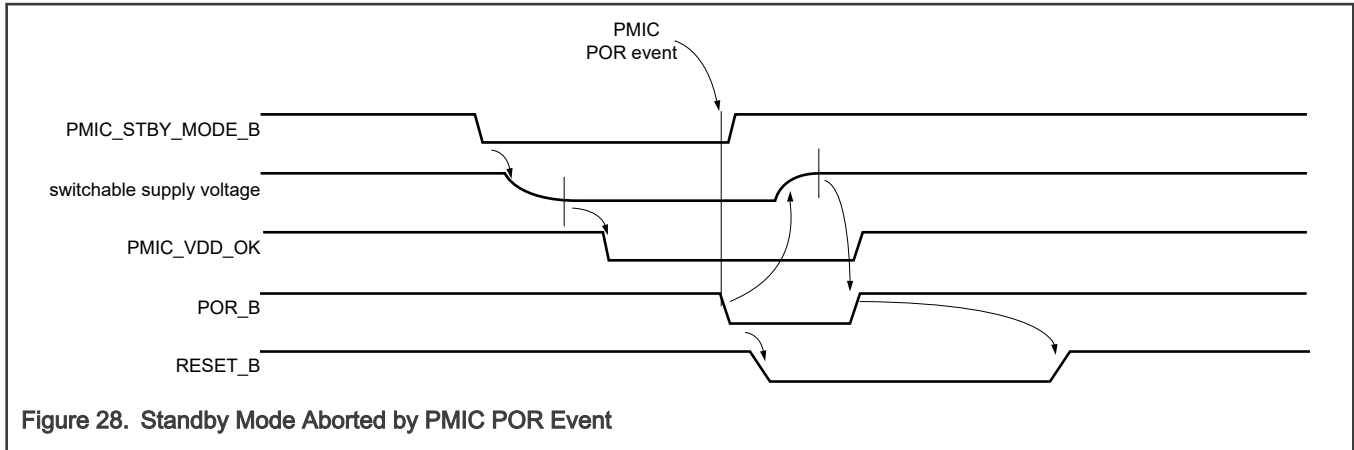


Figure 28. Standby Mode Aborted by PMIC POR Event

## 16 Peripheral specifications

### 16.1 Analog Modules

#### 16.1.1 SAR ADC

ADC performance specifications are only guaranteed when the injection current limits in the operating conditions table of this electrical specification are met.

Although functionally supported on devices with 2 ADCs, ADC performance specifications are not guaranteed for shared channels between the 2 ADCs if the input channel is sampled or converted simultaneously by both ADCs. For best performance in this case, the external capacitance at the input pin and reference pin should be maximized.

Table 19. SAR ADC

| Symbol    | Description                             | Min         | Typ | Max         | Unit | Condition                                 | Spec Number |
|-----------|---|-------------|-----|-------------|------|---|-------------|
| VAD_INPUT | ADC Input Voltage <sup>1</sup>          | VSS_AD<br>C | —   | VDD_AD<br>C | V    | on or off channels                        | —           |
| fAD_CK    | ADC Clock Frequency                     | 20          | —   | 80          | MHz  | —   | —           |
| tSAMPLE   | ADC Input Sampling Time <sup>2</sup>    | 275         | —   | —           | ns   | —   | —           |
| tCONV     | ADC Total Conversion Time <sup>3</sup>  | 1           | —   | —           | us   | —   | —           |
| tRECOVERY | ADC Initialization Time from power-down | —           | —   | 1           | us   | —   | —           |
| CAD_INPUT | ADC Input Capacitance                   | —           | —   | 7           | pF   | ADC component plus pad capacitance (~2pF) | —           |
| RAD_INPUT | ADC Input Series Resistance             | —           | —   | 1.25        | kΩ   | —   | —           |
| OFS       | ADC Offset Error <sup>4</sup>           | -6          | —   | 6           | LSB  | after calibration                         | —           |

Table continues on the next page...

Table 19. SAR ADC (continued)

| Symbol  | Description                                       | Min | Typ | Max | Unit | Condition   | Spec Number |
|---------|---|-----|-----|-----|------|---|-------------|
| GNE     | ADC Gain Error (full scale) <sup>4</sup>          | -6  | —   | 6   | LSB  | after calibration   | —           |
| DNL     | ADC Differential Non-linearity <sup>4, 5, 6</sup> | -1  | —   | 2   | LSB  | after calibration   | —           |
| INL     | ADC Integral Non-linearity <sup>4, 6</sup>        | -3  | —   | 3   | LSB  | after calibration   | —           |
| TUE     | ADC Total Unadjusted Error <sup>4, 6</sup>        | -8  | —   | 8   | LSB  | after calibration   | —           |
| SNR     | Signal-to-Noise Ratio <sup>4</sup>                | —   | 65  | —   | dBFS | input signal frequency <= 50KHz                                   | —           |
| THD     | Total Harmonic Distortion <sup>4</sup>            | —   | 72  | —   | dBFS | Input signal frequency <= 50KHz.                                  | —           |
| IAD_LKG | ADC Input Leakage Current <sup>7</sup>            | -1  | —   | 1   | uA   | TJ = 125C, Dedicated input channel, channel selection switch open | —           |
| IAD_LKG | ADC Input Leakage Current <sup>7</sup>            | -2  | —   | 2   | uA   | TJ = 125C, Shared channel, channel selection switch open          | —           |
| CP1     | ADC input pin capacitance 1                       | —   | —   | 4   | pF   | —   | —           |
| CP2     | ADC input pin capacitance 2                       | —   | —   | 0.5 | pF   | —   | —           |
| CS      | ADC input sampling capacitance                    | —   | —   | 4   | pF   | —   | —           |
| RSW1    | Internal resistance of analog source              | —   | —   | 600 | ohm  | —   | —           |
| RAD     | Internal resistance of analog source              | —   | —   | 150 | ohm  | —   | —           |

1. The reduced limits for VAD\_INPUT in this table are recommended for normal operation.
2. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t<sub>sample</sub>. After the end of the sample time t<sub>sample</sub>, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t<sub>sample</sub> depend on programming.
3. 1Msps is the ADC output rate and includes both sampling and analog to digital conversion.
4. ADC performance specifications are guaranteed when calibration uses maximum averaging i.e. when AVGEN = 1 and NRSMPL = 3.
5. During calibration, the ADC determines its (positive or negative) offset value and stores the result in an internal register. During each conversion, the offset value is subtracted from the raw result to compensate the individual ADC offset. Since the ADC cannot generate negative numbers, a negative calibration offset results in a minimum output code between 0 and 6. A positive calibration offset does not impact the max. code output of 4095. Calibration fails if it determines an offset larger than +/- 6 LSB.
6. This specification is taken with averaging through post process ADC data.
7. The maximum and minimum leakage current values are reached when Vin=VREF and Vin=0, respectively.

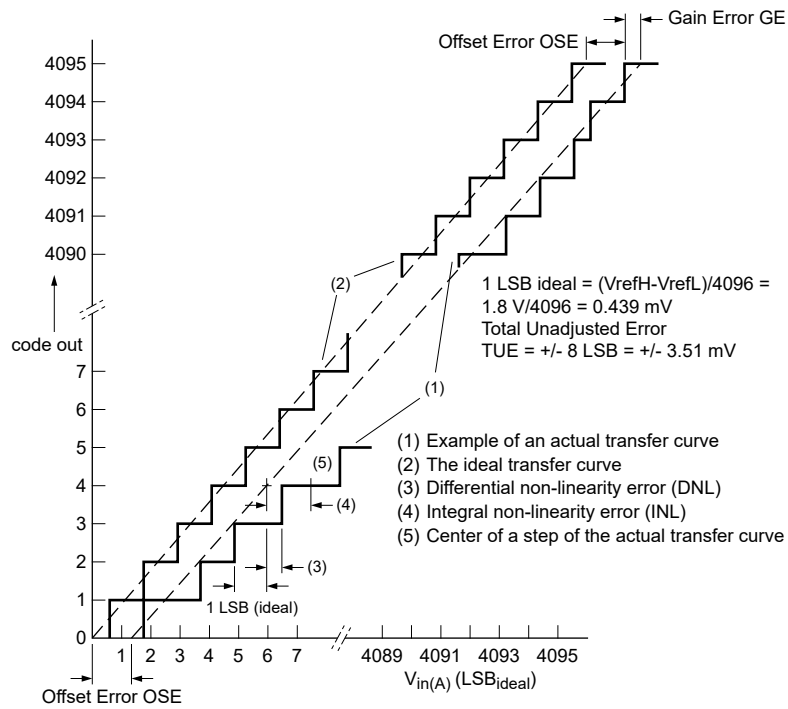


Figure 29. SAR ADC Specification Characteristics

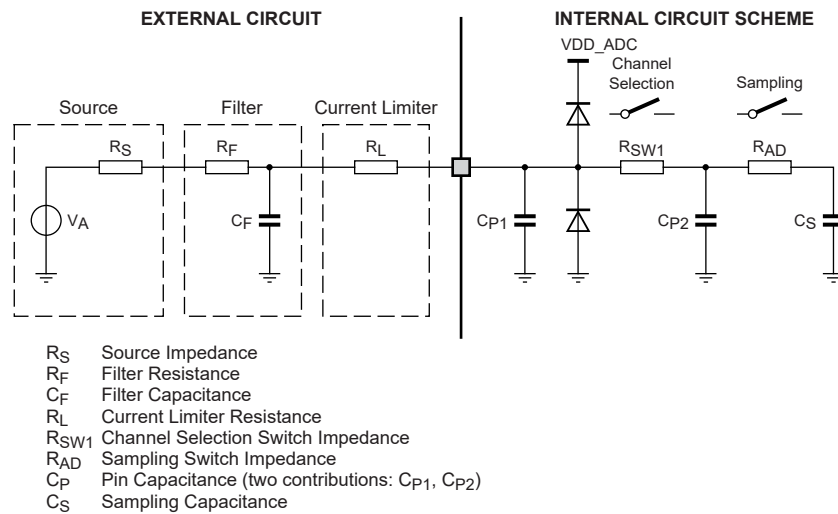


Figure 30. SAR ADC Input Circuit

### 16.1.2 Temperature Monitoring Unit (TMU)

The table below gives the specification for the Temperature Monitoring Unit (TMU). Specifications apply to all remote temperature sensors connected to the TMU on the device.



**Table 20. Temperature Monitoring Unit (TMU)**

| Symbol | Description                               | Min | Typ | Max | Unit | Condition             | Spec Number |
|--------|---|-----|-----|-----|------|-----------------------|-------------|
| TRANGE | Temperature monitoring range <sup>1</sup> | -45 | —   | 130 | C    | —                     | —           |
| TERR   | Temperature sensor error                  | -8  | —   | 8   | C    | TRANGE = -40C to 84C  | —           |
| TERR   | Temperature sensor error                  | -5  | —   | 5   | C    | TRANGE = 85C to 110C  | —           |
| TERR   | Temperature sensor error                  | -3  | —   | 3   | C    | TRANGE = 111C to 125C | —           |

1. Accuracy outside of operating range (-40 to 125) is not guaranteed.

### 16.1.3 Glitch Filter

**Table 21. Glitch Filter**

| Symbol  | Description  | Min | Typ | Max | Unit | Condition | Spec Number |
|---------|--|-----|-----|-----|------|-----------|-------------|
| TFILT   | Glitch filter max filtered pulse width <sup>1, 2, 3, 4</sup>   | —   | —   | 17  | ns   | —         | —           |
| TUNFILT | Glitch filter min unfiltered pulse width <sup>2, 3, 4, 5</sup> | 400 | —   | —   | ns   | —         | —           |

1. Pulses shorter than defined by the maximum value are guaranteed to be filtered (not passed).
2. Pulses in between the max filtered and min unfiltered may or may not be passed through.
3. See the device reference manual for which package pins include glitch filters on the pin input.
4. An input signal pulse is defined by the duration between the input signal's crossing of a  $V_{il}/V_{ih}$  threshold voltage level, and the next crossing of the opposite level.
5. Pulses larger than defined by the minimum value are guaranteed to not be filtered (passed).

### 16.1.4 IRQ

The following table gives the input specifications for the external interrupt pins.

tCYC refers to FIRC\_CLK.

**Table 22. IRQ**

| Symbol | Description          | Min | Typ | Max | Unit | Condition  | Spec Number |
|--------|----------------------|-----|-----|-----|------|------------|-------------|
| tIPWL  | IRQ pulse width low  | 4   | —   | —   | tCYC | MAXCNT = 3 | 1           |
| tIPWH  | IRQ pulse width high | 4   | —   | —   | tCYC | MAXCNT = 3 | 2           |

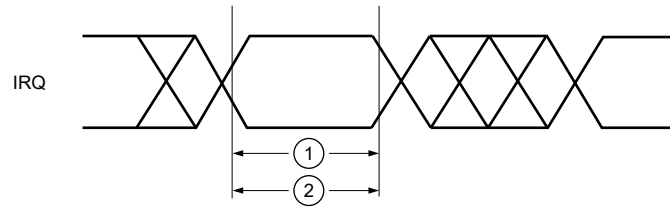


Figure 31. External Interrupt Timing (IRQ)

## 16.2 Clock and PLL Interfaces

### 16.2.1 DFS

The following table specifies the output frequency ranges and characteristics of the Digital Frequency Synthesizer (DFS).

Table 23. DFS

| Symbol         | Description                             | Min  | Typ | Max  | Unit | Condition                      | Spec Number |
|----------------|---|------|-----|------|------|--------------------------------|-------------|
| fDFS_CORE_CLK1 | Core DFS Output Clock 1 Frequency       | 40   | —   | 800  | MHz  | CORE_DFS1                      | —           |
| fDFS_PER_CLK1  | Peripheral DFS Output Clock 1 Frequency | 532  | —   | 800  | MHz  | PERIPH_DFS1                    | —           |
| fDFS_PER_CLK2  | Peripheral DFS Output Clock 2 Frequency | 40   | —   | 628  | MHz  | PERIPH_DFS2                    | —           |
| fDFS_PER_CLK3  | Peripheral DFS Output Clock 3 Frequency | 416  | —   | 800  | MHz  | PERIPH_DFS3                    | —           |
| fDFS_CLKIN     | DFS Input Clock Frequency               | 1300 | —   | 2622 | MHz  | —                              | —           |
| PER_jitter     | DFS Period Jitter <sup>1, 2</sup>       | -30  | —   | 30   | ps   | Even MFN                       | —           |
| PER_jitter     | DFS Period Jitter <sup>1, 2</sup>       | -45  | —   | 45   | ps   | fDFS_CLKIN = 2000 MHz, Odd MFN | —           |
| PER_Jitter     | DFS Period Jitter <sup>1, 2</sup>       | -30  | —   | 30   | ps   | fDFS_CLKIN = 2622 MHz, Odd MFN | —           |
| PER_jitter     | DFS Period Jitter <sup>1, 2</sup>       | -60  | —   | 60   | ps   | fDFS_CLKIN = 1300 MHz, Odd MFN | —           |

- For SoC clocks that are further divided down from the DFS output clock, the jitter is multiplied by a factor of  $\sqrt{N}$ , where N is the ratio of the DFS output clock and destination clock periods.
- Jitter value does not apply when the DFS clock is output on an external pin. In this case, the rise and fall time variations in the I/O pad are orders of magnitude more than the DFS and SoC mux jitter contributions.

Peripheral DFS output clock min jitter= $\text{Min}(\text{PER\_jitter}(\text{PLL})) \times (\text{sqrt}(\text{N})) + \text{Min}(\text{PER\_jitter}(\text{DFS}))$ . Peripheral DFS output clock max jitter= $\text{Max}(\text{PER\_jitter}(\text{PLL})) \times (\text{sqrt}(\text{N})) + \text{Max}(\text{PER\_jitter}(\text{DFS}))$ . Where N is the DFS division factor. All jitter numbers are in ps.

## 16.2.2 FIRC

Table 24. FIRC

| Symbol | Description                           | Min | Typ | Max | Unit | Condition                        | Spec Number |
|--------|---------------------------------------|-----|-----|-----|------|----------------------------------|-------------|
| fFIRC  | FIRC Target Frequency                 | —   | 48  | —   | MHz  | —                                | —           |
| δfVAR  | FIRC Frequency Variation <sup>1</sup> | -5  | —   | 5   | %    | Trimmed                          | —           |
| TSTART | Startup Time                          | —   | 10  | 20  | us   | After valid supply level reached | —           |

1. δfVAR defines how much the output frequency can shift over the specified temperature and voltage ranges of the device after initial factory trim.

## 16.2.3 SIRC

Table 25. SIRC

| Symbol | Description                           | Min | Typ | Max | Unit | Condition  | Spec Number |
|--------|---------------------------------------|-----|-----|-----|------|--|-------------|
| fSIRC  | SIRC Target Frequency Trimmed         | —   | 32  | —   | KHz  | Trimmed  | —           |
| PTA    | SIRC Trimming Resolution <sup>1</sup> | -1  | —   | 1   | %    | Trimmed 32KHz, 25C, 0.8V Core  | —           |
| δfVAR  | SIRC Frequency Variation <sup>2</sup> | -5  | —   | 5   | %    | Frequency variation across voltage and temperature range after trimming. | —           |
| TSTART | SIRC Startup Time                     | —   | —   | 50  | us   | —  | —           |

1. PTA defines how close the output frequency is to target after the initial factory trim.  
 2. δfVAR defines how much the output frequency can shift over the specified temperature and voltage ranges of the device.

## 16.2.4 FXOSC

Table 26. FXOSC

| Symbol    | Description                           | Min          | Typ | Max        | Unit | Condition                | Spec Number |
|-----------|---------------------------------------|--------------|-----|------------|------|--------------------------|-------------|
| fXTAL     | Input Frequency Range <sup>1, 2</sup> | 20           | —   | 40         | MHz  | Crystal mode             | —           |
| TCST      | Crystal Startup Time                  | —            | —   | 2          | ms   | Crystal mode             | —           |
| fBYP_SE   | FXOSC Bypass Frequency <sup>3</sup>   | —            | 40  | —          | MHz  | single-ended bypass mode | —           |
| VIH_EXTAL | EXTAL Input High Level <sup>4</sup>   | VCM_SE + 0.3 | —   | VDD_FX OSC | V    | Single-ended bypass mode | —           |

*Table continues on the next page...*

**Table 26. FXOSC (continued)**

| Symbol            | Description   | Min  | Typ            | Max          | Unit | Condition  | Spec Number |
|-------------------|---|------|----------------|--------------|------|--|-------------|
| VIL_EXTAL         | EXTAL Input Low Level <sup>4</sup>                    | 0    | —              | VCM_SE - 0.3 | V    | Single-ended bypass mode                               | —           |
| CLOAD             | XTAL/EXTAL pin load capacitance <sup>5</sup>          | —    | 8              | —            | pF   | Crystal mode   | —           |
| CS_XTAL           | XTAL/EXTAL pin on-chip stray capacitance <sup>5</sup> | —    | —              | 3            | pF   | —  | —           |
| VCM_SE            | Common Mode Voltage for Single ended Bypass           | —    | VDD_FX OSC / 2 | —            | mV   | —  | —           |
| Leakage_injection | EXTAL injection current                               | -50  | —              | 100          | nA   | Mean current flowing into EXTAL in crystal mode        | —           |
| Leakage_extal     | External Leakage on EXTAL Pin                         | -20  | —              | 20           | nA   | Bypass mode, 0.5V                                      | —           |
| EXTAL_AMP         | EXTAL_amplitude (p k-pk)                              | 300  | —              | 900          | mV   | Crystal mode   | —           |
| LT_Jitter         | Long term jitter                                      | -120 | —              | 120          | ps   | gm_sel=1111 with 40MHz crystal (NX5032GA and NX3225GA) | —           |

1. Recommended crystal frequencies are 20MHz, 24MHz, and 40MHz.
2. All specifications only valid for this frequency range if the correct FXOSC transconductance setting is used.
3. The input clock must be 40 MHz nominal frequency.
4. The input clock signal should be symmetric around common mode voltage.
5. Account for on-chip stray capacitance (CS\_XTAL) and PCB capacitance in the total XTAL/EXTAL pin load capacitance. CS\_XTAL don't include miller capacitance.

In crystal mode NX5032GA crystal at 20 MHz has a load cap of 8 pF and configure gm\_sel[3:0]=4'b0100 and NX3225GA crystal has a load cap of 8 pF and configure gm\_sel[3:0]=4'b100.

In crystal mode NX5032GA crystal at 24 MHz has a load cap of 8 pF and configure gm\_sel[3:0]=4'b0101 and NX3225GA has a load cap of 8 pF and configure gm\_sel[3:0]=4'b0110.

In crystal mode NX5032GA and NX3225GA crystal at 40 MHz (ALC enable) has a load cap of 8 pF and configure gm\_sel[3:0]=4'b1111.

In ALC disable mode the minimum crystal drive level should be greater than 500uW.

Duty cycle of the FXOSC clock when output on either the single-ended or LVDS CLKOUT pins is given in the I/O pad specifications.

See Hardware design guide for the recommended circuit for each mode.

RGMII specifications require clock source to have tolerance of +/- 50ppm. When using this mode, the crystal selected for system clock (FXOSC) should adhere to this specification.

## 16.2.5 PLL

The following table gives the operating frequencies and characteristics of the PLL, and applies to instances on the device. Actual operating frequencies for the device are constrained to the values given below.

PLL refers to the Core, Peripheral, Accelerator, and DDR reference PLLs on the device.

Spread spectrum clock modulation is only available on the Core, Accelerator and DDR reference PLLs.

**Table 27. PLL**

| Symbol          | Description   | Min  | Typ | Max  | Unit | Condition   | Spec Number |
|-----------------|---|------|-----|------|------|---|-------------|
| fPLL_CLKIN      | PLL Input Clock Frequency <sup>1</sup>              | 20   | —   | 100  | MHz  | Before PLL input divider.                         | —           |
| fPLL_CLKIN_PFD  | PLL Phase Detector Clock Frequency <sup>2</sup>     | 20   | —   | 40   | MHz  | After PLL input divider.                          | —           |
| fPLL_CORE_VCO   | Core PLL VCO Frequency Range <sup>3, 4, 5, 6</sup>  | 1300 | —   | 2622 | MHz  | without center-spread SSCG enabled                | —           |
| fPLL_CORE_PHI0  | Core PLL PHI0 Frequency <sup>5</sup>                | —    | —   | 1311 | MHz  | CORE_PLL_PHI0, without center-spread SSCG enabled | —           |
| fPLL_PER_VCO    | Peripheral PLL VCO Frequency Range                  | 1300 | —   | 2000 | MHz  | —   | —           |
| fPLL_PER_PHI0   | Peripheral PLL PHI0 Frequency                       | 100  | —   | 125  | MHz  | PERIPH_PLL_PHI0                                   | —           |
| fPLL_PER_PHI1   | Peripheral PLL PHI1 Frequency                       | —    | —   | 80   | MHz  | PERIPH_PLL_PHI1                                   | —           |
| fPLL_PER_PHI2   | Peripheral PLL PHI2 Frequency                       | 40   | —   | 80   | MHz  | PERIPH_PLL_PHI2                                   | —           |
| fPLL_PER_PHI3   | Peripheral PLL PHI3 Frequency                       | —    | —   | 133  | MHz  | PERIPH_PLL_PHI3                                   | —           |
| fPLL_PER_PHI4   | Peripheral PLL PHI4 Frequency                       | —    | —   | 200  | MHz  | PERIPH_PLL_PHI4                                   | —           |
| fPLL_PER_PHI5   | Peripheral PLL PHI5 Frequency                       | —    | —   | 125  | MHz  | PERIPH_PLL_PHI5                                   | —           |
| fPLL_PER_PHI7   | Peripheral PLL PHI7 Frequency                       | —    | —   | 100  | MHz  | PERIPH_PLL_PHI7                                   | —           |
| fPLL_ACCEL_VCO  | Accelerator PLL VCO Frequency Range <sup>5, 6</sup> | 1300 | —   | 2400 | MHz  | without center-spread SSCG enabled                | —           |
| fPLL_ACCEL_PHI1 | Accelerator PLL PHI1 Frequency <sup>5</sup>         | —    | —   | 600  | MHz  | ACCEL_PHI1, without center-spread SSCG enabled    | —           |

*Table continues on the next page...*

Table 27. PLL (continued)

| Symbol        | Description   | Min   | Typ | Max   | Unit | Condition   | Spec Number |
|---------------|---|-------|-----|-------|------|---|-------------|
| fPLL_DDR_VCO  | DDR PLL VCO Frequency Range <sup>5, 6, 7</sup>          | 1300  | —   | 1600  | MHz  | without center-spread SSCG enabled                                  | —           |
| fPLL_DDR_PHI0 | DDR PLL PHI0 Frequency <sup>5, 8</sup>                  | 800   | —   | 800   | MHz  | DDR_CLK (3200 MT/s), without center-spread SSCG enabled             | —           |
| fPLL_DDR_PHI0 | DDR PLL PHI0 Frequency <sup>8</sup>                     | 758   | —   | 758   | MHz  | DDR_CLK (3032 MT/s)   | —           |
| fPLL_DDR_PHI0 | DDR PLL PHI0 Frequency <sup>8</sup>                     | 666.5 | —   | 666.5 | MHz  | DDR_CLK (2666 MT/s)   | —           |
| fPLL_DDR_PHI0 | DDR PLL PHI0 Frequency <sup>8</sup>                     | 533.3 | —   | 533.3 | MHz  | DDR_CLK (2133 MT/s)   | —           |
| fPLL_DDR_PHI0 | DDR PLL PHI0 Frequency <sup>8</sup>                     | 466.6 | —   | 466.6 | MHz  | DDR_CLK (1866 MT/s)   | —           |
| fPLL_DDR_PHI0 | DDR PLL PHI0 Frequency <sup>8</sup>                     | 400   | —   | 400   | MHz  | DDR_CLK (1600 MT/s)   | —           |
| tLOCK         | System PLL Lock Time                                    | —     | —   | 100   | us   | —   | —           |
| PER_jitter    | System PLL Period Jitter <sup>9, 10, 11, 12</sup>       | -23   | —   | 23    | ps   | fPLL_CLKIN = 40MHz, fVCO = 2GHz, 6-sigma, SSCG & Frac mode disabled | —           |
| LT_jitter     | System PLL Long Term Jitter <sup>10, 12, 13</sup>       | -120  | —   | 120   | ps   | Saturated, 6-sigma  | —           |
| fPLL_MOD      | Spread Spectrum Clock Modulation Frequency <sup>7</sup> | 30    | —   | 64    | KHz  | —   | —           |

1. This refers to spec number 1 which is shown in the figure in Aurora port specifications
2. This specification is PLL input reference clock frequency after pre-divider.
3. Duty cycle of the system PLL clock when output on an external pin is given in the I/O pad specifications.
4. The frequencies are the nominal frequencies (i.e., what the PLL's VCO is configured to).
5. The max frequency in case of center-spread SSCG enabled for a modulation depth can be calculated as: Max frequency(with center-spread SSCG disabled) – (Modulation Depth(in %)/(2\*100))\* Max frequency (with center-spread SSCG disabled). For details, see section “Frequency modulation programming” in reference manual.
6. Same min frequency value applies for center-spread SSCG enabled as provided for center-spread SSCG disabled.
7. DDR PLL allows center-spread SSCG at fPLL\_MOD 32KHz @2% MD (modulation depth) and fPLL\_MOD 64KHz @ 1% MD
8. The DDR PHY internally multiplies the PLL\_DDR\_PHI0 by factor of two.
9. For chip clocks that are further divided down from the PLL output clock, the jitter is multiplied by a factor of SQRT(N), where N is the ratio of the PLL output clock and destination clock periods.
10. Jitter value does not apply when a PLL clock is output on an external pin. In this case, the rise and fall time variations in the I/O pad are orders of magnitude more than the PLL and SoC mux jitter contributions.
11. Jitter is dependent on the period of the PLL output clock, and the division ratio of the clock at the destination module.
12. Jitter is dependent on supply noise. Specified jitter values are valid for the FXOSC reference clock input only - not valid for FIRC reference clock input.
13. This specification is valid when all clock sources are stable.

**NOTE**

fPLL\_DDR\_PHI0 frequencies and data rate mentioned in this table are for LPDDR4. DDR3L frequencies and data rates are half of the LPDDR4.

### 16.3 Communication modules

#### 16.3.1 SPI

Table 28. SPI

| Symbol | Description                          | Min                            | Typ | Max   | Unit | Condition                            | Spec Number |
|--------|--------------------------------------|--------------------------------|-----|-------|------|--------------------------------------|-------------|
| tSCK   | SPI cycle time <sup>1,2</sup>        | 40                             | —   | 10000 | ns   | Master, MTFE=0                       | 1           |
| tSCK   | SPI cycle time <sup>1</sup>          | 25                             | —   | 10000 | ns   | Master, MTFE=1                       | 1           |
| tSCK   | SPI cycle time <sup>1,3</sup>        | 16.67                          | —   | 10000 | ns   | Slave Receive Mode                   | 1           |
| tSCK   | SPI cycle time <sup>1</sup>          | 40                             | —   | 10000 | ns   | Slave Transmit Mode                  | 1           |
| tCSC   | PCS to SCK delay <sup>4</sup>        | 20                             | —   | 10000 | ns   | —                                    | 2           |
| tASC   | After SCK delay <sup>5</sup>         | 20                             | —   | 10000 | ns   | —                                    | 3           |
| tSDC   | SCK duty cycle                       | 40                             | —   | 60    | %    | —                                    | 4           |
| tA     | Slave access time                    | —                              | —   | 40    | ns   | SS active to SOUT valid              | 5           |
| tDIS   | Slave SOUT disable time              | —                              | —   | 15    | ns   | SS inactive to SOUT hi-z or invalid  | 6           |
| tPCSC  | PCSx to PCSS time                    | 13                             | —   | —     | ns   | —                                    | 7           |
| tPASC  | PCSS to PCSx time                    | 13                             | —   | —     | ns   | —                                    | 8           |
| tSUI   | Input data setup time <sup>6,7</sup> | 15                             | —   | —     | ns   | Master, MTFE=0                       | 9           |
| tSUI   | Input data setup time <sup>6,8</sup> | 15 - N * ipg_clk_d spi_perio d | —   | —     | ns   | Master, MTFE=1, CPHA=0, SMPL_PTR = 1 | 9           |
| tSUI   | Input data setup time <sup>6</sup>   | 15                             | —   | —     | ns   | Master, MTFE=1, CPHA=1, SMPL_PTR = 1 | 9           |
| tSUI   | Input data setup time <sup>6</sup>   | 2                              | —   | —     | ns   | Slave Receive Mode                   | 9           |
| tHI    | Input data hold time <sup>6</sup>    | 0                              | —   | —     | ns   | Master, MTFE=0                       | 10          |
| tHI    | Input data hold time <sup>6</sup>    | 0 + N * ipg_clk_d spi_perio d  | —   | —     | ns   | Master, MTFE=1, CPHA=0, SMPL_PTR = 1 | 10          |

Table continues on the next page...

Table 28. SPI (continued)

| Symbol | Description   | Min                                 | Typ | Max                                | Unit | Condition  | Spec Number |
|--------|---|-------------------------------------|-----|------------------------------------|------|--|-------------|
| tHI    | Input data hold time <sup>6</sup>                       | 0                                   | —   | —                                  | ns   | Master, MTFE=1, CPHA=1, SMPL_PTR = 1   | 10          |
| tHI    | Input data hold time <sup>6</sup>                       | 4                                   | —   | —                                  | ns   | Slave Receive Mode   | 10          |
| tSUO   | Output data valid time (after SCK edge) <sup>9</sup>    | —                                   | —   | 5                                  | ns   | Master, MTFE=0 max CLOAD=25pF, max pad drive setting, SRE[2:0] = 101         | 11          |
| tSUO   | Output data valid time (after SCK edge) <sup>9</sup>    | —                                   | —   | 5 +<br>ipg_clk_d<br>spi_perio<br>d | ns   | Master, MTFE=1, CPHA=0 max CLOAD=25pF, max pad drive setting, SRE[2:0] = 101 | 11          |
| tSUO   | Output data valid time (after SCK edge) <sup>9</sup>    | —                                   | —   | 5                                  | ns   | Master, MTFE=1, CPHA=1 max CLOAD=25pF, max pad drive setting, SRE[2:0] = 101 | 11          |
| tSUO   | Output data valid time (after SCK edge) <sup>7, 9</sup> | —                                   | —   | 16                                 | ns   | Slave Transmit Mode, SRE[2:0] = 101  | 11          |
| tHO    | Output data hold time <sup>9</sup>                      | -2                                  | —   | —                                  | ns   | Master, MTFE=0 max CLOAD=25pF, max pad drive setting, SRE[2:0] = 101         | 12          |
| tHO    | Output data hold time <sup>9</sup>                      | -2 +<br>ipg_clk_d<br>spi_perio<br>d | —   | —                                  | ns   | Master, MTFE=1, CPHA=0 max CLOAD=25pF, max pad drive setting, SRE[2:0] = 101 | 12          |
| tHO    | Output data hold time <sup>9</sup>                      | -2                                  | —   | —                                  | ns   | Master, MTFE=1, CPHA=1 max CLOAD=25pF, max pad drive setting, SRE[2:0] = 101 | 12          |
| tHO    | Output data hold time <sup>9</sup>                      | 3                                   | —   | —                                  | ns   | Slave Transmit Mode, SRE[2:0] = 101  | —           |

1. The maximum SPI baud rate that is achievable in a dedicated master-slave connection depends on several parameters that are independent of the SPI module clocking capabilities (e.g. capacitive load of the signal lines, SPI slave clock-to-data delay, pad slew rate, etc.). The maximum achievable SPI baud rate needs to be evaluated in a corresponding SPI master-slave setup.
2. SMPL\_PTR should be set to 1. For SPI\_CTARN[BR] - 'Baud Rate Scaler' configuration is  $\geq 3$
3. Slave Receive Mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.



4. This value of 20 ns is with the configuration prescaler values: SPI\_CTARn[PCSSCK] - "PCS to SCK Delay Prescaler" configuration is "3" (01h) and SPI\_CTARn[CSSCK] - "PCS to SCK Delay Scaler" configuration is "2" (0000h)
5. This value of 20 ns is with the configuration prescaler values: SPI\_CTARn[PASC] - "After SCK Delay Prescaler" configuration is "3" (01h) and SPI\_CTARn[ASC] - "After SCK Delay Scaler" configuration is "2" (0000h)
6. Input timing assumes an input signal slew rate of 2ns (20%/80%).
7. For the case of both master and slave being NXP S32x devices, frequency of operation will be reduced to  $[1000 / 2 * \{t_{SUI\_master} + t_{SUO\_slave} + PCB\ delay\}]$  in ns.
8. N is number of protocol clock cycles where the master samples SIN in MTFE mode after SCK edge.
9. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the R<sub>DSO</sub>N of the I/O pad output driver.

Slave mode timing values given below are applicable when device is in MTFE=0.

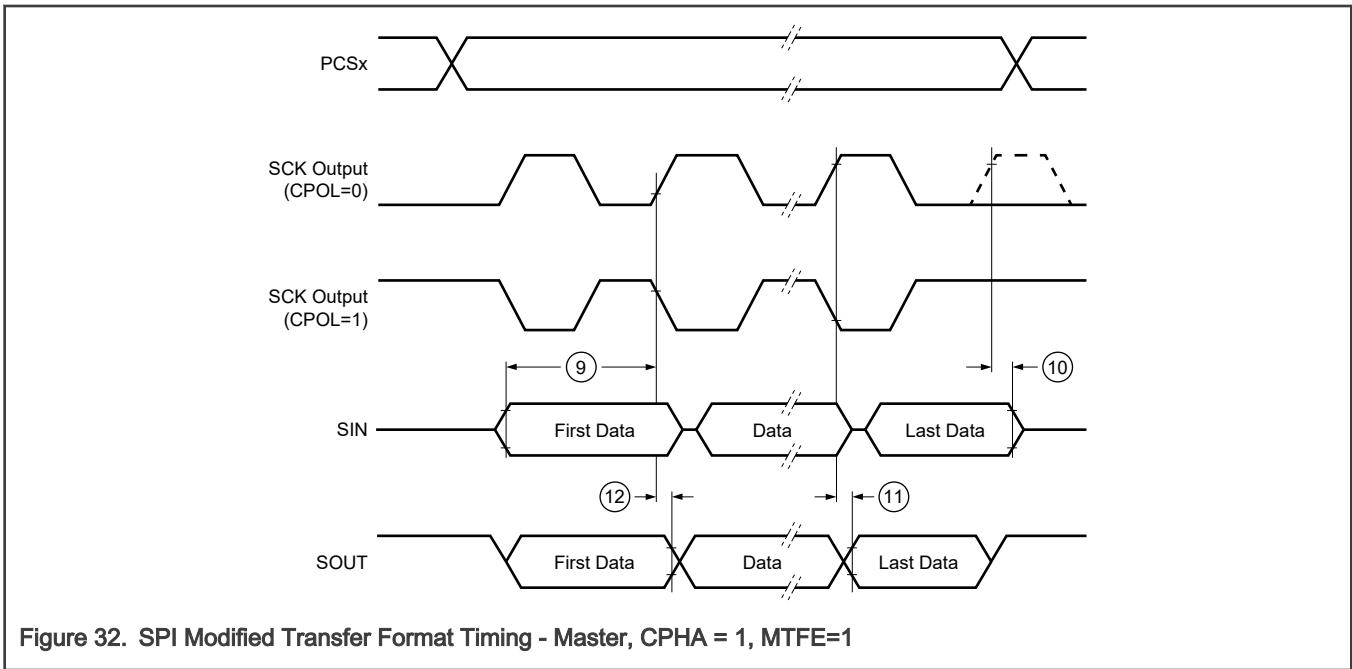


Figure 32. SPI Modified Transfer Format Timing - Master, CPHA = 1, MTFE=1

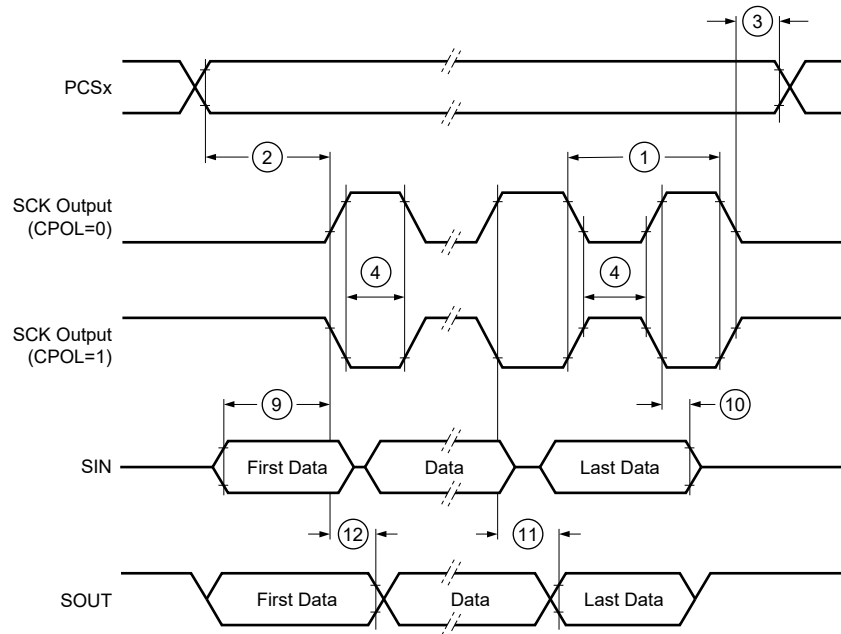


Figure 33. SPI Modified Transfer Format Timing - Master, CPHA = 0, MTFE=1

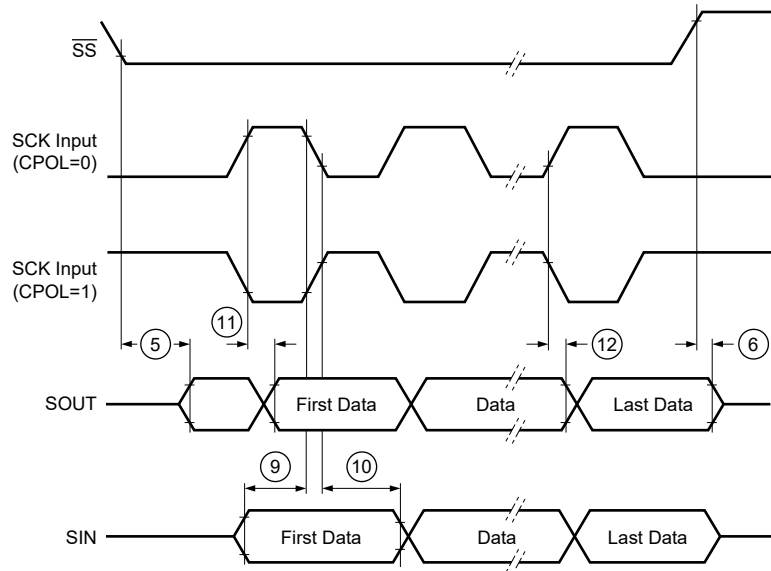


Figure 34. SPI Classic Timing - Slave CPHA = 1, MTFE=0

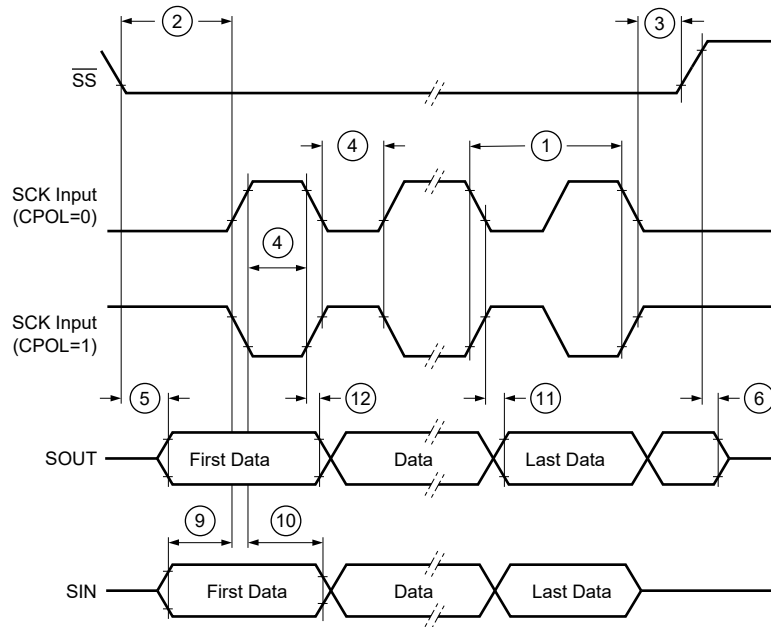


Figure 35. SPI Classic Timing - Slave CPHA = 0, MTFE=0

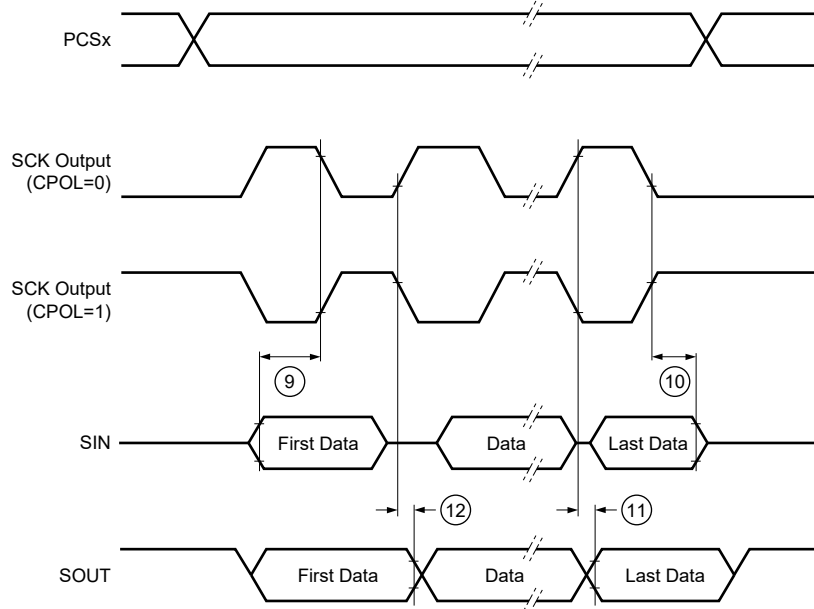


Figure 36. SPI Classic Timing - Master, CPHA = 1, MTFE=0

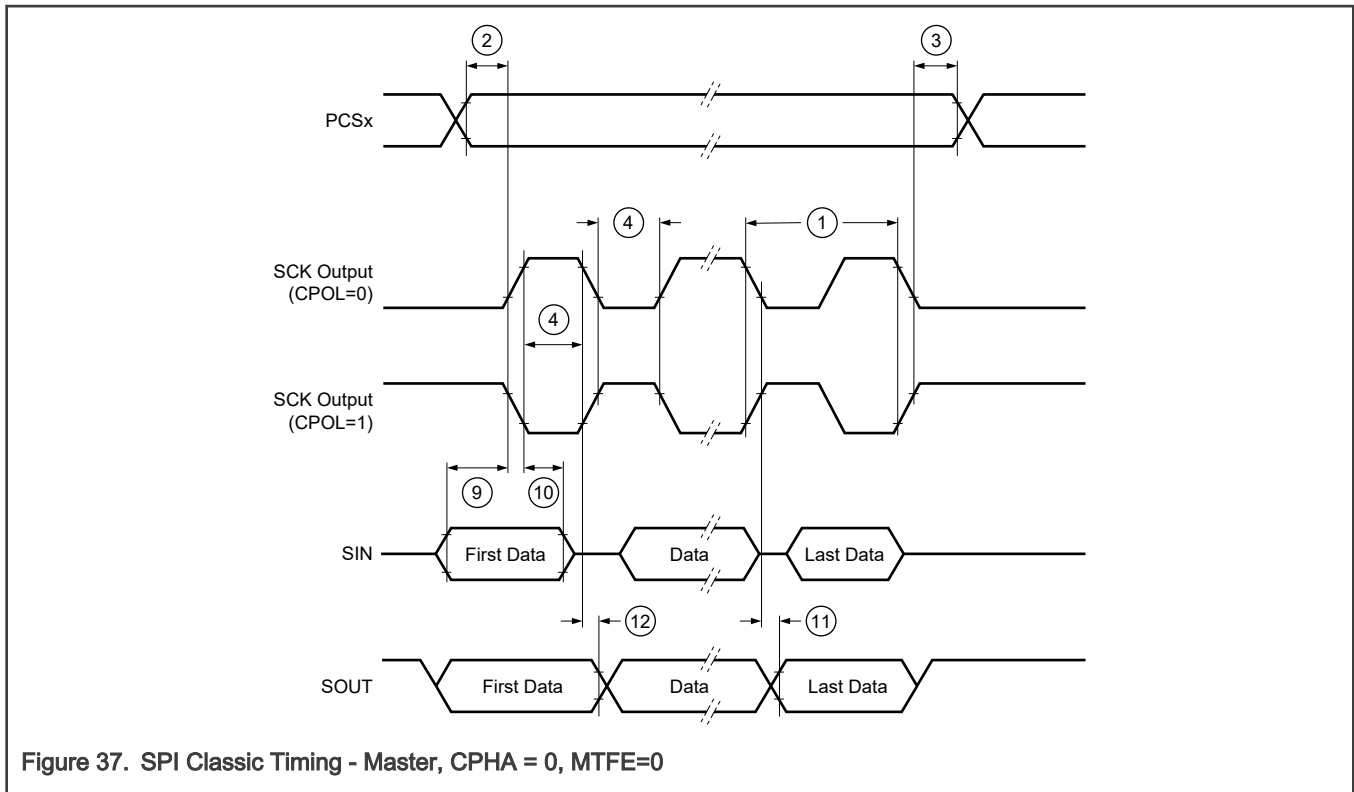


Figure 37. SPI Classic Timing - Master, CPHA = 0, MTFE=0

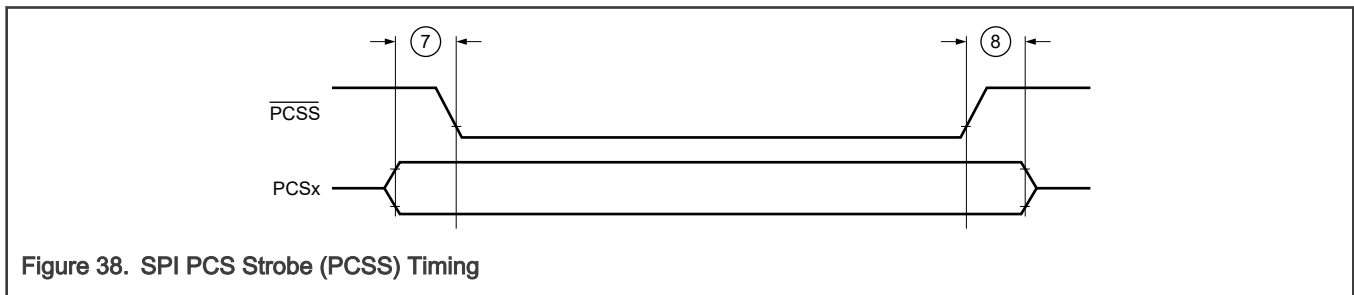


Figure 38. SPI PCS Strobe (PCSS) Timing

### 16.3.2 I2C

#### 16.3.2.1 I2C Input

Table 29. I2C Input

| Symbol | Description                                    | Min | Typ | Max | Unit                    | Condition                                 | Spec Number |
|--------|--|-----|-----|-----|-------------------------|---|-------------|
| tIH_SC | Input Start condition hold time <sup>1,2</sup> | 2   | —   | —   | MODULE<br>_CLK<br>cycle | —   | 1           |
| tCL    | Input Clock low time <sup>1,2</sup>            | 8   | —   | —   | MODULE<br>_CLK<br>cycle | —   | 2           |
| tIH    | Input Data hold time <sup>1,2</sup>            | 0   | —   | —   | ns                      | SDA transitions after<br>SCL falling edge | 4           |

Table continues on the next page...

Table 29. I2C Input (continued)

| Symbol   | Description  | Min | Typ | Max | Unit             | Condition                              | Spec Number |
|----------|--|-----|-----|-----|------------------|--|-------------|
| tCH      | Input Clock high time <sup>1,2</sup>                                       | 4   | —   | —   | MODULE_CLK cycle | —                                      | 6           |
| tISU     | Input Data setup time (standard mode) <sup>1,2,3</sup>                     | 250 | —   | —   | ns               | SDA transitions before SCL rising edge | 7           |
| tISU_F   | Input Data setup time (fast mode) <sup>1,2,3</sup>                         | 100 | —   | —   | ns               | SDA transitions before SCL rising edge | 7           |
| tISU_RSC | Input Start condition setup time (repeated start condition) <sup>1,2</sup> | 2   | —   | —   | MODULE_CLK cycle | —                                      | 8           |
| tISU_SC  | Input Start condition setup time <sup>1,2</sup>                            | 2   | —   | —   | MODULE_CLK cycle | —                                      | 9           |

1. MODULE\_CLK from the MC\_CGM is the clock driving the I2C block.
2. Input timing assumes an input signal slew rate of 3ns (20%/80%).
3. MODULE\_CLK frequency should be greater than 5 MHz for standard mode and 20 MHz for fast mode.

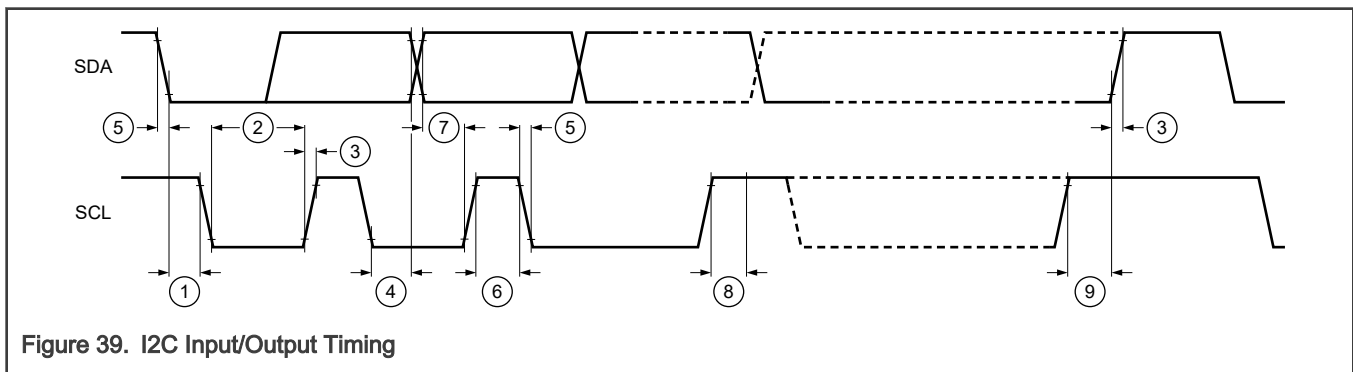


Figure 39. I2C Input/Output Timing

### 16.3.2.2 I2C Output

Table 30. I2C Output

| Symbol | Description                                       | Min | Typ | Max | Unit             | Condition | Spec Number |
|--------|---|-----|-----|-----|------------------|-----------|-------------|
| tOH_SC | Output Start condition hold time <sup>1,2,3</sup> | 6   | —   | —   | MODULE_CLK cycle | —         | 1           |
| tCL    | Output Clock low time <sup>1,2,3</sup>            | 10  | —   | —   | MODULE_CLK cycle | —         | 2           |

Table continues on the next page...

Table 30. I2C Output (continued)

| Symbol   | Description   | Min | Typ | Max | Unit                    | Condition      | Spec Number |
|----------|---|-----|-----|-----|-------------------------|----------------|-------------|
| tRISE    | SDA/SCL rise time <sup>1, 2, 3, 4</sup>                       | —   | —   | 100 | ns                      | SRE[2:0] = 110 | 3           |
| tOH      | Output Data hold time <sup>1, 2, 3</sup>                      | 7   | —   | —   | MODULE<br>_CLK<br>cycle | SRE[2:0] = 110 | 4           |
| tFALL    | SDA/SCL fall time <sup>1, 2, 3, 4</sup>                       | —   | —   | 100 | ns                      | SRE[2:0] = 110 | 5           |
| tCH      | Output Clock high time <sup>1, 2, 3</sup>                     | 10  | —   | —   | MODULE<br>_CLK<br>cycle | SRE[2:0] = 110 | 6           |
| tOSU     | Output Data setup time <sup>1, 2, 3</sup>                     | 2   | —   | —   | MODULE<br>_CLK<br>cycle | SRE[2:0] = 110 | 7           |
| tOSU_RSC | Output repeated start condition setup time <sup>1, 2, 3</sup> | 20  | —   | —   | MODULE<br>_CLK<br>cycle | SRE[2:0] = 110 | 8           |
| tOSU_SC  | Output start condition setup time <sup>1, 2, 3</sup>          | 11  | —   | —   | MODULE<br>_CLK<br>cycle | SRE[2:0] = 110 | 9           |

1. Timing valid for maximum external load CL = 400pF, at the maximum clock frequency defined by the I2C clock high and low time specifications.
2. MODULE\_CLK from the MC\_CGM is the clock driving the I2C block.
3. Programming IBFD (I2C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IBFD.
4. Because SCL and SDA are open-drain outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pullup resistor values

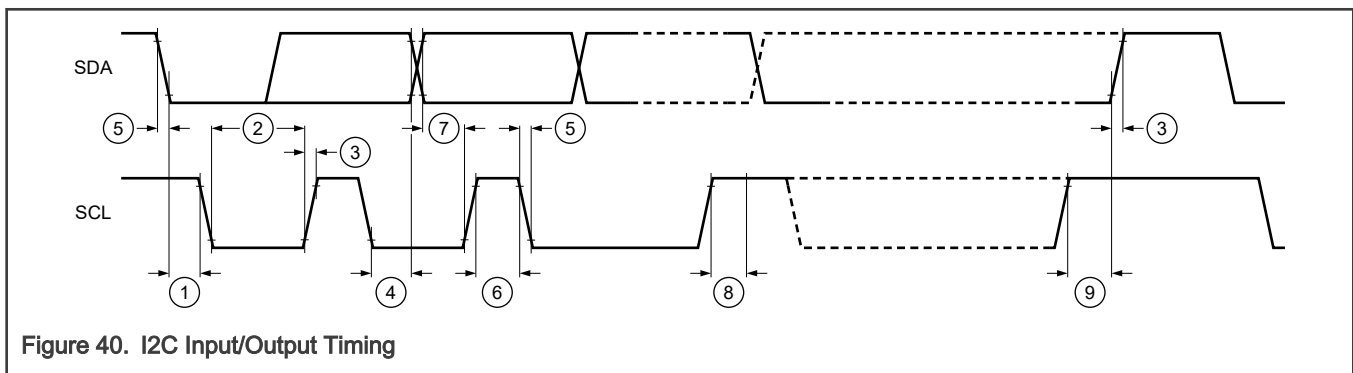


Figure 40. I2C Input/Output Timing

### 16.3.4 LIN

Table 31. LIN

| Symbol | Description | Min | Typ | Max | Unit | Condition                | Spec Number |
|--------|-------------|-----|-----|-----|------|--------------------------|-------------|
| RATE   | Bit Rate    | —   | —   | 2.0 | Mbps | UART mode SRE[2:0] = 110 | —           |
| RATE   | Bit Rate    | 4.8 | —   | 20  | Kbps | LIN mode SRE[2:0] = 110  | —           |

### 16.3.5 LPSPI

Table 32. LPSPI

| Symbol | Description   | Min              | Typ | Max                 | Unit | Condition | Spec Number |
|--------|---|------------------|-----|---------------------|------|-----------|-------------|
| fOP    | LPSPI operating frequency <a href="#">1, 2, 3, 4</a>          | fPER_CLK / 2048  | —   | 40                  | MHz  | Master    | —           |
| fOP    | LPSPI operating frequency <a href="#">3, 4, 5</a>             | —                | —   | 20                  | MHz  | Slave     | —           |
| tSPSCK | SPSCK period <a href="#">1, 2, 3, 4</a>                       | 25               | —   | 1 (fPER_CLK / 2048) | ns   | Master    | —           |
| tSPSCK | SPSCK period <a href="#">3, 4, 5</a>                          | 50               | —   | —                   | ns   | Slave     | —           |
| tLEAD  | Enable lead time (PCS to SPSCK delay) <a href="#">4, 6, 7</a> | tSPSCK - 3.5     | —   | —                   | ns   | Master    | —           |
| tLEAD  | Enable lead time (PCS to SPSCK delay) <a href="#">4, 6</a>    | 25               | —   | —                   | ns   | Slave     | —           |
| tLAG   | Enable lag time (after SPSCK delay) <a href="#">4, 8, 9</a>   | tSPSCK - 2.5     | —   | —                   | ns   | Master    | —           |
| tLAG   | Enable lag time (after SPSCK delay) <a href="#">4, 8</a>      | 25               | —   | —                   | ns   | Slave     | —           |
| tSW    | Clock (SPSCK) high or low time (duty cycle)                   | (tSPSCK / 2) - 3 | —   | (tSPSCK / 2) + 3    | ns   | Master    | —           |
| tSW    | Clock (SPSCK) high or low time (duty cycle)                   | (tSPSCK / 2) - 3 | —   | (tSPSCK / 2) + 3    | ns   | Slave     | —           |
| tSU    | Data setup time (inputs)                                      | 12               | —   | —                   | ns   | Master    | —           |

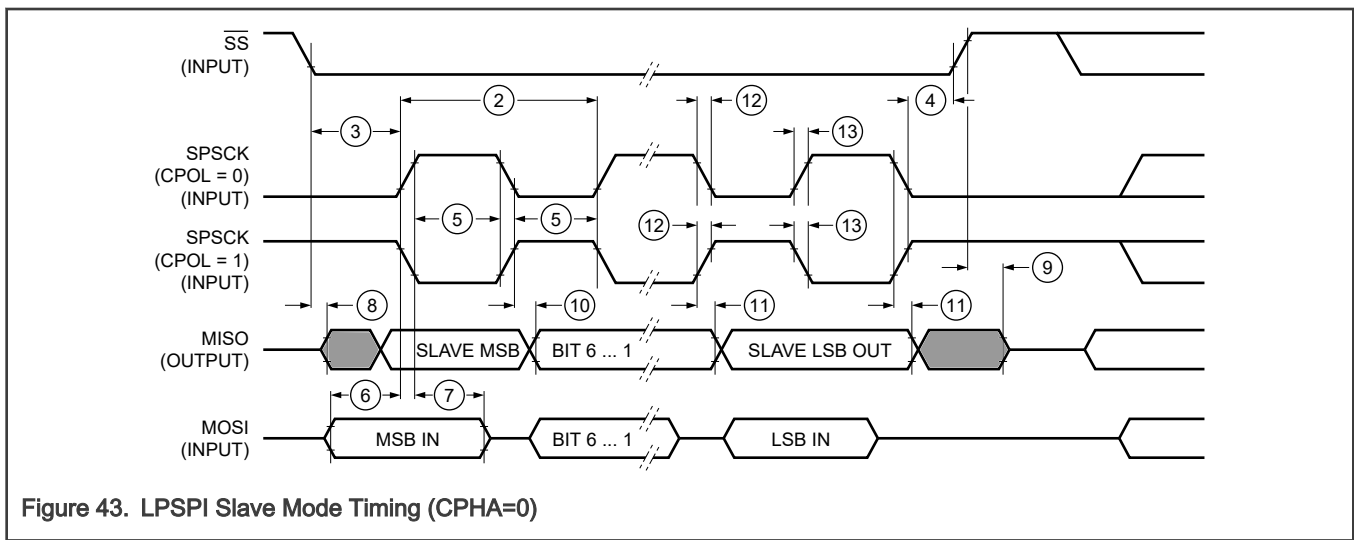
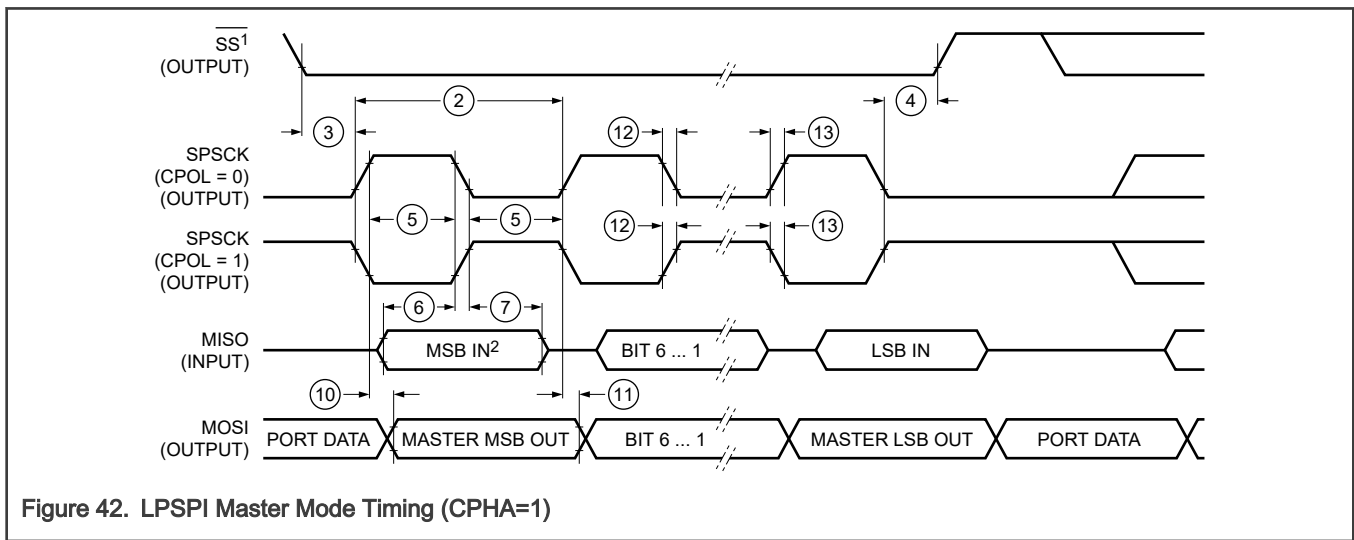
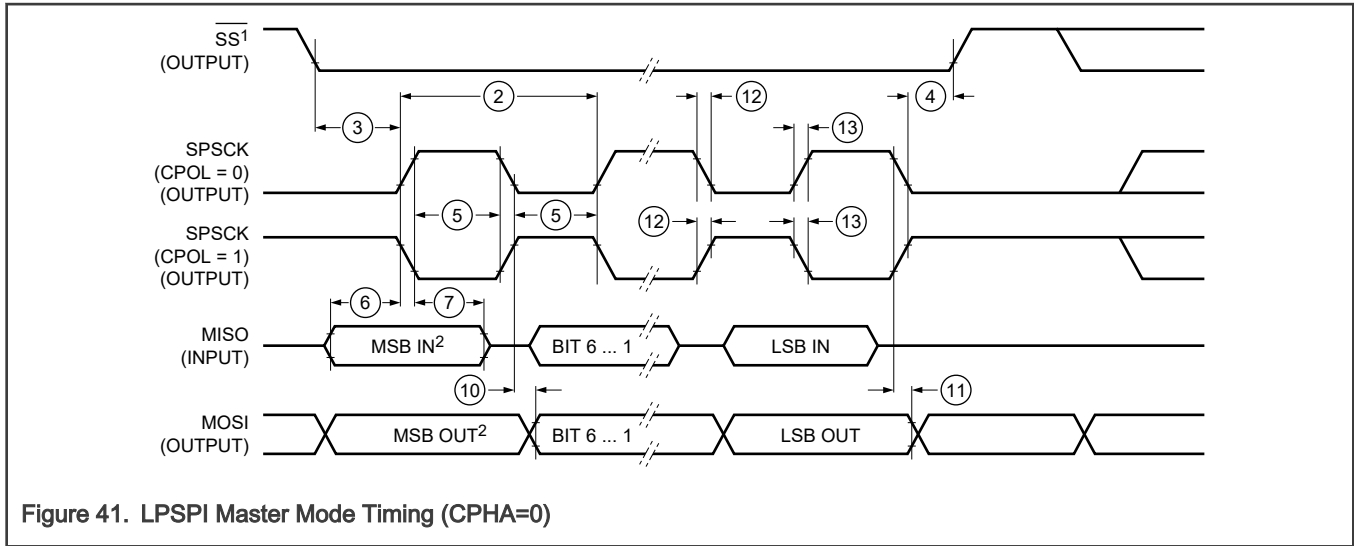
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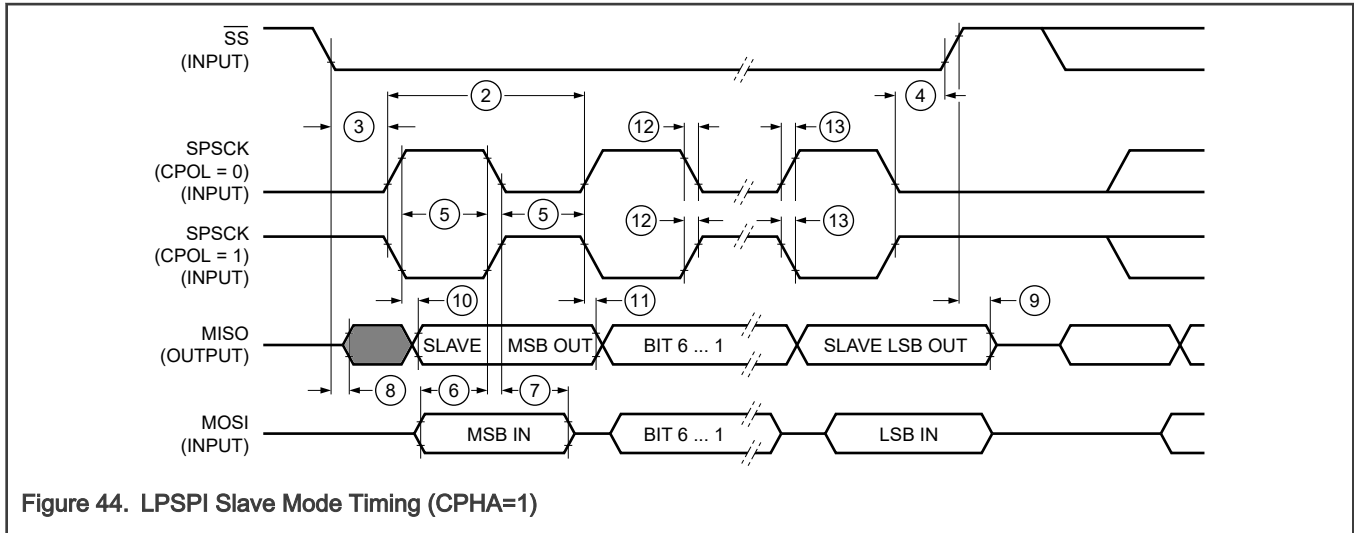
Table 32. LPSPI (continued)

| Symbol | Description                              | Min | Typ | Max  | Unit | Condition              | Spec Number |
|--------|--|-----|-----|------|------|------------------------|-------------|
| tSU    | Data setup time (inputs)                 | 4   | —   | —    | ns   | Slave                  | —           |
| tHO    | Data hold time (inputs)                  | 0   | —   | —    | ns   | Master                 | —           |
| tHO    | Data hold time (inputs)                  | 3   | —   | —    | ns   | Slave                  | —           |
| tA     | Slave access time                        | —   | —   | 12.5 | ns   | Slave                  | —           |
| tDIS   | Slave MISO disable time                  | —   | —   | 12.5 | ns   | Slave                  | —           |
| tV     | Data valid (after SPSSCK edge) 4, 10, 11 | —   | —   | 6    | ns   | Master, SRE[2:0] = 101 | —           |
| tV     | Data valid (after SPSSCK edge) 4, 10, 11 | —   | —   | 20   | ns   | Slave, SRE[2:0] = 101  | —           |
| tHO    | Data hold time (outputs) 4, 10, 11       | 0   | —   | —    | ns   | Master, SRE[2:0] = 101 | —           |
| tHO    | Data hold time (outputs) 4, 10, 11       | 0   | —   | —    | ns   | Slave, SRE[2:0] = 101  | —           |
| tRI_FI | Rise / Fall time (input) 12              | —   | —   | 1    | ns   | Master + Slave         | —           |

1. The maximum master mode LPSPI clock frequency can be no more than the peripheral clock frequency divided by 2.
2. fPER\_CLK is the frequency of the device peripheral clock (PER\_CLK).
3. The maximum LPSPI baud rate that is achievable in a dedicated master-slave connection depends on several parameters that are independent of the LPSPI module clocking capabilities (e.g. capacitive load of the signal lines, SPI slave clock-to-datadelay, pad slew rate, etc.). The maximum achievable LPSPI baud rate needs to be evaluated in a corresponding SPI master-slave setup.
4. All timing valid to 20% and 80% levels of the LPSPI I/O voltage supply on the device.
5. The maximum slave mode LPSPI clock frequency can be no more than the peripheral clock frequency divided by 4.
6. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where PCSSCK ranges from 0 to 255.
7.  $t_{PCSSCK} = (PCSSCK+1) * (2^{**}PRESCALE) * (1 / f_{PER\_CLK})$
8. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where SCKPCS ranges from 0 to 255.
9.  $t_{SCKPCS} = (SCKPCS+1) * (2^{**}PRESCALE) * (1 / f_{PER\_CLK})$
10. Timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output.
11. Output rise/fall time is determined by the output load and GPIO pad drive strength setting. See the GPIO specifications for detail.
12. The input rise/fall time specification applies to both clock and data, and is required to guarantee related timing parameters.







### 16.3.6 CAN

See GPIO pads for CAN specifications.

## 16.4 FlexRay

### 16.4.1 FlexRay - RxD

Table 33. FlexRay - RxD

| Symbol                | Description  | Min   | Typ | Max | Unit | Condition | Spec Number |
|-----------------------|--|-------|-----|-----|------|-----------|-------------|
| C_CCRxD               | Input capacitance on RxD pin   | —     | —   | 8   | pF   | —         | —           |
| dCCRxD01              | Sum of delay from actual input to the D input of the first FF, rising edge <sup>1</sup>  | —     | —   | 10  | ns   | —         | —           |
| dCCRxD10              | Sum of delay from actual input to the D input of the first FF, falling edge <sup>1</sup> | —     | —   | 10  | ns   | —         | —           |
| dCCRxAsymAccep<br>t15 | Acceptance of asymmetry at receiving CC with 15pF load <sup>1</sup>                      | -31.5 | —   | 44  | ns   | —         | —           |
| dCCRxAsymAccep<br>t25 | Acceptance of asymmetry at receiving CC with 25pF load <sup>1</sup>                      | -30.5 | —   | 43  | ns   | —         | —           |

1. FlexRay RxD timing assumes an input signal slew rate of 2ns (20%/80%).

### 16.4.2 FlexRay - TxD

Table 34. FlexRay - TxD

| Symbol                      | Description   | Min   | Typ | Max  | Unit | Condition  | Spec Number |
|-----------------------------|---|-------|-----|------|------|--|-------------|
| dCCTxAsym                   | Asymmetry of sending CC, dCCTxD50% - N x gdBit <sup>1</sup>   | -2.45 | —   | 2.45 | ns   | N=1, gdBit = 100ns, TxD load = 25pF max, SRE[2:0] = 110 (3.3V GPIO)        | —           |
| dCCTxDRISE25 + dCCTxDFALL25 | Sum of rise and fall time of TxD signal at the output pin <sup>1</sup>                              | —     | —   | 9    | ns   | TxD load = 25pF max, Z = 50ohms, delay = 0.6ns, SRE[2:0] = 110 (3.3V GPIO) | —           |
| dCCTxD01                    | Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge <sup>1</sup>  | —     | —   | 25   | ns   | TxD load = 25pF max, SRE[2:0] = 110 (3.3V GPIO)                            | —           |
| dCCTxD10                    | Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge <sup>1</sup> | —     | —   | 25   | ns   | TxD load = 25pF max, SRE[2:0] = 110 (3.3V GPIO)                            | —           |

1. Timing valid for maximum external load CL = 25pF, which is assumed to be a 8pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.

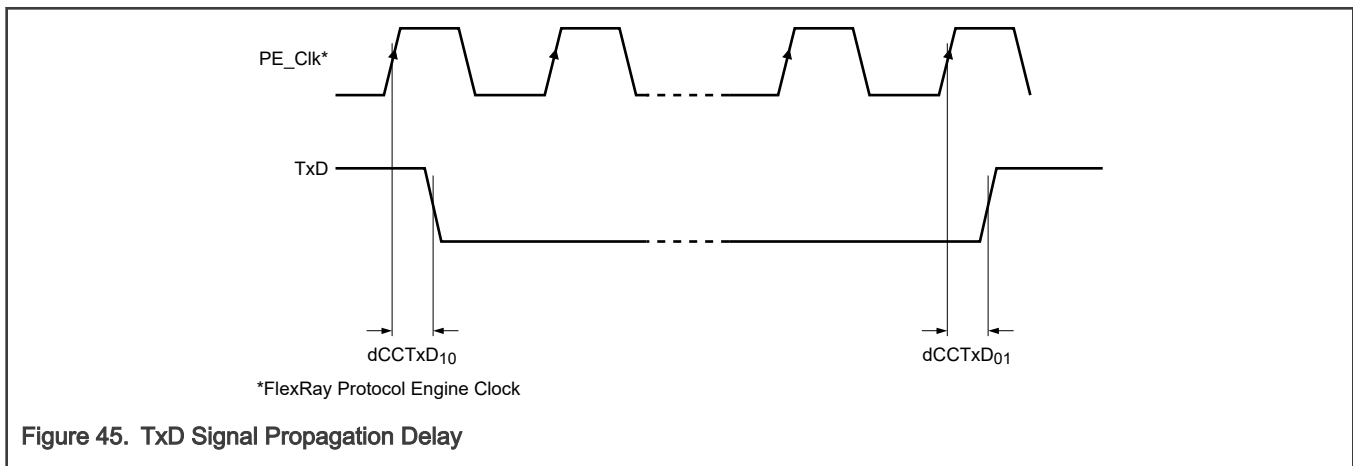


Figure 45. TxD Signal Propagation Delay

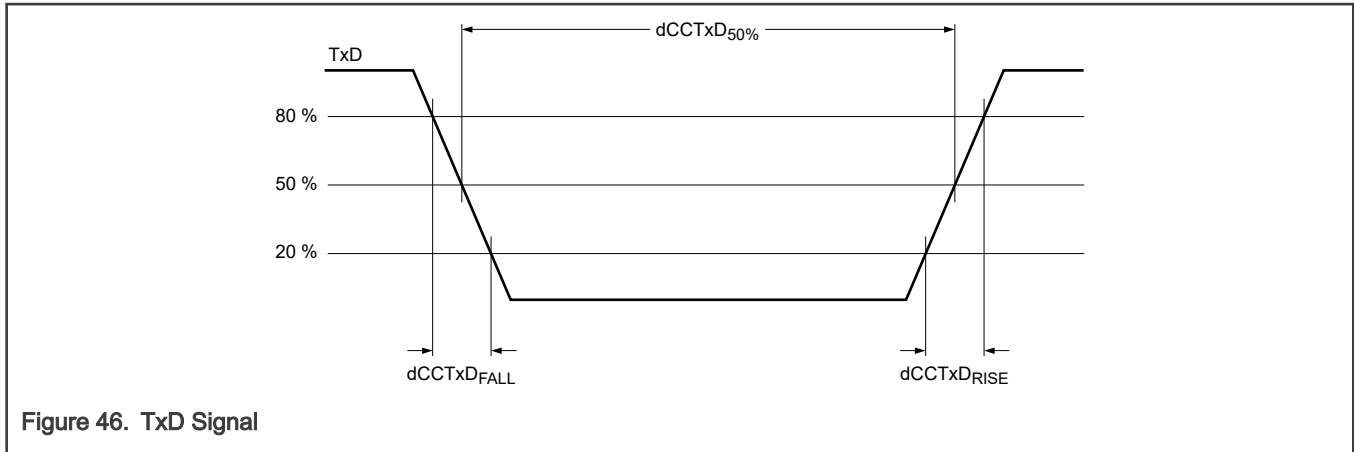


Figure 46. TxD Signal

### 16.4.3 FlexRay - TxEN

Table 35. FlexRay - TxEN

| Symbol        | Description   | Min | Typ | Max | Unit | Condition  | Spec Number |
|---------------|---|-----|-----|-----|------|--|-------------|
| dCCTxENRISE25 | Rise time of TxEN signal at CC <sup>1</sup>   | —   | —   | 9   | ns   | TxEN load = 25pF max, SRE[2:0] = 110 (3.3V GPIO) | —           |
| dCCTxENFALL25 | Fall time of TxEN signal at CC <sup>1</sup>   | —   | —   | 9   | ns   | TxEN load = 25pF max, SRE[2:0] = 110 (3.3V GPIO) | —           |
| dCCTxEN01     | Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge <sup>1</sup>  | —   | —   | 25  | ns   | TxEN load = 25pF max, SRE[2:0] = 110 (3.3V GPIO) | —           |
| dCCTxEN10     | Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge <sup>1</sup> | —   | —   | 25  | ns   | TxEN load = 25pF max, SRE[2:0] = 110 (3.3V GPIO) | —           |

1. Timing valid for maximum external load  $CL = 25pF$ , which is assumed to be a  $8pF$  load at the end of a  $50\Omega$ , un-terminated 5 inch microstrip trace on standard FR4 ( $1.5pF/inch$ ), ( $25pF$  total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the  $RDSON$  of the I/O pad output driver.

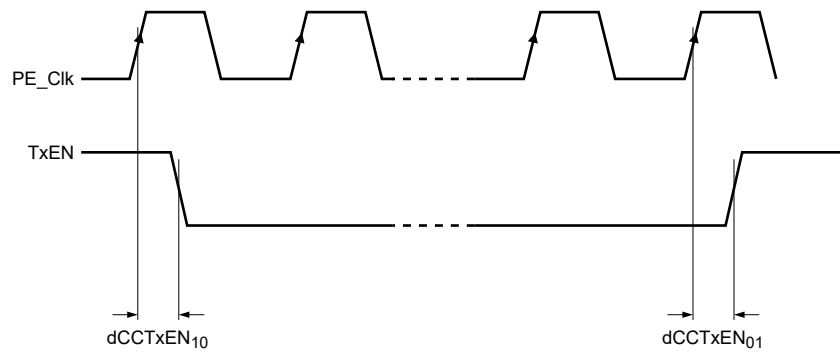


Figure 47. TxEN Signal Propagation Delay

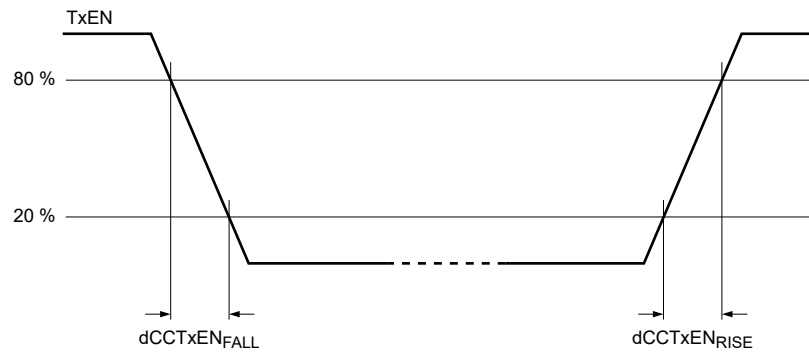


Figure 48. TxEN Signal

## 16.9 PCIe

Table 36. PCIe

| Symbol             | Description   | Min      | Typ | Max      | Unit | Condition        | Spec Number |
|--------------------|---|----------|-----|----------|------|------------------|-------------|
| UI                 | Unit Interval <sup>1</sup>                                | 399.88   | —   | 400.12   | ps   | 2.5GT/s          | —           |
| UI                 | Unit Interval <sup>1</sup>                                | 199.94   | —   | 200.06   | ps   | 5.0GT/s          | —           |
| UI                 | Unit Interval <sup>1</sup>                                | 124.9625 | —   | 125.0375 | ps   | 8.0GT/s          | —           |
| VTX-DIFF-PP        | Differential p-p Tx voltage swing <sup>1</sup>            | 0.8      | —   | 1.2      | Vp-p | 2.5GT/s, 5.0GT/s | —           |
| VTX-DE-RATIO-3.5dB | Tx de-emphasis level ratio <sup>1</sup>                   | 2.5      | —   | 4.5      | dB   | 2.5GT/s, 5.0GT/s | —           |
| VTX-DE-RATIO-6dB   | Tx de-emphasis level ratio <sup>1</sup>                   | 5        | —   | 7        | dB   | 5.0GT/s          | —           |
| TMIN-PULSE         | Instantaneous lone pulse width <sup>1</sup>               | 0.9      | —   | —        | UI   | 5.0GT/s          | —           |
| TTX-EYE            | Transmitter Eye including all jitter sources <sup>1</sup> | 0.75     | —   | —        | UI   | 2.5GT/s, 5.0GT/s | —           |

Table continues on the next page...

Table 36. PCIe (continued)

| Symbol                      | Description   | Min | Typ | Max   | Unit           | Condition | Spec Number |
|-----------------------------|---|-----|-----|-------|----------------|-----------|-------------|
| TTX-HF-DJ-DD                | Tx deterministic jitter > 1.5 MHz <sup>1</sup>  | —   | —   | 0.15  | UI             | 5.0GT/s   | —           |
| TTX-LF-RMS                  | Tx RMS jitter < 1.5 MHz <sup>1</sup>  | —   | 3   | —     | ps RMS         | 5.0GT/s   | —           |
| BWTX-PKG-PLL1               | Tx PLL BW corresponding to PKGTX-PLL1 <sup>1</sup>                                    | 8   | —   | 16    | MHz            | 5.0GT/s   | —           |
| BWTX-PKG-PLL1               | Tx PLL BW corresponding to PKGTX-PLL1 <sup>1</sup>                                    | 2   | —   | 4     | MHz            | 8.0GT/s   | —           |
| BWTX-PKG-PLL2               | Tx PLL BW corresponding to PKGTX-PLL2 <sup>1</sup>                                    | 5   | —   | 16    | MHz            | 5.0GT/s   | —           |
| BWTX-PKG-PLL2               | Tx PLL BW corresponding to PKGTX-PLL2 <sup>1</sup>                                    | 2   | —   | 5     | MHz            | 8.0GT/s   | —           |
| PKGTX-PLL1                  | Tx PLL peaking <sup>1</sup>   | —   | —   | 3     | dB             | 5.0GT/s   | —           |
| PKGTX-PLL1                  | Tx PLL peaking <sup>1</sup>   | —   | —   | 2     | dB             | 8.0GT/s   | —           |
| PKGTX-PLL2                  | Tx PLL peaking <sup>1</sup>   | —   | —   | 1     | dB             | 5.0GT/s   | —           |
| PKGTX-PLL2                  | Tx PLL peaking <sup>1</sup>   | —   | —   | 1     | dB             | 8.0GT/s   | —           |
| BWTX-PLL                    | Maximum Tx PLL bandwidth <sup>1</sup>   | 1.5 | —   | 22    | MHz            | 2.5GT/s   | —           |
| TTX-EYE-MEDIAN-to-MAXJITTER | Maximum time between the jitter median and max deviation from the median <sup>1</sup> | —   | —   | 0.125 | UI             | 2.5GT/s   | —           |
| VTX-FS-NO-EQ                | Full Swing Tx voltage with no TxEq <sup>1</sup>                                       | 800 | —   | 1300  | mVPP           | 8.0GT/s   | —           |
| VTX-EIEOS-FS                | Min Swing during EIEOS for full swing <sup>1</sup>                                    | 250 | —   | —     | mVPP           | 8.0GT/s   | —           |
| TTX-UTJ                     | Tx uncorrelated total jitter <sup>1</sup>   | —   | —   | 31.25 | ps PP @ 10e-12 | 8.0GT/s   | —           |
| TTX-UDJDD                   | Tx uncorrelated deterministic jitter <sup>1</sup>                                     | —   | —   | 12    | ps PP          | 8.0GT/s   | —           |
| VTX-BOOST-FS                | Tx boost ratio for full swing <sup>1</sup>  | 8   | —   | —     | dB             | 8.0GT/s   | —           |

Table continues on the next page...

Table 36. PCIe (continued)

| Symbol         | Description  | Min   | Typ | Max  | Unit      | Condition                         | Spec Number |
|----------------|--|-------|-----|------|-----------|-----------------------------------|-------------|
| VRX-DIFF-PP-CC | Differential Rx peak-peak voltage for common Refclk Rx architecture <sup>1</sup> | 0.175 | —   | 1.2  | V         | 2.5GT/s                           | —           |
| VRX-DIFF-PP-CC | Differential Rx peak-peak voltage for common Refclk Rx architecture <sup>1</sup> | 0.12  | —   | 1.2  | V         | 5.0GT/s                           | —           |
| TRX-EYE        | Receiver eye time opening <sup>1</sup>   | 0.4   | —   | —    | UI        | 2.5GT/s                           | —           |
| TRX-EYE        | Receiver eye time opening <sup>1</sup>   | 0.4   | —   | —    | UI        | 2.5GT/s                           | —           |
| TRX-TJ-CC      | Max Rx inherent timing error <sup>1</sup>  | —     | —   | 0.4  | UI        | 5.0GT/s                           | —           |
| TRX-DJ-DD_CC   | Max Rx deterministic timing error <sup>1</sup>                                   | —     | —   | 0.3  | UI        | 5.0GT/s                           | —           |
| VRX-EYE        | Receive eye voltage opening <sup>1</sup>   | —     | 120 | —    | mVPP diff | 5.0GT/s                           | —           |
| VRX-EYE        | Receive eye voltage opening <sup>1</sup>   | —     | 120 | —    | mVPP diff | 5.0GT/s                           | —           |
| VRX-SV-8G      | Eye height at TP2P <sup>1</sup>  | —     | 25  | —    | mVPP      | 8.0GT/s, -20dB Ch                 | —           |
| VRX-SV-8G      | Eye height at TP2P <sup>1</sup>  | —     | 50  | —    | mVPP      | 8.0GT/s, -12dB Ch                 | —           |
| VRX-SV-8G      | Eye height at TP2P <sup>1</sup>  | —     | 200 | —    | mVPP      | 8.0GT/s, -3dB Ch                  | —           |
| TRX-SV-8G      | Eye width at TP2P <sup>1</sup>   | 0.3   | —   | 0.35 | UI        | 8.0GT/s                           | —           |
| TRX-SV-SJ-8G   | Sinusoidal Jitter at 100MHz <sup>1</sup>   | —     | 0.1 | —    | UI PP     | 8.0GT/s                           | —           |
| TRX-SV-RJ-8G   | Random Jitter <sup>1</sup>   | —     | 2   | —    | ps RMS    | 8.0GT/s                           | —           |
| REXTPCIe       | External pin calibration resistance  | 198   | 200 | 202  | Ω         | —                                 | —           |
| RJREFCLK       | Reference clock random jitter (rms) <sup>1</sup>                                 | —     | —   | 3    | ps        | Integrated RJ from 12kHz to 20MHz | —           |
| RJREFCLK       | Reference clock random jitter (rms) <sup>1</sup>                                 | —     | —   | 2.2  | ps        | Integrated RJ from 2MHz to 20MHz  | —           |
| DJREFCLK       | Reference clock deterministic jitter (pk-pk) <sup>1</sup>                        | —     | —   | 5.7  | ps        | 200kHz to 100MHz                  | —           |

Table continues on the next page...

Table 36. PCIe (continued)

| Symbol      | Description   | Min  | Typ | Max         | Unit | Condition                         | Spec Number |
|-------------|---|------|-----|-------------|------|-----------------------------------|-------------|
| DJREFCLK    | Reference clock deterministic jitter (pk-pk) <sup>1</sup> | —    | —   | 2.8         | ps   | 1MHz to 20MHz                     | —           |
| RJ_SGMII    | Reference clock random jitter (rms)                       | —    | —   | 2.3         | ps   | Integrated RJ from 12kHz to 20MHz | —           |
| RJ_SGMII    | Reference clock random jitter (rms)                       | —    | —   | 1.7         | ps   | Integrated RJ from 2MHz to 20MHz  | —           |
| DJ_SGMII    | Reference clock deterministic jitter (pk-pk)              | —    | —   | 7.4         | ps   | 1MHz to 100MHz                    | —           |
| DJ_SGMII    | Reference clock deterministic jitter (pk-pk)              | —    | —   | 3.7         | ps   | 3MHz to 20MHz                     | —           |
| FREF_OFFSET | Reference clock frequency offset                          | -150 | —   | 150         | ppm  | —                                 | —           |
| DCREF_CLK   | Duty cycle  | 40   | —   | 60          | %    | —                                 | —           |
| VREF_CLK    | Voltage level   | 0    | —   | VDD_VP_PCIE | V    | —                                 | —           |
| IS_DIFF     | Differential input swing                                  | 0.3  | —   | —           | Vpp  | —                                 | —           |
| SWREF_CLK   | Input edge rate   | 0.4  | —   | 2           | V/ns | —                                 | —           |
| REF_CL_SKEW | Reference clock skew                                      | —    | —   | 200         | ps   | —                                 | —           |

1. The PCI Express link conforms to the PCI Express Base Specification, Revision 3.1. The summary of Transmitter and Receiver specifications are copied directly from the Base Specification. Consult the Base Specification for additional details.

NXP completed PCI-SIG compliance testing with the following PHY registers modified from default settings as described below. PHY register and programming details are provided in S32SERDESSUBSYSRM. PHY TX settings optimized for NXP validation board for SUP\_ANA\_TERM\_CTRL = 4 and TX\_VBOOST\_LVL = 4. PHY PLL bandwidth updated for MPLL\_BW\_OVRD\_VAL = 218 and MPLLA\_BW\_OVRD\_VAL = 197.

NXP internally does PCI-SIG TX compliance testing using external reference clock source.



## 16.6 GMAC and PFE

### 16.6.1 GMAC and PFE Management Interface

Table 37. GMAC and PFE Management Interface

| Symbol   | Description   | Min | Typ | Max | Unit | Condition      | Spec Number |
|----------|---|-----|-----|-----|------|----------------|-------------|
| fMDC     | MDC clock frequency   | —   | —   | 2.5 | MHz  | —              | MDC00       |
| MDIO_CH  | MDC pulse width high time   | 40  | —   | 60  | %    | —              | MDC14       |
| MDIO_CL  | MDC pulse width low time  | 40  | —   | 60  | %    | —              | MDC15       |
| MDIO_DOI | MDC falling edge to MDIO output invalid (minimum propagation delay) | 0   | —   | —   | ns   | SRE[2:0] = 100 | MDC10       |
| MDIO_DOV | MDC falling edge to MDIO output valid (maximum propagation delay)   | —   | —   | 15  | ns   | SRE[2:0] = 100 | MDC11       |
| MDIO_ISU | MDIO (input) to MDC rising edge setup time                          | 13  | —   | —   | ns   | —              | MDC12       |
| MDIO_IH  | MDIO (input) to MDC rising edge hold time                           | 0   | —   | —   | ns   | —              | MDC13       |

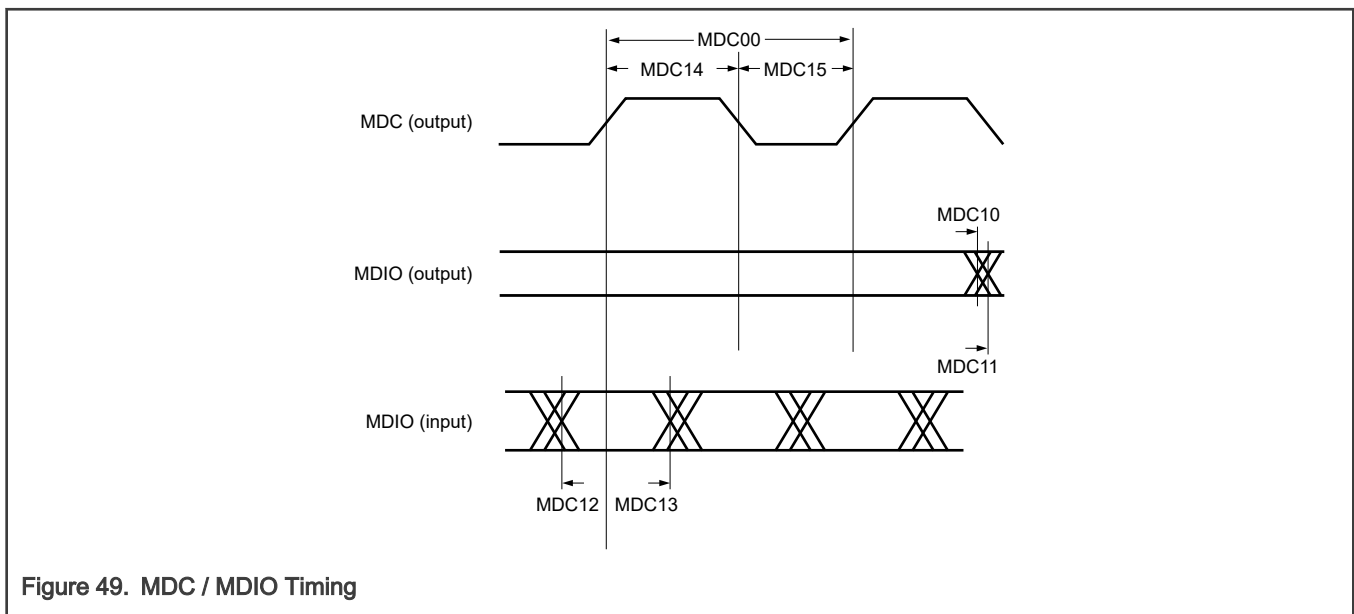


Figure 49. MDC / MDIO Timing

### 16.6.2 GMAC and PFE MII

Table 38. GMAC and PFE MII

| Symbol   | Description                                  | Min | Typ      | Max | Unit | Condition                   | Spec Number |
|----------|--|-----|----------|-----|------|-----------------------------|-------------|
| tCYC_RX  | RX_CLK period                                | —   | 40 / 400 | —   | ns   | 10/100 Mbps                 | —           |
| ΔtCYC_RX | RX_CLK duty cycle (tPWH / tCYC)              | 45  | —        | 55  | %    | —                           | —           |
| tS       | Input setup time to RX_CLK <sup>1</sup>      | 5   | —        | —   | ns   | 10/100 Mbps                 | —           |
| tH       | Input hold time to RX_CLK <sup>1</sup>       | 5   | —        | —   | ns   | 10/100 Mbps                 | —           |
| tCYC_TX  | TX_CLK period <sup>2</sup>                   | —   | 40 / 400 | —   | ns   | 10/100 Mbps, SRE[2:0] = 100 | —           |
| ΔtCYC_TX | TX_CLK duty cycle (tPWH / tCYC) <sup>2</sup> | 45  | —        | 55  | %    | SRE[2:0] = 100              | —           |
| tD       | Output delay from TX_CLK <sup>2</sup>        | 2   | —        | 25  | ns   | 10/100 Mbps, SRE[2:0] = 100 | —           |

1. Input timing assumes an input signal slew rate of 3ns (20%/80%).
2. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.

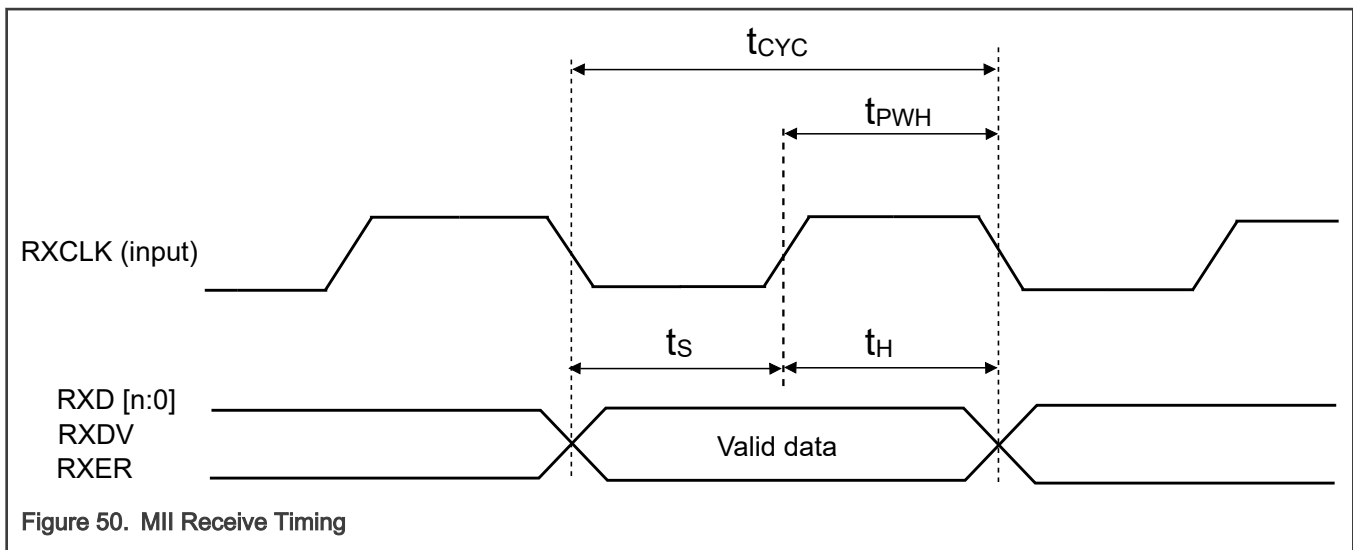


Figure 50. MII Receive Timing

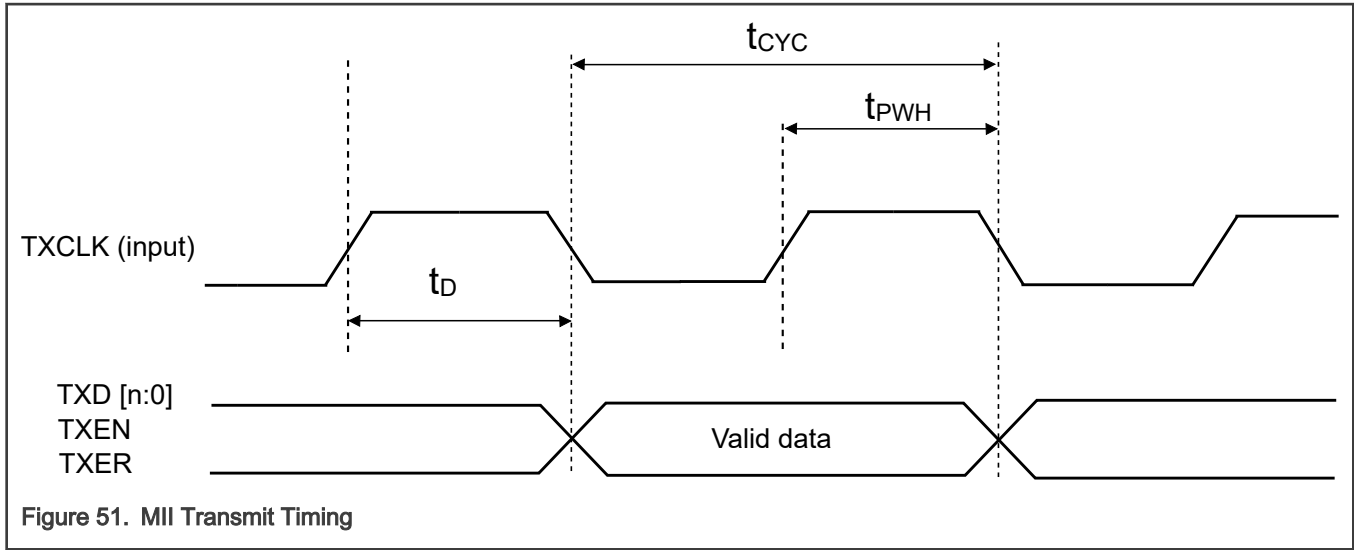


Figure 51. MII Transmit Timing

### 16.6.3 GMAC MII 50MHz

**NOTE**

GMAC MII 50MHz spec apply to GMAC only.

Table 39. GMAC MII 50MHz

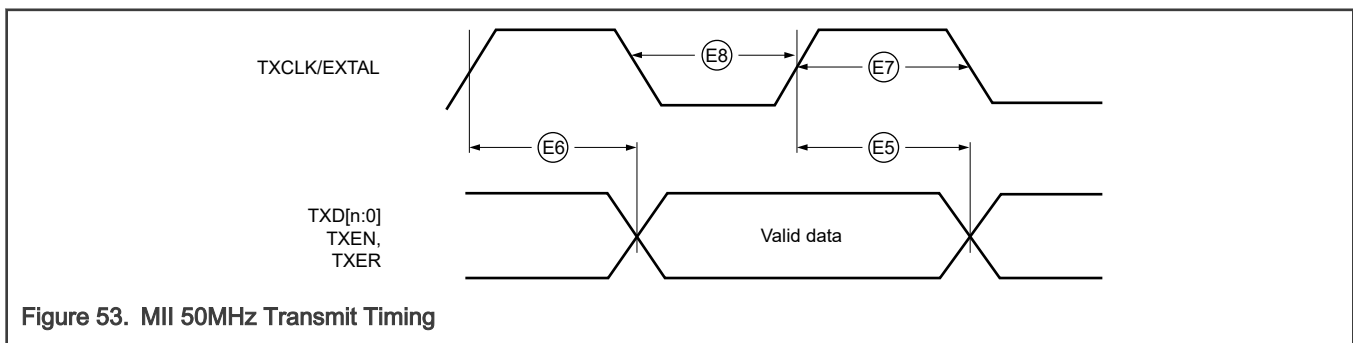
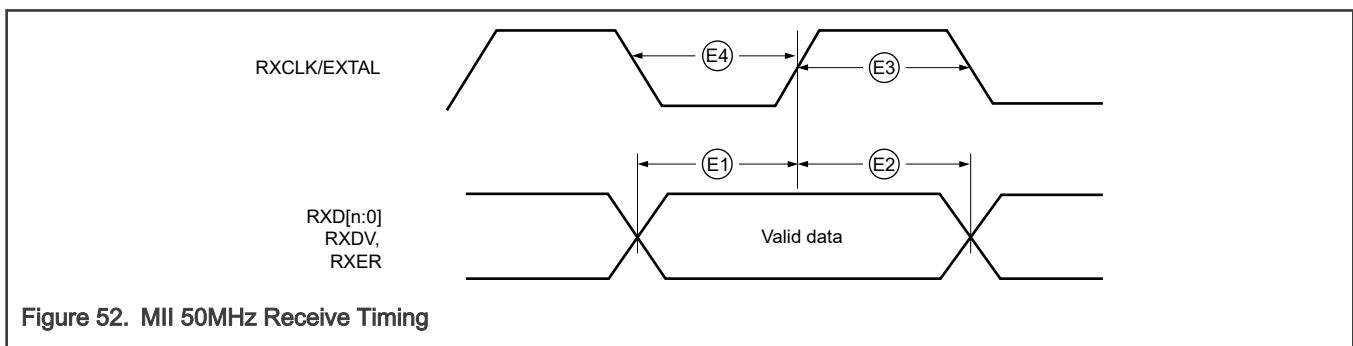
| Symbol  | Description   | Min | Typ | Max | Unit           | Condition | Spec Number |
|---------|---|-----|-----|-----|----------------|-----------|-------------|
| fRXCLK  | RXCLK frequency <sup>1</sup>                          | —   | —   | 50  | MHz            | —         | —           |
| dtRXCLK | RXCLK pulse width high <sup>1</sup>                   | 35  | —   | 65  | % RXCLK period | —         | E3          |
| dtRXCLK | RXCLK pulse width low <sup>1</sup>                    | 35  | —   | 65  | % RXCLK period | —         | E4          |
| tSETUP  | RXD[3:0], RXDV, RXER to RXCLK setup time <sup>1</sup> | 4   | —   | —   | ns             | —         | —           |
| tHOLD   | RXCLK to RXD[3:0], RXDV, RXER hold time <sup>1</sup>  | 2   | —   | —   | ns             | —         | —           |
| fTXCLK  | TXCLK frequency <sup>2</sup>                          | —   | —   | 50  | MHz            | —         | —           |
| dtTXCLK | TXCLK pulse width high <sup>2</sup>                   | 35  | —   | 65  | % TXCLK period | —         | E7          |
| dtTXCLK | TXCLK pulse width low <sup>2</sup>                    | 35  | —   | 65  | % TXCLK period | —         | E8          |

Table continues on the next page...

Table 39. GMAC MII 50MHz (continued)

| Symbol        | Description  | Min | Typ | Max | Unit | Condition | Spec Number |
|---------------|--|-----|-----|-----|------|-----------|-------------|
| tDATA_VALID   | TXCLK to TXD[3:0], TXDV, TXER valid <sup>2</sup>   | —   | —   | 15  | ns   | —         | E6          |
| tDATA_INVALID | TXCLK to TXD[3:0], TXDV, TXER invalid <sup>2</sup> | 2   | —   | —   | ns   | —         | E5          |

1. Input timing assumes an input signal slew rate of 3ns (20%/80%).
2. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch, (25pF total with margin). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.



### 16.6.4 GMAC and PFE RMII

Table 40. GMAC and PFE RMII

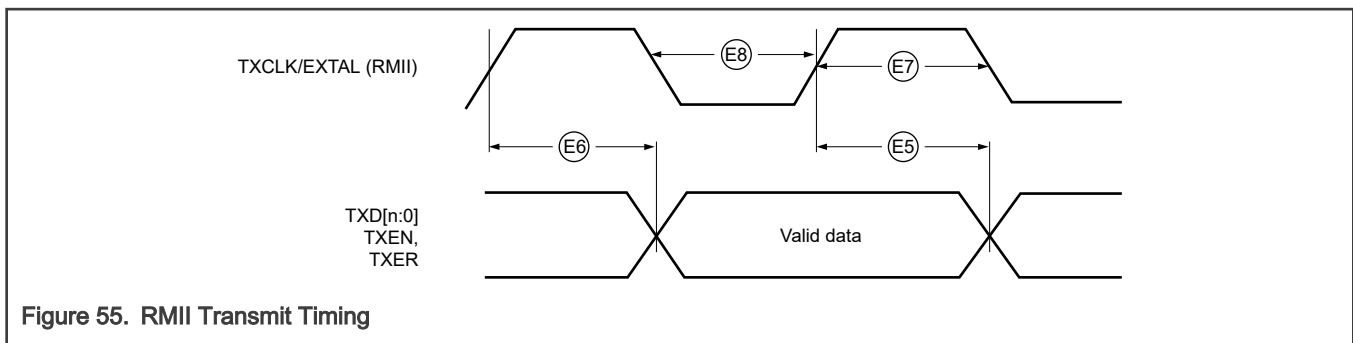
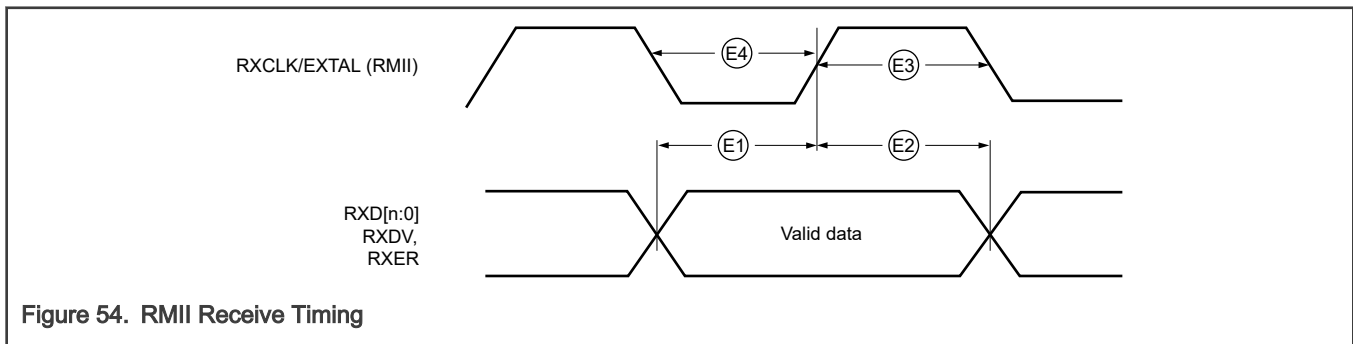
| Symbol     | Description  | Min | Typ | Max | Unit | Condition | Spec Number    |
|------------|--|-----|-----|-----|------|-----------|----------------|
| fRMII_CLK  | RMII input clock frequency (RMII_CLK)                      | —   | —   | 50  | MHz  | —         | —              |
| ΔtRMII_CLK | RMII_CLK duty cycle (tPWH / tCYC)                          | 35  | —   | 65  | %    | —         | E3, E4, E7, E8 |
| tS         | RXD[1:0], CRS_DV, RXER to RMII_CLK setup time <sup>1</sup> | 4   | —   | —   | ns   | —         | E1             |

Table continues on the next page...

Table 40. GMAC and PFE RMII (continued)

| Symbol        | Description   | Min | Typ | Max | Unit | Condition                    | Spec Number |
|---------------|---|-----|-----|-----|------|------------------------------|-------------|
| tH            | RMII_CLK to RXD[1:0], CRS_DV, RXER hold time <sup>1</sup> | 2   | —   | —   | ns   | —                            | E2          |
| tDATA_VALID   | RMII_CLK to TXD[1:0], TXEN data valid <sup>2</sup>        | —   | —   | 14  | ns   | CLOAD = 25pF, SRE[2:0] = 100 | E6          |
| tDATA_INVALID | RMII_CLK to TXD[1:0], TXEN data invalid <sup>2</sup>      | 2   | —   | —   | ns   | CLOAD = 25pF, SRE[2:0] = 100 | E5          |

1. Input timing assumes an input signal slew rate of 3ns (20%/80%).
2. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.



### 16.6.5 GMAC and PFE RGMII

You must set SRE[2:0]=101 for PFE\_MAC0\_TX\_CLK in RGMII mode of PFE GMAC0 at 3.3V.

Table 41. GMAC and PFE RGMII

| Symbol | Description                                | Min | Typ | Max | Unit | Condition      | Spec Number |
|--------|--|-----|-----|-----|------|----------------|-------------|
| Tcyc   | Clock cycle duration <sup>1, 2, 3, 4</sup> | 7.2 | —   | 8.8 | ns   | SRE[2:0] = 100 | —           |

Table continues on the next page...

Table 41. GMAC and PFE RGMII (continued)

| Symbol | Description   | Min  | Typ | Max | Unit | Condition      | Spec Number |
|--------|---|------|-----|-----|------|----------------|-------------|
| TskewT | Data to clock output skew (at transmitter) 2, 3, 4, 5 | -500 | —   | 500 | ps   | SRE[2:0] = 100 | —           |
| TskewR | Data to clock input skew (at receiver) 2, 4, 5        | 1    | —   | 2.6 | ns   | SRE[2:0] = 100 | —           |
| Duty_G | Clock duty cycle for Gigabit 2, 4, 6                  | 45   | —   | 55  | %    | SRE[2:0] = 100 | —           |
| Duty_T | Clock duty cycle for 10/100T 2, 4, 6                  | 40   | —   | 60  | %    | SRE[2:0] = 100 | —           |

- For 10 Mbps and 100 Mbps, T<sub>cy</sub> will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.
- Measured as defined in EIA/JESD 8-6 1995 with a timing threshold voltage of V<sub>DDQ</sub>/2
- Output timing valid for maximum external load CL = 15pF, which is assumed to be a 8pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.
- RGMII timing specifications are valid for both 1.8V and 3.3V nominal I/O pad supply voltage.
- For all versions prior to RGMII v2.0 specifications; This implies that PC board design will require clocks to be routed such that an additional delay of greater than 1.5 ns and less than 2 ns will be added to the associated clock signal. For 10/100, the max value is unspecified.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three T<sub>cy</sub> of the lowest speed transitioned between.

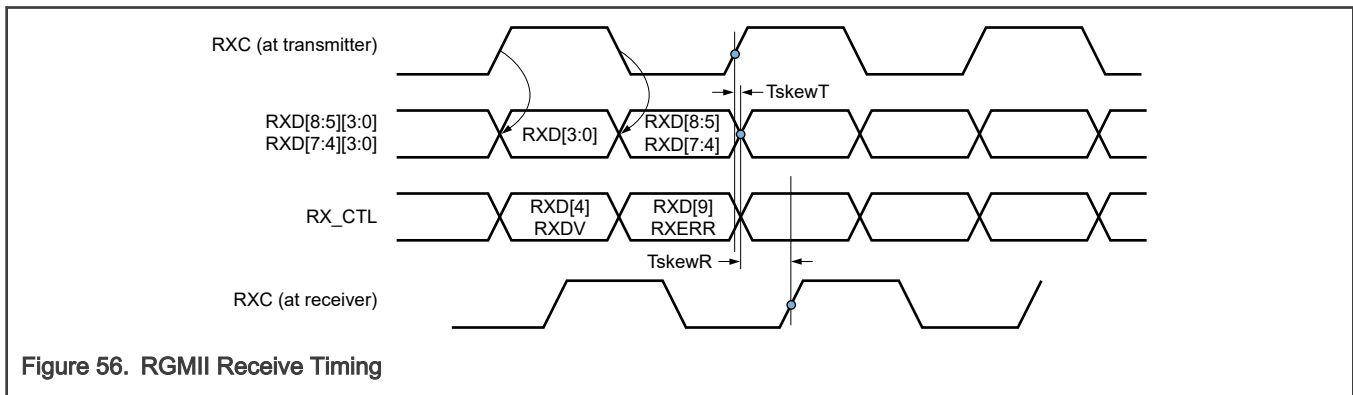


Figure 56. RGMII Receive Timing

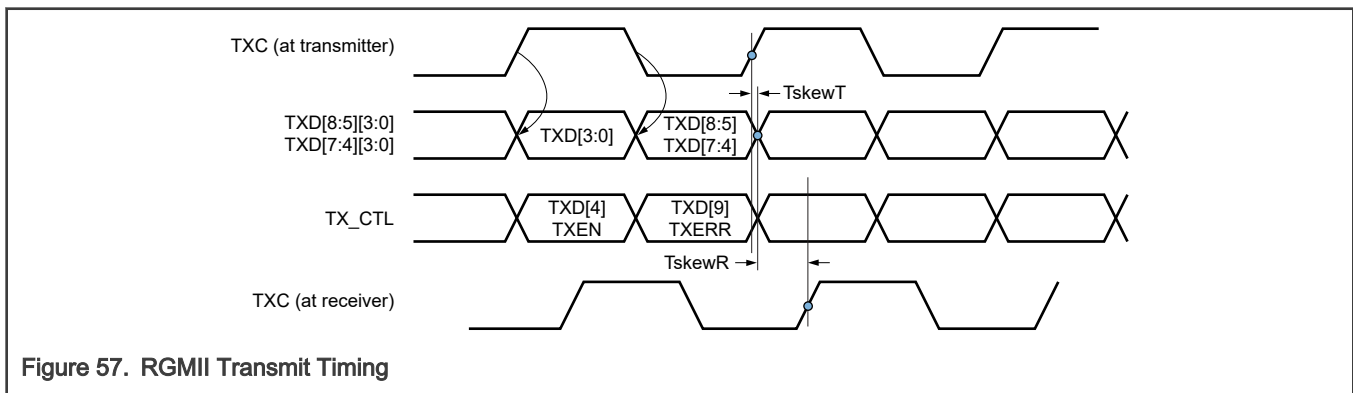


Figure 57. RGMII Transmit Timing

### 16.6.6 GMAC and PFE SGMII

Table 42. GMAC and PFE SGMII

| Symbol | Description  | Min     | Typ | Max     | Unit | Condition   | Spec Number |
|--------|--|---------|-----|---------|------|---|-------------|
| UI     | Unit Interval (mean)   | 799.92  | 800 | 800.08  | ps   | 1.25 Gbps bit rate, applies to both transmitter and receiver and supports 1 Gbps data rate    | —           |
| UI     | Unit Interval (mean)   | 319.968 | 320 | 320.032 | ps   | 3.125 Gbps bit rate, applies to both transmitter and receiver and supports 2.5 Gbps data rate | —           |
| trise  | Transmit Vod rise time (20-80%)  | —       | —   | 100     | ps   | —   | —           |
| tfall  | Transmit Vod fall time (20-80%)  | —       | —   | 100     | ps   | —   | —           |
| VOD    | Transmit Output Differential Voltage   | 400     | —   | 600     | mV   | 1.25Gbps  | —           |
| VOD    | Transmit Output Differential Voltage <sup>1</sup>  | 400     | —   | 600     | mV   | 3.125Gbps   | —           |
| RDOUT  | Transmit Differential Output Impedance   | 80      | 100 | 120     | Ohm  | —   | —           |
| Dj     | Transmit Deterministic Jitter  | —       | —   | 0.17    | UI   | —   | —           |
| Tj     | Transmit Total Jitter  | —       | —   | 0.35    | UI   | —   | —           |
| RDIN   | Receiver Differential Input Impedance  | 80      | —   | 120     | Ohm  | —   | —           |
| VIN    | Receiver Differential Input Voltage  | 200     | —   | 1200    | mV   | —   | —           |
| LOS    | Loss-of-signal threshold   | 75      | —   | 200     | mV   | —   | —           |
| Sjt    | Receiver deterministic jitter tolerance with sinusoidal noise <sup>2</sup>                     | —       | —   | 0.37    | UI   | —   | —           |
| DRjt   | Receiver combined random and deterministic jitter tolerance with sinusoidal noise <sup>2</sup> | —       | —   | 0.55    | UI   | —   | —           |
| Tjt    | Receiver total jitter tolerance  | —       | —   | 0.65    | UI   | —   | —           |

Table continues on the next page...

Table 42. GMAC and PFE SGMII (continued)

| Symbol | Description    | Min | Typ | Max               | Unit | Condition | Spec Number |
|--------|----------------|-----|-----|-------------------|------|-----------|-------------|
| BER    | Bit Error Rate | —   | —   | 10 <sup>-12</sup> | —    | —         | —           |

- VOD at 3.125Gbps is only applicable for PFE\_MAC0.
- The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the un-shaded region of the figure below.

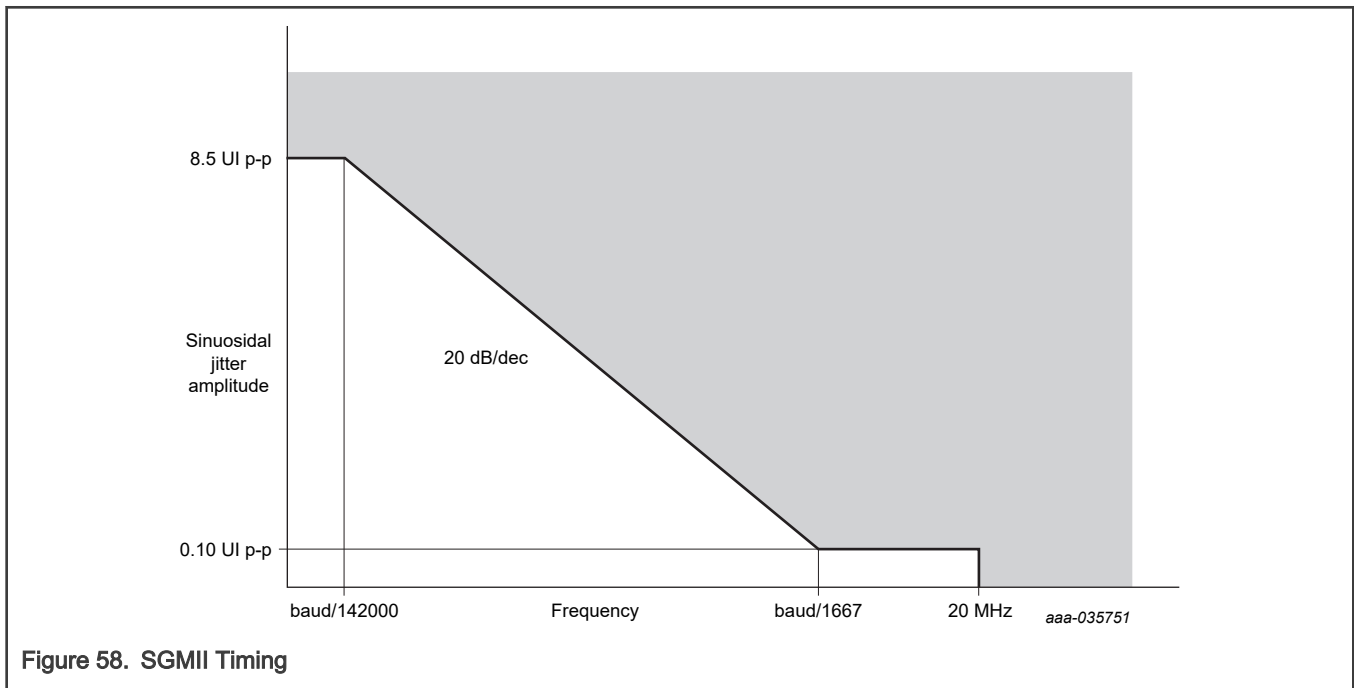


Figure 58. SGMII Timing

## 16.12 USB-ULPI

Table 43. USB-ULPI

| Symbol | Description                                       | Min | Typ   | Max | Unit | Condition | Spec Number |
|--------|---|-----|-------|-----|------|-----------|-------------|
| TCLK   | USB_CLKIN period                                  | —   | 16.67 | —   | ns   | —         | U1          |
| DFCLK  | USB_CLKIN duty cycle                              | —   | 50    | —   | %    | —         | —           |
| tISU   | Input setup time (control and data) <sup>1</sup>  | 5   | —     | —   | ns   | —         | U2          |
| tIH    | Input hold time (control and data) <sup>1</sup>   | 1   | —     | —   | ns   | —         | U3          |
| tOV    | Output valid time (control and data) <sup>2</sup> | —   | —     | 9.5 | ns   | —         | U4          |
| tOH    | Output hold time (control and data) <sup>2</sup>  | 0   | —     | —   | ns   | —         | U5          |

- Input timing assumes an input signal slew rate of 3ns (20%/80%).



- Output timing valid for maximum external load  $CL = 25pF$ , which is assumed to be a  $10pF$  load at the end of a  $50\Omega$ , un-terminated, 5 inch microstrip trace on standard FR4 with  $1.5pF/inch$  ( $25pF$  total with margin). For best signal integrity, the series resistance of the transmission line should match closely to the  $RDSON$  of the I/O pad output driver.

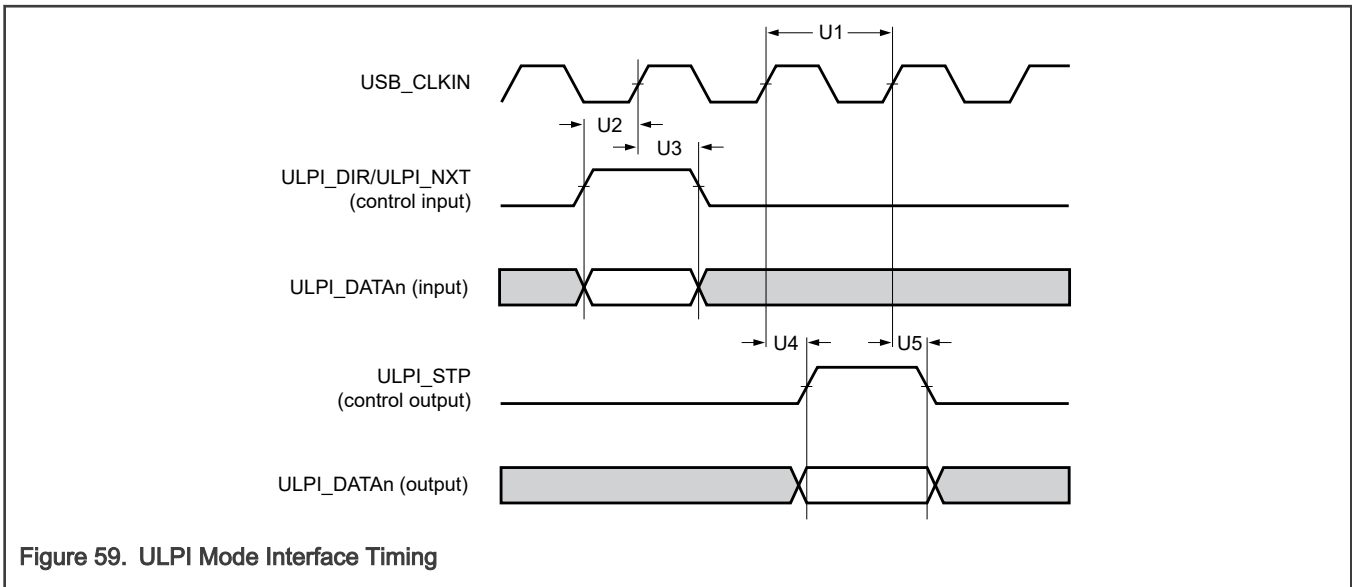


Figure 59. ULPI Mode Interface Timing

## 16.8 Memory interfaces

### 16.8.1 QuadSPI

An external resistor is needed to pull up a QuadSPI chip select signal.

### 16.8.2 QuadSPI Quad 1.8V DDR 66MHz

The  $SRE[2:0]=100$  for 18GPIO pads and  $SRE[2:0]=101$  for 1833Fast pads is the required drive setting to meet the timing.

$FLSHCR[TCSS]$  and  $FLSHCR[TCSH]$  should be set to 3.

All transitions measured at mid-supply ( $VDD_{IO\_QSPI}/2$ ).

Table 44. QuadSPI Quad 1.8V DDR 66MHz

| Symbol   | Description                                 | Min              | Typ | Max              | Unit | Condition        | Spec Number |
|----------|---|------------------|-----|------------------|------|------------------|-------------|
| fSCK     | SCK clock frequency <sup>1,2</sup>          | —                | —   | 66               | MHz  | DLL mode enabled | —           |
| tCL_SCK  | SCK clock low time <sup>1,2</sup>           | 6.818            | —   | —                | ns   | —                | —           |
| tCH_SCK  | SCK clock high time <sup>1,2</sup>          | 6.818            | —   | —                | ns   | —                | —           |
| tOD_DATA | Data output delay (w.r.t. SCK) <sup>1</sup> | 2.316            | —   | 4.802            | ns   | —                | —           |
| tOD_CS   | CS output delay (w.r.t. SCK) <sup>1,3</sup> | $5.016 - n/fSCK$ | —   | $1.802 + m/fSCK$ | ns   | —                | —           |

Table continues on the next page...

Table 44. QuadSPI Quad 1.8V DDR 66MHz (continued)

| Symbol | Description                                     | Min  | Typ | Max | Unit | Condition | Spec Number |
|--------|---|------|-----|-----|------|-----------|-------------|
| tDVW   | Input data valid window <sup>2</sup>            | 5.14 | —   | —   | ns   | —         | —           |
| tLSKEW | Skew target for Auto-learning mode <sup>4</sup> | 1.89 | —   | —   | ns   | —         | —           |

- Output timing valid for maximum external load CL = 20pF, which is assumed to be a 10pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
- Input timing assumes maximum input signal transition of 1ns (20%/80%).
- Where m=TCSS and n=TCSH-1.
- Data valid window includes DLL Margin, and determines LEARNING skew targets which can be more pessimistic than tISU\_SCK and tIH\_SCK.

### 16.8.3 QuadSPI Octal 1.8V SDR 133MHz

The SRE[2:0]=100 for 18GPIO pads and SRE[2:0]=101 for 1833Fast pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

All transitions measured at mid-supply (VDD\_IO\_QSPI/2).

Table 45. QuadSPI Octal 1.8V SDR 133MHz

| Symbol   | Description                                 | Min            | Typ | Max            | Unit | Condition        | Spec Number |
|----------|---|----------------|-----|----------------|------|------------------|-------------|
| fSCK     | SCK clock frequency <sup>1,2</sup>          | —              | —   | 133            | MHz  | DLL mode enabled | —           |
| tCL_SCK  | SCK clock low time <sup>1,2</sup>           | 3.383          | —   | —              | ns   | —                | —           |
| tCH_SCK  | SCK clock high time <sup>1,2</sup>          | 3.383          | —   | —              | ns   | —                | —           |
| tOD_DATA | Data output delay (w.r.t. SCK) <sup>1</sup> | -1.594         | —   | 1.594          | ns   | —                | —           |
| tOD_CS   | CS output delay (w.r.t. SCK) <sup>1,3</sup> | 3.016 - n/fSCK | —   | 2.704 + m/fSCK | ns   | —                | —           |
| tISU_SCK | Input setup time (w.r.t. SCK) <sup>2</sup>  | 0.580          | —   | —              | ns   | —                | —           |
| tIH_SCK  | Input hold time (w.r.t. SCK) <sup>2</sup>   | 0.9            | —   | —              | ns   | —                | —           |

- Output timing valid for maximum external load CL = 20pF, which is assumed to be a 10pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
- Input timing assumes maximum input signal transition of 1ns (20%/80%).
- Where m=TCSS and n=TCSH-1.

### 16.8.4 QuadSPI Octal 1.8V DDR 100MHz

The information in this section applies to Octal- and Hyperflash.

The SRE[2:0]=100 for 18GPIO pads and SRE[2:0]=101 for 1833Fast pads is the required drive setting to meet the timing.  
 FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.  
 All transitions measured at mid-supply (VDD\_IO\_QSPI/2).

**Table 46. QuadSPI Octal 1.8V DDR 100MHz**

| Symbol   | Description                                  | Min            | Typ | Max             | Unit | Condition  | Spec Number |
|----------|--|----------------|-----|-----------------|------|--|-------------|
| fSCK_DQS | SCK / DQS frequency <sup>1, 2</sup>          | —              | —   | 100             | MHz  | fSCK duty cycle distortion is in the range of 45%-55%. | —           |
| tCL_SCK  | SCK low time <sup>1, 2</sup>                 | 4.500          | —   | —               | ns   | —  | —           |
| tCH_SCK  | SCK high time <sup>1, 2</sup>                | 4.500          | —   | —               | ns   | —  | —           |
| tOD_DATA | Data output delay (w.r.t. SCK) <sup>2</sup>  | 1.016          | —   | 3.484           | ns   | —  | —           |
| tOD_CS   | CS output delay (w.r.t. SCK) <sup>2, 3</sup> | 3.016 - n/fSCK | —   | -0.016 + m/fSCK | ns   | —  | —           |
| tISU_DQS | Input setup time (w.r.t. DQS) <sup>1</sup>   | -0.816         | —   | —               | ns   | —  | —           |
| tIH_DQS  | Input hold time (w.r.t. DQS) <sup>1</sup>    | 3.684          | —   | —               | ns   | —  | —           |

1. Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
2. Output timing valid for maximum external load CL = 20pF, which is assumed to be a 10pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSO of the I/O pad output.
3. Where m=TCSS and n=TCSH-1.

### 16.8.5 QuadSPI Octal 1.8V DDR 133MHz

The information in this section applies to Octal- and Hyperflash.

The SRE[2:0]=100 for 18GPIO pads and SRE[2:0]=101 for 1833Fast pads is the required drive setting to meet the timing.  
 FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.  
 All transitions measured at mid-supply (VDD\_IO\_QSPI/2).

**Table 47. QuadSPI Octal 1.8V DDR 133MHz**

| Symbol   | Description                         | Min   | Typ | Max | Unit | Condition  | Spec Number |
|----------|-------------------------------------|-------|-----|-----|------|--|-------------|
| fSCK_DQS | SCK / DQS frequency <sup>1, 2</sup> | —     | —   | 133 | MHz  | DLL mode enabled, fSCK duty cycle distortion is in the range of 45%-55%. | —           |
| tCL_SCK  | SCK low time <sup>1, 2</sup>        | 3.383 | —   | —   | ns   | —  | —           |
| tCH_SCK  | SCK high time <sup>1, 2</sup>       | 3.383 | —   | —   | ns   | —  | —           |

*Table continues on the next page...*

Table 47. QuadSPI Octal 1.8V DDR 133MHz (continued)

| Symbol   | Description                                 | Min                | Typ | Max               | Unit | Condition | Spec Number |
|----------|---|--------------------|-----|-------------------|------|-----------|-------------|
| tOD_DATA | Data output delay (w.r.t. SCK) <sup>2</sup> | 0.816              | —   | 2.567             | ns   | —         | —           |
| tOD_CS   | CS output delay (w.r.t. SCK) <sup>2,3</sup> | 3.015 - n/<br>fSCK | —   | -1.33 +<br>m/fSCK | ns   | —         | —           |
| tISU_DQS | Input setup time (w.r.t. DQS) <sup>1</sup>  | -0.616             | —   | —                 | ns   | —         | —           |
| tIH_DQS  | Input hold time (w.r.t. DQS) <sup>1</sup>   | 2.767              | —   | —                 | ns   | —         | —           |

- Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
- Output timing valid for maximum external load CL = 20pF, which is assumed to be a 12pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
- Where m=TCSS and n=TCSH-1.

### 16.8.6 QuadSPI Octal 1.8V SDR 100MHz

The SRE[2:0]=100 for 18GPIO pads and SRE[2:0]=101 for 1833Fast pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

All transitions measured at mid-supply (VDD\_IO\_QSPI/2).

Table 48. QuadSPI Octal 1.8V SDR 100MHz

| Symbol   | Description                                 | Min                | Typ | Max               | Unit | Condition | Spec Number |
|----------|---|--------------------|-----|-------------------|------|-----------|-------------|
| fSCK     | SCK clock frequency <sup>1,2</sup>          | —                  | —   | 100               | MHz  | —         | —           |
| tCL_SCK  | SCK clock low time <sup>1,2</sup>           | 4.5                | —   | —                 | ns   | —         | —           |
| tCH_SCK  | SCK clock high time <sup>1,2</sup>          | 4.5                | —   | —                 | ns   | —         | —           |
| tOD_DATA | Data output delay (w.r.t. SCK) <sup>2</sup> | -2.822             | —   | 2.822             | ns   | —         | —           |
| tOD_CS   | CS output delay (w.r.t. SCK) <sup>2,3</sup> | 3.016 - n/<br>fSCK | —   | 5.160 +<br>m/fSCK | ns   | —         | —           |
| tISU_SCK | Input setup time (w.r.t. SCK) <sup>1</sup>  | 3.036              | —   | —                 | ns   | —         | —           |
| tIH_SCK  | Input hold time (w.r.t. SCK) <sup>1</sup>   | 0.9                | —   | —                 | ns   | —         | —           |

- Input timing assumes an input signal transition of 1ns (20%/80%).
- Output timing valid for maximum external load CL = 20pF, which is assumed to be a 10pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.
- Where m=TCSS and n=TCSH-1.

### 16.8.7 QuadSPI Quad 1.8V SDR 133MHz

The SRE[2:0]=100 for 18GPIO pads and SRE[2:0]=101 for 1833Fast pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

All transitions measured at mid-supply (VDD\_IO\_QSPI/2).

Table 49. QuadSPI Quad 1.8V SDR 133MHz

| Symbol   | Description                                 | Min                | Typ | Max               | Unit | Condition        | Spec Number |
|----------|---|--------------------|-----|-------------------|------|------------------|-------------|
| fSCK     | SCK clock frequency <sup>1,2</sup>          | —                  | —   | 133               | MHz  | DLL mode enabled | —           |
| tCL_SCK  | SCK low time <sup>1,2</sup>                 | 3.383              | —   | —                 | ns   | —                | —           |
| tCH_SCK  | SCK high time <sup>1,2</sup>                | 3.383              | —   | —                 | ns   | —                | —           |
| tOD_DATA | Data output delay (w.r.t. SCK) <sup>1</sup> | -0.594             | —   | 1.594             | ns   | —                | —           |
| tOD_CS   | CS output delay (w.r.t. SCK) <sup>1,3</sup> | 4.016 - n/<br>fSCK | —   | 4.204 +<br>m/fSCK | ns   | —                | —           |
| tISU_SCK | Input setup time (w.r.t. SCK) <sup>2</sup>  | 0.580              | —   | —                 | ns   | —                | —           |
| tIH_SCK  | Input hold time (w.r.t. SCK) <sup>2</sup>   | 1.000              | —   | —                 | ns   | —                | —           |

1. Output timing valid for maximum external load CL = 20pF, which is assumed to be a 10pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
2. Input timing assumes maximum input signal transition of 1ns (20%/80%).
3. Where m=TCSS and n=TCSH-1.

### 16.8.8 QuadSPI Quad 3.3V DDR 66MHz

The SRE[2:0]=100 for 18GPIO pads and SRE[2:0]=101 for 1833Fast pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

All transitions measured at mid-supply (VDD\_IO\_QSPI/2).

Table 50. QuadSPI Quad 3.3V DDR 66MHz

| Symbol   | Description                                 | Min   | Typ | Max   | Unit | Condition        | Spec Number |
|----------|---|-------|-----|-------|------|------------------|-------------|
| fSCK     | SCK clock frequency <sup>1,2</sup>          | —     | —   | 66    | MHz  | DLL mode enabled | —           |
| tCL_SCK  | SCK clock low time <sup>1,2</sup>           | 6.818 | —   | —     | ns   | —                | —           |
| tCH_SCK  | SCK clock high time <sup>1,2</sup>          | 6.818 | —   | —     | ns   | —                | —           |
| tOD_DATA | Data output delay (w.r.t. SCK) <sup>1</sup> | 2.316 | —   | 4.802 | ns   | —                | —           |

Table continues on the next page...

**Table 50. QuadSPI Quad 3.3V DDR 66MHz (continued)**

| Symbol | Description                                     | Min            | Typ | Max            | Unit | Condition | Spec Number |
|--------|---|----------------|-----|----------------|------|-----------|-------------|
| tOD_CS | CS output delay (w.r.t. SCK) <sup>1,3</sup>     | 5.016 - n/fSCK | —   | 1.802 + m/fSCK | ns   | —         | —           |
| tDVW   | Input data valid window <sup>2</sup>            | 5.14           | —   | —              | ns   | —         | —           |
| tLSKEW | Skew target for Auto-learning mode <sup>4</sup> | 1.89           | —   | —              | ns   | —         | —           |

1. Output timing valid for maximum external load CL = 20pF, which is assumed to be a 10pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
2. Input timing assumes maximum input signal transition of 1ns (20%/80%).
3. Where m=TCSS and n=TCSH-1.
4. Data valid window includes DLL Margin, and determines LEARNING skew targets which can be more pessimistic than tISU\_SCK and tIH\_SCK..

### 16.8.9 QuadSPI Quad 3.3V SDR 104MHz

The SRE[2:0]=100 for 18GPIO pads and SRE[2:0]=101 for 1833Fast pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

All transitions measured at mid-supply (VDD\_IO\_QSPI/2).

**Table 51. QuadSPI Quad 3.3V SDR 104MHz**

| Symbol   | Description                                 | Min            | Typ | Max            | Unit | Condition | Spec Number |
|----------|---|----------------|-----|----------------|------|-----------|-------------|
| fSCK     | SCK clock frequency <sup>1,2</sup>          | —              | —   | 104            | MHz  | —         | —           |
| tCL_SCK  | SCK clock low time <sup>1,2</sup>           | 4.327          | —   | —              | ns   | —         | —           |
| tCH_SCK  | SCK clock high time <sup>1,2</sup>          | 4.327          | —   | —              | ns   | —         | —           |
| tOD_DATA | Data output delay (w.r.t. SCK) <sup>1</sup> | -2.330         | —   | 2.880          | ns   | —         | —           |
| tOD_CS   | CS output delay (w.r.t. SCK) <sup>1,3</sup> | 3.391 - n/fSCK | —   | 5.901 + m/fSCK | ns   | —         | —           |
| tISU_SCK | Input setup time (w.r.t. SCK) <sup>2</sup>  | 2.152          | —   | —              | ns   | —         | —           |
| tIH_SCK  | Input hold time (w.r.t. SCK) <sup>2</sup>   | 2.0            | —   | —              | ns   | —         | —           |

1. Timing valid for maximum external load CL = 20pF, which is assumed to be a 10pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.
2. Input timing assumes maximum input signal transition of 1ns (20%/80%).
3. Where m=TCSS and n=TCSH-1.

### 16.8.10 QuadSPI Octal 1.8V DDR 166MHz

The information in this section applies to Octal- and Hyperflash.

The SRE[2:0]=000 for 18GPIO pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply

**Table 52. QuadSPI Octal 1.8V DDR 166MHz**

| Symbol   | Description                                 | Min            | Typ | Max             | Unit | Condition  | Spec Number |
|----------|---|----------------|-----|-----------------|------|--|-------------|
| fSCK-DQS | SCK/DQS frequency <sup>1,2</sup>            | —              | —   | 166             | MHz  | fSCK duty cycle distortion is in the range of 45%-55%. | —           |
| tCL_SCK  | SCK low time <sup>1,2</sup>                 | 2.711          | —   | —               | ns   | —  | —           |
| tCH_SCK  | SCK high time <sup>1,2</sup>                | 2.711          | —   | —               | ns   | —  | —           |
| tOD_DATA | Data output delay (w.r.t. SCK) <sup>1</sup> | 0.616          | —   | 2.095           | ns   | —  | —           |
| tOD_CS   | CS output delay (w.r.t. SCK) <sup>1,3</sup> | 3.016 - n/fSCK | —   | -1.805 + m/fSCK | ns   | —  | —           |
| tIH_DQS  | Input hold time (w.r.t. DQS) <sup>2</sup>   | 2.105          | —   | —               | ns   | —  | —           |
| tISU_DQS | Input setup time (w.r.t. DQS) <sup>2</sup>  | -0.616         | —   | —               | ns   | —  | —           |

1. Output timing valid for maximum external load CL = 20pF, which is assumed to be a 12pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
2. Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
3. Where m=TCSS and n=TCSH-1.

### 16.8.11 QuadSPI Octal 1.8V DDR 200MHz

In Single SRE configuration SRE[2:0]=000 for Data & CLK both, and in Split SRE configuration SRE[2:0]=000 for Data & SRE[2:0]=110 for CLK are the required drive settings to meet the timing for 18GPIO pad.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply

**Table 53. QuadSPI Octal 1.8V DDR 200MHz**

| Symbol   | Description                      | Min  | Typ | Max | Unit | Condition  | Spec Number |
|----------|----------------------------------|------|-----|-----|------|--|-------------|
| fSCK-DQS | SCK/DQS frequency <sup>1,2</sup> | —    | —   | 200 | MHz  | fSCK duty cycle distortion is in the range of 45%-55%. | —           |
| tCL_SCK  | SCK low time <sup>1,2</sup>      | 2.25 | —   | —   | ns   | —  | —           |

*Table continues on the next page...*

**Table 53. QuadSPI Octal 1.8V DDR 200MHz (continued)**

| Symbol   | Description                                 | Min            | Typ | Max             | Unit | Condition   | Spec Number |
|----------|---|----------------|-----|-----------------|------|---|-------------|
| tCH_SCK  | SCK high time <sup>1,2</sup>                | 2.25           | —   | —               | ns   | —   | —           |
| tOD_DATA | Data output delay (w.r.t. SCK) <sup>1</sup> | 0.616          | —   | 1.634           | ns   | Split SRE configuration, SRE[2:0]=000 for Data and SRE[2:0]=110 for CLK | —           |
| tOD_DATA | Data output delay (w.r.t. SCK) <sup>1</sup> | 0.772          | —   | 1.79            | ns   | Single SRE configuration, SRE[2:0]=000                                  | —           |
| tOD_CS   | CS output delay (w.r.t. SCK) <sup>1,3</sup> | 3.016 - n/fSCK | —   | -2.266 + m/fSCK | ns   | —   | —           |
| tIH_DQS  | Input hold time (w.r.t. DQS) <sup>2</sup>   | 1.644          | —   | —               | ns   | —   | —           |
| tISU_DQS | Input setup time (w.r.t. DQS) <sup>2</sup>  | -0.586         | —   | —               | ns   | —   | —           |

- Output timing valid for maximum external load CL = 20pF, which is assumed to be a 12pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
- Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
- Where m=TCSS and n=TCSH-1.

### 16.8.12 QuadSPI configurations

The below table shows a subset of the QuadSPI module configurations for different speeds and data rates. The configuration values for each case are equally applicable to Quad, Octal and HyperFlash interfaces, so long as the maximum clock frequency as per [Table 55](#) is not exceeded.

**Table 54. QuadSPI configurations**

| -             | DDR-200MHz                | DDR-133MHz                | SDR-133MHz            | SDR-104MHz            | DDR-66MHz             |
|---------------|---------------------------|---------------------------|-----------------------|-----------------------|-----------------------|
| DQS mode      | External DQS Edge Aligned | External DQS Edge Aligned | Internal pad loopback | Internal pad loopback | Internal pad loopback |
| Sampling mode | DDR                       | DDR                       | SDR                   | SDR                   | DDR                   |
| DLL Mode      | DLL Enable                | DLL Enable                | DLL Bypass            | DLL Bypass            | DLL Enable            |
| Data Learning | No                        | No                        | No                    | No                    | Yes                   |
| IO Voltage    | 1.8V                      | 1.8V                      | 1.8V                  | 3.3V                  | 1.8V/3.3V             |
| Frequency     | 166/200 MHz               | 100/133 MHz               | 100/133 MHz           | 104 MHz               | 66 MHz                |
| FLSHCR[TDH]   | 1                         | 1                         | 0                     | 0                     | 1                     |
| FLSHCR[TCSH]  | 3                         | 3                         | 3                     | 3                     | 3                     |

*Table continues on the next page...*



**Table 54. QuadSPI configurations (continued)**

| -                      | DDR-200MHz                 | DDR-133MHz | SDR-133MHz | SDR-104MHz | DDR-66MHz |
|------------------------|----------------------------|------------|------------|------------|-----------|
| FLSHCR[TCSS]           | 3                          | 3          | 3          | 3          | 3         |
| MCR[DLPEN]             | 0                          | 0          | 0          | 0          | 1         |
| DLLCR[DLEN]            | 1                          | 1          | 0          | 0          | 1         |
| DLLCR[FREQEN]          | 1                          | 0          | 0          | 0          | 0         |
| DLLCR[DLL_REFCNTR]     | 2                          | 2          | NA         | NA         | 2         |
| DLLCR[DLLRES]          | 8                          | 8          | NA         | NA         | 8         |
| DLLCR[SLV_FINE_OFFSET] | 0                          | 0          | 0          | 0          | 0         |
| DLLCR[SLV_DLY_OFFSET]  | 0                          | 0          | 0          | 0          | 3         |
| DLLCR[SLV_DLY_COARSE]  | NA                         | NA         | 0          | 0          | 0         |
| DLLCR[SLAVE_AUTO_UPDT] | 1                          | 1          | 0          | 0          | 1         |
| DLLCR[SLV_EN]          | 1                          | 1          | 1          | 1          | 1         |
| DLLCR[SLV_DLL_BYPASS]  | 0                          | 0          | 1          | 1          | 0         |
| DLLCR[SLV_UPD]         | 1                          | 1          | 1          | 1          | 1         |
| SMPR[DLLFSMPF]         | 3 (200 Mhz)<br>4 (166 Mhz) | 4          | 0          | 0          | NA        |
| SMPR[FSDLY]            | 0                          | 0          | 0          | 0          | 1         |
| SMPR[FSPHS]            | NA                         | NA         | 1          | 1          | NA        |

### 16.8.13 QuadSPI interfaces

The QuadSPI module supports 2 interfaces; QSPI A & QSPI B. These interfaces are not independent & the QSPI chapter of the reference manual should be consulted for their usage. The table below summarizes which specifications are supported on each interface.

**Table 55. QuadSPI interfaces**

| Specification / Interface | 3.3V Quad               | 1.8V Quad                   | 1.8V Octal                                   | 1.8V Hyperflash     |
|---------------------------|-------------------------|-----------------------------|--|---------------------|
| <b>QSPI A</b>             | n/a                     | SDR 100/133MHz<br>DDR 66MHz | SDR 100/133MHz<br>DDR<br>100/133/166/200 MHz | DDR 100/133/166 MHz |
| <b>QSPI B</b>             | SDR 104MHz<br>DDR 66MHz | SDR 100/133MHz<br>DDR 66MHz | SDR 100/133MHz<br>DDR 100/133MHz             | DDR 100/133MHz      |

### 16.8.14 QuadSPI timing diagrams

The sections shows the QuadSPI timing diagrams for all modes supported by the device. All data is based on a negative edge data launch from the device.

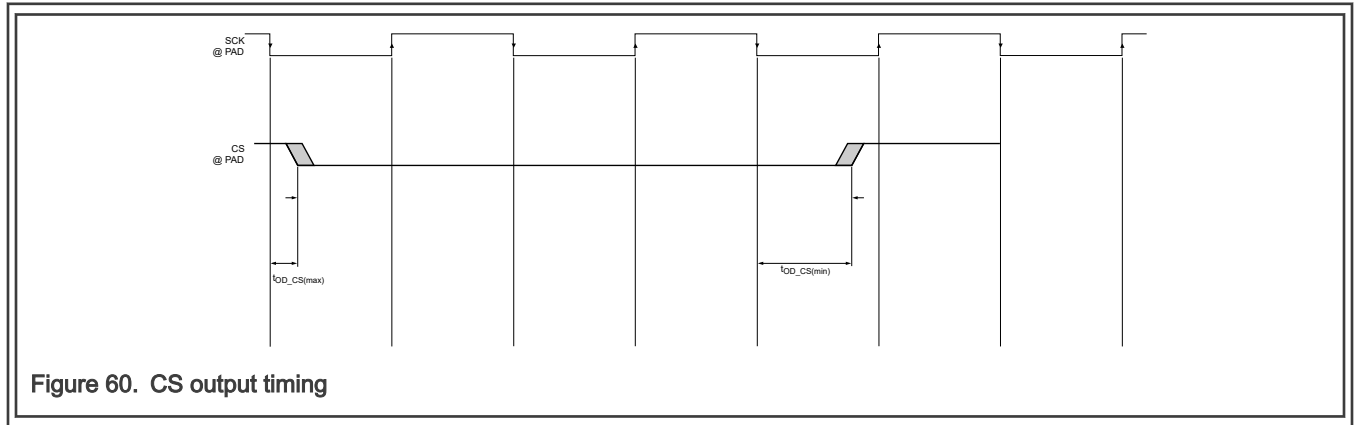


Figure 60. CS output timing

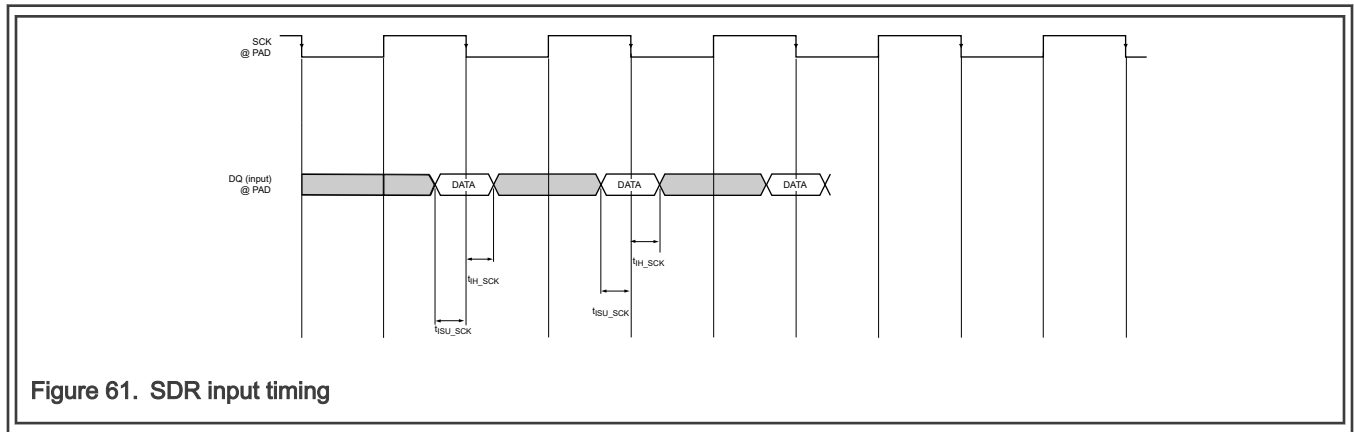


Figure 61. SDR input timing

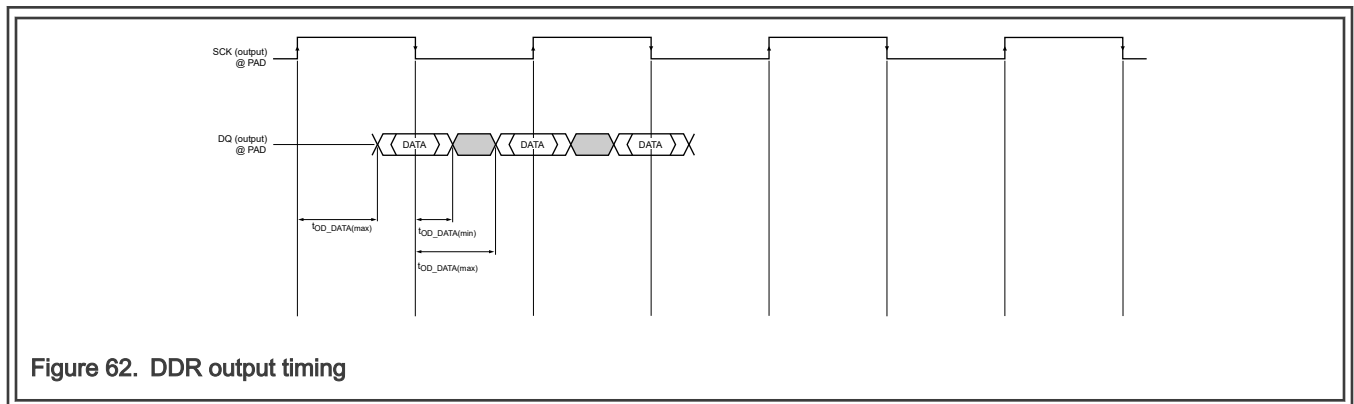


Figure 62. DDR output timing

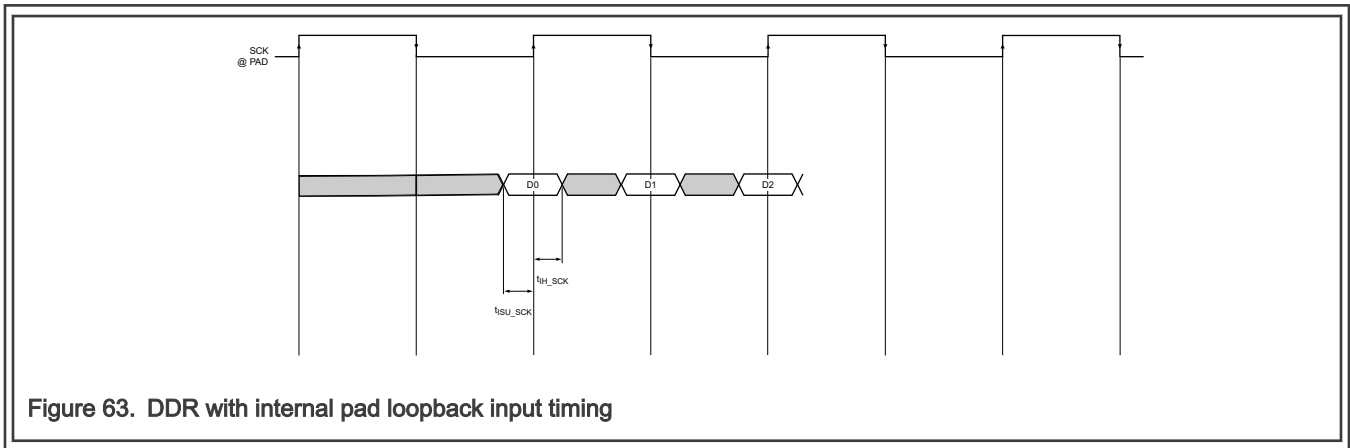


Figure 63. DDR with internal pad loopback input timing

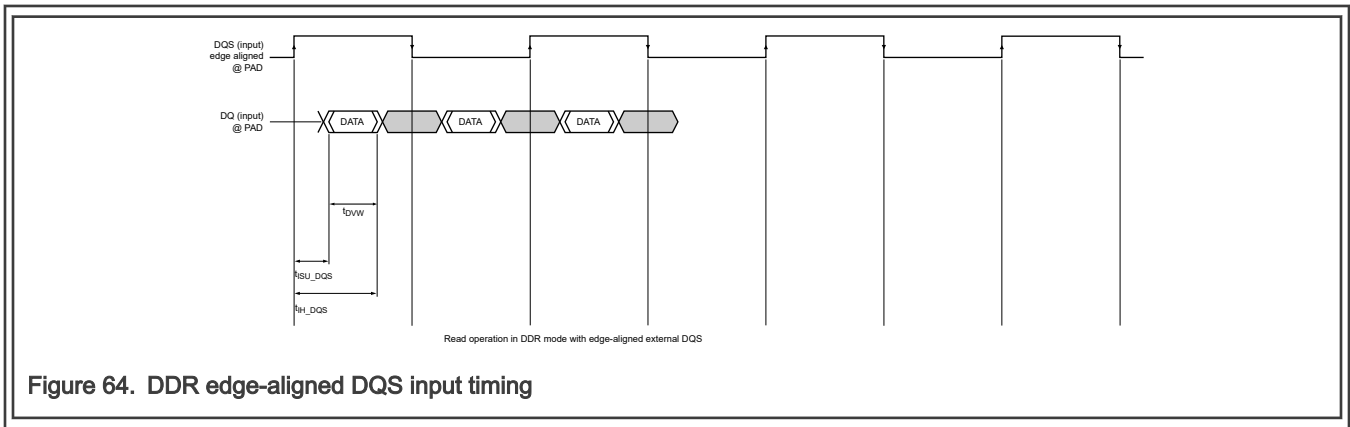


Figure 64. DDR edge-aligned DQS input timing

## 16.9 DDR

### 16.9.1 DDR

The chip supports the following memory types:

1. LPDDR4 SDRAM compliant to JEDEC209-4B LPDDR4 JEDEC standard release.
2. DDR3L SDRAM compliant to JESD79-3-1A DDR3L JEDEC standard release July, 2010.

DDR operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the chip's Hardware Design Guide Document.

LPDDR4 routing constraints are documented in the chip's Hardware Design Guidelines Document.

### 16.9.2 DDR Common DC Input

The specifications given in the table below represent the common DC input conditions for all DDR interface modes. Unless otherwise specified, all input specifications (both common and DDR standard specific) are measured at the host PHY input pins. Subsequent sections list input parameters for the specific memory interface standards.

**Table 56. DDR Common DC Input**

| Symbol       | Description                             | Min        | Typ | Max          | Unit | Condition | Spec Number |
|--------------|---|------------|-----|--------------|------|-----------|-------------|
| IIZ-VREF     | VREF input leakage current <sup>1</sup> | -50        | —   | 50           | uA   | —         | —           |
| IIZ-BP       | Input leakage current <sup>2</sup>      | -50        | —   | 50           | uA   | —         | —           |
| VIH-DC_BPDAT | Input high voltage threshold            | VREF+0.085 | —   | —            | V    | —         | —           |
| VIL-DC_BPDAT | Input low voltage threshold             | —          | —   | vref - 0.085 | V    | —         | —           |

1. Leakage is valid for Vref over the range  $0 \leq V_{IN} \leq V_{DD\_IO\_DDR0}$ , with Vref input function enabled. All pins not under test = VDD\_IO\_DDR0.
2. Leakage current is measured when the pin is configured to a high-impedance state with all on-die termination disabled. Leakage is valid for any input except for Vref over the range:  $0 \leq V_{IN} \leq V_{DD\_IO\_DDR0}$ . All pins not under test = VSS or VDD\_IO\_DDR0.

### 16.9.3 DDR Common DC Output

**Table 57. DDR Common DC Output**

| Symbol | Description   | Min | Typ       | Max | Unit | Condition | Spec Number |
|--------|---|-----|-----------|-----|------|-----------|-------------|
| ROnPu  | Output driver pull-up impedance: DQ, DQS outputs <sup>1</sup>             | —   | 120,60,40 | —   | Ohm  | —         | —           |
| ROnPd  | Output driver pull-down impedance: DQ, DQS outputs <sup>1</sup>           | —   | 120,60,40 | —   | Ohm  | —         | —           |
| ROnPu  | Output driver pull-up impedance: address, command <sup>1</sup>            | —   | 120,60,40 | —   | Ohm  | —         | —           |
| ROnPd  | Output driver pull-down impedance: address, command <sup>1</sup>          | —   | 120,60,40 | —   | Ohm  | —         | —           |
| ROnPu  | Output driver pull-up impedance: DDR0_RESET_B, CKE outputs <sup>2</sup>   | —   | 18-28     | —   | Ohm  | —         | —           |
| ROnPd  | Output driver pull-down impedance: DDR0_RESET_B, CKE outputs <sup>2</sup> | —   | 18-28     | —   | Ohm  | —         | —           |

1. Calibrated at  $V_{DD\_IO\_DDR0} / 2$ .
2. For the DDR0\_RESET\_B pin and CKE pin, the driver is in maximum strength and impedance value is process dependent.

NOTE: Refer to IBIS model for the complete IV curve characteristics.

### 16.9.4 DDR3L DC Input

Table 58. DDR3L DC Input

| Symbol | Description                            | Min  | Typ  | Max  | Unit        | Condition | Spec Number |
|--------|--|------|------|------|-------------|-----------|-------------|
| Vref   | Input reference voltage <sup>1,2</sup> | 30.1 | 31.1 | 32.1 | %VDD_IO_DDR | —         | —           |

- Externally supplied Vref is not recommended. Internal Vref generation through local Vref generation at each receiver is preferred.
- If the external Vref to the receivers is enabled, DDR0\_VREF is expected to be set to a nominal value of  $(VDD\_IO\_DDR0/2) * RxAtten$  (RxAttenuation for DDR3L is 0.623) through a voltage divider in order to track VDD\_IO\_DDR0 level. It can be adjusted in the system to margin the input DQ signals, although this margin does not necessarily represent the eye height since a change in Vref also changes the input receiver common mode, altering receiver performance.

### 16.9.5 DDR3L Output Timing

Table 59. DDR3L Output Timing

| Symbol    | Description  | Min | Typ  | Max | Unit | Condition | Spec Number |
|-----------|--|-----|------|-----|------|-----------|-------------|
| tCK(avg)  | Average clock period <sup>1,2</sup>                                  | —   | 1.25 | —   | ns   | —         | —           |
| tOS(Vref) | Command and address setup time to CK (to Vref levels) <sup>1,2</sup> | 350 | —    | —   | ps   | —         | —           |
| tOH(Vref) | Command and address hold time to CK (to Vref levels) <sup>1,2</sup>  | 350 | —    | —   | ps   | —         | —           |
| tDOeye    | Output data eye <sup>1,2</sup>                                       | 0.6 | —    | —   | UI   | —         | —           |

- All measurements are in reference to the Vref level.
- Measurements were done with signals terminated with a 50ohm resistor terminated to VDD\_IO\_DDR0/2, Phy output is calibrated to a drive strength of 40ohms. Slew rate AtxSlewRate was set to 0x3FF (PreDrvMode=3, PreN=F,PreP=F); TxSlewRate was set 0x3FF (PreDrvMode=3, PreN=F,PreP=F).

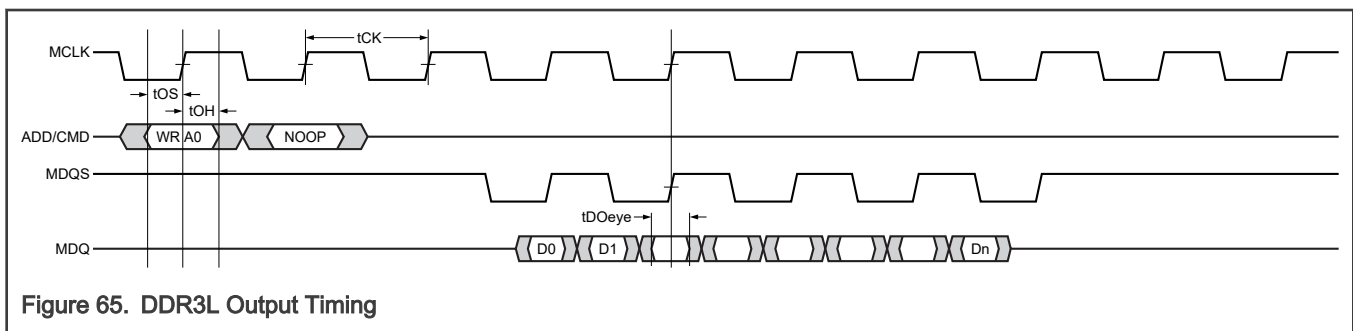


Figure 65. DDR3L Output Timing

### 16.9.6 LPDDR4 DC Input timing

Table 60. LPDDR4 DC Input timing

| Symbol | Description                               | Min | Typ      | Max | Unit | Condition | Spec Number |
|--------|---|-----|----------|-----|------|-----------|-------------|
| Vref   | Internal reference voltage <sup>1,2</sup> | —   | Variable | —   | V    | —         | —           |

1. Because termination at the DRAMs is configurable, there is no fixed setting. The Vref value is dependent on driver impedance Ron and system effective ODT impedance Rtt.
2. Externally supplied Vref is not recommended. Internal Vref generation through local Vref generation at each receiver is preferred.

### 16.9.7 LPDDR4 Output Timing

Table 61. LPDDR4 Output Timing

| Symbol   | Description                       | Min  | Typ   | Max | Unit | Condition | Spec Number |
|----------|-----------------------------------|------|-------|-----|------|-----------|-------------|
| tCK(avg) | Average clock period <sup>1</sup> | —    | 0.625 | —   | ns   | —         | —           |
| tDOeye   | Output data eye <sup>1,2,3</sup>  | 0.55 | —     | —   | UI   | —         | —           |
| tCAOeye  | CA output data eye <sup>1,4</sup> | 0.62 | —     | —   | UI   | UI=625ps  | —           |

1. Measurements were done with signals terminated with a 50ohm resistor terminated to VSS, Phy output is calibrated to a drive strength of 40ohms. Slew rate AtxSlewRate was set to 0x1FF (PreDrvMode=1, PreN=F,PreP=F); TxSlewRate was set 0x1FF (PreDrvMode=1, PreN=F, PreP=F).
2. tDOeye is trained to be shifted min 200 ps from DQS edge (tDQS2DQ learning).
3. Tx DQS to MCLK edges are trained to be aligned.
4. Addr/Cmd is centered aligned by training.

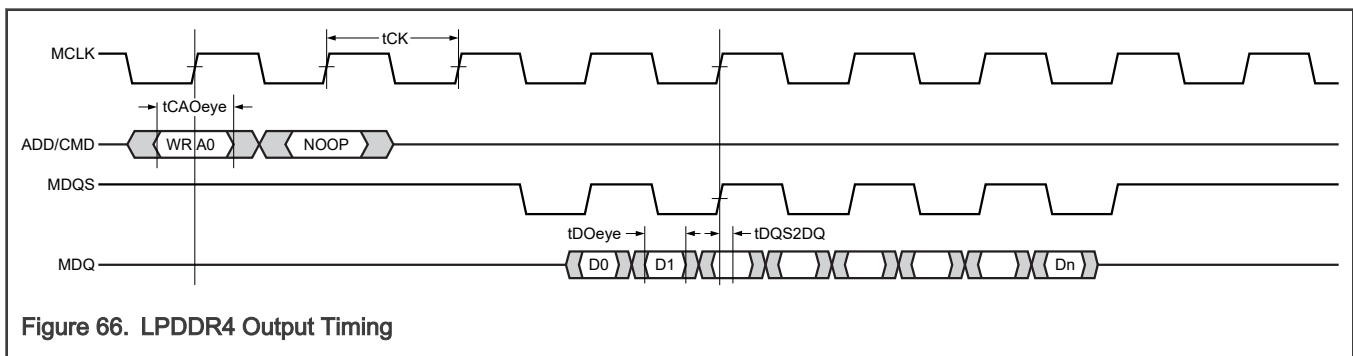


Figure 66. LPDDR4 Output Timing

## 16.10 uSDHC

### 16.10.1 uSDHC SD3.0/eMMC5.1 DDR

The SRE[2:0]=101 is required drive setting to meet the timing.

All uSDHC parameters are measured at mid-supply (VDD\_IO\_SDHC/2).

Table 62. uSDHC SD3.0/eMMC5.1 DDR

| Symbol | Description                                   | Min  | Typ | Max | Unit | Condition            | Spec Number                    |
|--------|---|------|-----|-----|------|----------------------|--------------------------------|
| fpp    | Clock frequency (eMMC5.1 DDR) <sup>1</sup>    | —    | —   | 52  | MHz  | —                    | SD1                            |
| fpp    | Clock frequency (SD3.0 DDR) <sup>1</sup>      | —    | —   | 50  | MHz  | —                    | SD1                            |
| tWL    | Clock low time                                | 8.8  | —   | —   | ns   | —                    | —                              |
| tWH    | Clock high time                               | 8.8  | —   | —   | ns   | —                    | —                              |
| tTLH   | Clock rise time <sup>1,2</sup>                | —    | —   | 0.8 | ns   | —                    | —                              |
| tTHL   | Clock fall time <sup>1,2</sup>                | —    | —   | 0.8 | ns   | —                    | —                              |
| tOD    | SDHC output delay (output valid) <sup>1</sup> | 2.7  | —   | 5.6 | ns   | SDHC_CLK to SDHC_DAT | SD2                            |
| tOD    | SDHC output delay (output valid) <sup>1</sup> | -5.6 | —   | 2.6 | ns   | SDHC_CLK to SDHC_CMD | SD6<br>(See SDR-52 MHz figure) |
| tISU   | SDHC Input setup time <sup>3</sup>            | 1.6  | —   | —   | ns   | SDHC_DAT to SDHC_CLK | SD3                            |
| tISU   | SDHC Input setup time <sup>3</sup>            | 4.8  | —   | —   | ns   | SDHC_CMD to SDHC_CLK | SD7<br>(See SDR-52 MHz figure) |
| tIH    | SDHC Input hold time <sup>3</sup>             | 1.5  | —   | —   | ns   | SDHC_CLK to SDHC_DAT | SD4                            |
| tIH    | SDHC Input hold time <sup>3</sup>             | 1.5  | —   | —   | ns   | SDHC_CLK to SDHC_CMD | SD8<br>(See SDR-52 MHz figure) |

- Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin).
- The SDHC\_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC\_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
- Input timing assumes an input signal slew rate of 3ns (20%/80%).

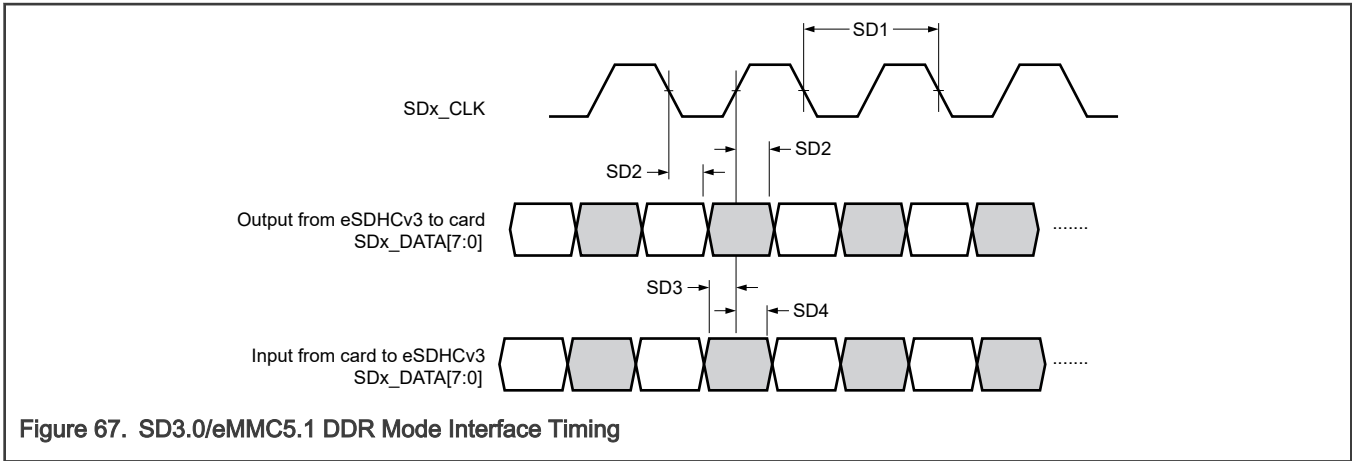


Figure 67. SD3.0/eMMC5.1 DDR Mode Interface Timing

### 16.10.2 uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR

The SRE[2:0]=101 is required drive setting to meet the timing.

All uSDHC parameters are measured at mid-supply (VDD\_IO\_SDHC/2).

Table 63. uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR

| Symbol | Description   | Min  | Typ | Max   | Unit | Condition                       | Spec Number |
|--------|---|------|-----|-------|------|---------------------------------|-------------|
| fpp    | Clock frequency (low speed) <sup>1, 2</sup>                     | —    | —   | 400   | kHz  | —                               | SD1         |
| fpp    | Clock frequency (SD/SDIO full speed/high speed) <sup>2, 3</sup> | —    | —   | 25/50 | MHz  | —                               | SD1         |
| fpp    | Clock frequency (eMMC full speed/high speed) <sup>2, 4</sup>    | —    | —   | 20/52 | MHz  | —                               | SD1         |
| fOD    | Clock frequency (identification mode) <sup>2</sup>              | 100  | —   | 400   | kHz  | —                               | SD1         |
| tWL    | Clock low time  | 8.8  | —   | —     | ns   | —                               | SD2         |
| tWH    | Clock high time   | 8.8  | —   | —     | ns   | —                               | SD3         |
| tTLH   | Clock rise time <sup>2, 5</sup>                                 | —    | —   | 0.8   | ns   | —                               | SD4         |
| tTHL   | Clock fall time <sup>2, 5</sup>                                 | —    | —   | 0.8   | ns   | —                               | SD5         |
| tOD    | SDHC output delay (output valid) <sup>2</sup>                   | -5.6 | —   | 2.6   | ns   | SDHC_CLK to SDHC_CMD / SDHC_DAT | SD6         |
| tISU   | SDHC Input setup time <sup>6</sup>                              | 4.8  | —   | —     | ns   | SDHC_CMD / SDHC_DAT to SDHC_CLK | SD7         |
| tIH    | SDHC Input hold time <sup>6</sup>                               | 1.5  | —   | —     | ns   | SDHC_CLK to SDHC_CMD / SDHC_DAT | SD8         |

1. In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7V to 3.6V.
2. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin).



3. In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.
4. In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.
5. The SDHC\_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC\_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
6. Input timing assumes an input signal slew rate of 3ns (20%/80%).

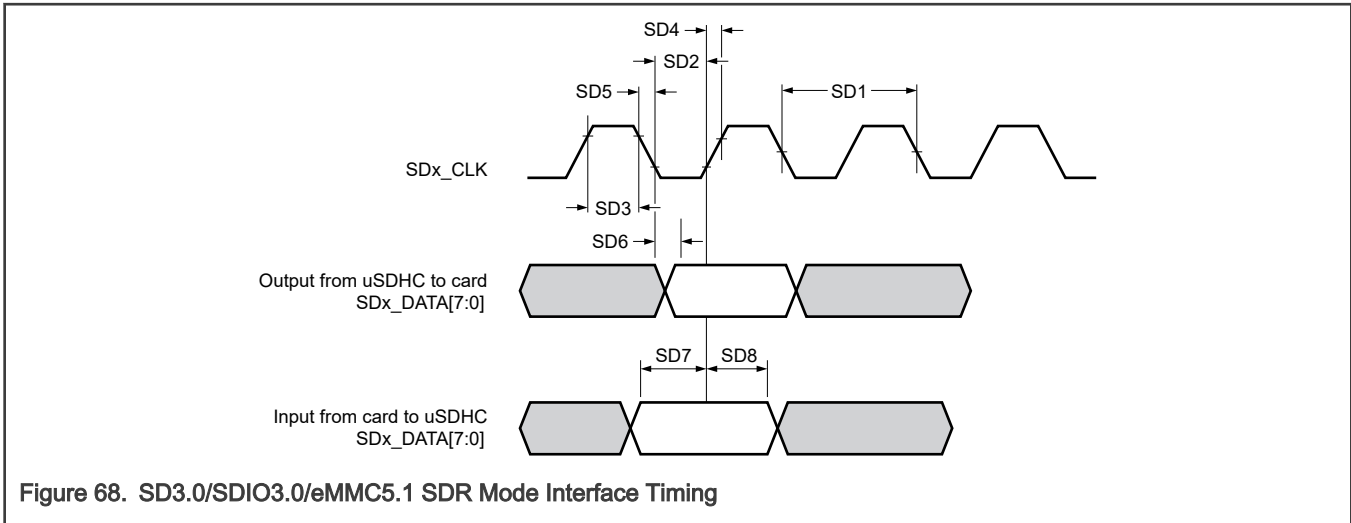


Figure 68. SD3.0/SDIO3.0/eMMC5.1 SDR Mode Interface Timing

### 16.10.3 uSDHC SDR-100MHz

The SRE[2:0]=101 is required drive setting to meet the timing.

All uSDHC parameters are measured at mid-supply (VDD\_IO\_SDHC/2).

Table 64. uSDHC SDR-100MHz

| Symbol | Description                         | Min  | Typ | Max | Unit | Condition                       | Spec Number |
|--------|-------------------------------------|------|-----|-----|------|---------------------------------|-------------|
| tCLK   | Clock frequency <sup>1</sup>        | —    | —   | 100 | MHz  | —                               | SD1         |
| tCL    | Clock low time                      | 4.5  | —   | —   | ns   | —                               | SD2         |
| tCH    | Clock high time                     | 4.5  | —   | —   | ns   | —                               | SD3         |
| tTLH   | Clock rise time <sup>1,2</sup>      | —    | —   | 0.8 | ns   | —                               | —           |
| tTHL   | Clock fall time <sup>1,2</sup>      | —    | —   | 0.8 | ns   | —                               | —           |
| tOD    | uSDHC output delay <sup>1</sup>     | -3.5 | —   | 1.3 | ns   | SDHC_CLK to SDHC_CMD / SDHC_DAT | SD4         |
| tISU   | uSDHC input setup time <sup>3</sup> | 1.3  | —   | —   | ns   | SDHC_CMD / SDHC_DAT to SDHC_CLK | SD6         |
| tIH    | uSDHC input hold time <sup>3</sup>  | 1.5  | —   | —   | ns   | SDHC_CLK to SDHC_CMD / SDHC_DAT | SD7         |

1. Output timing valid for maximum external load CL = 15pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the R<sub>DSOn</sub> of the I/O pad output driver.

- The SDHC\_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC\_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
- Input timing assumes an input signal slew rate of 1ns (20%/80%).

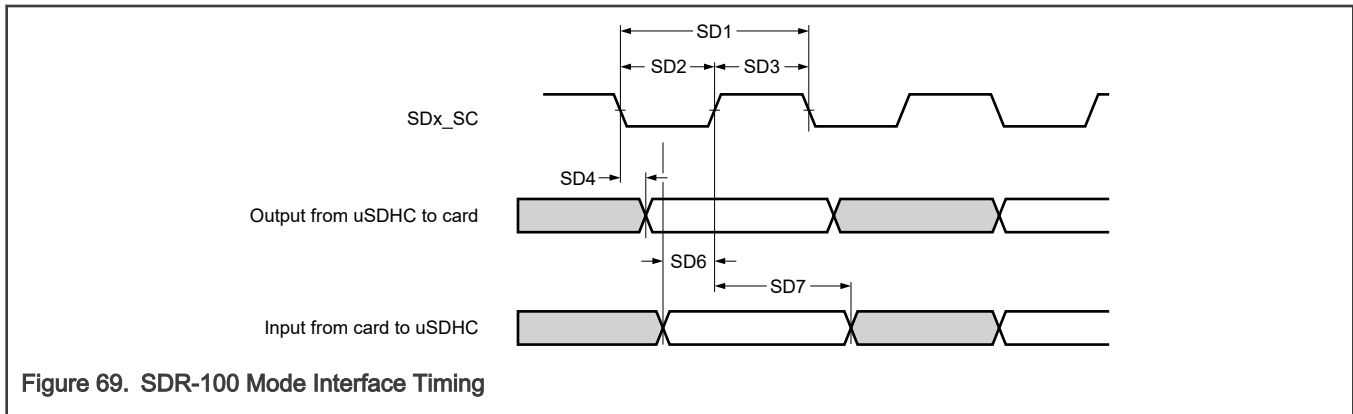


Figure 69. SDR-100 Mode Interface Timing

### 16.10.4 uSDHC SDR-HS200

The SRE[2:0]=000 is required drive setting to meet the timing.

All uSDHC parameters are measured at mid-supply (VDD\_IO\_SDHC/2).

Table 65. uSDHC SDR-HS200

| Symbol | Description                      | Min  | Typ | Max | Unit | Condition                       | Spec Number |
|--------|----------------------------------|------|-----|-----|------|---------------------------------|-------------|
| tCLK   | Clock frequency <sup>1</sup>     | —    | —   | 200 | MHz  | —                               | SD1         |
| tCL    | Clock low time                   | 2.2  | —   | —   | ns   | —                               | SD2         |
| tCH    | Clock high time                  | 2.2  | —   | —   | ns   | —                               | SD3         |
| tTLH   | Clock rise time <sup>1,2</sup>   | —    | —   | 0.8 | ns   | —                               | —           |
| tTHL   | Clock fall time <sup>1,2</sup>   | —    | —   | 0.8 | ns   | —                               | —           |
| tOD    | uSDHC output delay <sup>1</sup>  | -1.2 | —   | 0.6 | ns   | SDHC_CLK to SDHC_CMD / SDHC_DAT | SD4         |
| tODW   | Input data window <sup>3,4</sup> | 2.6  | —   | —   | ns   | —                               | SD8         |

- Output timing valid for maximum external load CL = 15pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the the I/O pad output driver.
- The SDHC\_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC\_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
- Input timing assumes an input signal slew rate of 1ns (20%/80%).
- Input timing also applicable for SDHC\_CMD also.

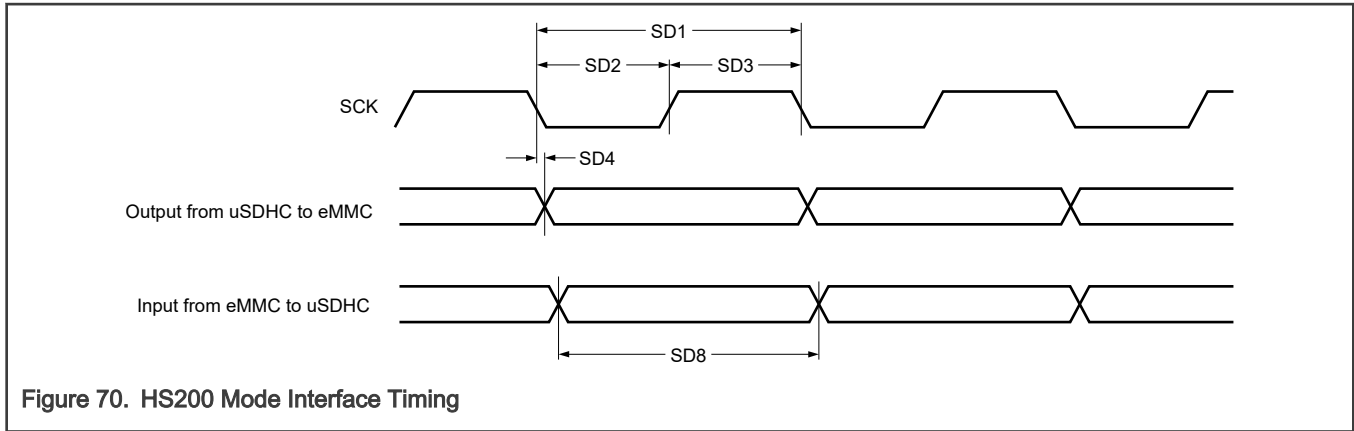


Figure 70. HS200 Mode Interface Timing

### 16.10.5 uSDHC DDR-HS400

In Split SRE configuration SRE[2:0]=000 for Data/CMD and SRE[2:0]=111 for CLK are the required drive settings to meet the timing.

Data transitions measured at 35%/65% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 66. uSDHC DDR-HS400

| Symbol | Description   | Min  | Typ | Max  | Unit | Condition            | Spec Number |
|--------|---|------|-----|------|------|----------------------|-------------|
| fPP    | Clock frequency <sup>1</sup>                        | 133  | —   | 200  | MHz  | —                    | SD1         |
| tCL    | Clock low time                                      | 2.35 | —   | —    | ns   | —                    | SD2         |
| tCH    | Clock high time                                     | 2.35 | —   | —    | ns   | —                    | SD3         |
| tTLH   | Clock rise time <sup>1,2</sup>                      | —    | —   | 0.8  | ns   | —                    | —           |
| tTHL   | Clock fall time <sup>1,2</sup>                      | —    | —   | 0.8  | ns   | —                    | —           |
| tOD1   | Output skew from Edge of Data to SCK <sup>1,3</sup> | 0.65 | —   | —    | ns   | —                    | SD4         |
| tOD2   | Output skew from Edge of SCK to Data <sup>1,3</sup> | 0.65 | —   | —    | ns   | —                    | SD5         |
| tRQ    | Input skew <sup>4,5</sup>                           | —    | —   | 0.45 | ns   | —                    | SD6         |
| tRQH   | Hold skew <sup>4,5</sup>                            | —    | —   | 0.45 | ns   | —                    | SD7         |
| tOD    | uSDHC Output delay <sup>1</sup>                     | -1.2 | —   | 0.9  | ns   | SDHC_CLK to SDHC_CMD | SD5         |

- Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 10 pF load at the end of a 500ohm, un-terminated, 2-inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.
- The SDHC\_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC\_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
- Board skew margin between CLK and DATA/CMD is considered as +/-50 ps in calculations
- Input timing assumes an input signal slew rate of 1ns (20%/80%).
- Spec numbers SD6 and SD7 are also applicable for the CMD input timing for HS400 mode in enhanced strobe mode. For HS400 mode without enhanced strobe, CMD input timing is the same as for HS200 mode.

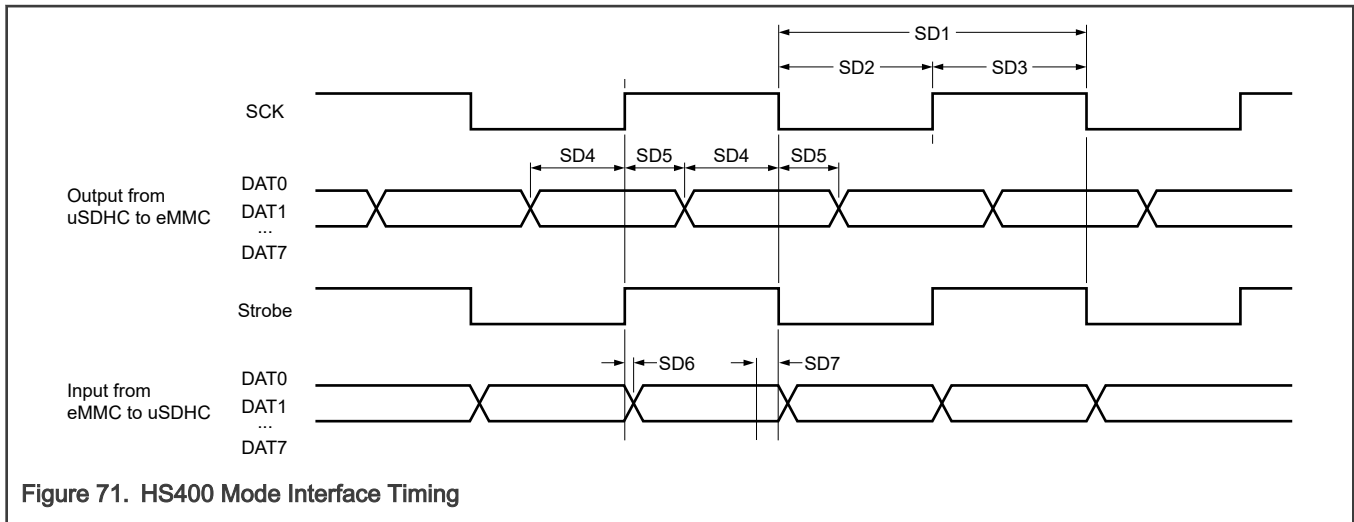


Figure 71. HS400 Mode Interface Timing

## 16.11 Debug modules

### 16.11.1 JTAG Boundary Scan

The following table gives the JTAG specifications in boundary scan mode.

The SRE[2:0]=100 or SRE[2:0]=101 is required drive setting to meet the timing.

Table 67. JTAG Boundary Scan

| Symbol       | Description                                   | Min | Typ | Max  | Unit | Condition | Spec Number |
|--------------|---|-----|-----|------|------|-----------|-------------|
| tJCYC        | TCK cycle time <sup>1, 2, 3</sup>             | 100 | —   | —    | ns   | —         | 1           |
| tJDC         | TCK clock pulse width <sup>2, 3</sup>         | 45  | —   | 55   | %    | —         | 2           |
| tTCKRISE     | TCK rise/fall time <sup>2, 4</sup>            | —   | —   | 3    | ns   | —         | 3           |
| tTMSS, tTDIS | TMS, TDI data setup time <sup>2, 5</sup>      | 5   | —   | —    | ns   | —         | 4           |
| tTMSH, tTDIH | TMS, TDI data hold time <sup>2, 5</sup>       | 5   | —   | —    | ns   | —         | 5           |
| tTDOV        | TCK low to TDO data valid <sup>2, 6, 7</sup>  | —   | —   | 17.5 | ns   | —         | 6           |
| tTDOI        | TCK low to TDO data invalid <sup>2, 6</sup>   | 0   | —   | —    | ns   | —         | 7           |
| tTDOHZ       | TCK low to TDO high impedance <sup>2, 6</sup> | —   | —   | 17.5 | ns   | —         | 8           |
| tJCMPPW      | JCOMP assertion time <sup>2</sup>             | 100 | —   | —    | ns   | —         | 9           |
| tJCMPS       | JCOMP setup time to TCK high <sup>2</sup>     | 40  | —   | —    | ns   | —         | 10          |

Table continues on the next page...

Table 67. JTAG Boundary Scan (continued)

| Symbol  | Description  | Min | Typ | Max | Unit | Condition | Spec Number |
|---------|--|-----|-----|-----|------|-----------|-------------|
| tBSDV   | TCK falling edge to output valid <sup>2, 6, 8</sup>                    | —   | —   | 600 | ns   | —         | 11          |
| tBSDVZ  | TCK falling edge to output valid out of high impedance <sup>2, 6</sup> | —   | —   | 600 | ns   | —         | 12          |
| tBSDVHZ | TCK falling edge to output high impedance <sup>2, 6</sup>              | —   | —   | 600 | ns   | —         | 13          |
| tBSDST  | Boundary scan input valid to TCK rising edge <sup>2</sup>              | 15  | —   | —   | ns   | —         | 14          |
| tBSDHT  | TCK rising edge to boundary scan input invalid <sup>2</sup>            | 15  | —   | —   | ns   | —         | 15          |

1. JTAG port interface speed only. Does not apply to boundary scan timing.
2. These specifications apply to JTAG boundary scan mode only.
3. TCK pin must have external pull down.
4. The TCK rise/fall time specification applies to the input clock transition required in order to meet the TDO output specifications that are relative to TCK.
5. Input timing assumes an input signal slew rate of 3ns (20%/80%).
6. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the selected RDSO of the I/O pad output driver.
7. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
8. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

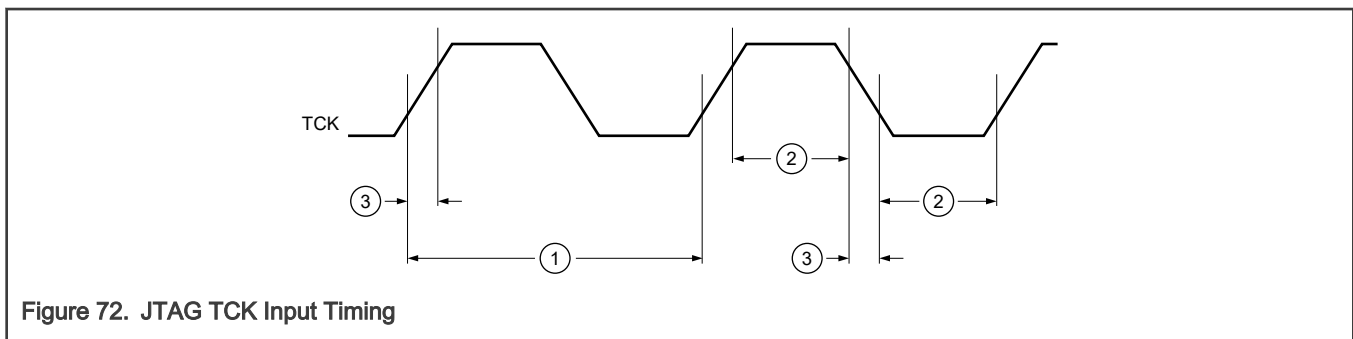


Figure 72. JTAG TCK Input Timing

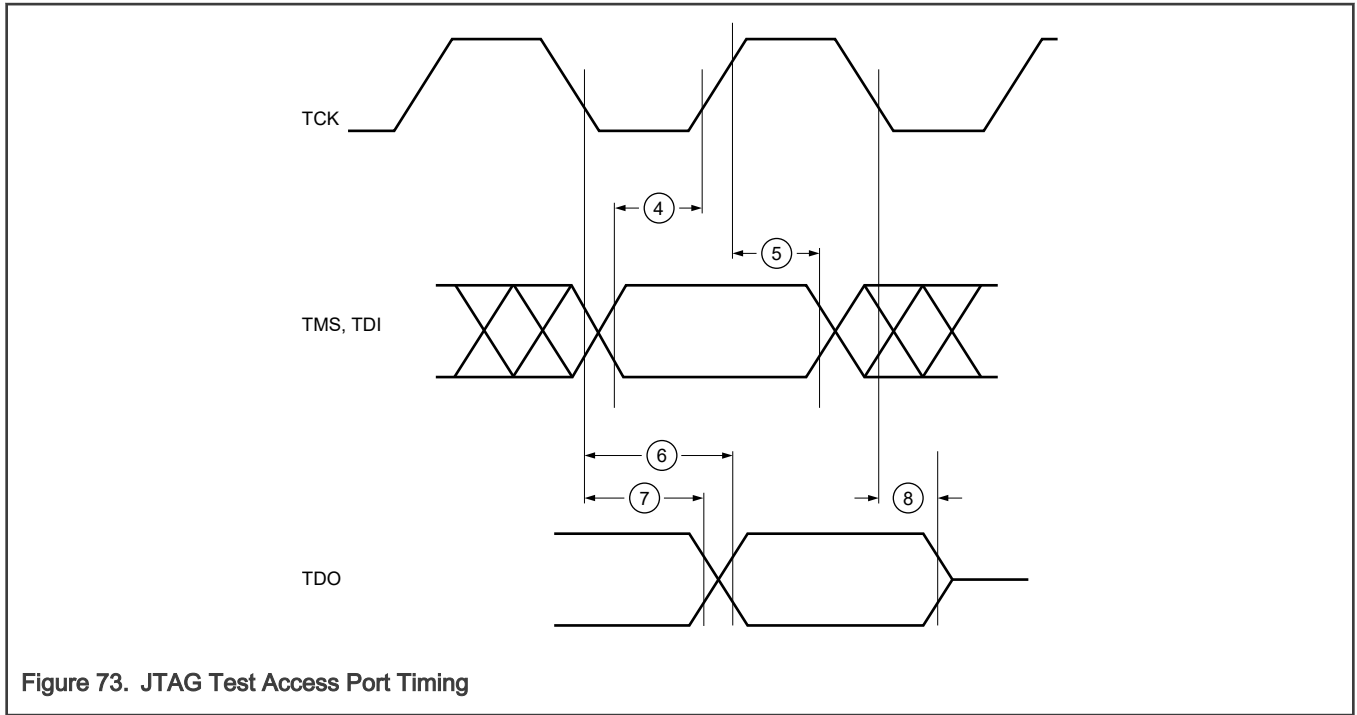


Figure 73. JTAG Test Access Port Timing

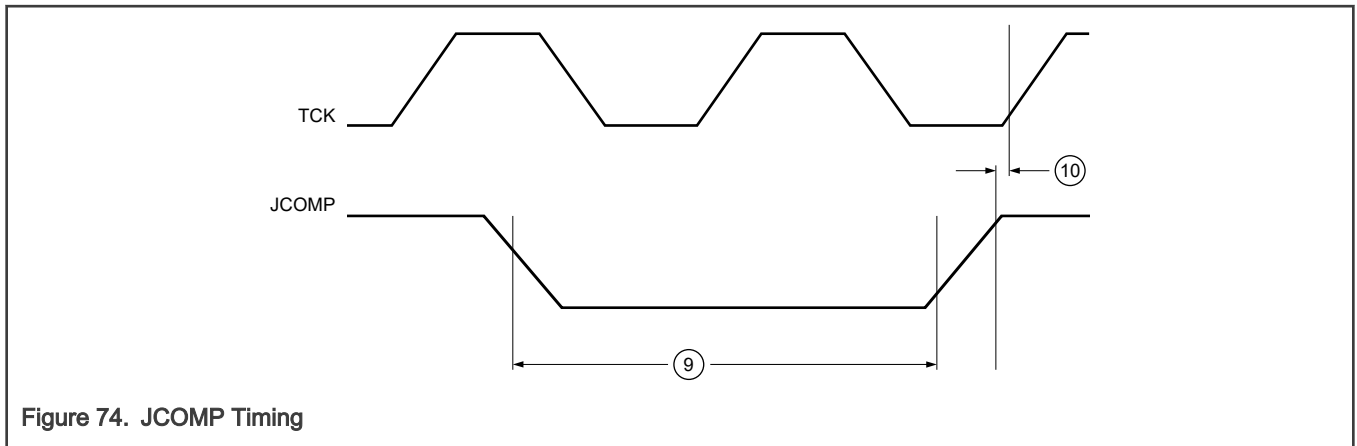


Figure 74. JCOMP Timing

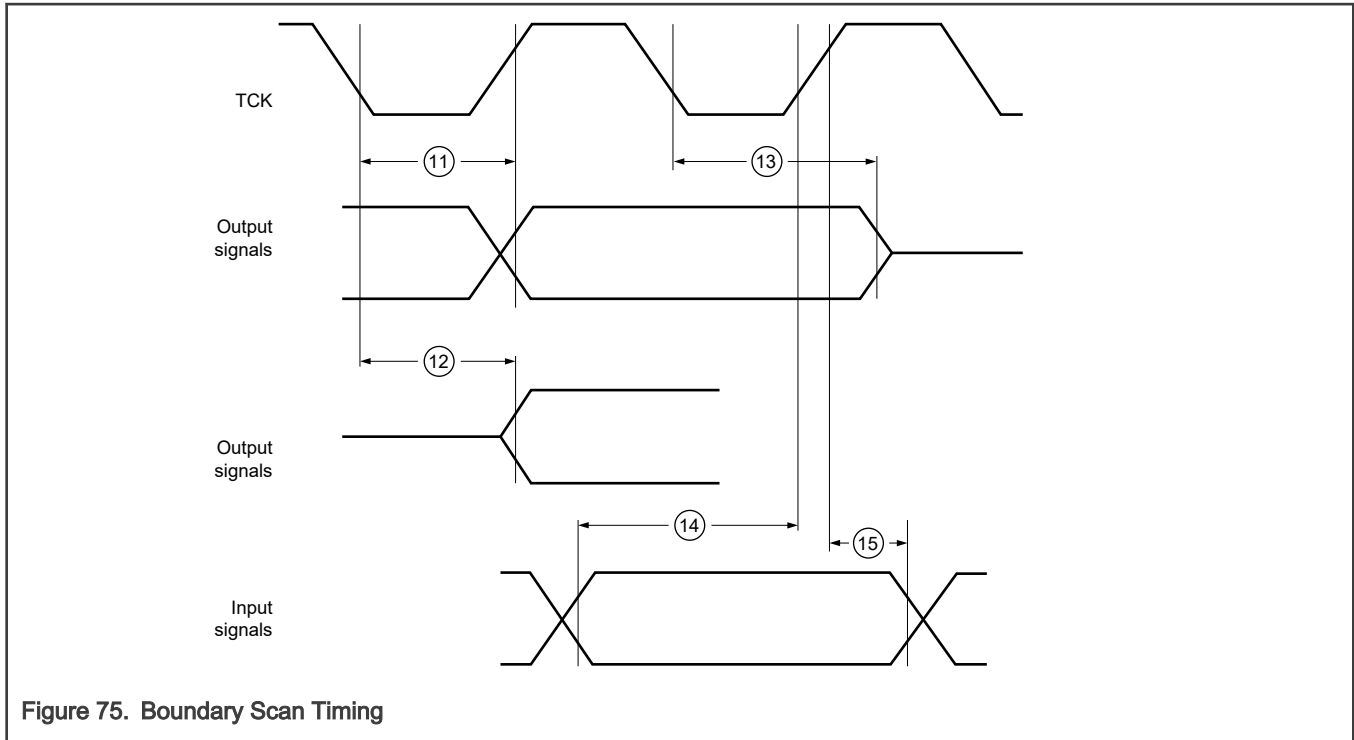


Figure 75. Boundary Scan Timing

### 16.11.2 JTAG Debug Interface Timing

The following table gives the JTAG specifications in debug interface mode.

Table 68. JTAG Debug Interface Timing

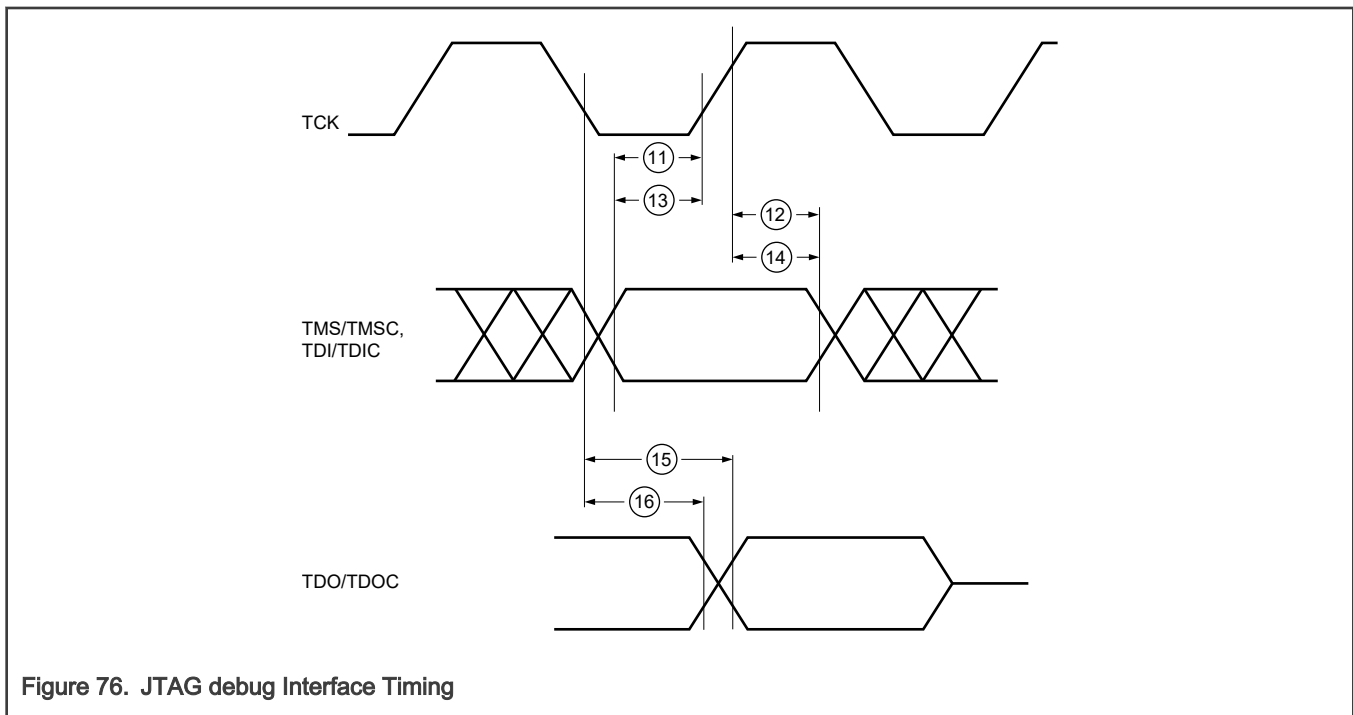
| Symbol | Description   | Min | Typ | Max | Unit | Condition | Spec Number |
|--------|---|-----|-----|-----|------|-----------|-------------|
| tTCYC  | Absolute minimum TCK cycle time (TDO sampled on posedge of TCK) <sup>1, 2</sup> | 50  | —   | —   | ns   | —         | —           |
| tTCYC  | Absolute minimum TCK cycle time (TDO sampled on negedge of TCK) <sup>1, 2</sup> | 25  | —   | —   | ns   | —         | —           |
| tJDC   | TCK clock pulse width   | 45  | —   | 55  | %    | —         | —           |
| tNTDIS | TDI data setup time <sup>3</sup>  | 5   | —   | —   | ns   | —         | 11          |
| tNTDIH | TDI data hold time <sup>3</sup>   | 5   | —   | —   | ns   | —         | 12          |
| tNTMSS | TMS data setup time   | 5   | —   | —   | ns   | —         | 13          |
| tNTMSH | TMS data hold time  | 5   | —   | —   | ns   | —         | 14          |

Table continues on the next page...

**Table 68. JTAG Debug Interface Timing (continued)**

| Symbol | Description  | Min | Typ | Max  | Unit | Condition | Spec Number |
|--------|--|-----|-----|------|------|-----------|-------------|
| tNTDOD | TDO propagation delay from falling edge of TCK <sup>4, 5</sup> | —   | —   | 17.5 | ns   | —         | 15          |
| tNTDOH | TDO hold time with respect to falling edge of TCK <sup>4</sup> | 1   | —   | —    | ns   | —         | 16          |
| tTDOHZ | TCK low to TDO high impedance <sup>4</sup>                     | —   | —   | 17.5 | ns   | —         | —           |

1. Maximum frequency for TCK is limited to 6MHz during BOOTROM startup of the device, when the system clock is the trimmed 48MHz FIRC.
2. TCK pin must have external pull down.
3. Input timing assumes an input signal slew rate of 3ns (20%/80%).
4. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.
5. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.



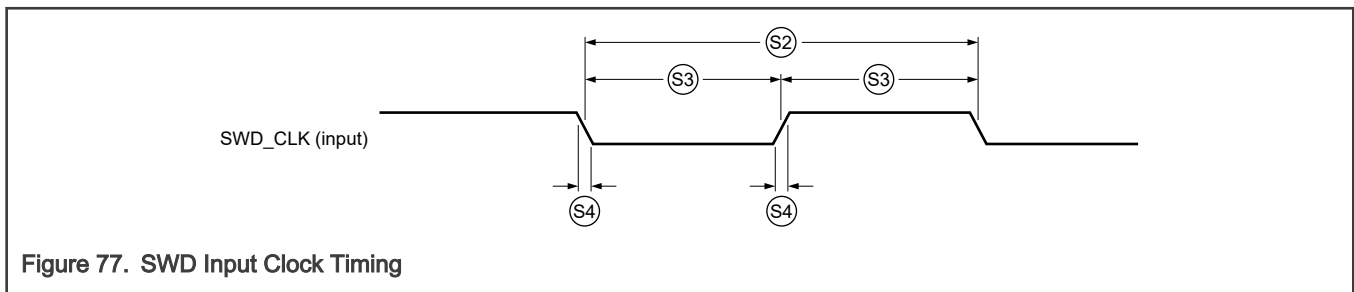
### 16.11.3 SWD electrical specifications

The following table describes the SWD electrical characteristics. Measurements are with maximum output load of 30pF, input transition of 1ns and pad configured SRE[2:0] =100.



**Table 69. SWD electrical specifications**

| Symbol | Description  | Min    | Typ | Max | Unit | Condition | Spec Number |
|--------|--|--------|-----|-----|------|-----------|-------------|
| S1     | SWD_CLK frequency                                      | —      | —   | 33  | MHz  | —         | S1          |
| S2     | SWD_CLK cycle period                                   | 1 / S1 | —   | —   | ns   | —         | S2          |
| S3     | SWD_CLK pulse width                                    | 40     | —   | 60  | %    | —         | S3          |
| S4     | SWD_CLK rise and fall times                            | —      | —   | 1   | ns   | —         | S4          |
| S9     | SWD_DIO input data setup time to SWD_CLK rise          | 5      | —   | —   | ns   | —         | S9          |
| S10    | SWD_DIO input data hold time after SWD_CLK rising edge | 5      | —   | —   | ns   | —         | S10         |
| S11    | SWD_CLK high to SWD_DIO output data valid              | —      | —   | 22  | ns   | —         | S11         |
| S12    | SWD_CLK high to SWD_DIO output data hi-Z               | —      | —   | 22  | ns   | —         | S12         |
| S13    | SWD_CLK high to SWD_DIO output data invalid            | 0      | —   | —   | ns   | —         | S13         |



**Figure 77. SWD Input Clock Timing**

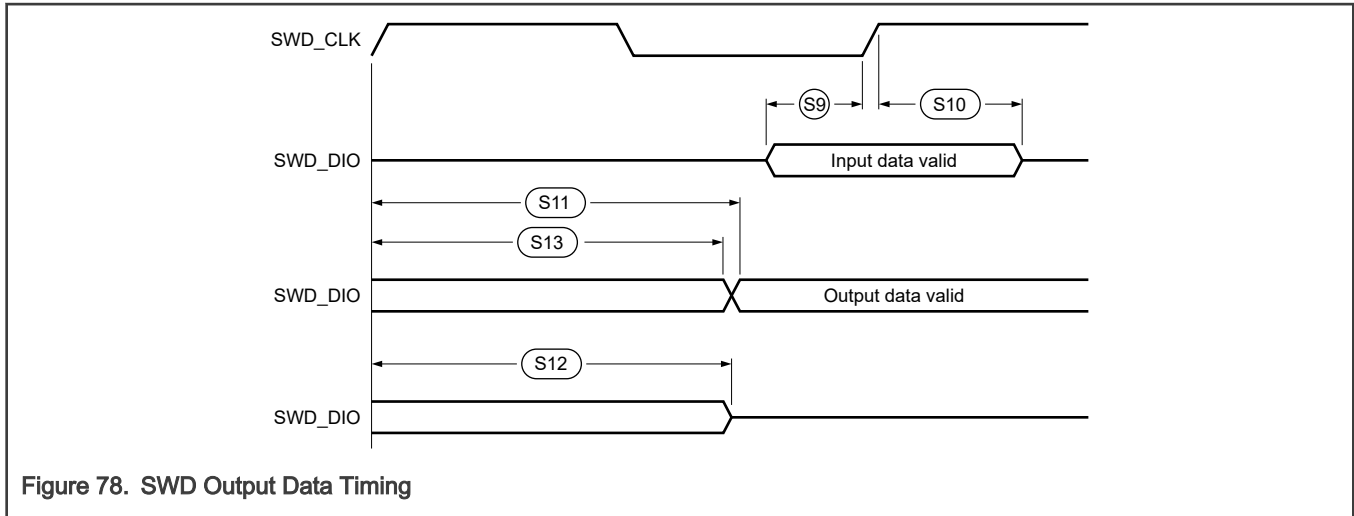


Figure 78. SWD Output Data Timing

## 17 Pinouts

For package pinouts and signal descriptions, see device Reference Manual.

## 18 Packaging

The S32G3 is offered in the following package types.

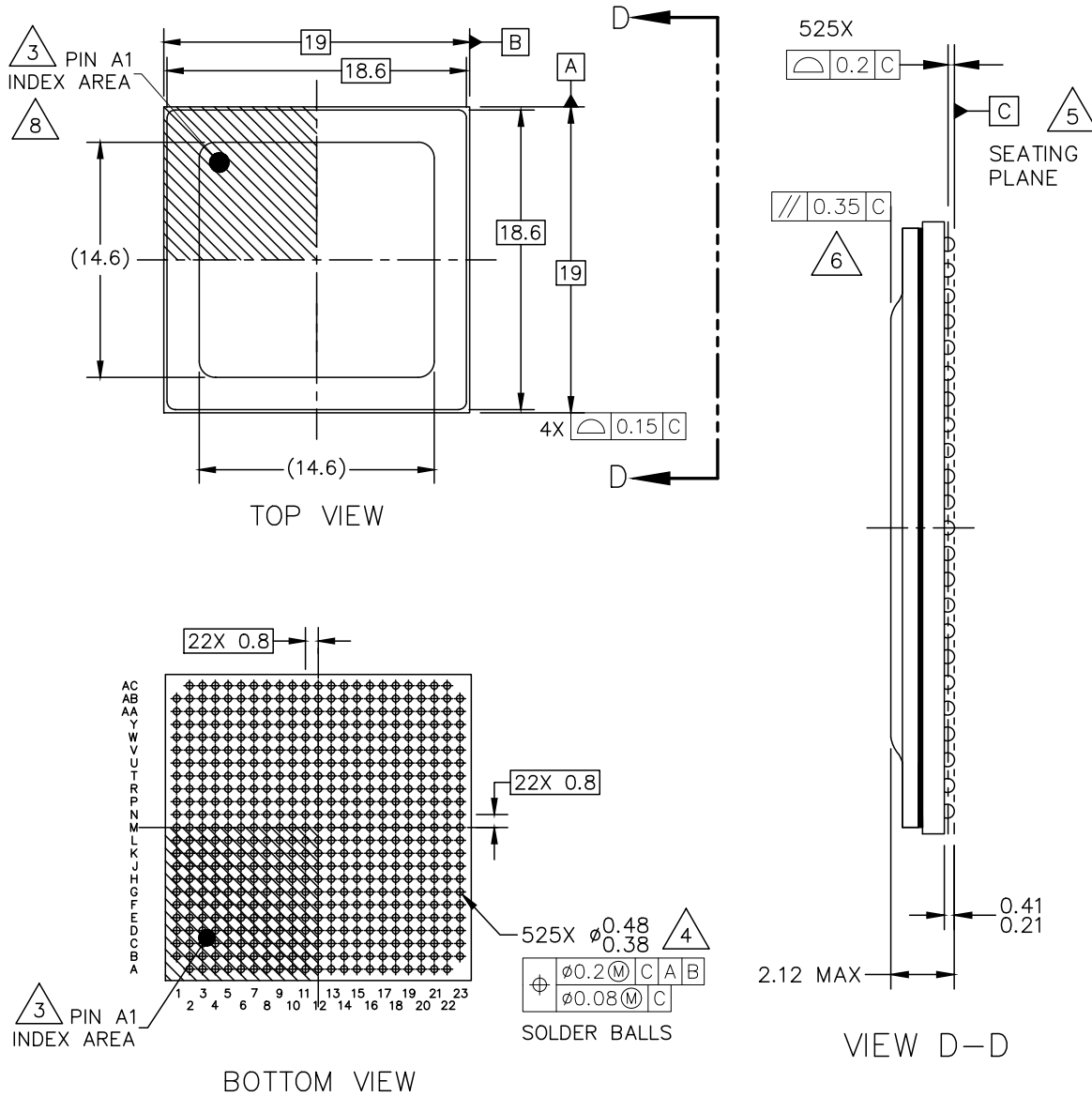
| Package type   | Document number |
|----------------|-----------------|
| 525-ball FCBGA | 98ASA01463D     |

### NOTE

To find a package drawing, go to <http://www.nxp.com> and perform a keyword search for the drawing's document number or see below figures.

H-FC-PBGA-525 I/O  
19 X 19 X 1.97 PKG, 0.8 PITCH

SOT1655-5



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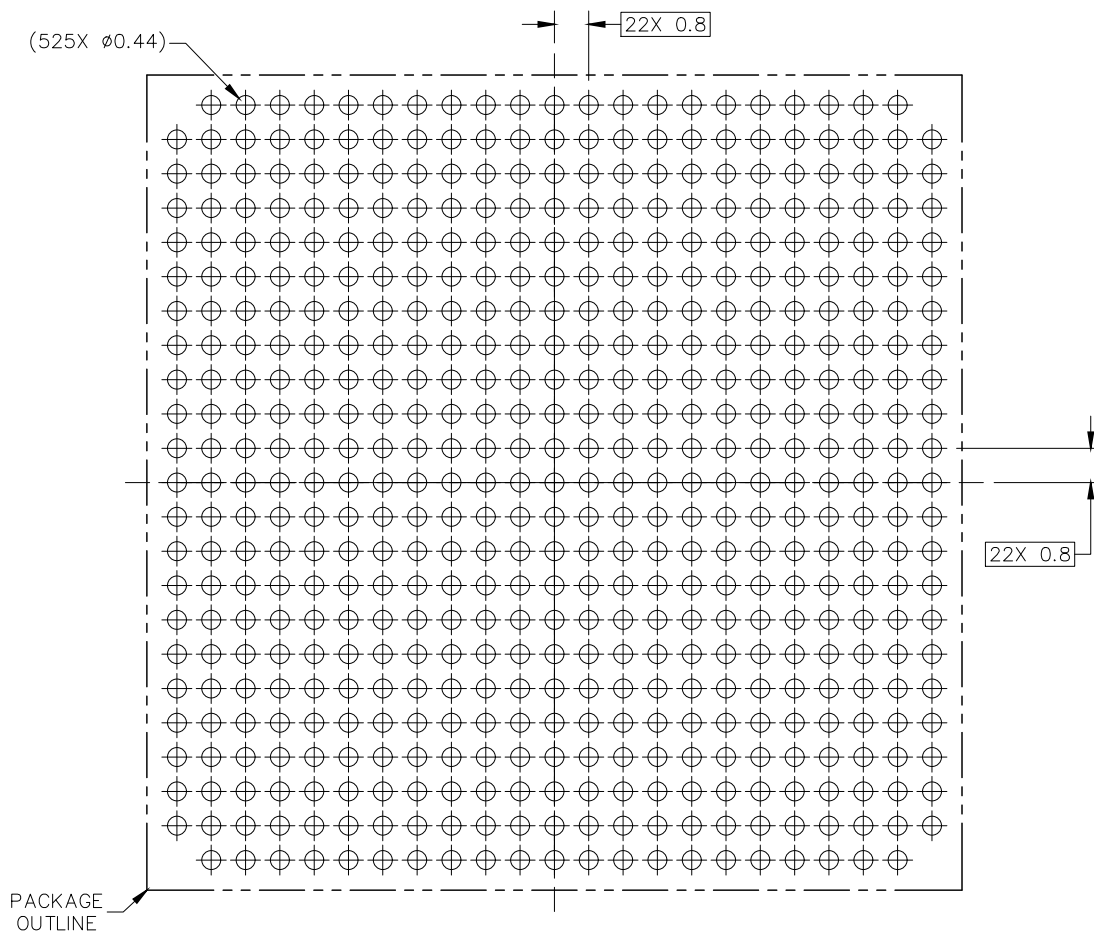
DATE: 13 SEP 2022

|  |                        |                                |                |                 |
|--|------------------------|--------------------------------|----------------|-----------------|
| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON JEDEC | DRAWING NUMBER:<br>98ASA01463D | REVISION:<br>D | PAGE:<br>1 OF 5 |
|--|------------------------|--------------------------------|----------------|-----------------|

Figure 79. Package outline

H-FC-PBGA-525 I/O  
 19 X 19 X 1.97 PKG, 0.8 PITCH

SOT1655-5



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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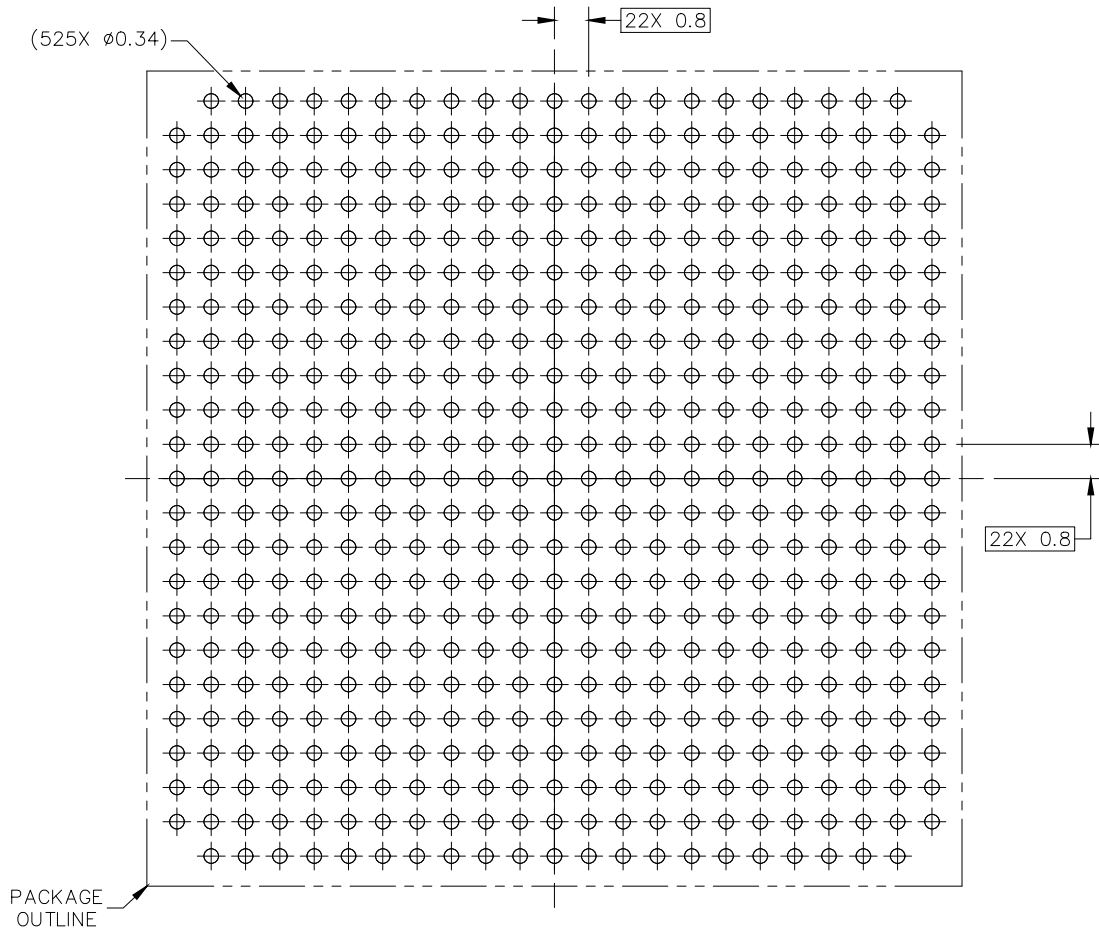
DATE: 13 SEP 2022

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|--|------------------------|--------------------------------|----------------|------------|

Figure 80. Soldering footprint part 1 of 3

H-FC-PBGA-525 I/O  
 19 X 19 X 1.97 PKG, 0.8 PITCH

SOT1655-5



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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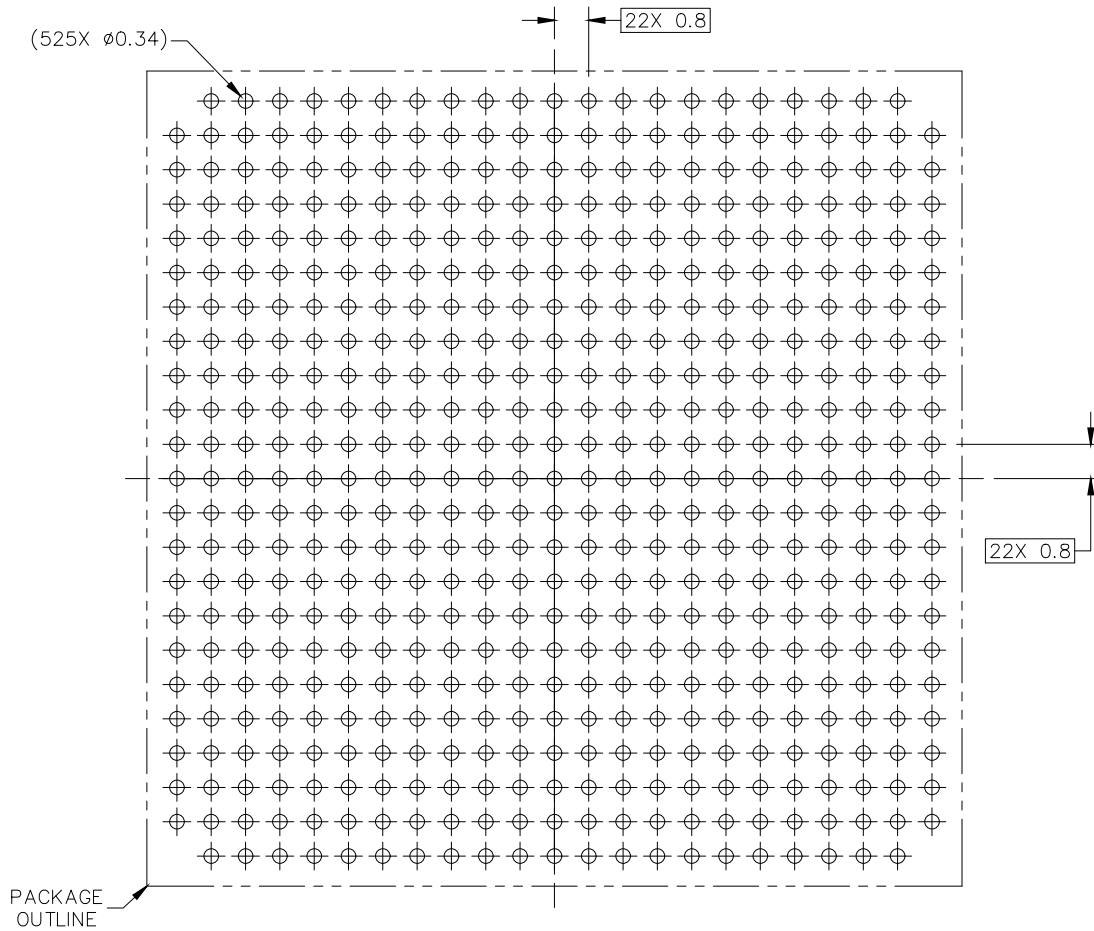
DATE: 13 SEP 2022

|  |                        |                                |                |            |
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| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON JEDEC | DRAWING NUMBER:<br>98ASA01463D | REVISION:<br>D | PAGE:<br>3 |
|--|------------------------|--------------------------------|----------------|------------|

Figure 81. Soldering footprint part 2 of 3

H-FC-PBGA-525 I/O  
 19 X 19 X 1.97 PKG, 0.8 PITCH

SOT1655-5



RECOMMENDED STENCIL THICKNESS 0.125MM

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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|  |                        |                                |                |            |
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| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON JEDEC | DRAWING NUMBER:<br>98ASA01463D | REVISION:<br>D | PAGE:<br>4 |
|--|------------------------|--------------------------------|----------------|------------|

Figure 82. Soldering footprint part 3 of 3

H-FC-PBGA-525 I/O  
 19 X 19 X 1.97 PKG, 0.8 PITCH

SOT1655-5

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
7. LID OVERHANG ON SUBSTRATE NOT ALLOWED.
8. VENT AREA BETWEEN LID AND SUBSTRATE, SIZE MAY VARY.



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|  |                        |                                |                |            |
|--|------------------------|--------------------------------|----------------|------------|
| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON JEDEC | DRAWING NUMBER:<br>98ASA01463D | REVISION:<br>D | PAGE:<br>5 |
|--|------------------------|--------------------------------|----------------|------------|

Figure 83. Package outline notes

## 19 Revision history

The following table lists the changes in this document.

| Rev 2, Feb 2023  |
|--|
| <ul style="list-style-type: none"> <li>• In section "Absolute Max Ratings", updated figure title to match with specifications "Input overshoot/undershoot voltage for each GPIO pad type".</li> <li>• In section "Operating conditions", added note to Tj and Ta as "The junction temperature (Tj) range specification...".</li> <li>• In section "Operating conditions", added figure "ADC supply sequencing".</li> <li>• In section "GPIO pads": <ul style="list-style-type: none"> <li>— for TR_TF_33 with SRE[2:0] = 100 changed min from 1.75V to 1.90V.</li> <li>— for TR_TF_33 with SRE[2:0] = 101 changed min from 0.05V to 1.00V and max changed from 8.25V to 8.50V.</li> <li>— for TR_TF_33 with SRE[2:0] = 110 changed min from 0.01V to 0.50V and max changed from 7.0V to 7.30V.</li> <li>— for TR_TF_33 with SRE[2:0] = 111 changed min from 0.005V to 0.04V and max changed from 5.5V to 6.0V.</li> </ul> </li> <li>• In section "SAR ADC", paragraph at top of table is updated to mention from "...capacitance at the input pin should..." to "...capacitance at the input pin and reference pin should...".</li> <li>• In section "Temperature Monitoring Unit (TMU)", updated TRANGE min as -45 and max as 130 and added a footnote "Accuracy outside of operating range (-40 to 125) is not guaranteed."</li> <li>• In section "FXOSC", added paragraph as "In ALC disable mode the minimum...".</li> <li>• In section "PLL", added footnote to fPLL_DDR_PHI0 as "DDR PLL allows center-spread SSCG at...".</li> <li>• In section "PLL", added footnotes to Jitter specifications to mention jitter dependency.</li> <li>• In section "FlexRay - RxD", deleted uCCLogic_1 and uCCLogic_2 specifications.</li> <li>• In section "PCIe", updated paragraph "NXP internally does PCI-SIG TX...".</li> <li>• In section "QuadSPI Octal 1.8V DDR 166MHz": <ul style="list-style-type: none"> <li>— Updated voltage measurement levels "Data transitions measured at 30%/70% supply...".</li> <li>— Updated tIH_DQS min from 2.145 ns to 2.105 ns</li> <li>— Updated tISU_DQS min from -0.496 ns to -0.616 ns</li> </ul> </li> <li>• In section "QuadSPI Octal 1.8V DDR 200MHz": <ul style="list-style-type: none"> <li>— Updated voltage measurement levels "Data transitions measured at 30%/70% supply...".</li> <li>— Updated SRE "In Single SRE configuration...".</li> <li>— Updated tOD_DATA for single and split SRE configurations.</li> <li>— Updated tIH_DQS min from 1.684 ns to 1.644 ns.</li> <li>— Updated tISU_DQS min from -0.466 ns to -0.586 ns.</li> </ul> </li> <li>• In section "QuadSPI configurations" SMPR[DLLFSMPF] is updated to 4 for 166 MHz.</li> <li>• In section "uSDHC DDR-HS400": <ul style="list-style-type: none"> <li>— Updated SRE "In Split SRE configuration SRE[2:0]=000...".</li> <li>— Updated voltage measurement levels "Data transitions measured at 35%/65% supply...".</li> </ul> </li> </ul> |

*Table continues on the next page...*



**Rev 2, Feb 2023**

- Updated tCL and tCH min to 2.35 ns.
- Updated descriptions of tOD1 and tOD2 and updated its value to 0.65 ns.
- Added tOD (uSDHC Output delay).
- Added package drawing.
- Datasheet classification updated to "Technical Data".

**Rev 2 Draft C, Sep 2022**

- In "Absolute Max Ratings"
  - Added note "All specifications associated with VIN are measured at the SoC pin."
  - Added spec Max LVDS RX or TX pin injection (IINJ\_LVDS)
  - VIN specification:
    - updated footnote "Absolute maximum DC VIN levels for a powered..."
    - Added V\_OS\_US\_10 for 1.8V and updated condition of overshoot and undershoot specifications.
    - Added footnote "DC case limit. Overshoot/Undershoot beyond this range..."
  - For Overshoot/Undershoot specs updated footnote, "For AC Signals in a 3.3V supply domain, if..."
- In section "Operating Conditions" Added footnoted to VIN\_18 and VIN\_33 "DC case limit. Overshoot/Undershoot beyond this range..."
- In section "Operating Conditions" IINJ\_D is split into powered and unpowered and related footnotes added."
- In section "Clock frequency ranges" added fSDHC\_CLK for DDR HS400.
- In section "Device Power and Operating Current Specifications", for PVDD\_STBY in condition corrected a typographic figure from VDD=0.8V, to VDD\_STBY = 0.8V.
- Added section "Power-down".
- In section "Aurora PLL" added footnote to fPLL\_CLKIN as "40MHz is the only internal input reference..".
- In section "Reset Duration" added a paragraph as "The durations specified "Reset Duration" table and the corresponding figures...." and added below three figures:
  - Reset\_b pad detailed behavior during core supply brownout
  - Reset\_b pad detailed behavior during pad HV supply brownout
  - Reset\_b pad detailed behavior during power down
- Below figure "RESET\_B pad detailed behavior", added information as "he RESET\_B pad behavior described in the diagram and the related VRSE\_RESET\_B parameter spec also apply to the case of core VDD droop after power-up."
- In section "SIRC", PTA description changed from "SIRC Post Trim Accuracy" to "SIRC trimming resolution" and "SIRC Frequency Variation" condition updated to "Frequency variation across voltage and temperature range".
- In section "I2C" PER\_CLK changed to MODULE\_CLK.
- Added section "CAN".
- In QuadSPI sections, removed DQS and added condition as "fSCK duty cycle distortion is in the range of 45%-55%."

*Table continues on the next page...*

**Rev 2 Draft C, Sep 2022**

- In uSDHC:
  - Changed title from "uSDHC DDR-52MHz" to "uSDHC SD3.0/eMMC5.1 DDR" and from "uSDHC SDR-52MHz" to "uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR" and other figure name updates.
  - In uSDHC added phrase as "All uSDHC parameters are measured at mid-supply (VDD\_IO\_SDHC/2)."
  - In "SDR-100 Mode Interface Timing" figure deleted SD5 and SD8.
  - In section "uSDHC SDR-HS200" added footnote to tODW as "Input timing also applicable for SDHC\_CMD also."
  - In "uSDHC DDR-HS400" added footnote to tRQ and tRQH as "Spec numbers SD6 and SD7 are also applicable for the CMD input timing for HS400 mode..."
  - Deleted some redundant figures.

**Rev 2 Draft B, May 2022**

- In "GMAC and PFE RGMII" section added paragraph "You must set SRE[2:0]=101 for PFE\_MAC0\_TX\_CLK in RGMII mode of PFE GMAC0 at 3.3V."

**Rev 2 Draft A, Apr 2022**

- In "Block diagram" mentioned that the diagram represents the features of S32G399A, the superset chip in the S32G3 family.
- In section "Absolute maximum ratings":
  - Changed from ADC reference supply to ADC supply for "VAD\_INPUT", min value changed from "VREFL\_ADC - 0.6" to "VSS\_ADC - 0.6" and max value changed from "VREFH\_ADC + 0.5" to "VDD\_ADC + 0.5".
  - Added more information to below footnotes attached to VIN:
    - Absolute maximum DC VIN levels for a powered device....
    - Absolute minimum DC VIN level for a powered device is....
  - Footnote attached to "IINJ\_A" changed to "Allowed for a cumulative duration of 50 hours operation over the lifetime of the device at maximum T<sub>j</sub>, with VDD\_ADC ≤ 1.92V, VSS\_ADC = 0V".
  - Added symbol names and footnote to overshoot specifications as "For AC signals, if VDD\_IO ≤ 3.3V, max VIN overshoot is limited to...."
- In section "Operating Conditions":
  - Changed from ADC reference supply to ADC supply for "VAD\_INPUT", min value updated from "VREFL\_ADC - 0.35" to "VSS\_ADC - 0.35" and max value updated from "VREFH\_ADC + 0.25" to "VDD\_ADC + 0.25".
  - Footnote attached to frequency specs updated to correct the modulation depth used in formula. Changed "...plus the modulation depth (max 1.5%) ..." to "...plus half the modulation depth..."
  - For "VDD\_EFUSE" specs, updated related footnote to add "See device hardware design guidelines document for more details."
  - Updated below footnotes attached to VIN\_18 and VIN\_33:

*Table continues on the next page...*

**Rev 2 Draft A, Apr 2022**

- From: "Additional +0.3V are supported for DC signal." to "For AC signals, allowed max  $V_{IN} \leq V_{DD\_IO^*}$  for lifetime operation. If AC....".
- From: "Absolute minimum level for  $V_{IN}$  signal is -0.3V." to "The min DC  $V_{IN}$  level for a powered device is -0.3V. If AC.....".
- Footnote attached to "VRAMP\_LV" is updated "On slow ramps, the RESET\_B pin may be observed to be asserted..."
- Total power specifications updated for S32G398A (thermal use case) changed from 8.18 to 8.35 A, S32G379A (thermal use case) changed from 7.46 to 8.08 W, S32G378A (thermal use case) changed from 7.24 to 8.02 W.
- In "Total power specifications" for 1.8V supply rail added in condition "All 1.8V supplies at 1.8V".
- Max values updated for the specs in section "Static power specifications for I/O Domains"
- In section "Device Power and Operating Current Specifications" :
  - For symbol "PVDD\_STBY", typ value changed from 48 to 58  $\mu$ W.
  - For symbol "PVDD\_IO\_STBY", typ value changed from 120 to 110  $\mu$ W.
- In section "Device Power and Operating Current Specifications" for symbol "PVDD\_IO\_PCIEn" (Powered down state), max value changed from 1.4 to 1.5 mW.
- In section "Device Power and Operating Current Specifications" for symbol "PVDD\_IO\_PCIEn" with condition "All circuits enabled,  $V_{DD\_IO\_PCIEn}=1.8V$ , Gen3 8Gbps, 2 lanes. Per IP instance", added footnote "This specification can be considered a worst case maximum..."
- In section "GPIO Pads", added symbols "VOL" and "VOH" and added a footnote attached to these symbols "For current at this voltage see IOL/IOH specs respectively".
- Removed a note "VOH/VOL values should be calculated based on the provided  $R_{DS(on)}$ , IOH/IOL values and IBIS models".
- In figure "1.8V/3.3V GPIO pad detailed behavior during power up", updated "weak pull-down" to "weak pull-down as per ILKG\_3318 specification".
- Under the figure "1.8V/3.3V GPIO pad detailed behavior during power up", removed the paragraph "The weak pull-down is 100 Kohm and is separate from the usual selectable 12Kohm internal pull resistor...."
- In section "SAR ADC" , for symbol "VAD\_INPUT" min value changed to "VSS\_ADC" and max value changed to "VDD\_ADC".
- In section "DFS", added symbol "PER\_Jitter" with min value -30ps and max value 30ps with condition  $f_{DFS\_CLKIN}=2622$  Mhz, Odd MFN.
- In section "PLL" :
  - Added symbol "fPLL\_DDR\_PHI0" with description "DDR PLL PHI0 Frequency" and min, max value 758 Mhz and condition  $DDR\_CLK$  (3032MT/s).
  - Footnote "PLL refers to the Core, Peripheral, Accelerator, and DDR reference PLLs on the device" and "Spread spectrum clock modulation is only available on the Core, Accelerator and DDR reference PLLs" moved to the top of the section.
  - The formula for calculating the max frequency is updated in the related footnote "The max frequency in case of center-spread SSCG enabled for a modulation....".
- In PCIe specifications external reference clock pins related specs are added.

*Table continues on the next page...*

**Rev 2 Draft A, Apr 2022**

- In section "GMAC and PFE SGMII", For symbol UI the description updated to "Unit interval (mean)".
- Added sentence "All transitions measured at mid-supply (VDD\_IO\_QSPI/2)" and removed "Clock measurements done with respect to VDD\_IO\_QSPI/2 level" in all QuadSPI modes.
- Removed symbol "tDVW" from the following sections:
  - "QuadSPI Quad 1.8V SDR 133MHz"
  - "QuadSPI Octal 1.8V DDR 100MHz"
  - "QuadSPI Octal 1.8V DDR 133MHz"
  - "QuadSPI Octal 1.8V DDR 166MHz"
  - "QuadSPI Octal 1.8V DDR 200MHz"
  - "QuadSPI Octal 1.8V SDR 100MHz"
  - "QuadSPI Octal 1.8V SDR 133MHz"
  - "QuadSPI Quad 3.3V SDR 104MHz"
- Added introduction sentence "The information in this section applies to Octal- and Hyperflash" in following sections :
  - QuadSPI Octal 1.8V DDR 100MHz
  - QuadSPI Octal 1.8V DDR 133MHz
  - QuadSPI Octal 1.8V DDR 166MHz
- In section "QuadSPI configurations", added introduction "The below table shows a subset of the QuadSPI module configurations for different speeds and data rate....".
- In section "QuadSPI configurations", updated SMPR[DLLFSMPF] setting for DDR-200MHz from 4 to 3.
- In section "DDR", updated the sentence to "LPDDR4 SDRAM compliant to JEDEC209-4B LPDDR4 JEDEC standard release."
- In section "DDR Common DC Output", for symbol "ROnPu" and "ROnPd", in description CLK changed to CKE outputs and footnote attached to them updated as "For the DDR0\_RESET\_B pin and CKE pin...."
- Added section "DDR3L DC Input Timing".
- Section name changed from "LPDDR4 DC Input" to "LPDDR4 DC Input Timing" and from "LPDDR4 Output" to "LPDDR4 Output Timing".
- Section "uSDHC DDR-HS400" updated thoroughly.
- Updated "Legal information"

**Rev 1, Nov 2021**

- Updated datasheet classification to "Advance information"
- Updated Introduction, Feature comparison.
- In section "Absolute Max Ratings" and "Operating conditions", VDD\_LV\_PLL is deleted as it is shorted with VDD inside the die and this supply no longer needs to be driven from outside.
- In section "Absolute Max Ratings", for Symbol "VAD\_INPUT" Min changed from "-0.3" to "VREFL\_ADC -0.6".

*Table continues on the next page...*

**Rev 1, Nov 2021**

- In section "Absolute Max Ratings", for Symbol "VAD\_INPUT" Max changed from "VREFH\_ADC" to "VREFH\_ADC + 0.5".
- In section "Absolute Max Ratings", for Symbol "VAD\_INPUT" footnote added "Allowed for a cumulative duration of 50 ...".
- In section "Absolute Max Ratings" two footnotes attached to VIN are updated:
  - Absolute maximum VIN levels ...
  - Absolute minimum VIN level for ...
- In section "Absolute Max Ratings", for Symbol "IINJ\_A" Min changed from "-2" to "-1".
- In section "Absolute Max Ratings", for Symbol "IINJ\_A" Max changed from "2" to "1".
- In section "Absolute Max Ratings" in a footnote attached to IINJ\_A "Non-disturb of ADC channels during current ...."
- In section "Operating Conditions", added note " $\Delta$ VDD\* specifications are applicable to the supplies mentioned ...".
- In section "Operating Conditions", for Symbol "fSYS\_A53" Max changed from "1100" to "1311".
- In section "Operating Conditions", SVS feature is removed.
- In section "operating conditions" removed " $\Delta$ VDD\_IO\_DDR" differential as this has a lone supply in its condition.
- In section "Operating Conditions", Symbol "VRAMP\_HV" is seperated for 1.8V and 3.3V IOs and 3.3V IOs limit is updated to 50V/ms.
- In section "Operating Conditions", for Symbol "VAD\_INPUT" Min changed from "VREFL\_ADC" to "VREFL\_ADC - 0.35".
- In section "Operating Conditions", for Symbol "VAD\_INPUT" Max changed from "VREFH\_ADC" to "VREFH\_ADC + 0.25".
- In section "Operating Conditions", for Symbol "IINJ\_A" Min changed from "-1 mA" to "-20 uA".
- In section "Operating Conditions", for Symbol "IINJ\_A" Max changed from "1 mA" to "20 uA".
- In section "Operating Conditions", for Symbol "IINJ\_A" footnote updated "The SAR ADC electrical specifications ar...".
- In section "Operating conditions" for symbol " $\Delta$ VDD\_HV\_18\_ANA" added footnotes to clarify VDD\_EFUSE supply conditions and added another footnote to say "VREFH\_ADCn has a differential voltage of +/-100mV".
- In section "Operating Conditions", for "LPDDR4 I/O voltage supply" typ value added as 1.1V.
- In section "Operating Conditions", footnote attached to IINJ\_D is updated "IINJ\_D specifications are per pin for an unpowered..." and removed one "GPIO electrical specifications and ...".
- In section "Operating Conditions", added paragraph "The device hardware design guide summarizes ...".
- In section "Clock frequency ranges", removed some non applicable clocks.
- In section "Clock frequency ranges", for Symbol fA53\_CORE\_DIV2\_CLK is updated to 655.5 MHz.
- In section "Clock frequency ranges", for Symbol fA53\_CORE\_DIV10\_CLK is updated to 131.1 MHz.
- In section "Clock frequency ranges", for Symbol fXBAR\_2X\_CLK min added as 48 MHz.
- In section "Clock frequency ranges", for Symbol fPFE\_MAC\_2\_TX\_CLK and fPFE\_MAC\_2\_RX\_CLK max updated to 312.5 MHz.
- In section "Clock frequency ranges", for Symbol fSDHC\_CLK min updated to 133 MHz.
- In section "Thermal Characteristics", added values.
- In section "Total power specifications for 0.8V and 1.8V Analog Domains", added 0.8V values.

*Table continues on the next page...*

**Rev 1, Nov 2021**

- In section "power sequencing" updated steps 3 and 4 and added note "For step 4, it is acceptable for the 1.8V ..."
- In section "Power sequencing", added a figure "1.8V supply timing with respect to PMIC\_VDD\_OK during Standby Mode Exit".
- In section "Aurora Pads", Symbol "VCM\_LVDS\_RX" and "VDIFF\_LVDS\_RX" is added.
- In section "PMC Bandgap", values added.
- In section "SAR ADC", added footnote to VAD\_INPUT "The reduced limits for VAD\_INPUT ....".
- In section "DFS", Symbol "fDFS\_CORE\_CLK2" and "fDFS\_PER\_CLK5" are removed.
- In section "DFS", formula is moved from footnote to sentence with some clarifications.
- In section "DFS", for Symbol "fDFS\_PER\_CLK2" max updated to 628 MHz and fDFS\_CLKIN max updated to 2622 MHz.
- In section "FXOSC", added specs "VIH\_EXTAL", "VIL\_EXTAL", "CLOAD", "VCM\_SE"
- In section "FXOSC", removed differential bypass mode specs which includes fBYP\_DIFF and related figure.
- In section "PLL", removed  $\Delta f_{PLL\_MOD}$  spec and all specs "with center-spread enabled" in condition column. Added a footnote to specs which have "without center-spread enabled" in the condition column as "The max frequency in case of center-spread SSCG...".
- In section "PLL" added footnote to fPLL\_CORE\_VCO, fPLL\_ACCEL\_VCO and fPLL\_DDR\_VCO as "Same min frequency value applies for center-spread...".
- In section "PLL", for Symbol "fPLL\_CORE\_VCO" with condition "without center-spread SSCG enabled" Max changed from "2600" to "2622".
- In section "PLL", for Symbol "fPLL\_PER\_PHI5" with condition "PERIPH\_PLL\_PHI5" Max changed from "500" to "125".
- In section "PLL", for Symbol "fPLL\_ACCEL\_VCO" with condition "without center-spread SSCG enabled" Max changed from "2436" to "2400".
- In section "PLL", for Symbol "fPLL\_CORE\_PHI0" max updated to 1311 MHz.
- In section "SPI", for Symbol "tSUI" with condition "Master, MTFE=1, CPHA=0, SMPL\_PTR = 1" footnote value added "N is number of protocol clock cycles whe...".
- In section "FlexRay - TxD", a missing spec is added "dCCTxD10".
- In all QuadSPI modes, moved footnote "Clock measurements done with respect to VDD\_IO\_QSPI/2 level." to top of the table
- In section "QuadSPI Quad 1.8V DDR 66MHz", Symbol "tISU\_SCK" and "tIH\_SCK" are deleted.
- In section "QuadSPI Quad 1.8V DDR 66MHz" added tLSKEW.
- In section "QuadSPI Octal 1.8V DDR 100MHz", Symbol "tCK2CKmin", "tCK2CKmax", "tIH\_PCS" and "tISU\_PCS" are deleted.
- In section "QuadSPI Octal 1.8V DDR 133MHz", Symbol "tCK2CKmin" and "tCK2CKmax" are deleted.
- In section "QuadSPI Quad 3.3V DDR 66MHz", Symbol "tISU\_SCK" and "tIH\_SCK" are deleted.
- In section "QuadSPI Quad 3.3V DDR 66MHz", Symbol "tLSKEW" is added.
- In section "QuadSPI Octal 1.8V DDR 166MHz/200MHz", updated SRE.
- In all QuadSPI sections updated TCSS and TCSH value is updated to 3.
- Section "QuadSPI interfaces" and "QuadSPI configurations" are updated.

*Table continues on the next page...*

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|---|
| <b>Rev 1, Nov 2021</b>  |
| <ul style="list-style-type: none"><li>• In section DDR, added paragraph "DDR operation with the standards stated..." and "LPDDR4 routing constraints are documented ..."</li><li>• In section "uSDHC DDR-HS400" added min value to 133 MHz.</li><li>• In section "JTAG Boundary Scan", updated "The SRE[2:0]=100 or SRE[2:0]=101 is required drive setting to meet the timing."</li><li>• In section "SWD electrical specifications", SRE updated to SRE[2:0]=100.</li><li>• Added section "Packaging".</li><li>• Updated "Security" and "Suitability for use" disclaimers.</li></ul> |
| <b>Rev 1 Draft E, July 2021</b>   |
| <ul style="list-style-type: none"><li>• Subsequent updates throughout the data sheet.</li></ul>   |
| <b>Rev 1 Draft D, Apr 2021</b>  |
| <ul style="list-style-type: none"><li>• Subsequent updates throughout the data sheet.</li></ul>   |
| <b>Rev 1 Draft C, Jan 2021</b>  |
| <ul style="list-style-type: none"><li>• Subsequent updates throughout the data sheet.</li></ul>   |
| <b>Rev 1 Draft B, Apr 2020</b>  |
| <ul style="list-style-type: none"><li>• Subsequent updates throughout the data sheet.</li></ul>   |
| <b>Rev 1 Draft A, Feb 2020</b>  |
| <ul style="list-style-type: none"><li>• Initial release.</li></ul>  |

## Legal information

### Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
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