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i.MX 7ULP Applications Processor Silicon Revision B1 to B2 Comparison

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Contents

1 Introduction

This document provides information on changes in the i.MX 7ULP Applications Processor between silicon revisions B1 and B2.

2 Hardware and software compatibility between silicon revisions B1 and B2

2.1 Hardware board-level compatibility

No board-level changes are required to use silicon revision B2 in systems designed for silicon revision B1.

2.2 Software compatibility

Software designed for silicon revision B1 will run on silicon revision B2 without modification.

3 Changes between silicon revisions B1 and B2

3.1 Updated part number

The orderable part numbers are changed from MCIMX7Uxxxxxxx**C** (silicon revision B1) to MCIMX7Uxxxxxxx**D** (silicon revision B2).

3.2 Updated part revision number in the JTAG ID and SIM ID

The device identification register (JTAG ID) allows the revision number and part number to be read through the JTAG Test Access Port (TAP). See the device identification register section of the i.MX 7ULP Applications Processor Reference Manual for details. This table shows the Part Identification Number (PIN) and the Part Revision Number (PRN) for each i.MX 7ULP silicon revision.

The contents of the JTAD ID register are also mirrored in a SIM register called JTAG_ID_REG (address 0x410A_308C).

Table 1. JTAG device identification register information

Silicon Revision	Part Identification Number (PIN)	Part Revision Number (PRN)
B1	10'b0011100001	4’b00**10**
B2	10'b0011100001	4’b00**11**

3.3 [Fuses] DIR_BT_DIS fuse moved to a non-ECC fuse bank

On silicon revision B1, the DIR_BT_DIS fuse was located in an fuse word where ECC is supported. If ECC is supported, the fuse word can only be programmed once. Programming DIR_BT_DIS in the factory would have prevented customers from being able to program other fuses in the same fuse word.

The DIR_BT_DIS fuse has been moved to a non-ECC fuse word to avoid this conflict.

- DIR_BT_DIS fuse location on silicon revision B1: Bank 2, Word 7, Bit 13
- DIR_BT_DIS fuse location on silicon revision B2: Bank 1, Word 7, Bit 8

On silicon revision B2, DIR_BT_DIS will be programmed in the factory. The previous fuse location is now reserved.

3.4 [Fuses] Added fuses to support the PMC temperature sensor

The PMC Temperature Sensor is used to measure die temperature with high accuracy. This is controlled by the software application which must implement the specific procedure described in the reference manual. This procedure relies on a calibration constant (TSENS_TCAL) that is programmed by NXP.

On silicon revision B2, fuses were allocated for this calibration constant. The fuses are called TSENS_TCAL and are located fuse Bank3, Word 5, Bits [7:0].

The TSENS_TCAL value can be read by software at address 410A_65D0[7:0].

For details on using this function, see chapter Power Management Controller (PMC), section " Using the PMC temperature sensor" in the i.MX 7ULP Reference Manual (IMX7ULPRM).

3.5 [Fuses] OTFAD CRC calculation enabled via fuse

On silicon revision B1, OTFAD CRC calculation was enabled by default after reset.

On silicon revision B2, OTFAD CRC calculation is disabled by default at reset and can be enabled using the KEY_BLOB_EN fuse at Bank 29, Word 4, fuse address 0x12C0[5].

3.6 Increased PLLs lock time default lock time

The reset value for the SCG_xPLLLOCK_CNFG registers and the APLLLOCK_CNFG register have been increased to provide longer PLL lock time.

As noted in the i.MX 7ULP Reference Manual, the PLL lock time should be configured for 150 µs or greater.

On silicon revision B2, the reset value of SCG_xPLLLOCK_CNFG was changed from 16'h0468 to 16'h1468.

On silicon revision B2, the reset value of APLLLOCK_CNFG was changed from 16'h0468 to 16'h1468.

3.7 [Power] DDR interface internal pull-ups/pull-downs disabled during VLLS mode

In CA7 VLLS mode, the pull-ups and pull-downs on the DDR interface should be automatically disabled to conserve power. On silicon revision B1, an issue was discovered in which the pull-ups could become enabled randomly as either a pull-up or pull-down during CA7 VLLS mode. This can cause additional power consumption.

Silicon revision B2 corrected this issue.

3.8 [Power] DDR interface input buffers disabled during VLLS mode

In CA7 VLLS mode, the input buffers on the DDR interface should be automatically disabled to conserve power. On silicon revision B1, an issue was discovered in which the input buffers could become enabled randomly during CA7 VLLS mode. This can cause additional power consumption.

Silicon revision B2 corrected this issue.

3.9 [Interrupts] CA7 PMU interrupt assigned

On silicon revision B1, the CA7 Performance Monitoring Unit (PMU) interrupt is not connected, so the PMU functions that are driven by the hardware event cannot be enabled during performance profiling.

Silicon revision B2 corrected this issue by adding an OR gate between PMU interrupt output and A7 CTI interrupt at vector position 17.

3.10 [Interrupts] NMI_b not serviced by CM4 core when used as wake event from VLLS mode

This issue was previously documented as errata number ERR011424.

Silicon revision B2 corrected the issue.

3.11 [Boot] Corrected CA7 boot failure causing CM4 boot to fail also

On silicon revision B1, in dual boot mode with HAB enabled, if the CA7 fails to boot, SNVS is moved to the fail state. This also causes the CM4 boot to fail. The desired behavior is the CM4 should not fail to boot just because the CA7 boot failed. The expected CA7 boot flow of moving to USB serial download mode is also prevented.

On silicon revision B2, these issues have been fixed .

3.12 [Security] WDOG2 timeout event on HAB parts

On silicon revision B1, the WDOG2 is enabled by default from reset and can trigger a non-fatal security violation in SNVS causing the Serial Download boot flow to fail in HAB closed devices .

On silicon revision B2, the WDOG2 is disabled at reset enabling users to use serial download boot mode in HAB closed devices .

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