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Engineering Bulletin

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In-Circuit Programming of FLASH Memory Using the Monitor Mode for the MC68HC908GR8

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Introduction

This engineering bulletin describes how to perform in-circuit programming (ICP) of the FLASH memory using monitor mode.

Two methods are discussed here:

- Using the M68ICS08GR in-circuit simulator (ICS) with P&E Microsystems software
- Using P&E Microsystems software with an external communications circuit

ICP is a process where user code is programmed into the device's FLASH memory after the part has been assembled into the application. ICP also allows the original users code to be erased and re-programmed. This method can be used in development, production/manufacturing and in a field environment.

Using Monitor Mode for FLASH Programming

Motorola's current solution for ICP is the In-Circuit Simulators and P&E's software.

The software and ICSs allow programming of the parts on the simulator or in the target circuit via a MON08 ribbon cable. The software also allows programming of the part without the ICS, with an external communications circuit.

All of the programming described in this engineering bulletin is accomplished by placing the part into monitor mode. In this mode, erasing and programming are done through a single-wire interface with the host computer.

The two ways to enter monitor mode are:

- The ICS provides the entry requirements to enter standard monitor mode. These entry requirements must be implemented on the target board if the ICS is not used.
- A second way to enter monitor mode, that does not require a high voltage on the $\overline{\text{IRQ}}$ pin, is called forced monitor mode. This mode does not need to meet all the monitor mode entry conditions of the standard monitor mode, but it does require the part to be blank (erased).

This engineering bulletin describes how to connect the part, communicate at different baud rates, place it into monitor mode, pass security, and erase and program the part. If the security code is not known, the contents of the FLASH can't be read, but the FLASH can be erased and reprogrammed.

Information on the M68ICS08GP can be found at:
http://www.motorola.com/mcu/
P&E Microsystems software can be downloaded free from that company's Web site.

NOTE: *All of the oscillators used in this application note were the 4 pin "powered" or "canned" type oscillators. Discussing all the different vendors of crystals, ceramic oscillators, other required external components, and component layout variables would be too extensive.*

ICP Using M68ICS08GR8's MON08 Interface

Use this procedure for performing ICP using the ICS's MON08 cable to the target application.

1. Materials required:
   a. PC with P&E software installed (version 1.25 or higher)
   b. M68ICS08GR simulator
   c. Adapter/connector to connect the female end of the MON08 cable to the part on the target application
   d. Pin assignment diagram (see **Figure 1** and **Figure 2**)
   e. Monitor mode entry requirements (see **Table 1**)
   f. Crystal oscillator on the target, or from an external clock source, with a value from **Table 2**
   g. Target board must have the ability to perform a power-on reset (POR) not just a reset (required to enter monitor mode).
2. Connections (see **Figure 3**):
   a. 9-pin serial cable from PC to the ICS
   b. 5 volts to the ICS
   c. MON08 cable from J4 of the ICS to the target board with these connections:
      — MON08 GND to the V_{SS} pin on the part
      — MON08 RST to the $\overline{RST}$ pin on the part
      — MON08 IRQ to the $\overline{IRQ}$ pin on the part
      — MON08 PTA0 to the PTA0 pin on the part
      — MON08 PTA1 to the PTA1 pin on the part
      — MON08 PTB0 to the PTB0 pin on the part
      — MON08 PTB1 to the PTB1 pin on the part
   d. ICS jumpers in these positions:
      — W4 and W10 to V_{TST}
      — W3 to normal
      — W6 to 5 V
   e. It is assumed that all V_{DD} and V_{SS} pins on the part are already connected.

3. Operation — Standard monitor mode entry:
   a. Launch P&E's WINIDE in the ICS08GRZ software.
   b. Open desired file. (Demo file can be used.)
   c. Assemble/Compile the file (see **Figure 7**).
   d. Turn on power to the ICS.
   e. Turn on power to the target.
   f. Launch the programmer.
   g. From "Target Hardware Type," select "Class II" (see **Figure 8**).
   h. From "PC Serial Port Configuration," select the PC port you are using and the appropriate baud rate (see **Table 2**).
   i. From "Target MCU Security Bytes" select appropriate security code (blank part = FF).
   j. Select "Contact Target with these Settings…"
   k. Follow the instructions in the "Power down/up Dialog" windows.
   l. Select appropriate algorithm for the part.
   m. Double click on "Erase Module" – EM (see **Figure 9**)
   n. Double click on "Program Module" – PM
   o. Record security bytes. This information can be seen by quitting and then re-entering the programmer. The S19 record will have the same security bytes as the part just programmed as long as it is not changed. The security bytes consist of the information stored in the interrupt vectors, $FFF6–$FFFD.
4. Operation — Forced monitor mode entry:
   a. Blank part with oscillator value from **Table 2**:
      — Move jumper W4 and W10 to Vdd_MCU.
      — PTB0 and PTB1 connections are not required.
   b. Blank part with 32.768-kHz oscillator, 9600 baud:
      — Move jumper W3 to the "Forced 0" position.

ICP Using the External Communications Circuit (No ICS)

Use this procedure for performing ICP via an external communications circuit in place of this ICS to the target application.

1. Materials required:
   a. PC with P&E software installed (version 1.25 or higher).
   b. Adapter/connector to connect the male end of the 9 pin serial cable to the part on the target application.
   c. RS-232 communications circuit. Also needed is a 5-volt power source to power this circuit. (see **Figure 4**, **Figure 5**, and **Figure 6**)
   d. Pin assignment diagram (see **Figure 1** and **Figure 2**)
   e. Monitor mode entry requirements (see **Table 1**)
   f. Crystal oscillator on the target, or from an external clock source, with a value from **Table 2**
   g. Target board must have the ability to perform a POR not just a reset (required to enter monitor mode).
2. Connections (see **Figure 4**):
   a. 9-pin serial cable from PC to the communications circuit
   b. V+ pin of the RS-232 part to the $\overline{\text{IRQ}}$ pin of the part
   c. Communications pin of HC125 to PTA0 of the part.
   d. Target pin requirements:
      — PTA1 of part to V_{SS}
      — PTB0 of the part to V_{DD} via pullup resistor
      — PTB1 of the part to V_{SS}
      — $\overline{\text{RESET}}$ has an internal pullup resistor.
   e. It is assumed that all V_{DD} and V_{SS} pins on the part are already connected.
3. Operation — Standard monitor mode entry:
   a. Launch P&E's WINIDE in the ICS08GR software.
   b. Open desired file. (Demo file can be used.)
   c. Assemble/Compile the file (see **Figure 7**).

d. Apply power to the Communications Circuit.

e. Turn on power to the target.

f. Launch the programmer.

g. From “Target Hardware Type” select “Class III” (see **Figure 8**).

h. From “PC Serial Port Configuration,” select the PC port you are using and the appropriate baud rate (see **Table 2**).

i. From “Target MCU Security Bytes,” select appropriate security code (blank part = FF).

j. Select “Contact Target with these Settings…”

k. Follow the instructions in the “Power Cycle Dialog” window.

l. Select appropriate algorithm for the part.

m. Double click on “Erase Module” – EM (see **Figure 9**).

n. Double click on “Program Module” – PM.

o. Record security bytes. This information can be seen by quitting and then re-entering the programmer. The S19 record will have the same security bytes as the part just programmed as long as it is not changed. The security bytes consist of the information stored in the interrupt vectors, $FFF6–$FFFD.

4. Operation — Forced monitor mode entry:

   a. Blank part with oscillator value from **Table 2**. See **Figure 5**.

      — Remove connection to $\overline{\text{IRQ}}$ pin of the part.

      — $\overline{\text{IRQ}}$ has internal pullup resistor.

      — PTB0 and PTB1 connections are not required.

      — If the crystal oscillator in the target is not a value listed in **Table 2**, it is possible to "overdrive" the target crystal, with an external clock, for the short duration of the programming sequence. An example would be overdriving a target’s 32.768-kHz crystal with a 9.8304-MHz external clock.

   b. Blank part with 32.768-kHz oscillator. See **Figure 6**.

      — Connect $\overline{\text{IRQ}}$ pin to V_{SS}.

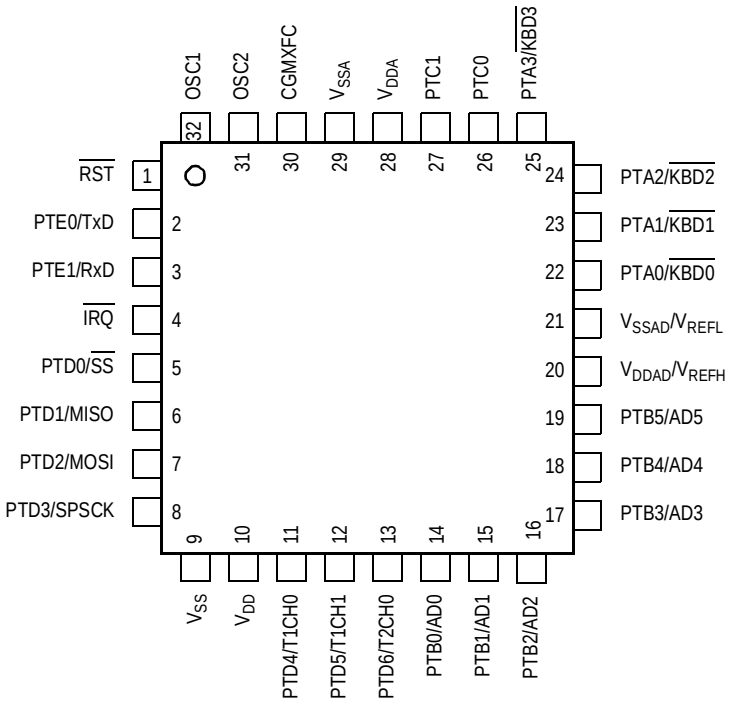
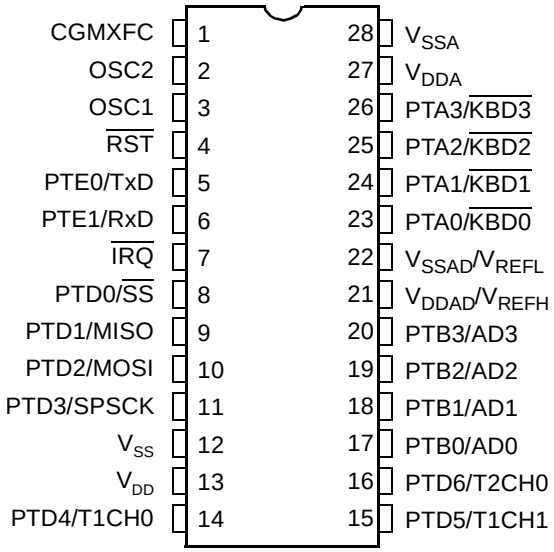


Figure 1. QFP Pin Assignment



NOTE: Ports PTB4, PTB5, PTC0, and PTC1 are available only with the QFP.

Figure 2. 28-Pin Pin Assignments

Table 1. Monitor Mode Signal Requirements and Options

$\overline{IRQ}$	RESET	$FFFE/ $FFFF	PLL	PTB0	PTB1	External Clock(1)	CGMOUT	Bus Frequency	COP	For Serial Communication			Comment
										PTA0	PTA1	Baud Rate(2) (3)	
X	GND	X	X	X	X	X	0	0	Disabled	X	X	0	No operation until reset goes high
V_{TST}	V_{DD} or V_{TST}	X	OFF	1	0	9.8304 MHz	4.9152 MHz	2.4576 MHz	Disabled	1	0	9600	PTB0 and PTB1 voltages only required if $\overline{IRQ}$ = V_{TST}
										X	1	DNA	
V_{DD}	V_{DD}	$FFFF	OFF	X	X	9.8304 MHz	4.9152 MHz	2.4576 MHz	Disabled	1	0	9600	External frequency always divided by 4
										X	1	DNA	
GND	V_{DD}	$FFFF	ON	X	X	32.768 kHz	4.9152 MHz	2.4576 MHz	Disabled	1	0	9600	PLL enabled (BCS set) in monitor code
										X	1	DNA	
V_{DD} or GND	V_{TST}	$FFFF	OFF	X	X	X	—	—	Enabled	X	X	—	Enters user mode — will encounter an illegal address reset
V_{DD} or GND	V_{DD} or V_{TST}	Non-blank	OFF	X	X	X	—	—	Enabled	X	X	—	Enters user mode

1. External clock is derived by a 32.768-kHz crystal or a 9.8304-MHz off-chip oscillator.
2. PTA0 = 1 if serial communication; PTA0 = X if parallel communication
3. PTA1 = 0 Æ serial, PTA1 = 1 Æ parallel communication for security code entry
4. DNA = does not apply, X = don't care

Table 2. Crystal Frequency vs. Baud Rate

Crystal Frequency (MHz)	Internal Bus Frequency (MHz)	Baud Rate
4.9152	1.2288	4800
9.8304	2.4576	9600
14.7456	3.6864	14,400
19.6608	4.9152	19,200
29.4912	7.3728	28,800

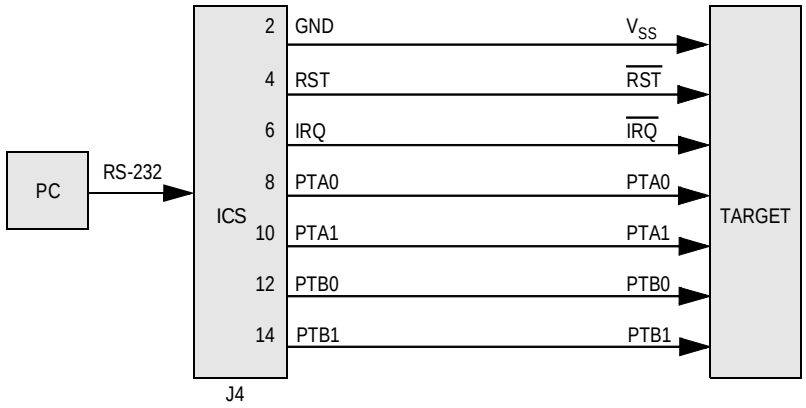


Figure 3. MC68HC908GR8 MON08 Connections

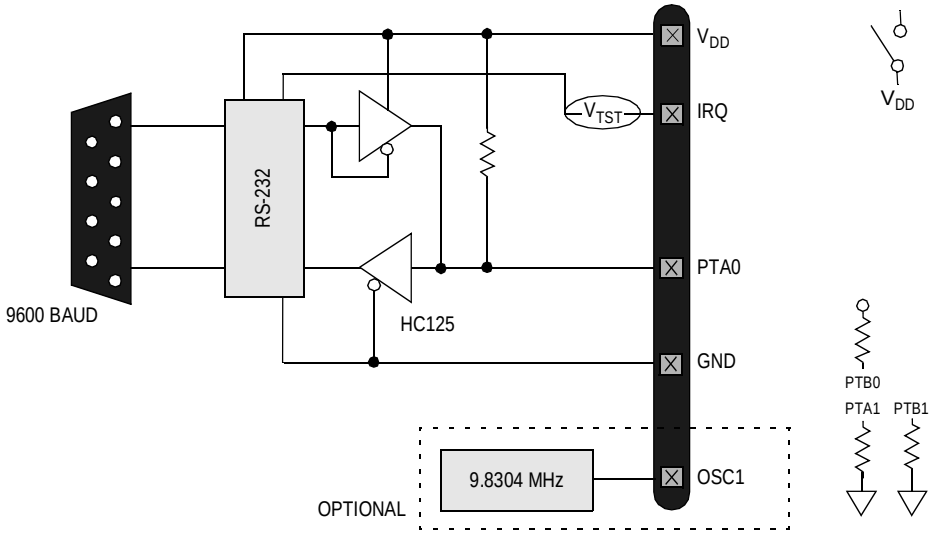


Figure 4. MC68HC908GR8 Standard Monitor Mode (9.8304 MHz)

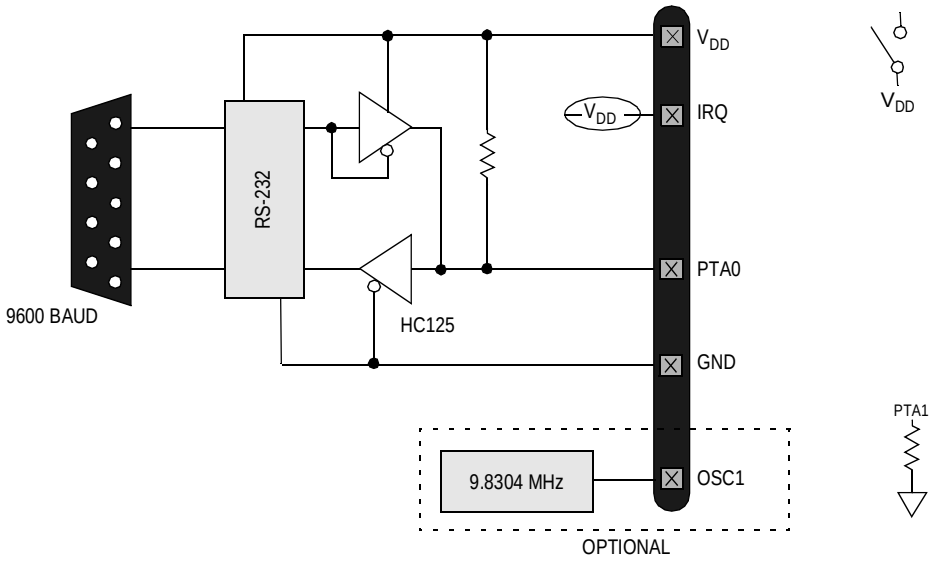


Figure 5. MC68HC908GR8 Forced Monitor Mode (9.8304 MHz)

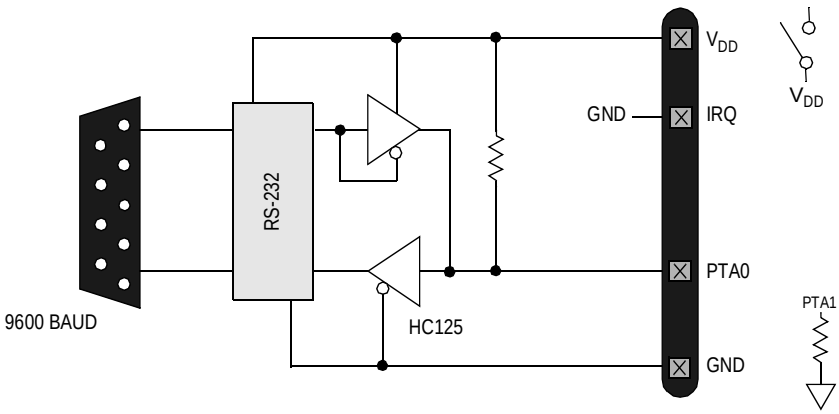


Figure 6. MC68HC908GR8 Forced Monitor Mode (32.768 kHz)

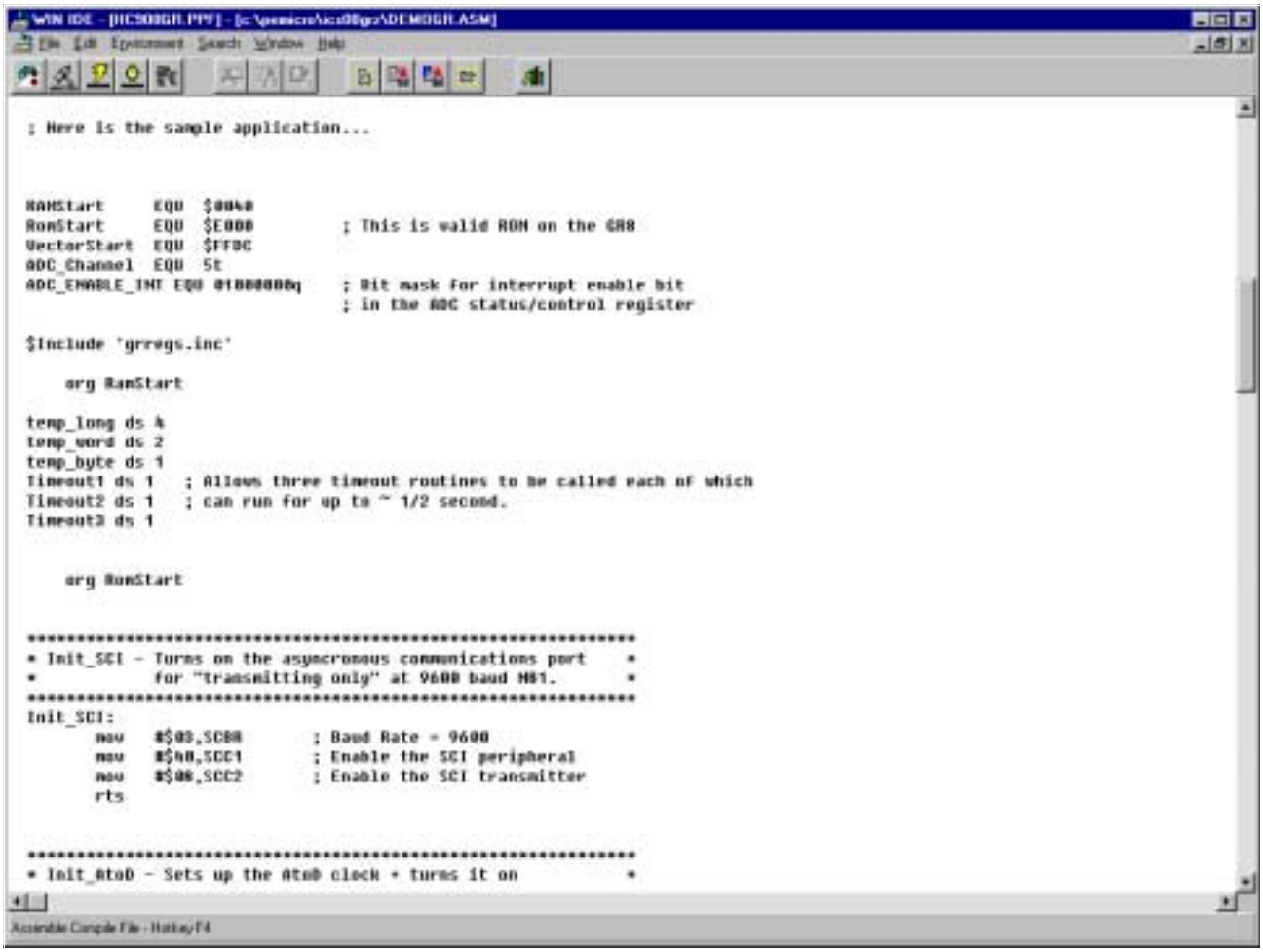


Figure 7. P&E's WINIDE Window

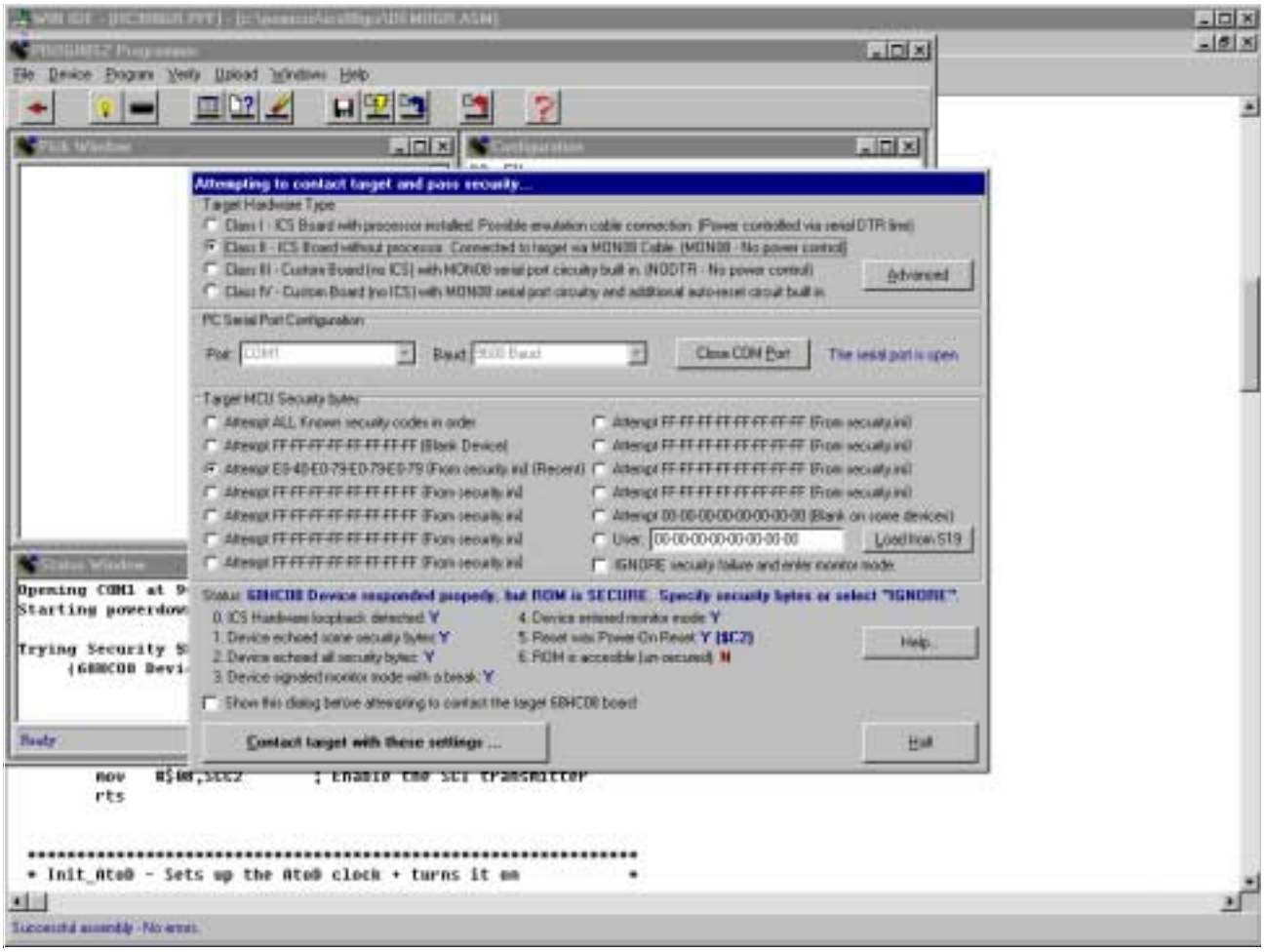


Figure 8. P&E's Target and Security Window

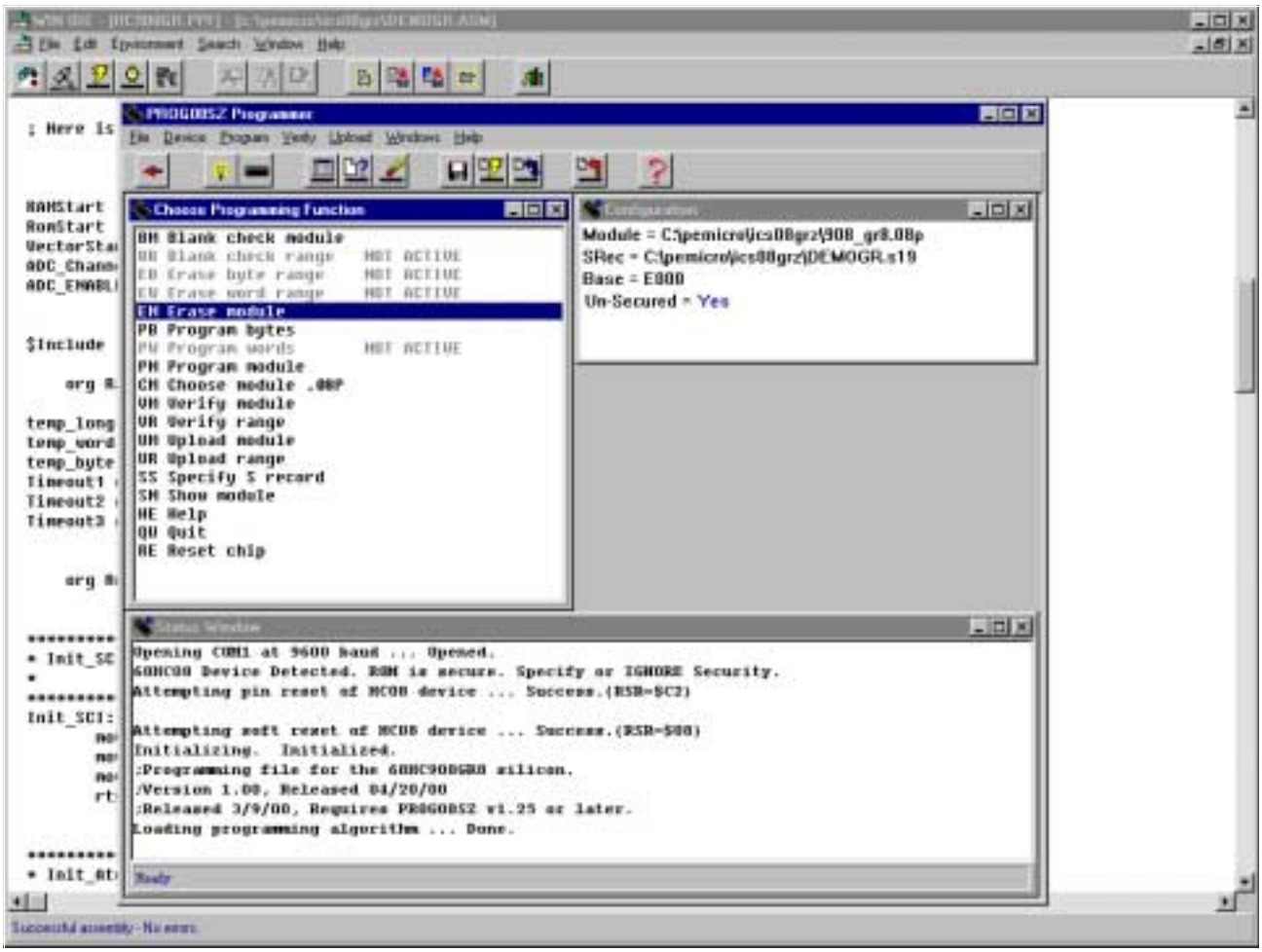


Figure 9. P&E's Programmer Window

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