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Change Summary of the MC9S12DP256 mask set 0K79X versus 0K36N

By Joachim Krücken
BEOS MCU Design
Munich/Germany

Introduction

Several improvements will be introduced in the second mask set of the MC9S12DP256 0K79X versus the initial mask set 0K36N. Some of those are not 100% backwards compatible, i.e. they will require minor software modifications or will have an influence on device parameters and external component selection. The purpose of this document is to give a brief overview of the improvements made and the potential impact to the application. It is not intended to replace a full specification and it does not describe bug fixes announced in the errata sheet. Device specifications from release 2.0 onwards will reflect those changes.

Each section contains a paragraph about compatibility, explaining the impact of the changes from mask set 0K36N to 0K79X.

ADC – Analog Digital Converter

| | |
|--|--|
| Conversion Complete Flag Register | The address of the conversion complete flag register (CCF) is moved from \$07 to \$0B. This is to improve scalability for future derivatives having up to 16 channels. |
| <i>Compatibility</i> | Software will require new compilation using new register address. |



CRG – Clock and Reset Generator Module

The clock and reset module has been enhanced achieving three major goals:

1. Greater Wake-up capabilities in Pseudo STOP mode
2. Simplification of various power reduction options
3. Improved clock qualification and startup circuitry

RTI, COP in Pseudo Stop mode

Two bits have been added to the CRG control register, allowing the RTI and COP to keep running in Pseudo STOP mode. This will allow a precise periodic wake up from Pseudo STOP, giving low power consumption.

| | | | | | | | | |
|-------|-----------------------------|-------|------|-----|---|-----|-----|------|
| \$_06 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | CME | PLLON | AUTO | ACQ | 0 | PRE | PCE | SCME |
| W | | | | | | | | |
| RESET | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| | = Unimplemented or reserved | | | | | | | |

Figure 1. PLLCTL Register

PRE — Pseudo STOP RTI Enable

The RTI counter continues to run while the device is in Pseudo STOP mode depending on the setting of this bit and if the RTI is enabled; i.e. RTR[6:4] are unequal to “000”.

- 1 = RTI continues to run while the device is in Pseudo STOP Mode
- 0 = RTI is stopped during Pseudo STOP Mode

NOTE: *If the PRE bit is clear the RTI dividers will go static whilst Pseudo STOP Mode is active. The RTI dividers will not initialize like in Wait mode with RTIWAI bit set (RTI Stops in Wait).*

PCE — Pseudo STOP COP Enable

The COP counter continues to run while the device is in Pseudo STOP mode depending on the setting of this bit and if COP is enabled; i.e. CR[2:0] are unequal to “000”.

1 = COP continues to run during Pseudo STOP Mode
0 = COP is stopped during Pseudo STOP Mode

NOTE: *If the PCE bit is clear the COP dividers will go static whilst Pseudo STOP Mode is active. The COP dividers will not initialize like in Wait Mode with COPWAI bit set (COP Stops in Wait).*

| | |
|------------------------|---|
| Compatibility | 100% |
| COP, RTI in BDM active | On mask set 0K36N there is no way to stop the COP when BDM is active, i.e. while debugging. A bit RSBCK - Bit6 of the COPCTL - has been added. If this bit is set COP and RTI are stopped when BDM is active. This bit can be written anytime in special mode, but only once in user mode, if no special write has been occurred prior. |
| Simplified power modes | <p>Three bits associated with WAIT mode are part of the CRG module. The new scheme explained is much simpler than the actual one.</p> <ol style="list-style-type: none"> 1. CWAI If this bit is set, all clocks to the core are stopped. This means that the BDM cannot be used if the CPU is in WAIT mode. 2. SYSWAI If this bit is set, all clocks to all peripheral modules as well as the core are stopped. This is a significant power saving compared to individually disabling the modules in WAIT mode, since the whole clock tree is turned off. 3. PLLWAI If this bit is set, the PLL is stopped in WAIT mode. The clock monitor and self clock mode are disabled. |
| Compatibility | Since the change also fixes a known erratum, software needs to be changed to exploit the full potential of the change. |
| Startup behavior | The PLL can be selected as a main system clock even if the PLL is not locked. This is only possible in manual mode (AUTO = 0) and the PLL must be in tracking mode or being locked, i.e. a switch to PLL clock is not possible if the PLL is still in acquisition mode. |
| Compatibility | 100% |

VCO Gain In order to further improve the PLL jitter characteristics the voltage to frequency gain of the VCO has been reduced by 1/3 of the value present on the 0K36N silicon.

Compatibility This has an influence on the optimum selection for resistors and capacitors of the external XFC filter components. Therefore the values for the filter resistance and capacitances should be reviewed.

EEPROM

A new sector modify command (\$60 = erase sector followed by a word program) has been added to the EEPROM. The address and data written to the array during the command sequence are used to do the following:

1. Sector erase the sector of EEPROM containing the address written to.
2. Program the address written to with the written data.

With two commands written to the pipeline (sector modify command followed by a word program of the other word in the 4 bytes sector) the whole EEPROM sector (4 bytes) can be erased and written in one handler routine, minimizing the software overhead.

Compatibility 100%

EEPROM and Flash

New flexibility of the NVM protection scheme is achieved by allowing the user to write the protection bits (EOPEN, EPDIS, respectively FOPEN, FPHDIS, FPLDIS) from unprotected state to protected but not vice versa in user mode. This allows a startup in unprotected state and depending on external stimuli a reprogramming or a protection by software.

Compatibility 100%

IIC

The polarity of the signal to clear the IBCF and IBAL flags is changed. The IIC module is now consistent with the 68HC912KD128 and the 68HC912DG128.

Compatibility This requires a change in the software.

MSCAN — CAN Module

The msCAN will have five receive buffers instead of four. This has no effect on the software but relaxes the requirements on interrupt response time even further.

Compatibility 100%

PIM — Port Integration Module

For improved design flexibility (when targeting reduced pin count derivatives with less than five CAN modules) a module routing register has been added which allows re-routing of CAN and SPI module inputs and outputs to selected input/output pins.

Compatibility 100%

CAUTION: *If customers wish to migrate from the MC9S12DP256 with five CAN and three SPI modules in a 112 pin QFP package to smaller devices or 80 pin packages, careful pin and module planning should be performed to avoid rewriting of code, or even worse, a new layout of the PC board.*

Module Re-routing feature To make best use out of the available modules combined with small pin count packages, several CAN and the SPI I/Os can be routed to different

pins under software control. This is achieved by the module routing register located in the PIM module

| | | | | | | | | |
|-------|-----------------------------|--------|--------|--------|--------|--------|--------|--------|
| \$_17 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | MODRR6 | MODRR5 | MODRR4 | MODRR3 | MODRR2 | MODRR1 | MODRR0 |
| W | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | = Unimplemented or reserved | | | | | | | |

Figure 2. Module Routing Register

CAN Modules

Depending on the number of device specific CAN modules each device features, the following CAN modules are available

- 5 CANs: CAN0 - 4, in 80QFP CAN3 is not available
- 4 CANs: CAN0, 1, 2 and 4.
- 3 CANs: CAN0, 1 and 4.
- 2 CANs: CAN0, 4.
- 1 CAN: CAN0.

For devices with less than 5 CANs, CAN0 and CAN4 modules may require rerouting to make them accessible. This feature is very useful for selecting i/o pin connections for the BDLC, IIC, CAN0 and CAN4 modules. If either the BDLC or IIC are required, CAN0 and CAN4 can be redirected towards other pins.

MODRR[1:0] — CAN0 Routing

These two bits control the re-routing of the CAN0 module to port M pins.

Table 1. CAN0 Routing

| MODRR[1] | MODRR[0] | RxCAN0 | TxCAN0 |
|----------|----------|--------------------|--------------------|
| 0 | 0 | PM0 | PM1 |
| 0 | 1 | PM2 ⁽¹⁾ | PM3 ⁽¹⁾ |
| 1 | 0 | PM4 ⁽²⁾ | PM5 ⁽²⁾ |
| 1 | 1 | Reserved | |

1. Routing to this pin becomes effective only if CAN1 is disabled.
 2. Routing to this pin becomes effective only if CAN2 is disabled.

MODRR[3:2] — CAN4 Routing

These two bits control the re-routing of the CAN4 module to port J or port M pins.

Table 2. CAN4 Routing

| MODRR[3] | MODRR[2] | RxCAN4 | TxCAN4 |
|----------|----------|--------------------|--------------------|
| 0 | 0 | PJ6 | PJ7 |
| 0 | 1 | PM4 ⁽¹⁾ | PM5 ⁽¹⁾ |
| 1 | 0 | PM6 ⁽²⁾ | PM7 ⁽²⁾ |
| 1 | 1 | Reserved | |

1. Routing to this pin becomes effective only if CAN2 is disabled and CAN0 is disabled if routed there.
2. Routing to this pin becomes effective only if CAN3 is disabled.

SPI Modules

All three SPI modules can be routed to various pins. SPI0 can be routed to Port M. This is useful for the 80-Pin package option when CAN1 and CAN2 are not used, but an SPI is required. SPI1, SP2 can be routed from Port P (PWM) to Port H available on the 112 Pin package, thus freeing up valuable PWM channels.

MODRR[4] — SPI0 Routing

This bit controls the re-routing of the SPI0 module to port M pins.

Table 3. SPI0 Routing

| MODRR[4] | MISO0 | MOSI0 | SCK0 | SS0 |
|----------|--------------------|--------------------|--------------------|--------------------|
| 0 | PS4 | PS5 | PS6 | PS7 |
| 1 | PM2 ⁽¹⁾ | PM4 ⁽²⁾ | PM5 ⁽²⁾ | PM3 ⁽¹⁾ |

1. Routing to this pin becomes effective only if CAN1 is disabled and CAN0 is disabled if routed there.
2. Routing to this pin takes effect only if CAN2 is disabled, CAN0 is disabled if routed there and CAN4 is disabled if routed there.

MODRR[5] — SPI1 Routing

This bit controls the re-routing of the SPI1 module to port H pins.

Table 4. SPI1 Routing

| MODRR[5] | MISO1 | MOSI1 | SCK1 | SS1 |
|----------|-------|-------|------|-----|
| 0 | PP0 | PP1 | PP2 | PP3 |
| 1 | PH0 | PH1 | PH2 | PH3 |

MODRR[6] — SPI2 Routing

This bit controls the re-routing the SPI2 module to port H pins.

Table 5. SPI2 Routing

| MODRR[6] | MISO2 | MOSI2 | SCK2 | SS2 |
|----------|-------|-------|------|-----|
| 0 | PP4 | PP5 | PP7 | PP6 |
| 1 | PH4 | PH5 | PH6 | PH7 |

I/O Port Electrical Characteristics

The drive strength in reduced drive mode has been reduced from 1/3 of the full drive (equivalent to an RDSon of 160Ω) to 1/6 of the full drive (equivalent to 320Ω). This has been done in order to improve the EMC behavior of the device.

Compatibility

In some rare cases the electrical interface has to be reviewed.

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ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852-26668334

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