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Differences Between the HC908AZ60A and HC908GZ60

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Introduction

This engineering bulletin highlights the differences between two 8-bit microcontrollers, namely the HC908AZ60A and the HC908GZ60. This document should assist users who are familiar with the HC908AZ60A and who intend to develop a system using the HC908GZ60.

NOTE: *With the exception of mask set errata documents, if any other Motorola document contains information that conflicts with the information in the device data sheet, the data sheet should be considered to have the most current and correct data.*

Differences Guide

This section should be used as a quick guide to determine the main differences between the devices. Using **Table 1**, you can note the differences most relevant to your system, and then consult the relevant area in the **Device Differences** section for more detailed information. This engineering bulletin should be used in conjunction with the most recent specification for each device, to ensure that all differences have been captured.

Table 1. Summary of Differences

Module	HC908AZ60A	HC908GZ60
	Different pin out from HC908GZ60. Available in 64-pin QFP only.	Different pin out from HC908AZ60A. Available in 32-pin LQFP, 48-pin LQFP and 64-pin QFP.
Monitor Mode	Entry requires different port pin settings.	Entry requires different port pin settings. Also has forced monitor mode.
Low Voltage Inhibit (LVI)	5 V operation.	3.3 V & 5 V operation.
Configuration Register CONFIG1	Bit polarities and positions different from HC908GZ60.	Bit polarities and positions different from HC908AZ60A.
Configuration Register CONFIG2	Located at $FE09 with many bits different from HC908GZ60.	Located at $001E with many bits different from HC908AZ60A. MCLK options set in this register. (MCLK is output on PTD0).
Clock Generator Module (CGM)	Contains XLD bit in PBWC register.	Extra registers. No XLD bit.
Memory Map	FLASH, RAM and many registers located at different addresses from the HC908GZ60. 1K bytes of EEPROM available.	FLASH, RAM and many registers located at different addresses from the HC908AZ60A. Contains no on-chip EEPROM. (Could emulate EEPROM using FLASH.)
Serial Communications Interface (SCI) / Enhanced Serial Communications Interface (ESCI)	Has an SCI.	Has an Enhanced SCI that contains all the features of the SCI, with extra prescaler divider options plus an arbiter. The ESCI is LIN compatible.
Analog to Digital Converter (ADC)	8-bit ADC with 15 channels available.	64-pin QFP — 10-bit ADC with 24 channels available. 48-pin LQFP — 10-bit ADC with 16 channels available. 32-pin LQFP — 10-bit ADC with 10 channels available.

Table 1. Summary of Differences (Continued)

Module	HC908AZ60A	HC908GZ60
Programmable Interrupt Timer (PIT) / Timebase Module (TBM)	Has a Programmable Interrupt Timer (PIT). The PIT is always inactive in stop mode.	Has a Timebase Module (TBM). Setting the OSCENINSTOP bit in CONFIG2 enables the TBM to remain active in stop mode.
Keyboard Interrupt (KBI)	5 keyboard interrupt pins. Interrupt triggered by falling edge and/or low level.	8 keyboard interrupt pins on 64-pin QFP and 48-pin LQFP. 4 keyboard interrupt pins on 32-pin LQFP. Interrupt triggered by falling edge and/or low level, and by rising edge and/or high level.
Port A		Has software selectable pull-ups.
Port C	MCLK signal is output on PTC2 and is selected using bit 7 of DDRC register.	Extra I/O pin (PTC6) available on 48-pin LQFP and 64-pin QFP. (32-pin LQFP has only PTC[1:0] available). PTC[4:0] have higher current drive (20 mA sink/source) capability. Port C has software selectable pull-ups.
Port D		MCLK is output on PTD0 when enabled via CONFIG2 register and by setting bit DDRD0 in register DDRD. Port D has software selectable pull-ups.
Port F		Available in 64-pin QFP only. PTF[3:0] have higher current drive (20 mA sink/source) capability.
RSTB		Has internal pull-up.
IRQB		Has internal pull-up.
Resets and Interrupts	Interrupt vectors different from HC908GZ60.	Interrupt vectors different from HC908AZ60A. Contains interrupt status registers that contain flags indicating the interrupt source.

Device Differences

Pin Assignments

The HC908AZ60A is available in a 64-pin QFP package. However, the HC908GZ60 has three different package options: 32-pin LQFP, 48-pin LQFP and 64-pin QFP.

NOTE: *Although both devices are available in the 64-pin QFP package, the pin assignment for each device is completely different. As a result, when designing system hardware, the designer must pay particular attention to the pin assignment for the device being used. The pin assignment for each device can be found in the relevant device specification.*

Monitor Mode

Entry to monitor mode requires different port pin settings, depending on the device being used. The monitor mode entry conditions for the HC908AZ60A are shown in **Table 2**.

Table 2. HC908AZ60A Monitor Mode Entry Conditions

IRQ Pin	PTC0 Pin	PTC1 Pin	PTA0 Pin	PTC3 Pin	Mode	CGMOUT	Bus Frequency
V_{HI}	1	0	1	1	Monitor	CGMXCLK/2 or CGMVCLK/2	CGMOUT/2
V_{HI}	1	0	1	0	Monitor	CGMXCLK	CGMOUT/2

The HC908GZ60 also has two types of monitor mode available, normal monitor mode and forced monitor mode. Forced monitor mode is provided to reduce circuit requirements when performing in-circuit programming. It allows entry to monitor mode without the high voltage on the IRQ pin, provided the reset vectors are blank. When entering monitor mode in this way, all port B pin requirements and conditions, including the PTB4 frequency divider selection, are not in effect. The COP is always disabled in forced monitor mode, regardless of the state of IRQ or RST. However, in normal monitor mode, the COP is disabled only if V_{TST} is applied to either the IRQ pin and/or the RST pin. For the HC908AZ60A, the COP is disabled, provided V_{HI} is applied to either the IRQ pin and/or the RST pin. If the high voltage is removed, setting the COPD bit in the CONFIG1 register will disable the COP. **Table 3** shows the conditions for entry to normal monitor mode and forced monitor mode for the HC908GZ60.

Table 3. HC908GZ60 Monitor Mode Entry Conditions

IRQ Pin	RST Pin	PTA0 Pin	PTA1 Pin	PTB0 Pin	PTB1 Pin	PTB4 Pin	Reset Vectors	Mode	CGMOUT	Bus Frequency
V_{TST}	V_{DD} or V_{TST}	1	0	1	0	0	X	Normal Monitor	CGMXCLK	CGMOUT/2
V_{TST}	V_{DD} or V_{TST}	1	0	1	0	1	X	Normal Monitor	CGMXCLK/2 or CGMVCLK/2	CGMOUT/2
V_{DD} or GND	V_{DD}	1	0	X	X	X	$FF (blank)	Forced Monitor	CGMXCLK/2 or CGMVCLK/2	CGMOUT/2

Low Voltage Inhibit (LVI)

The LVI module allows a device to monitor the V_{DD} voltage. When enabled, the LVI module generates a reset when V_{DD} falls below the trip voltage, V_{tripf}. The HC908GZ60 has selectable trip points for 3.3 V and 5.0 V operation, with the default being 3.3 V operation. The LVI on the HC908AZ60A has a trip point for 5.0 V operation only. Also, on the HC908AZ60A only, an LVI reset occurs if V_{DD} falls below the trip voltage and remains at or below that level for nine or more consecutive cycles. On the HC908GZ60, the LVI reset will occur if V_{DD} falls below the trip voltage. For actual trip voltages, refer to the electrical specifications section of the device specification. Note that the trip ranges for 5.0 V operation are different for the two devices.

For the HC908GZ60 device, the LVI's default mode of operation after a power-on-reset (POR) is 3.3 V. When POR is released, if V_{DD} is below the 5 V trip voltage but above the 3.3 V trip voltage, the device will still operate, because the trip voltage will have defaulted to the 3.3 V level. However, care must be taken in a 5 V system to ensure that V_{DD} is above the 5 V mode trip voltage after POR is released and the LVI has been configured for 5 V operation. Also, if a 5 V system is used, then the user must select 5 V operation after every POR.

Configuration register CONFIG1 contains bits that are used to control the operation of the LVI. Whilst the address of CONFIG1 is the same for both devices, the bit polarity and bit positions for LVI related functions in these registers are different for HC908AZ60A and HC908GZ60. The differences are covered in more detail in the **Configuration Registers** section.

Configuration Registers

Each devices contain two configuration registers: CONFIG1 and CONFIG2 for HC908GZ60, and CONFIG-1 and CONFIG-2 for HC908AZ60A. CONFIG1 (HC908GZ60) and CONFIG-1 (HC908AZ60A) are both located at $001F,

whereas CONFIG2 (HC908GZ60) is located at $001E and CONFIG-2 (HC908AZ60A) at $FE09.

The configuration registers are used to initialize various options and can be written to only once after each reset. Out of reset, the configuration register will read the default settings. These registers are important as they are used to set up various options that affect the operation of the device. Consequently, it is recommended that these registers are written to immediately after reset.

CONFIG2 on the HC908GZ60 contains three bits that control the various MCLK options. MCLK is a clock signal, which, when enabled, is output from the HC908GZ60 on PTD0. It can be used to clock other devices in the system. The MCLK signal can be generated from the crystal or from the bus clock. The MCLKSEL bit determines which one will be the source. The other two bits associated with MCLK select the divider value or switch off the MCLK. The availability of MCLK on PTD0 allows the MCU to clock external devices at various frequencies. It can also prove useful when developing code. For example, it can be used to check that the PLL has been programmed to the correct frequency, by setting up the PLL, waiting for it to lock, switching the bus clock to the PLL clock, then selecting the bus clock with no divide as the source for MCLK. An oscilloscope can be connected to PTD0 and used to verify that the frequency of MCLK matches the desired PLL frequency.

The following subsections provide more detailed information on the configuration register options.

CONFIG1 versus CONFIG-1

The CONFIG1 (HC908GZ60) and CONFIG-1 (HC908AZ60A) registers are shown in **Figure 1** and **Figure 2**.

CONFIG1	Bit 7	6	5	4	3	2	1	0
$001F	COPRS	LVISTOP	LVIRSTD	LVIPWRD	LVI5OR3	SSREC	STOP	COPD
Reset:	0	0	0	0	See note	0	0	0

Figure 1. HC908GZ60 Configuration Register 1 (CONFIG1)

NOTE: *LVI5OR3 is reset only via POR*

Bit 7 (COPRS) — COP Rate Select Bit

COPRS selects the COP timeout period. When this bit is set, the COP timeout period is 2^{13} - 2^4 COPCLK cycles. When this bit is clear, the timeout period is 2^{18} - 2^4 COPCLK cycles.

Bit 6 (LVISTOP) — LVI Enable in Stop Mode Bit

When LVIPWRD bit is clear, setting the LVISTOP bit enables the LVI to operate during stop mode.

Bit 5 (LVIRSTD) — LVI Reset Disable Bit

When set, LVIRSTD disables the reset signal from the LVI module.

Bit 4 (LVIPWRD) — LVI Power Disable Bit

When set, LVIPWRD disables the LVI module.

Bit 3 (LVI5OR3) — LVI 5 V or 3 V Operating Mode Bit

This bit selects the voltage operating mode of the LVI module. When this bit is set, the LVI operates in 5 V mode. LVI5OR3 is reset only by a POR. It is unaffected by all other resets. After a POR, the LVI's default mode of operation is 3.3 V. If a 5 V system is used the user must set this bit to raise the trip point for 5 V operation. This must be done after every POR.

Bit 2 (SSREC) — Short Stop Recovery Bit

Setting this bit enables the CPU to exit stop mode with a delay of 32 CGMXCLK cycles instead of 4096 CGMXCLK cycles. Note that exiting stop mode by an LVI reset will result in the long stop recovery.

Bit 1 (STOP) — STOP Instruction Enable Bit

When set, this bit enables the STOP instruction.

Bit 0 (COPD) — COP Disable Bit

Setting this bit disables the COP module.

CONFIG-1	Bit 7	6	5	4	3	2	1	0
$001F	LVISTOP	R	LVIRST	LVIPWR	SSREC	COPL	STOP	COPD
Reset:	0	1	1	1	0	0	0	0

Figure 2. HC908AZ60A Configuration Register 1 (CONFIG-1)

R = Reserved

Bit 7 (LVISTOP) — LVI Enable in STOP Mode Bit

If LVIPWR bit is set, setting the LVISTOP bit will enable the LVI to operate during stop mode.

Bit 5 (LVIRST) — LVI Reset Enable Bit

When set, LVIRST enables the reset signal from the LVI module.

Bit 4 (LVIPWR) — LVI Power Enable Bit

When set, LVIPWR enables the LVI module.

Bit 3 (SSREC) — Short Stop Recovery Bit

Setting this bit to a 1 enables the CPU to exit stop mode with a delay of 32 CGMXCLK cycles instead of 4096 CGMXCLK cycles. Note that exiting stop mode by an LVI reset will result in the long stop recovery.

Bit 2 (COPL) — COP Long Timeout Bit

COPL selects the COP timeout period. When this bit is set, the COP timeout period is 2^{13} - 2^4 COPCLK cycles. When this bit is clear, the timeout period is 2^{18} - 2^4 COPCLK cycles.

Bit 1 (STOP) — STOP Instruction Enable Bit

When set, this bit enables the STOP instruction.

Bit 0 (COPD) — COP Disable Bit

Setting this bit disables the COP module.

CONFIG2 versus CONFIG-2

The CONFIG2 (HC908GZ60) and CONFIG-2 (HC908AZ60A) registers are shown in **Figure 3** and **Figure 4**.

CONFIG2	Bit 7	6	5	4	3	2	1	0
$001E	Read only 0	MCLKSEL	MCLK1	MCLK0	MSCANEN	TMCLKSEL	OSCENINSTOP	SCIBDSRC
Reset:	0	0	0	0	See note	0	0	1

Figure 3. HC908AZ60A Configuration Register 2 (CONFIG-2)

NOTE: *MSCANEN is reset only via POR.*

Bit 6 (MCLKSEL) — MCLK Source Select Bit

When this bit is set, the crystal frequency is selected as the MCLK source. When this bit is clea,r the bus frequency will be the MCLK source. This bit is used in conjunction with bits MCLK[1:0].

Bit 5 and bit 4 (MCLK1 and MCLK0) — MCLK Output Select Bits

Setting MCLK1 and/or MCLK0 enables the PTD0/$\overline{SS}$ pin to be used as a MCLK output clock, provided bit DDR0 in register DDRD is set. **Table 4** shows the possible options

Table 4. MCLK Output Select

MCLK1	MCLK0	MCLK Frequency
0	0	MCLK not enabled
0	1	Clock
1	0	Clock divided by 2
1	1	Clock divided by 4

Bit 3 (MSCANEN) — MSCAN08 Enable Bit

Setting this bit enables the MSCAN08 module and allows the MSCAN08 to use the PTC0/PTC1 pins. MSCANEN is reset only by a POR. It is unaffected by all other resets.

Bit 2 (TMCLKSEL) — Timebase Clock Select Bit

Setting this bit enables an extra divide-by-128 prescaler in the timebase module.

Bit 1 (OSCENINSTOP) — Oscillator Enable in Stop Mode Bit

When set, this bit enables the oscillator to continue to generate clocks in stop mode. This function is used to keep the timebase running while the rest of the MCU stops. When this bit is clear, the oscillator will cease to generate clocks while in stop mode. The default state for this option is clear.

Bit 0 (SCIBDSRC) — SCI Baud Rate Clock Source Bit

This bit controls the clock source used for the enhanced serial communications interface (ESCI) and affects the frequency that the ESCI operates at. The default is for this bit to be set, which means that the internal data bus clock is used as the source for the ESCI. When clear, the external oscillator is used as the clock source.

CONFIG-2		Bit 7	6	5	4	3	2	1	0
$FE09	Read:	EEDIVCLK	R	R	MSCAND	AT60A	R	R	AZxx
	Write:					R			
Reset:		0	0	0	1	0	0	0	0

Figure 4. HC908AZ60A Configuration Register 2 (CONFIG-2)

R = Reserved

Bit 7 (EEDIVCLK) — EEPROM Timebase Divider Clock Select Bit

This bit selects the reference clock source for the EEPROM-1 and EEPROM-2 timebase divider modules.

Bit 4 (MSCAND) — MSCAN08 Disable Bit

Setting this bit disables the MSCAN08 module.

Bit 3 (AT60A) — Device Indicator Bit

This read-only bit is used to distinguish the MC68HC908AS60A and MC68HC908AZ60A from older non 'A' suffix versions. When this bit is set, the device is 'A' version (0.5µ technology)

Bit 0 (AZxx) — AZxx Emmulator Enable Bit

When set, this bit enables the MC68HC08AZxx emulator configuration. Note that this bit is reset only by a POR.

Clock Generator Module (CGM)

Register Differences

The PLL on the HC908GZ60 has five registers available to set up the PLL, whereas the HC908AZ60A has three. The register addresses are different, and some bits in the HC908GZ60 registers are reserved.

On the HC908AZ60A, bits[3:0] in the PLL control register (PCTL) always read as 1, and the write feature is unimplemented. On the HC908GZ60, bits[3:2] of the PLL control register (PCTL) are reserved, and bits[1:0] represent VPR[1:0]. VPR[1:0] are the VCO power-of-two range select bits; they control the VCO's hardware power-of-two range multiplier, E.

For both devices, it is recommended that the LOCK bit in register PBWC is used to perform crystal loss detection. To use this method, set up the PLL as normal, ensuring that the AUTO bit is set, and that PLL interrupts are enabled by setting PLLIE. Subsequently, a PLL interrupt will occur when the LOCK bit changes polarity. The PLL interrupt service routine should check the LOCK bit. If it is clear then it is possible that the crystal has been lost. If the crystal has been lost the PLL will try to lock to the 'zero' frequency; however, it will not achieve lock but will operate at approximately a third to a fifth of the programmed frequency, which will allow failsafe code to be executed.

The PLL Bandwidth Control Register (PBWC) on the HC908AZ60A has an extra bit, namely XLD, whose function is to perform crystal loss detection. However, this bit may interpret external noise as a clock signal, resulting in false results being obtained. Therefore, it is recommended that the LOCK bit in register PBWC be used to perform crystal loss detection (using the method outlined above).

The HC908AZ60A has one other PLL register, the PLL Programming Register (PPG), which contains four multiplier select bits, MUL[7:4]; these bits control the modulo feedback divider that selects the VCO frequency multiplier, N. This register also includes four VCO Range Select bits, VRS[7:4], that control the hardware center-of-range linear multiplier, L.

The HC908GZ60 has three registers that perform the same task as register PPG on the HC908AZ60A. PLL multiplier select register high (PMSH), PLL multiplier select low (PMSL), and PLL VCO Range Select Register (PMRS) are used to set up the VCO frequency multiplier, N, and the hardware center-of-range multiplier, L.

Note that register PPG (HC908AZ60A), registers PMSH, PMSL, and PMRS, and bits VPR[1:0] in PCTL (HC908GZ60) cannot be written to when the PLL is enabled (PLLON=1). Therefore, for both devices, the PLL initialization software should switch off the PLL (PLLON to 0) before programming these registers with the appropriate values. Once these registers are programmed, the PLL can then be enabled.

Refer to the Programming the PLL section in the most recent specification for each device, where a step-by-step guide is provided on how to calculate the appropriate values of E (HC908GZ60 only), N and L, depending on the crystal frequency being used and the desired bus frequency. Also, before engaging the PLL, via the BCS bit in the PLL Control Register (PCTL), ensure that the PPG register (HC908AZ60A), and registers PMSH, PMSL, and PMRS (HC908GZ60) are programmed with appropriate values for the system.

CGM in Stop Mode

The oscillator on the HC908GZ60 can continue to operate during stop mode if the OSCENINSTOP bit (bit 1 in CONFIG2) is set. If this bit is clear (default setting), then the oscillator will be disabled during stop mode.

On the HC908AZ60A, the STOP instruction disables the CGM.

Filter Options

The HC908GZ60 specification shows two types of filter circuits and provides a table giving example filter component values.

Memory Map

Both devices have 60K of on-chip FLASH and 2K of on-chip RAM, however, the locations of the FLASH and RAM are different for each device. Also, the HC908AZ60A has 1K of EEPROM, whereas the HC908GZ60 has none. Application notes AN2183 and AN2346 describe methods of emulating EEPROM using FLASH, which may be of interest to HC908GZ60 users. **Table 5** shows the addresses of FLASH, RAM, and EEPROM for each device.

Table 5. Memory Addresses

Device	FLASH	RAM	EEPROM
HC908AZ60A	$0450–04FF $0580–05FF $0E00–7FFF $8000–FDFF	$0050–044F $0A00–0DFF	$0800–09FF $0600–07FF
HC908GZ60	$0462–04FF $0980–1B7F $1E20–7FFF $8000–FDFF	$0040–043F $0580–097F	None

The HC908AZ60A and the HC908GZ60 contain many registers that share the same functionality but are located at different addresses, or that include bits that have different polarities. Also, there are registers that are unique to each device. Consequently, it is very important to check the addresses of the registers to ensure that all software header files are correct for the device being used.

Enhanced Serial Communications Interface versus Serial Communications Interface

The HC908GZ60 has an Enhanced Serial Communications Interface (ESCI) and the HC908AZ60A has a Serial Communications Interface (SCI). The ESCI module supports all the features of the SCI module on the HC908AZ60A, but it has an extra prescaler register and an arbiter module. The extra prescaler register allows the user to make fine scale adjustments to the baud rate.

The role of the arbiter module is to support the software on communication tasks, such as bit time measurement and bus arbitration. It consists of a 9-bit counter with a 1-bit overflow plus control logic. Two registers are associated with the arbiter module: the ESCI arbiter control register (SCIACTL) and the ESCI arbiter data register (SCIADAT). SCIADAT is used to store the eight least significant bits of the arbiter counter and SCIACTL stores the most significant bit of the arbiter counter. Also, the CPU uses SCIACTL to control arbiter operation.

The arbiter module allows bit time measurements to be performed easily without the requirement for a timer channel. Two methods of bit time measurement are available:

1. Measuring the length of a break signal (negative pulse) on the RxD/PTE1 pin.
2. Measuring the time between falling edges on the RxD/PTE1 pin.

Method 1 will be very useful in applications where the detection of a break character (negative pulse) is required. Method 2 allows the arbiter to be easily configured as a simple timer, to count the time between falling edges on the RxD/PTE1 pin. The resulting count could be used to check the baud rate of the incoming signal.

The arbiter can also be used in arbitration mode to resolve bus conflicts occurring when the ESCI device is transmitting information on the TxD pin at the same time as another device is driving data onto the RxD pin.

The ESCI Baud Rate Register, SCBR, in the ESCI module on the HC908GZ60, contains two bits known as LINT (bit 7) and LINR (bit 6). These bits are useful in LIN systems as, when they are set, they enable the transmission or detection of 11-bit or 12-bit break characters.

Finally, the baud rate clock source for the ESCI can be selected via the configuration bit ESCIBDSRC (bit 0 in the CONFIG2 register located at $001E). When this bit is set, the internal data bus clock is used as the source for the ESCI. When it is clear, the external oscillator is used as the clock source.

Analog to Digital Converter

The HC908GZ60 has a 10-bit analog to digital converter (ADC), whereas the HC908AZ60A has an 8-bit ADC. Also, the 64-pin QFP version of the HC908GZ60 has 24 ADC channels available, compared to the HC908AZ60A's 15 ADC channels. (The 48-pin LQFP package option has 16 ADC channels

available, and the 32-pin LQFP package option has 10 ADC channels available).

The HC908GZ60 ADC offers four modes of result justification.These are selected by setting bits MODE1 and MODE0 (Modes of Result Justification Bits) in ADCLK, the ADC Clock Register. The four modes are Left Justified Mode, Right Justified Mode, Left Justified Sign Data Mode and 8-bit Truncation Mode. After reset, Right Justified Mode is selected.

Left Justified Mode

places the eight most significant bits of the result in ADC data register high (ADRH). This mode is useful if the result is to be treated as an 8-bit result. The two least significant bits are in ADC data register low (ADRL) and can be ignored. However, ADRL must be read after ADRH, or no subsequent conversions will be stored.

Right Justified Mode

The two most significant bits of the result are stored in ADRH, and the eight least significant bits of the result are stored in ADRL. This mode is used when a 10-bit unsigned result is required.

Left Justified Sign Data Mode

The eight most significant bits of the result are stored in ADRH, but the most significant bit of the 10-bit result AD9, located in ADRH, is complemented. This mode is useful when the result must be represented as a signed magnitude from mid-scale (for example, in applications where crossover detection is required).

8-bit Truncation Mode

The eight most significant bits of the result are stored in ADRL, and the two least significant bits of the result are ignored. In this mode, the user is not required to read ADRH as well as ADRL, and ADRL is updated each time an ADC single channel conversion is completed. 8-bit Truncation Mode allows compatibility with an 8-bit ADC.

Timebase Module versus Programmable Interrupt Timer

The HC908GZ60 contains a timebase module (TBM), whereas the HC908AZ60A has a programmable interrupt timer (PIT).

The timebase module generates periodic interrupts at user selectable rates, using a counter clocked by the external clock source. The clock source for the TBM is either the crystal frequency or the crystal frequency divided by 128. (Setting the TMCLKSEL bit (bit 2 in CONFIG2) selects an additional 128 divide of the external clock.) The TBM generates a periodic interrupt by dividing the selected clock source by 8, 16, 32, 64, 128, 2048, 8192 or 32 768.

If the OSCENINSTOP bit (bit 1 in CONFIG2) is set, then the timebase module remains active after execution of the STOP instruction. The timebase module can be used in this mode to generate a periodic wakeup from stop mode.

The programmable interrupt timer (PIT) is a periodic interrupt timer whose counter is clocked internally via software programmable options. The PIT can be programmed to divide the internal bus clock by 1, 2, 4, 8, 16, 32 or 64, in order to generate the PIT clock source. Unlike the TBM, the PIT is always inactive after the execution of a STOP instruction.

Keyboard Interrupt

There are eight keyboard interrupt pins on the HC908GZ60 in 64-pin QFP and 48-pin LQFP packages (four in the 32-pin LQFP package), whereas the HC908AZ60A has five. For both devices, the interrupts can be programmed to be edge-only or edge-and-level sensitive interrupts. On the HC908AZ60A, keyboard interrupts can be triggered on a falling edge and/or a low level. The HC908GZ60 offers greater flexibility in that interrupts can be triggered on a falling edge and/or a low level as well as on a rising edge and/or a high level. To select the desired trigger polarity, write a 0 or a 1 to the relevant KBIP[7:0] bit in the Keyboard Interrupt Polarity Register (KBIP) located at $0448. Writing a 1 enables the corresponding keyboard interrupt pin to latch an interrupt request when a rising edge and/or a high level is detected. Conversely, writing a 0 enables the corresponding keyboard interrupt pin to latch an interrupt request when a falling edge and/or a low level is detected.

Port A

Port A on the HC908GZ60 has software configurable pull-up devices, when configured as an input port.

Port C

There is an extra Port C pin (PTC6) on the 48-pin LQFP and 64-pin QFP package options on the HC908GZ60 (the 32-pin LQFP has only PTC[1:0] available). PTC[4:0] (HC908GZ60) have a higher current (20 mA) sink/source capability. Also, port C on the HC908GZ60 has software configurable pull-up devices, when configured as an input port.

The HC908AZ60A can output the bus frequency to a signal known as MCLK on PTC2, if DDR7 bit is set in the DDRC register. On the HC908GZ60, extra divider options have been added to the MCLK output, which can be set to the crystal frequency or to the bus frequency. However, MCLK is output on the PTD0/$\overline{SS}$ pin instead of PTC2, and is controlled via three bits in the configuration register, CONFIG2, plus bit DDR0 in register DDRD. Refer to the **Configuration Registers** section for more details.

Port D

Port D on the HC908GZ60 has software configurable pull-up devices, when configured as an input port.

Also, the HC908GZ60 can output the bus frequency to a signal known as MCLK on PTD0, if bit DDR0 is set in the DDRD register and MCLK is enabled

via the CONFIG2 register (see the **Configuration Registers** section for more details).

Port F

On the HC908GZ60, PTF[3:0] are higher current drive (20 mA sink/source capability) port pins. Port F is available only on the 64-pin QFP package.

Reset and IRQ Pins

The reset and IRQ pins on the HC908GZ60 have an internal pull-up resistor.

Resets and Interrupts

Table 6 provides a comparison of the Reset and Interrupt vectors on the HC908GZ60 and the HC908AZ60A.

The HC908GZ60 also contains four interrupt status registers located at $FE04 to $FE07. Each interrupt source has an interrupt status register flag that, when set, indicates that an interrupt request is present. The interrupt status registers can be useful when debugging.

Table 6. Comparison of Reset and Interrupt Vectors

Priority	Address (High/Low)	HC908GZ60	HC908AZ60A
Lowest	$FFCC:FFCD	TIM2 channel 5	TIMA channel 5
	$FFCE:FFCF	TIM2 channel 4	TIMA channel 4
	$FFD0:FFD1	TIM2 channel 3	ADC conversion complete
	$FFD2:FFD3	TIM2 channel 2	Keyboard
	$FFD4:FFD5	MSCAN08 transmit	SCI transmit
	$FFD6:FFD7	MSCAN08 receive	SCI receive
	$FFD8:FFD9	MSCAN08 error	SCI error
	$FFDA:FFDB	MSCAN08 receiver wakeup	CAN transmit
	$FFDC:FFDD	TBM	CAN receive
	$FFDE:FFDF	ADC conversion complete	CAN error
	$FFE0:FFE1	Keyboard	CAN wakeup
	$FFE2:FFE3	ESCI transmit	SPI transmit
	$FFE4:FFE5	ESCI receive	SPI receive
	$FFE6:FFE7	ESCI error	TIMB overflow
	$FFE8:FFE9	SPI transmit	TIMB channel 1
	$FFEA:FFEB	SPI receive	TIMB channel 0
	$FFEC:FFED	TIM2 overflow	TIMA overflow
	$FFEE:FFEF	TIM2 channel 1	TIMA channel 3
	$FFF0:FFF1	TIM2 channel 0	TIMA channel 2
	$FFF2:FFF3	TIM1 overflow	TIMA channel 1
	$FFF4:FFF5	TIM1 channel 1	TIMA channel 0
	$FFF6:FFF7	TIM1 channel 0	PIT
	$FFF8:FFF9	CGM change in lock	PLL
	$FFFA:FFFB	IRQ	IRQ
	$FFFC:FFFD	SWI	SWI
Highest	$FFFE:FFFF	RESET	RESET

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