

Clearing the Receive Data Register Full Flag in the SCI During 9-Bit Data Mode

Covers HCS08 Microcontrollers

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Introduction

This bulletin clarifies how to clear the receive data register full (RDRF) flag in the serial communications interface (SCI) on the HCS08 Family of microcontrollers when 9-bit data mode is used. The full bit clearing sequence is given when a 9-bit character is received.

RDRF Bit Clearing Sequence

The SCI module's 9-bit data mode is selected by setting the mode select bit (M) in the SCI x control register 1 (SCIxC1). When the HCS08's SCI is configured for 9-bit data mode, the ninth bit of the result is stored in the SCI x control register 3 (SCIxC3) in the R8 bit, separate from the other eight bits, which are in the SCI x data register (SCIxD).

When a character is received, the RDRF flag is set to signal that a character has been received and is ready to be read. In some data sheets, the clearing sequence for this flag is described as first reading the SCIxS1 with RDRF = 1, then reading the data in SCIxD. This is valid for the 8-bit data mode.

When 9-bit data mode is selected, an extra step is required to clear RDRF and that is to read the ninth data bit (R8) in the SCIxC3 register. To clear RDRF, read the SCIxS1 register with RDRF = 1, just as in 8-bit mode. Then comes the additional step, read SCIxC3 to get the ninth data bit and save if needed. Now read SCIxD to get the other eight data bits. The reads of SCIxC3 and SCIxD can occur in either order.

Using this sequence will prevent the RDRF flag from remaining set and causing the program to misinterpret the SCI received data.

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