

MPC57xx Flash Erase-Suspend and Erase-Abort Operations

Contents

1 Introduction

This engineering bulletin provides guidance on the use of the flash erase-suspend and erase-abort operations for the MPC57xx family of devices.

1	Introduction.....	1
2	MPC57xx Flash Erase-Suspend and Erase-Abort operations.....	1

2 MPC57xx Flash Erase-Suspend and Erase-Abort operations

MPC57xx flash memory arrays may experience extended erase times after prolonged use of the erase-suspend or erase-abort operations provided by the flash memory controller. Use of these operations will normally be part of an EEPROM emulation driver and the extended erase time may eventually lead to the need for early EEPROM block retirement. The remaining flash blocks will still be available for EEPROM emulation use.

The erase-suspend/abort operations are used in rare situations, in which an “Immediate” write must halt an erase operation already in progress on one of the other flash blocks. For example, to avoid unacceptable write latencies for critical data during an unplanned power-down, an “Immediate” write operation may be needed to ensure that data is properly recorded prior to final power loss.



MPC57xx Flash Erase-Suspend and Erase-Abort operations

Applications that use standard automotive EEPROM emulation at traditional data storage rates will not experience any loss of capability. However, applications that may artificially drive the use of erase-suspend or erase-abort at higher rates should be reviewed to ensure no long-term reduction in EEPROM write/erase endurance can occur. Please consult your local NXP technical support engineers for assistance. Please also consult NXP application note, [AN4868 “EEPROM Emulation with Qorivva MPC55x, MPC56xx, and MPC57xx Microcontrollers”](#) for details on recommended EEPROM emulation best practices.

How to Reach Us:**Home Page:**nxp.com**Web Support:**nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, AltiVec, C-5, CodeTest, CodeWarrior, ColdFire, ColdFire+, C-Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. ARM, AMBA, ARM Powered, Artisan, Cortex, Jazelle, Keil, SecurCore, Thumb, TrustZone, and μ Vision are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. ARM7, ARM9, ARM11, big.LITTLE, CoreLink, CoreSight, DesignStart, Mali, mbed, NEON, POP, Sensinode, Socrates, ULINK and Versatile are trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© 2017 NXP B.V.

Document Number EB851
Revision 0, 03/2017

