

DSP56371E Digital Signal Processor

Mask 1L41N

General remark: In order to prevent the use of instructions or sequences of instructions that do not operate correctly, we encourage you to use the "lint563" program to identify such cases and use alternative sequences of instructions. This program is available as part of the DSP Tools CLAS package.

Silicon Errata

Errata Number: ES131

Applies to Mask: 1L41N

Description (Added 11/28/00):

When all of the following conditions are true:

1. Executing a conditional change of flow (branch, jump) instruction and the branch or jump is *not* taken,
and
2. One of the two program memory words following that instruction includes an address or displacement (as a whole word, or as a field),
and
3. DMA transactions *are* occurring simultaneously,

the address or displacement might not be calculated correctly.

Workaround: Do one of the following:

- A. If only the second word after the instruction includes the address or displacement, add one NOP after the conditional branch,

or
- B. If the first word after the instruction includes the address or displacement, add two NOPs after the conditional branch.

Errata Number: ES139

Applies to Mask: 1L41N

Description (Added 10/01/03):

When the ESAI is in synchronous mode, the Output Flags update a half serial clock early.

Instead of updating on the rising edge of the bit clock (assuming ESAI clock polarity is configured for rising edge outputs) at the start of a frame in normal mode or at the start of each slot in network mode, the Output Flag updates on the previous falling edge of the bit clock (half a bit clock earlier).

If the ESAI clock polarity is configured for falling edge outputs, then the Output Flag will update half a bit clock before the start of a frame in normal mode or at the start of each slot in network mode at the rising edge of the bit clock.

This errata also applies to ESAI_1.

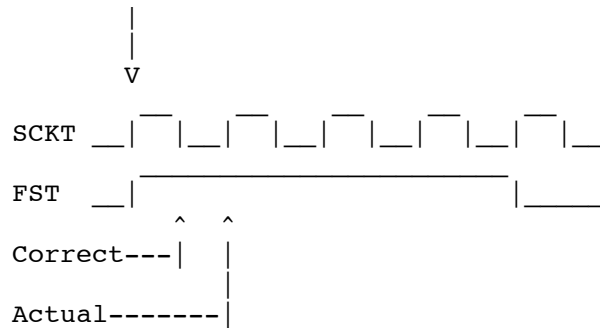
Errata Number: ES140

Applies to Mask: 1L41N

Description (Added 10/01/03):

When providing an external word length FST and bit clock (SCKT) to the ESAI transmitter, the transmitter may lose the first bit if the SCKT clock trails the FST. It is important to maintain equal length signal paths for both the FST and SCKT clocks in slave mode.

FST and SCKT should be synchronous as shown by the arrow at the top of the following figure.



The correct time to latch the FST is on the falling edge when the clock polarity bit is clear. However, when SCKT trails FST it is actually being latched on the following rising edge as shown.

If the ESAI inputs the FST rising edge before the SCKT rising edge that generated it then it will "skip" a bit and assume the first bit has already been driven and start to output the second bit. The ESAI would be one bit ahead of the external device.

This errata also applies to ESAI_1.

Workaround: The SCKT clock should be synchronous with the FST clock and should not trail it when the ESAI transmitter is in slave mode.

Errata Number: ED1

Applies to Mask: 1L41N

Description (Added 11/9/98)

XY memory data move does not work properly under one of the following two situations:

1. The X-memory move destination is internal I/O and the Y-memory move source is a register used as destination in the previous adjacent move from non Y-memory
2. The Y-memory move destination is a register used as source in the next adjacent move to non Y-memory.

Here are examples of the two cases (where x:(r1) is a peripheral)

Example 1:

```
move #12,y0
move x0,x:(r7) y0,y:(r3) ;(while x:(r7) is a peripheral).
```

Example 2:

```
mac    x1,y0,a x1,x:(r1)+    y:(r6)+,y0
move   y0,y1
```

Any of the following alternatives can be used:

- A. Separate these two consecutive moves by any other instruction.
- B. Split XY Data Move to two moves.

Pertains to: DSP56300 Family Manual, Section B-5 "Peripheral pipeline restrictions.

Errata Number: ED4

Applies to Mask: 1L41N

Description (Added 10/31/1997)

The following instructions should not start at address LA:

MOVE to/from Program space {MOVEM, MOVEP (only the P space options)}

This is not a bug but a documentation update (Appendix B, DSP56300 Family Manual).

Errata Number: ED28

Applies to Mask: Applies to Mask: 1L41N

Description (Added 1/7/1997; identified as Documentation Errata 2/1/99)

When two consecutive LAs have a conditional branch instruction at LA-1 of the internal loop, the part does not operate properly. For example, the following sequence may generate incorrect results:

```

        DO #5, LABEL1
        NOP
        DO #4, LABEL2
        NOP
        MOVE (R0) +
        BSCC _DEST          ;conditional branch at LA-1 of
                           ;internal loop
        NOP                ;internal LA
LABEL2
        NOP                ;external LA
LABEL1
        NOP
        NOP
        _DEST  NOP
        NOP
        RTS

```

Workaround: Put an additional NOP between LABEL2 and LABEL1.

Pertains to: DSP56300 Family Manual, Appendix B, Section B-4.1.3, "At LA-1."

Errata Number: ED32

Applies to Mask: 1L41N

Description (Added 11/9/98; identified as a Documentation errata 2/1/99)

When returning from a long interrupt (by RTI instruction), and the first instruction after the RTI is a move to a DALU register (A, B, X, Y), the move may not be correct, if the 16-bit arithmetic mode bit (bit 17 of SR) is changed due to the restoring of SR after RTI.

Workaround: Replace the RTI with the following sequence:

```

movec    ssl,sr
nop
rti

```

Pertains to: DSP56300 Family Manual. Add a new section to Appendix B that is entitled "Sixteen-Bit Compatibility Mode Restrictions."

Errata Number: ED33

Applies to Mask: 1L41N

Description (added 12/16/98; identified as a Documentation errata 2/1/99):

When Stack Extension mode is enabled, a use of the instructions BRKcc or ENDDO inside do loops might cause an improper operation.

If the loop is non nested and has no nested loop inside it, the errata is relevant only if LA or LC values are being used outside the loop.

Workaround: If Stack Extension is used, emulate the BRKcc or ENDDO as in the following examples. We split between two cases, finite loops and do forever loops.

1. Finite DO loops (i.e. not DO FOREVER loops)

=====

BRKcc

Original code:

```

do #N,label1
.....
.....
                                do #M,label2
                                .....
                                .....
                                BRKcc
                                .....
                                .....

```

```

label2
.....
.....

```

label1

Will be replaced by:

```

do #N, label1
.....
.....
                                do #M, label2
                                .....
                                .....
                                Jcc    fix_brk_routine
                                .....
                                .....

```

```

nop_before_label2
                                nop    ;This instruction must be NOP.

```

```

label2
.....
.....

```

label1

```

.....
.....

```

```

fix_brk_routine
    move #1,lc
    jmp  nop_before_label2

```

ENDDO

Original code:

```

do #M,label1
.....
.....
do #N,label2
.....
.....
ENDDO
.....
.....

```

label2

```

.....
.....

```

label1

Will be replaced by:

```

do #M,label1
.....
.....
do #N, label2
.....
.....
JMP    fix_enddo_routine

```

nop_after_jump

```

NOP ; This instruction must be NOP.
.....
.....

```

label2

```

.....
.....

```

label1

```

.....
.....

```

fix_enddo_routine

```

move #1,lc
move #nop_after_jump,la
jmp  nop_after_jump

```

2. DO FOREVER loops

=====

BRKcc

Original code:

```

do #M,label1
.....
.....
do forever,label2

```

```

        .....
        .....
        BRKcc
        .....
        .....
label2
        .....
        .....
label1
Will be replaced by:
        do #M,label1
        .....
        .....
                do forever,label2
                .....
                .....
                JScC    fix_brk_forever_routine    ; <---
note: JScC and not Jcc
                .....
                .....
nop_before_label2
                nop        ; This instruction must be NOP.
label2
        .....
        .....
label1
        ....
        ....

fix_brk_forever_routine
        move ssh,x:<..>; <..> is some reserved not used
address (for temporary data)
        move #nop_before_label2,ssh
        bclr #16,ssl ;
        move #1,lc
        rti        ; <---- note: "rti" and not "rts" !

ENDDO
-----

```

Original code:

```

do #M,label1
        .....
        .....
        do forever,label2
        .....
        .....
        ENDDO
        .....
        .....
label2
        .....

```



```
label1 .....
label1
```

Will be replaced by:

```
do #M,label1
.....
.....
do forever,label2
.....
.....
JSR      fix_enddo_routine    ; <--- note:
JSR and not JMP
nop_after_jump
NOP ; This instruction should be NOP
.....
.....
label2
.....
.....
label1
....
....
fix_enddo_routine
nop
move #1,lc
bclr #16,ssl
move #nop_after_jump,la
rti ; <--- note: "rti" and not "rts"
```

Pertains to: DSP56300 Family Manual, Section B-4.2, "General Do Restrictions."

Errata Number: ED34

Applies to Mask: 1L41N

Description: (Added 1/5/99; identified as a Documentation errata 2/1/99)

When stack extension is enabled, the read result from stack may be improper if two previous executed instructions cause sequential read and write operations with SSH. Two cases are possible:

Case 1:

For the first executed instruction: move from SSH or bit manipulation on SSH (i.e. jclr, brclr, jset, brset, btst, bset, jset, bsclr, jsclr).

For the second executed instruction: move to SSH or bit manipulation on SSH (i.e. jsr, bsr, jscc, bscc).

For the third executed instruction: an SSL or SSH read from the stack result may be improper - move from SSH or SSL or bit manipulation on SSH or SSL (i.e., bset, bclr, bchg, jclr, brclr, jset, brset, btst, bset, jset, bsclr, jsclr).

Workaround: Add two NOP instructions before the third executed instruction.

Case 2:

For the first executed instruction: bit manipulation on SSH (i.e. bset, bclr, bchg).

For the second executed instruction: an SSL or SSH read from the stack result may be improper - move from SSH or SSL or bit manipulation on SSH or SSL (i.e., bset, bclr, bchg, jclr, brclr, jset, brset, btst, bset, jset, bsclr, jsclr).

Workaround: Add two NOP instructions before the second executed instruction.

Pertains to: DSP56300 Family Manual, Appendix B, add a new section called "Stack Extension Enable Restrictions." Cover all cases. Also, in Section 6.3.11.15, add a cross reference to this new section.

Errata Number: ED52**Applies to Mask: 1L41N****Description** (Added 10/01/03):

When using an 'external relative word length frame sync', the ESAI transmitter outputs are not always tri-stated when they should be. Normally, if the last slot in a frame has been transmitted, but the next frame sync has not been received, the transmitter will tri-state until the next frame-sync. However, the ESAI transmitter will not always tri-state in this case. This will prevent other devices from driving the data line. This errata also applies to ESAI_1.

The DSP56371UM indicates in 8.4.4.3 and 9.4.4.3 the following: "Enabled transmitters are tri-stated during these gaps" does not apply to an external word relative framesync on the DSP56371 ESAI or ESAI_1.

Workaround: Do not use an external relative word length framesync when other devices may need to drive the transmitter data line.

Pertains to: DSP56371 User Manual. Section 8.4.4.3, ESAI and Section 9.4.4.3 ESAI_1.

Errata Number: ED53**Applies to Mask: 1L41N****Description** (Added 10/01/03):

The receiver overrun flag (ROE) is not being cleared properly when read by the DSP.

This errata also applies to ESAI_1

Workaround: Instead of a read of the SAISR with the ROE bit set followed by a read of the receiver data registers, the SAISR register has to be read *after* the receiver data registers for all enabled receivers have been read in order to clear the flag.

Pertains to: DSP56371 User Manual, Section 8.3.6.6 SAISR Receiver Overrun Flag (ROE) and Section 9.3.6.6 SAISR Receiver Overrun Flag (ROE).

Errata Number: ED54

Applies to Mask: Applies to Mask: 1L41N

Description (Added 10/01/03):

The debugger software for the ONYX series of parts expects to be able to reset the DSP using the JTAG port. In the DSP56371, this function is not connected.

Workaround: The DSP56371 must be reset using the reset pin.

Pertains to: *DSP56300 Family Manual*, Rev. 3, Chapter 7, Debugging Support.

Errata Number: ED55

Applies to Mask: 1L41N

Description (Added 10/01/03):

When the DAX is used in the slave mode of operation, the underrun error flag (XAUR) is not reliable.

Workaround: Do not use the DAX underrun error flag when operating in slave mode.

Pertains to: DSP56371 User Manual, Section 10.5.7.2 DAX Transmit Underrun Flag (XAUR).

Errata Number: ED56

Applies to Mask: 1L41N

Description (Added 10/01/03):

The receive frame rate divider control (RDC) in the RCCR register determines the number of slots in one frame, and RSMA/RSMB can enable/disable individual slot. Disabling the last slot via the RSMA/RSMB registers also inadvertently disables the first slot.

This errata also applies to ESAI_1.

Workaround: If the first slot needs to be enabled, the last slot also has to be enabled. i.e. If the RDC bits define 8 slots per frame, then in order for the first slot (slot 0) to be enabled, the last slot (slot 7) must also be enabled.

Pertains to: DSP56371 User Manual, Section 8.3.13 Receive Slot Mask Registers (RSMA, RSMB) and Section 9.3.13 Receive Slot Mask Registers (RSMA, RSMB).

Errata Number: ED57

Applies to Mask: 1L41N

Description (Added 10/29/04):

The DSP56371 User Manual fails to note that the OD0 bit of the PCTL register should not be changed when the Low Power Divider (LPD) is zero. The OD0 bit can be changed in conjunction with or prior to the changing of the LPD.

Workaround: Do not change the OD0 bit if the LPD is zero. If the OD0 bit is to be changed when the LPD is zero, change the LPD to a non-zero value first then change the OD0 bit. The LPD can be set back to zero in the same instruction or any subsequent instruction.

Pertains to: DSP56371 User Manual, Section 5, PLL and Clock Generator.

Errata Number: ED58**Applies to Mask: 1L41N****Description** (Added 10/29/04):

The DSP56371UM fails to note that when the SHI is set in master mode and the SHI clock is an output, Fosc must be greater than 8 x sck. i.e. the DSP system clock (Fosc) must be 8 times greater than the SHI clock.

Workaround: Do not use the SHI in master mode as an output when the system clock/shi clock ratio is set to 8 or less.

Pertains to: DSP56371 User Manual, Section 7, Serial Host Interface.

NOTES

1. An over-bar (i.e., $\overline{\text{xxxx}}$) indicates an active-low signal.
2. The letters in the right column tell which DSP56371 mask numbers apply.
3. The DSP website has additional documentation updates that can be accessed at the following URL:
<http://www.freescale.com/>

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