ERRATA SHEET

Date: **2007 Jan 22**
Document Release: **Version 1.0**
Device Affected: **P89LPC9102**

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

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Identification:

The typical P89LPC9102 devices have the following top-side marking:

> P89LPC9102x   x
>
> xxxxxxx   xx
>
> xxYYWW R

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC9102:

Revision Identifier (R)	Comment
'A'	Initial device revision
'B'	Timer0/1.2 fixed

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	fixed in revision	added
ADC.1	Single Step mode multi channel boundary interrupt	none	v1.0
DIVM.1	Using DIVM in power-down mode	none	v1.0
TIMER0/1.2	Counter feature of Timer 1 does not function	B	v1.0

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	fixed in revision	added
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Errata Notes

Note	Short Description	added
IRC.1	Internal RC oscillator accuracy	v1.0
V_{DD}.1	V_{DD} Power cycling.	v1.0

Functional Deviations of P89LPC9102

ADC.1:   **Single Step mode multi channel boundary interrupt**

Introduction: The ADC on the LPC9102 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Single Step mode where the ADC will step through the selected channels on each ADC start condition.

Problem: When the ADC is in Single Step mode with more than 1 channel selected, and a boundary interrupt occurs to any of the lower selected channel-bits, a write to the ADMODA register to clear the BNDI bit before all the selected channels are converted will reset the channel selection counter and the ADC will go back and wait at the lowest selected channel for the next conversion. .

Workarounds: 1)   Clear the lower channel bits including the boundary interrupted channel in ADCINS register before the next start request.

2)   Use the default boundary channel, not clear BNDI bit until all channels are converted.

DIVM.1:   **Using DIVM in power-down mode**

Introduction: The LPC9102 has a DIVM register that can be used to divide the cclk down. Using DIVM can greatly reduce power when in active mode.

Problem: When DIVM is used in active mode and power-down mode is then entered the LPC9102 can not be waken up from power down mode.

Workaround: Before entering powerdown mode set DIVM back to 0x00. This way the LPC9102 will be operating full speed for one instruction before entering power-down mode. After the LPC9102 has been waken up DIVM can be set back to its original value.

TIMER0/1.2:   **Counter feature of Timer1 does not function correctly**

Introduction: The Timers on the LPC9102 have the ability to be clocked by an external port pin T0 or T1, in this case the Timer acts as a counter of an external signal.

Problem: The counter feature of Timer 1 does not function correctly, when an external signal is hooked up to the T1 port pin and the Timer 1 is set-up to be used as a counter the TH1 and / or TL1 will not count the external pulses.

Workaround: No known workaround.

Electrical and Timing Specification Deviations of P89LPC9102

No known errata

Errata Notes

V_{DD}.1:   **V_{DD} Power cycling**

To generate a proper Power-On-Reset (POR), V_{DD} must have dropped below 0.2V before being powered back up. Power-cycling without V_{DD} having dropped below 0.2V may result in incorrect Program Counter values.

Please also see the V_{POR} specification in LPC9102 Datasheet, DC electrical characteristics. Section 8.15 (Reset) states that during a power cycle, V_{DD} must fall below V_{POR}.

IRC.1:   **Internal RC oscillator accuracy**

To be able to guarantee the Internal RC oscillator accuracy over the full operating range the V_{DD} supply has to be decoupled sufficiently. Sufficient decoupling is dependant on the noise level in the application, typically a 0.1uF should be sufficient for most applications.

Noise on the V_{DD} supply pins can cause the Internal RC oscillator to go slightly outside of the specified range.