ES_P89LPC9103

Errata sheet P89LPC9103

Rev. 02 — 6 May 2010 **Errata sheet**

Document information

Info	Content
Keywords	P89LPC9103 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table at the end of the document.

Revision history

Rev	Date	Description
02	20100506	• The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.

Contact information

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1. Product identification

The P89LPC9103 devices typically have the following top-side marking:

P89LPC9103x x

xxxxxxx xx

xxYYWW R

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC9103:

Table 1. Device revision table

Revision identifier (R)	Revision description
'A'	Initial device revision
'B'	Timer0/1.2 fixed

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Fixed in revision
ADC.1	Single Step mode multi channel boundary interrupt	none
DIVM.1	Using DIVM in power-down mode	none
UART.1	Breakdetect trips after 10 zero bits	none

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Fixed in revision
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Table 4. Errata notes

Note	Short description	Fixed in revision
V_{DD}.1	V_{DD} power cycling	none
IRC.1	Internal RC oscillator accuracy	none

3. Functional problems detail

3.1 ADC.1: Single Step mode multi-channel boundary interrupt

Introduction:

The ADC on the P89LPC9103 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Single Step mode where the ADC will step through the selected channels on each ADC start condition.

Problem:

When the ADC is in Single Step mode with more than one channel selected, and a boundary interrupt occurs to any of the lower selected channel-bits, a write to the ADMODA register to clear the BNDI bit before all the selected channels are converted will reset the channel selection counter and the ADC will go back and wait at the lowest selected channel for the next conversion.

Work-around:

1. Clear the lower channel bits including the boundary interrupted channel in ADCINS register before the next start request.
2. Use the default boundary channel, not clear BNDI bit until all channels are converted.

3.2 DIVM.1: Using DIVM in power-down mode

Introduction:

The P89LPC9103 has a DIVM register that can be used to divide the cclk down. Using DIVM can greatly reduce power when in active mode.

Problem:

When DIVM is used in active mode and power-down mode is then entered the P89LPC9103 can not be waken up from power-down mode.

Work-around:

Before entering power-down mode set DIVM back to 0x00. This way the P89LPC9103 will be operating full speed for one instruction before entering power-down mode. After the P89LPC9103 has been waken up DIVM can be set back to its original value.

3.3 UART.1: Breakdetect trips after 10 zero bits

Introduction:

The UART on the P89LPC9103 has the ability to detect a breakdetect signal. A break signal is a 11 bit long low signal on the RxD input of the UART.

Problem:

The breakdetect flag will be set after 10 low bits on the RxD input of the UART. When 9 bit mode is used and all 9 data bits are 0 and the start bit is zero this will be detected as a breakdetect.

Work-around:

No known work-around.

4. AC/DC deviations detail

No known errata

5. Errata notes

5.1 V_{DD}.1: V_{DD} power cycling

To generate a proper Power-On Reset (POR), V_{DD} must have dropped below 0.2 V before being powered back up. Power-cycling without V_{DD} having dropped below 0.2 V may result in incorrect Program Counter values.

Please also see the V_{POR} specification in P89LPC9103 data sheet, DC electrical characteristics. The Reset section of the data sheet states that during a power cycle, V_{DD} must fall below V_{POR}.

5.2 IRC.1: Internal RC oscillator accuracy

To be able to guarantee the Internal RC oscillator accuracy over the full operating range the V_{DD} supply has to be decoupled sufficiently. Sufficient decoupling is dependent on the noise level in the application, typically a 0.1 uF capacitor should be sufficient for most applications.

Noise on the V_{DD} supply pins can cause the Internal RC oscillator to go slightly outside of the specified range.

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